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MAX20343/MAX20344

Ultra-Low Quiescent Current, Low Noise 3.5W Buck-Boost Regulator

General Description

The MAX20343/MAX20344 is an ultra-low quiescent current, non-inverting buck-boost converter with 1A current capability at 3.5V intended for applications that require long run times while also demanding bursts of high current. The device employs a unique control algorithm which seamlessly transitions between buck, buck-boost, and boost modes, minimizing discontinuities and subharmonics in the output voltage ripple. The low 1.9V input voltage for startup allows users to power the device from a variety of sources, and the near-zero minimum operating voltage gives the user the ability to extract as much as possible from their energy source. The MAX20343/MAX20344 has also been designed to keep inductance and output capacitance requirements as low as possible for space-constrained applications.

The MAX20343/MAX20344 is ideal for power in optical sensor applications as well as for powering radios in low power, wide area network (LPWAN) applications since in both cases noise must be minimal and efficiency must be high. For instance, the small light-load output voltage ripple allows a photoplethysmography (PPG) system to operate at low LED currents without interference. Additionally, seamless transitions between operating modes enables the use of dynamic voltage scaling (DVS) to minimize headroom on the LED and to save power in such systems. In applications where a low-power-density battery must be buffered by a super-capacitor to provide large LPWAN type bursts of current, the ultra-low operating voltage of the MAX20343/MAX20344 allows the user to extract as much energy as possible from the super capacitor. The low output inductance/capacitance requirement allows a small total solution size. For example in PPG systems, this provides the flexibility to place the MAX20343/MAX20344 on a remote optical module if overcrowding on the main PCB is an issue.

The MAX20343/MAX20344 is available with a highly configurable I²C serial interface or as a single-pin-enabled fixed-programming version. See [Table 3](#) for specific device settings. MAX20343 operates over the -40°C to +85°C temperature range, is available in a 16-bump, 1.77mm x 2.01mm, 0.4mm pitch WLP package and a 12-pin, 2.50mm x 2.50mm, 0.5mm pitch FC2QFN package. MAX20344 operates over the -40°C to +125°C temperature range, and is available in a 12-pin, 2.50mm x 2.50mm, 0.5mm pitch FC2QFN package.

Applications

- Biometric Optical Sensing Including PPG • IoT
- LPWAN (LTE/NB-IoT, LTE/Cat-M1) • Industrial Sensors

Benefits and Features

- Extend System Run Time
 - Ultra-Low, 3.5µA (typ) Quiescent Current
 - 250mW Output Power with 500mV Input Voltage
 - Dynamic Voltage Scaling (DVS)
- Low, Continuous Noise Profile
 - Eliminates Discontinuities Across Operating Voltage Range
 - Eliminates Post-Filtering LDO in Noise Sensitive Applications
- Adaptable Load Transient Response
 - Adjustable Peak Current for Optimal Performance in Each Application
 - Fast Load Transient Response Minimizes Settling Time
 - Optional Feedback Integrator
 - Enable for up to 3.5W Output Power Capabilities
 - Disable for up to 1.75W Output Power and Faster Load Transient Settling Time
 - FAST Pin Pretriggers Load Response and Offers Improved Load Transient
- Flexible Control Options
 - I²C Interface with Status Interrupts
 - EN and Status Pins, Single-Resistor V_{OUT} Selection (RSEL)
 - See [Table 3](#) for specific device defaults.
- Extended Operating Temperature from -40°C to +85°C (MAX20343), -40°C to +125°C (MAX20344)
- Optimally Sized for Small Applications
 - 16-bump, 1.77mm x 2.01mm, 0.4mm Pitch WLP
 - 12-pin, 2.50mm x 2.50mm, 0.5mm Pitch Flip-Chip QFN
 - Inductor/Capacitor Available in 0603/0402 Case Sizes

[Ordering Information](#) appears at end of data sheet.

Simplified Block Diagram

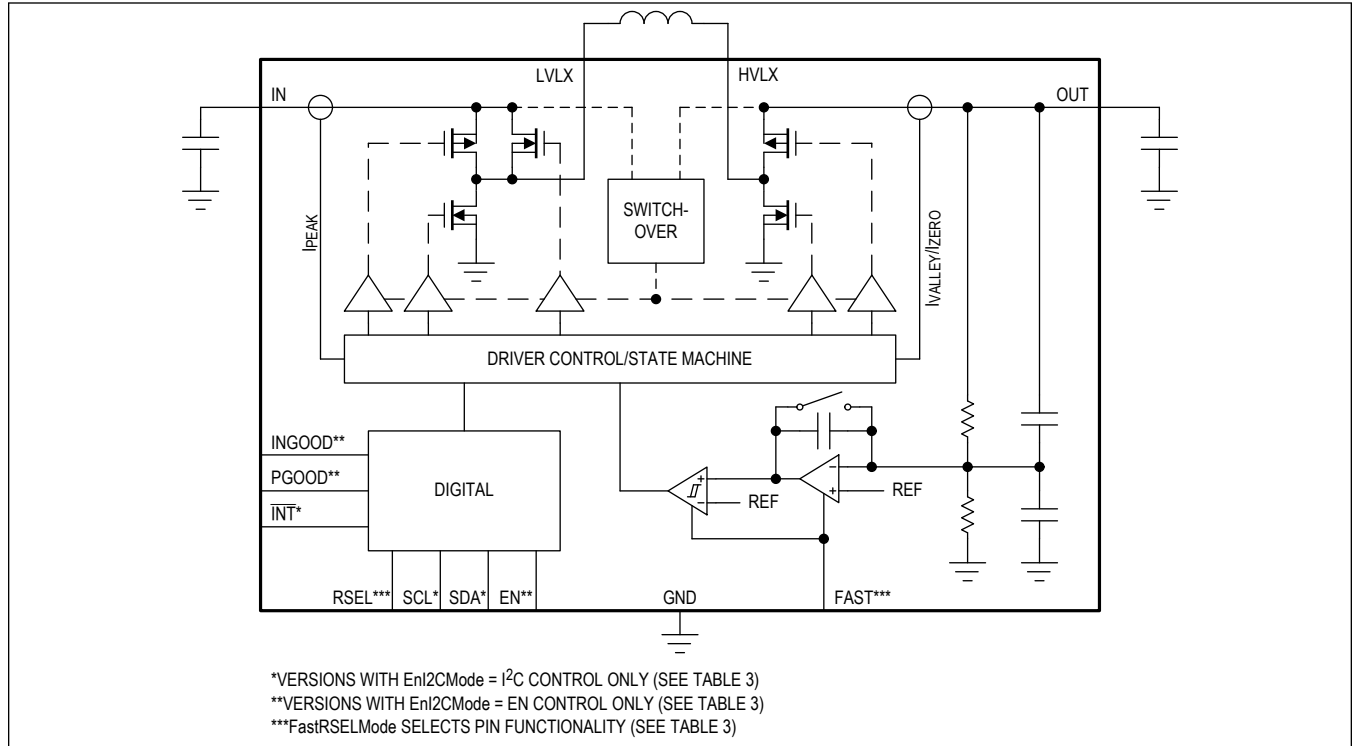


TABLE OF CONTENTS

| | |
|--|----|
| General Description | 1 |
| Applications | 1 |
| Benefits and Features | 1 |
| Simplified Block Diagram | 2 |
| Absolute Maximum Ratings | 7 |
| Package Information | 7 |
| 16-BUMP WLP | 7 |
| 12-Pin FC2QFN | 7 |
| Electrical Characteristics | 8 |
| Typical Operating Characteristics | 11 |
| Pin Configurations | 16 |
| I ² C-Controlled WLP | 16 |
| Single-Pin-Enabled WLP | 16 |
| I ² C-Controlled FC2QFN | 17 |
| Single-Pin-Enabled FC2QFN | 17 |
| Pin Description | 18 |
| Functional Diagram | 20 |
| Functional Diagram | 20 |
| Detailed Description | 21 |
| Startup Voltage | 21 |
| Architectural Description | 21 |
| Switching Phases | 21 |
| Buck-Boost Mode | 21 |
| Buck-Only Mode | 22 |
| Inductor Peak and Valley Current Limits | 22 |
| Integrator Control Loop Disable | 23 |
| Input Operating Voltage | 23 |
| Output Operating Power and Other Optimizations | 24 |
| Device Control | 24 |
| I ² C-Controlled | 24 |
| Single-Pin-Enabled | 25 |
| Dynamic Voltage Scaling (DVS) | 25 |
| RSEL Voltage Setting | 25 |
| Register Map | 28 |
| MAX20343/MAX20344 | 28 |
| Register Details | 28 |
| Applications Information | 34 |
| Input and Output Capacitance | 34 |
| Inductor Selection | 35 |

TABLE OF CONTENTS (CONTINUED)

| | |
|--|----|
| Soft-Start | 35 |
| I ² C Interface | 35 |
| Slave Address | 35 |
| Start, Stop, and Repeated Start Conditions | 35 |
| Bit Transfer | 36 |
| Single-Byte Write | 36 |
| Burst Write | 36 |
| Single Byte Read | 37 |
| Burst Read | 37 |
| Acknowledge Bits | 38 |
| Register Values | 39 |
| Typical Application Circuits | 41 |
| Optical Heart Rate LED Supply | 41 |
| LPWAN Radio Supply | 41 |
| Ordering Information | 42 |
| Revision History | 43 |

LIST OF FIGURES

| | |
|---|----|
| Figure 1. The Buck-Boost Regulator and Switching Phases | 21 |
| Figure 2. Buck-Boost Inductor Current in Buck-Boost Mode | 21 |
| Figure 3. Buck-Boost Inductor Current in Buck-Only Mode | 22 |
| Figure 4. Minimum BBstIPSet2 Limit for Given BBstIPSet1 Setting | 23 |
| Figure 5. Recommended BBstIPSet1 and BBstIPSet2 Settings | 23 |
| Figure 6. MAX20343/MAX20344 RSEL Startup Sequence | 26 |
| Figure 7. Buck-Boost Required Minimum Input/Output Capacitance | 34 |
| Figure 8. I ² C START, STOP, and REPEATED START Conditions | 36 |
| Figure 9. Write Byte Sequence | 36 |
| Figure 10. Burst Write Sequence | 37 |
| Figure 11. Read Byte Sequence | 37 |
| Figure 12. Burst Read Sequence | 38 |
| Figure 13. Acknowledge Bits | 38 |

LIST OF TABLES

| | |
|--|----|
| Table 1. RSEL SELECTION TABLE | 26 |
| Table 2. Characteristics and Device Settings | 27 |
| Table 3. Register Bit Default Values | 39 |
| Table 4. Register Default Values | 40 |

Absolute Maximum Ratings

| | | | |
|---|---|--|-----------------|
| IN, OUT, SDA, SCL, EN, FAST, RSEL, PGOOD, INGOOD, INT, CAP..... | -0.3V to +6.0V | FC2QFN) (derate 17.04mW/°C above +70°C)..... | 1363.20mW |
| LVLX..... | -0.3V to V _{IN} + 0.3V | Operating Temperature Range | |
| HVLX..... | -0.3 to min(V _{OUT} + 0.3V, +6.0V) | MAX20343..... | -40°C to +85°C |
| Continuous Power Dissipation (Multilayer Board, T _A = +70°C) (4 x 4 Array 16-Ball, 1.77mm x 2.01mm, 0.4mm.. | | MAX20344..... | -40°C to +125°C |
| Pitch WLP) (derate 17.26mW/°C above +70°C).... | 1380.80mW | Junction Temperature | +150°C |
| Continuous Power Dissipation (Multilayer Board, T _A = +70°C) (12-Pin, 2.50mm x 2.50mm, 0.5mm Pitch | | Storage Temperature Range | -40°C to +150°C |
| | | Soldering Temperature (reflow) | +260°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16-BUMP WLP

| | |
|--|--|
| Package Code | W161C2+1 |
| Outline Number | 21-100328 |
| Land Pattern Number | Refer to Application Note 1891 |
| THERMAL RESISTANCE, SINGLE-LAYER BOARD | |
| Junction-to-Ambient (θ _{JA}) | |
| Junction-to-Case Thermal Resistance (θ _{JC}) | |
| THERMAL RESISTANCE, FOUR-LAYER BOARD | |
| Junction-to-Ambient (θ _{JA}) | 57.93°C/W |

12-Pin FC2QFN

| | |
|--|---------------------------|
| Package Code | F122B2F+1 |
| Outline Number | 21-100331 |
| Land Pattern Number | 90-100130 |
| THERMAL RESISTANCE, SINGLE-LAYER BOARD | |
| Junction-to-Ambient (θ _{JA}) | |
| Junction-to-Case Thermal Resistance (θ _{JC}) | |
| THERMAL RESISTANCE, FOUR-LAYER BOARD | |
| Junction-to-Ambient (θ _{JA}) | 58.70°C/W |
| Junction-to-Case Thermal Resistance (θ _{JC}) | 23.10°C/W |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{IN} = +1.8V$ to $+5.5V$, $C_{IN} = 5\mu F$, $C_{OUT} = 8\mu F$, $T_J = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{IN} = +3.7V$, $L = 1\mu H$, Limits are 100% tested at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|-----------------|---|--|------|------|------|---------|
| BUCK-BOOST | | | | | | | |
| Input Voltage Range | V_{IN_START} | Input voltage required for startup (Note 2) | | 1.9 | | 5.5 | V |
| Quiescent Supply Current | I_Q | No load, $V_{OUT} = 5V$, $V_{IN} = 3.7V$ | $SwoFrcIN = 1$, $T_A = +85^\circ C$ (MAX20343) | | 3.51 | 5 | μA |
| | | | $SwoFrcIN = 1$, $T_A = +125^\circ C$ (MAX20344) | | | 12.5 | |
| | I_{Q_FAST} | | FAST = 1 | | 35 | | μA |
| Shutdown Supply Current | I_{SHDN} | I^2C controlled | | | 0.3 | | μA |
| Maximum Output Operative Power (Note 3) | P_{MAX} | Integrator enabled, $V_{IN} > 2.7V$, $V_{OUT} \geq 3.2V$ | $BBstFETScale = 0$, $L = 1\mu H$, $C_{OUT} = 8\mu F$ | 3.5 | | | W |
| | | | $BBstFETScale = 1$, $L = 2.2\mu H$, $C_{OUT} = 4\mu F$ | 1.75 | | | |
| | | Integrator disabled, $V_{IN} > 3.2V$ (Note 4), $V_{OUT} \geq 3.2V$ | $BBstFETScale = 0$, $L = 1\mu H$, $C_{OUT} = 8\mu F$, $T_A = +85^\circ C$ (MAX20343) | 3.2 | | | |
| | | | $BBstFETScale = 0$, $L = 1\mu H$, $C_{OUT} = 8\mu F$, $T_A = +125^\circ C$ (MAX20344) | 2.9 | | | |
| | | | $BBstFETScale = 1$, $L = 2.2\mu H$, $C_{OUT} = 4\mu F$, $T_A = +85^\circ C$ (MAX20343) | 1.75 | | | |
| | | | $BBstFETScale = 1$, $L = 2.2\mu H$, $C_{OUT} = 4\mu F$, $T_A = +125^\circ C$ (MAX20344) | 1.6 | | | |
| Output-Voltage Set Range | V_{OUT} | 50mV step resolution | | 2.5 | | 5.5 | V |
| | | | $V_{IN} < 2.1V$, $SwoFrcIN = 0$ (see the Input Operating Voltage section) | 3.2 | | 5.5 | |
| Average Output-Voltage Accuracy | ACC_OUT | $I_{OUT} = 1mA$, $C_{OUT_EFF} = 8\mu F$ | | -2.4 | | +2.4 | % |
| Line Regulation Error | V_{LINE_REG} | | | -1 | | +1 | %/V |
| Load Regulation Error | V_{LOAD_REG} | Integrator enabled, $V_{IN} = 2.7V$, $V_{OUT} = 3.3V$, $BBstFETScale = 0$, $P_{OUT} = 3.5W$ | | | -1 | | % |
| | | Integrator disabled, $V_{IN} = 3.7V$, $V_{OUT} = 5V$, $P_{OUT} = 1.5W$, $BBstFETScale = 1$, $C_{OUT} = 4\mu F$, $L = 2.2\mu H$ | | | -3.2 | | |

Electrical Characteristics (continued)

($V_{IN} = +1.8V$ to $+5.5V$, $C_{IN} = 5\mu F$, $C_{OUT} = 8\mu F$, $T_J = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{IN} = +3.7V$, $L = 1\mu H$, Limits are 100% tested at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|----------------------|---|---|-----|-------|-----|-------------------------|
| Line Transient Response | V_{LINE_TRAN} | $V_{OUT} = 3.4V$, V_{IN} from 3.4V to 2.9V, 1 μs fall time, $I_{LOAD} = 750mA$, $BBstIntegEn = 1$, $SwoFrcIN = 0$ | | | 0 | | mV |
| Load Transient Response | V_{LOAD_TRAN} | $V_{OUT} = 5V$, $V_{IN} = 3.7V$, $I_{LOAD} = 10\mu A$ to 700mA, $BBstIntegEn = 1$ | | | -150 | | mV |
| Input Supply Current During Startup | I_{IN_STUP} | $V_{IN} = 3.6V$, $V_{OUT} = 5V$, $I_{LOAD} = 0$ | | | 1 | | mA/ $C_{OUT}(\mu F)$ |
| Maximum Output Power During Startup (Note 3) | $I_{PWR_MAX_STUP}$ | $BBstFETScale = 0$ | | 400 | 600 | | mW |
| | | $BBstFETScale = 1$ | | 200 | 300 | | |
| Startup Time | $t_{STARTUP}$ | Time from $V_{OUT} = 0V$ to final value | I^2C controlled | | 9.6 | | ms |
| | | | RSEL, $BBstRampEn = 0$ | | 32 | | |
| PGOOD Threshold | V_{PGOOD} | | | | 84.7 | | $\%V_{OUT}$ |
| PGOOD Threshold Hysteresis | V_{PGOOD_HYS} | | | | 2.25 | | $\%V_{OUT}$ |
| Active Discharge Current | I_{ACTD} | | | | 20 | | mA |
| Passive Discharge Resistance | R_{PSVD} | | | | 1.2 | | k Ω |
| Input UVLO Rising Threshold | $V_{IN_UVLO_R}$ | V_{IN} rising | Soft-start active, $SwoFrcIN = 1$, or V_{OUT} set below 3.3V | | 1.836 | | V |
| | | | V_{OUT} set higher than 3.3V, $SwoFrcIN = 0$, soft-start period complete | | 2.185 | | |
| Input UVLO Falling Threshold | $V_{IN_UVLO_F}$ | V_{IN} falling | Soft-start active, $SwoFrcIN = 1$, or V_{OUT} set below 3.3V | | 1.782 | | V |
| | | | V_{OUT} set higher than 3.3V, $SwoFrcIN = 0$, soft-start period complete | | 2.101 | | |
| Output UVLO Falling Threshold | $V_{OUT_UVLO_F}$ | V_{OUT} falling | | | 1.873 | | V |
| Output UVLO Rising Threshold | $V_{OUT_UVLO_R}$ | V_{OUT} rising | | | 1.963 | | V |
| DIGITAL | | | | | | | |
| SDA, EN, SCL, \overline{INT} , PGOOD, INGOOD FAST, RSEL Input Leakage Current | I_{LK_IO} | $T_J = +25^\circ C$ | | -1 | | +1 | μA |

Electrical Characteristics (continued)

($V_{IN} = +1.8V$ to $+5.5V$, $C_{IN} = 5\mu F$, $C_{OUT} = 8\mu F$, $T_J = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$, $V_{IN} = +3.7V$, $L = 1\mu H$, Limits are 100% tested at $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|------------------------------|------|-----|------|---------|
| SDA, EN, SCL, FAST Input Logic High | V_{IO_IH} | | 1.4 | | | V |
| SDA, EN, SCL, FAST Input Logic Low | V_{IO_IL} | | | | 0.4 | V |
| SDA, \overline{INT} , PGOOD, INGOOD Output Logic Low | V_{IO_OL} | $I_{OL} = 4mA$ | | | 0.4 | V |
| SCL Clock Frequency | f_{SCL} | MAX20343B/E/F/G/I, MAX20344E | 400 | | 680 | kHz |
| | | All other versions | | | 680 | |
| Bus Free Time Between STOP and START Condition | t_{BUF} | | 0.75 | | | μs |
| START Condition (Repeated) Hold Time | t_{HD_STA} | (Note 5) | 0.35 | | | μs |
| Low Period of SCL Clock | t_{LOW} | | 0.75 | | | μs |
| High Period of SCL Clock | t_{HIGH} | | 0.35 | | | μs |
| Setup Time for a Repeated START Condition | t_{SU_STA} | | 0.35 | | | μs |
| Data Hold Time | t_{HD_DAT} | (Note 6) | 0 | | 0.53 | μs |
| Data Setup Time | t_{SU_DAT} | | 100 | | | ns |
| Setup Time for STOP Condition | t_{SU_STO} | | 0.35 | | | μs |
| Spike Pulse Widths Suppressed by Input Filter | t_{SP} | | 50 | | | ns |

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design.

Note 2: Output power across the input operating voltage range is limited by input current. Refer to TOC03 for details on how the power limit changes with V_{IN} .

Note 3: The parameter is not production tested and values are generated through characterization only.

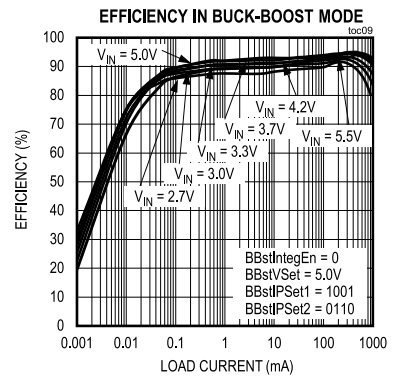
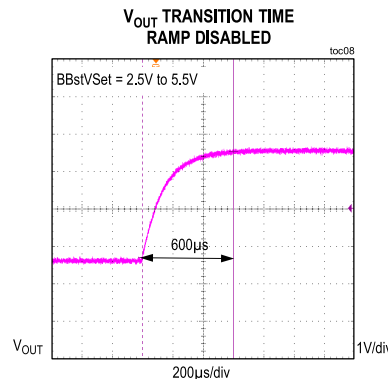
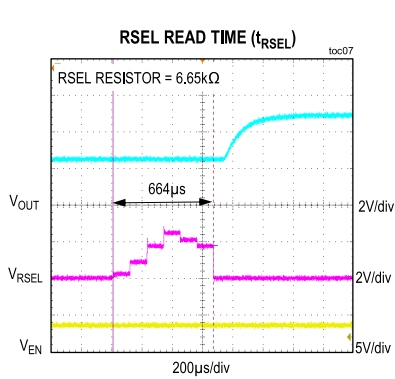
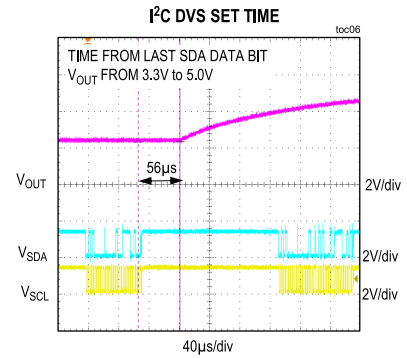
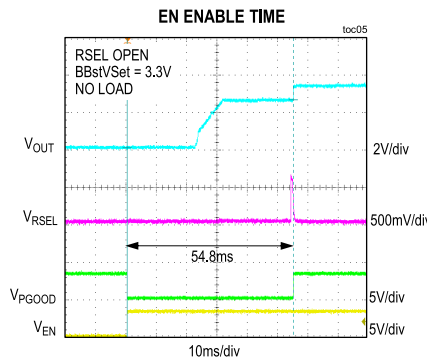
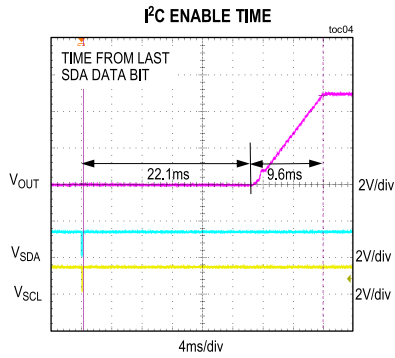
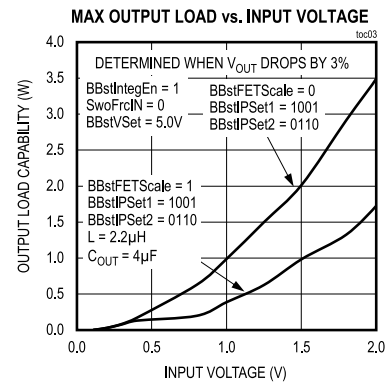
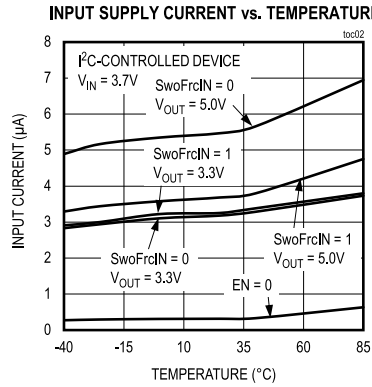
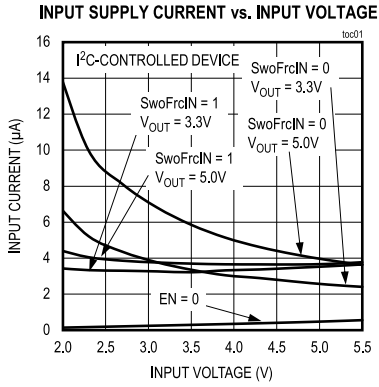
Note 4: Operation down to 2.7V is supported with the integrator disabled, but stability is only guaranteed up to 1.75W output power. Beyond 1.75W, oscillations could occur unless output capacitance is increased.

Note 5: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 6: The maximum t_{HD_DAT} has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

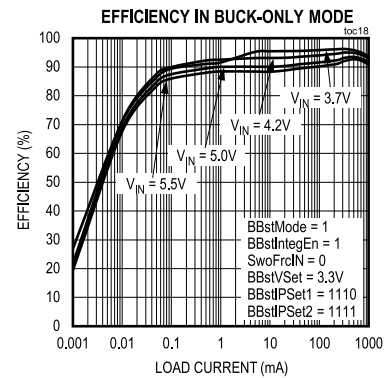
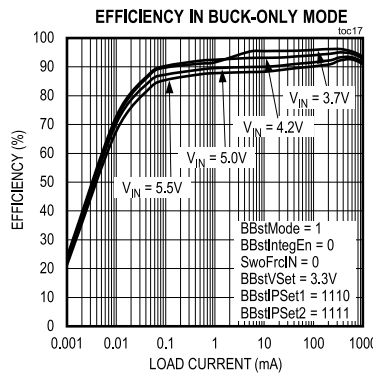
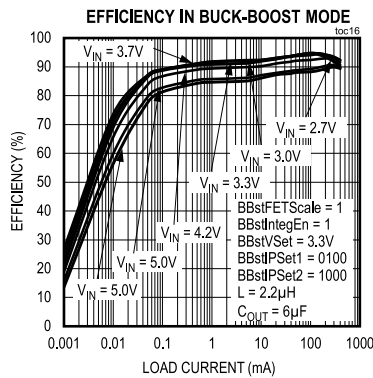
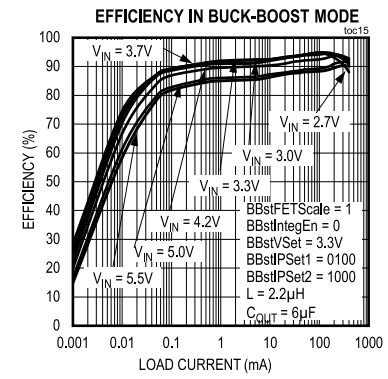
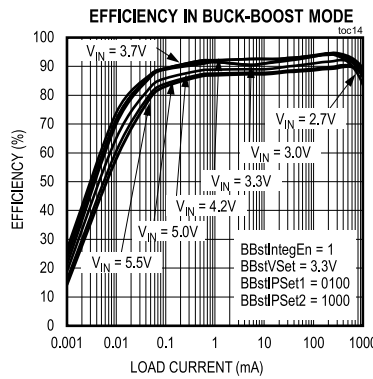
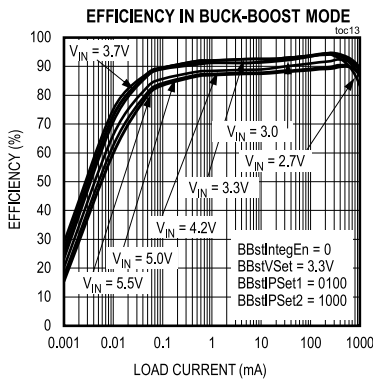
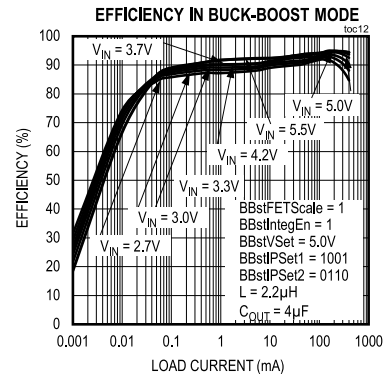
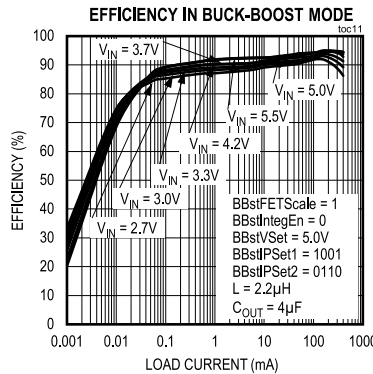
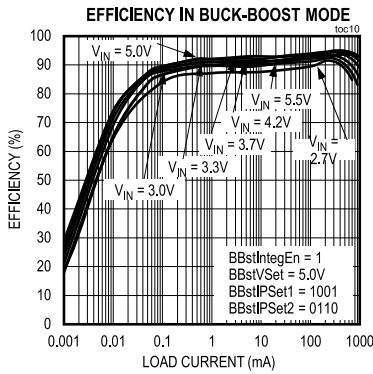
Typical Operating Characteristics

($V_{IN} = +3.7V$, $C_{IN} = GRM155R60J226ME11$, refer to [Figure 7](#) single capacitor derating, $C_{OUT} = 2x GRM155R60J226ME11$, $L = 1\mu H$, $BBstZCCmpDis = 0$, $BBstLowEMI = 0$, $BBstMode = 0$, $SwoFrcIN = 1$, $BBstIPAdptDis = 0$, $BBstFETScale = 0$, $T_A = +25^\circ C$, unless otherwise noted.)



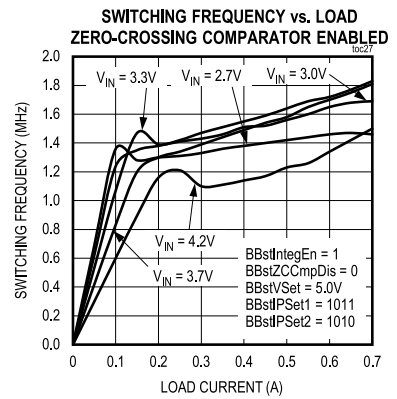
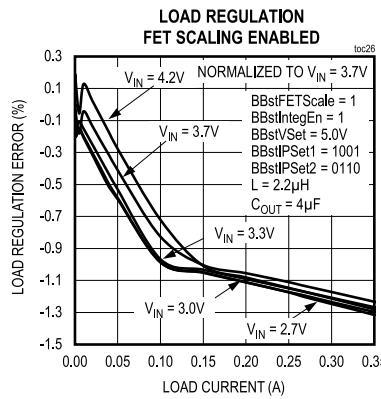
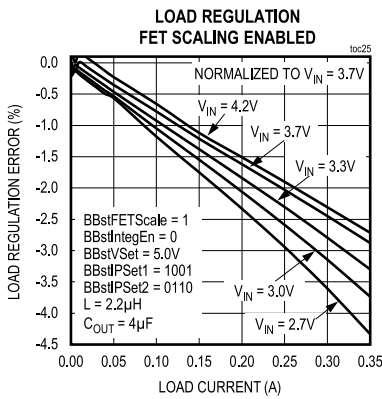
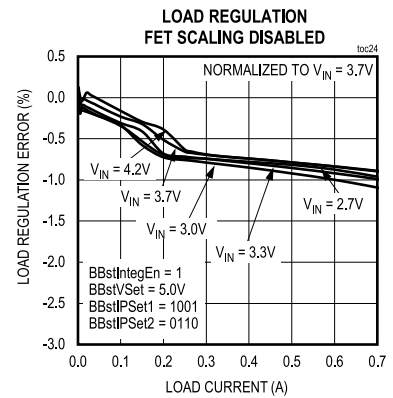
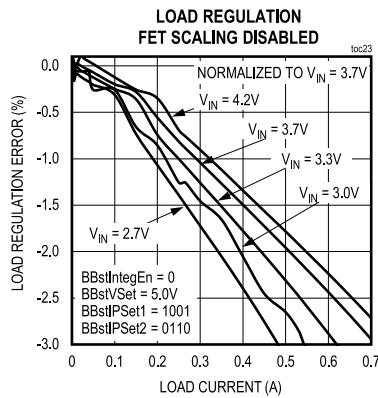
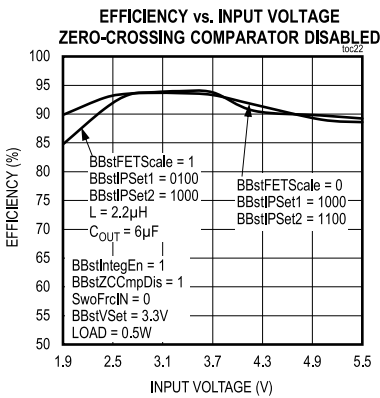
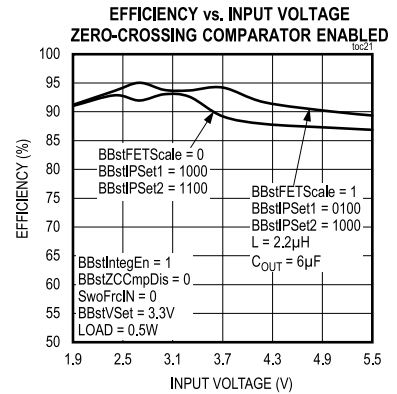
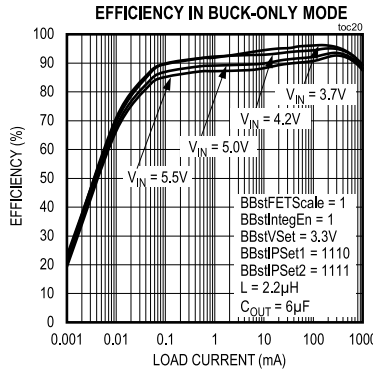
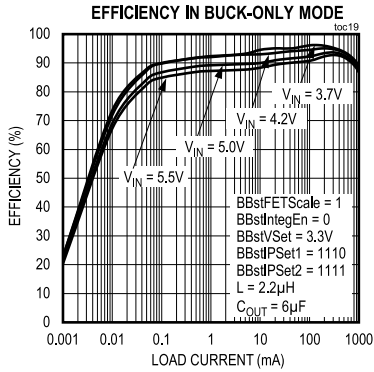
Typical Operating Characteristics (continued)

($V_{IN} = +3.7V$, $C_{IN} = GRM155R60J226ME11$, refer to [Figure 7](#) single capacitor derating, $C_{OUT} = 2x GRM155R60J226ME11$, $L = 1\mu H$, $BBstZCCmpDis = 0$, $BBstLowEMI = 0$, $BBstMode = 0$, $SwoFrcIN = 1$, $BBstIPAdptDis = 0$, $BBstFETScale = 0$, $T_A = +25^\circ C$, unless otherwise noted.)



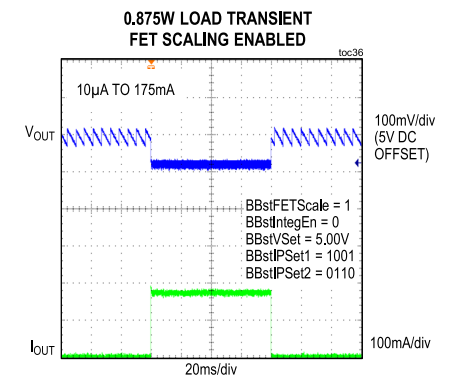
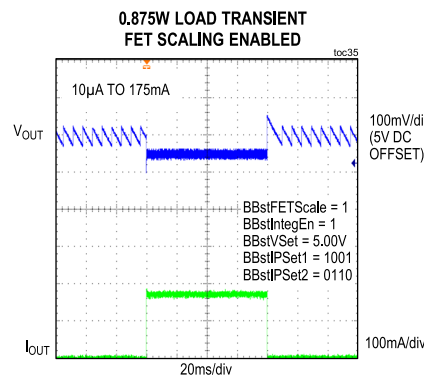
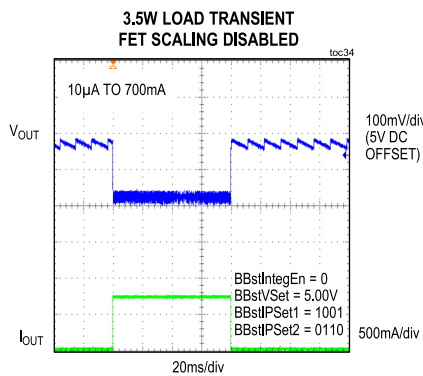
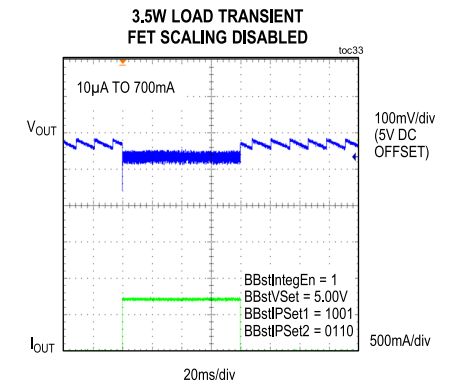
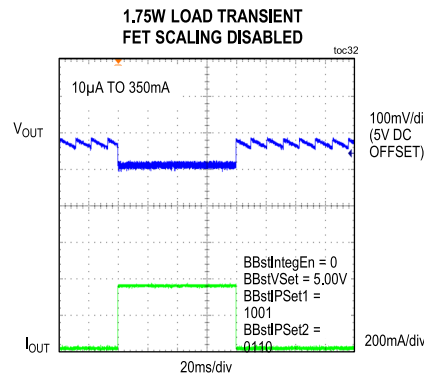
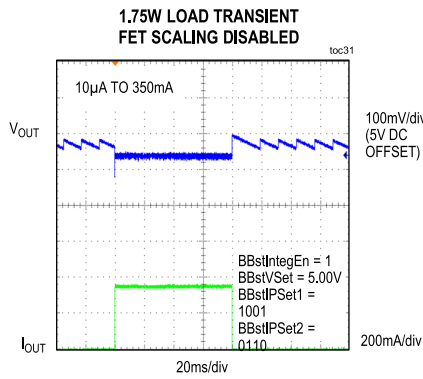
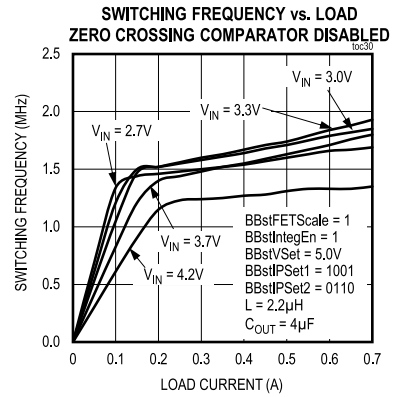
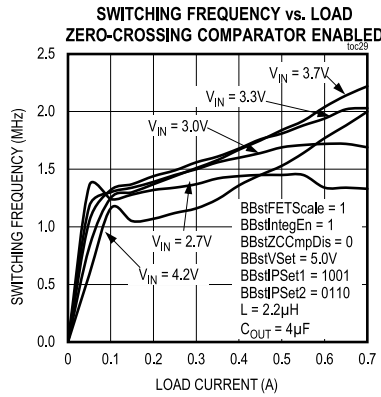
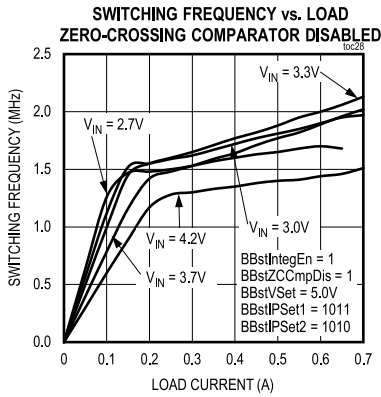
Typical Operating Characteristics (continued)

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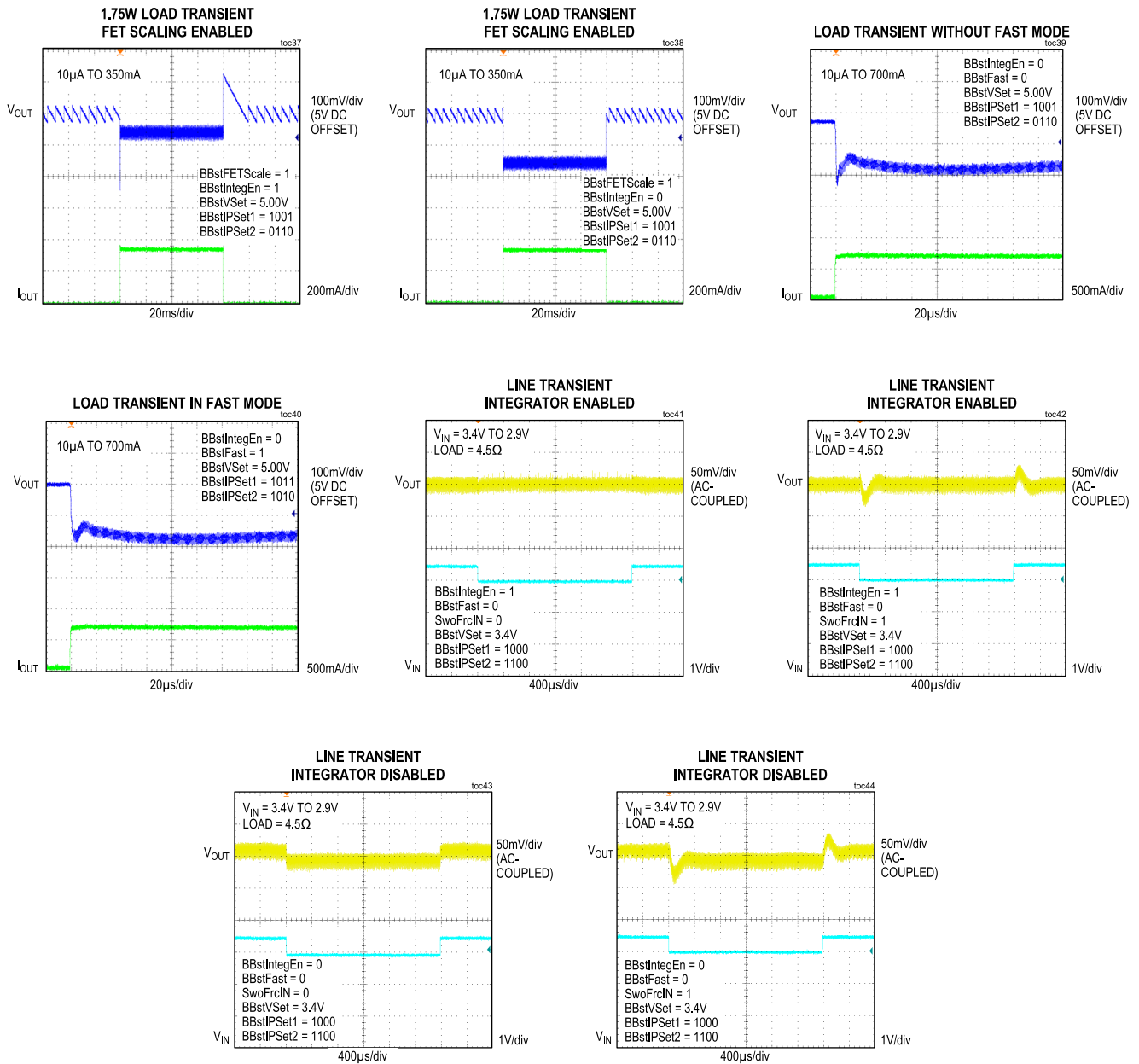
Typical Operating Characteristics (continued)

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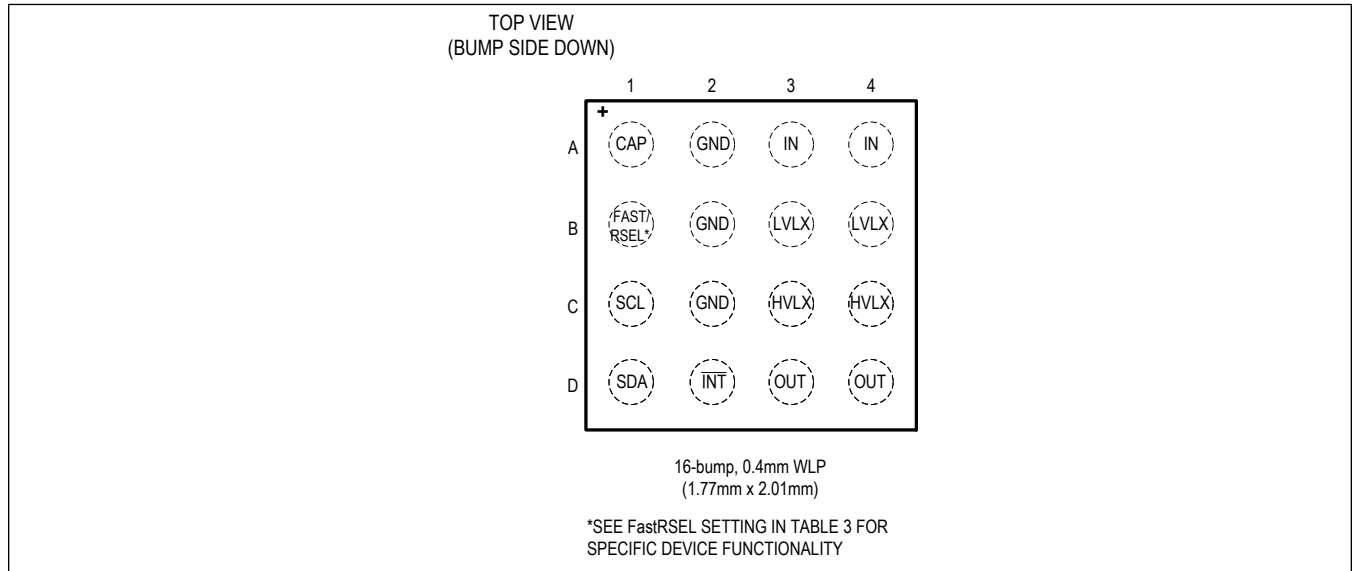
Typical Operating Characteristics (continued)

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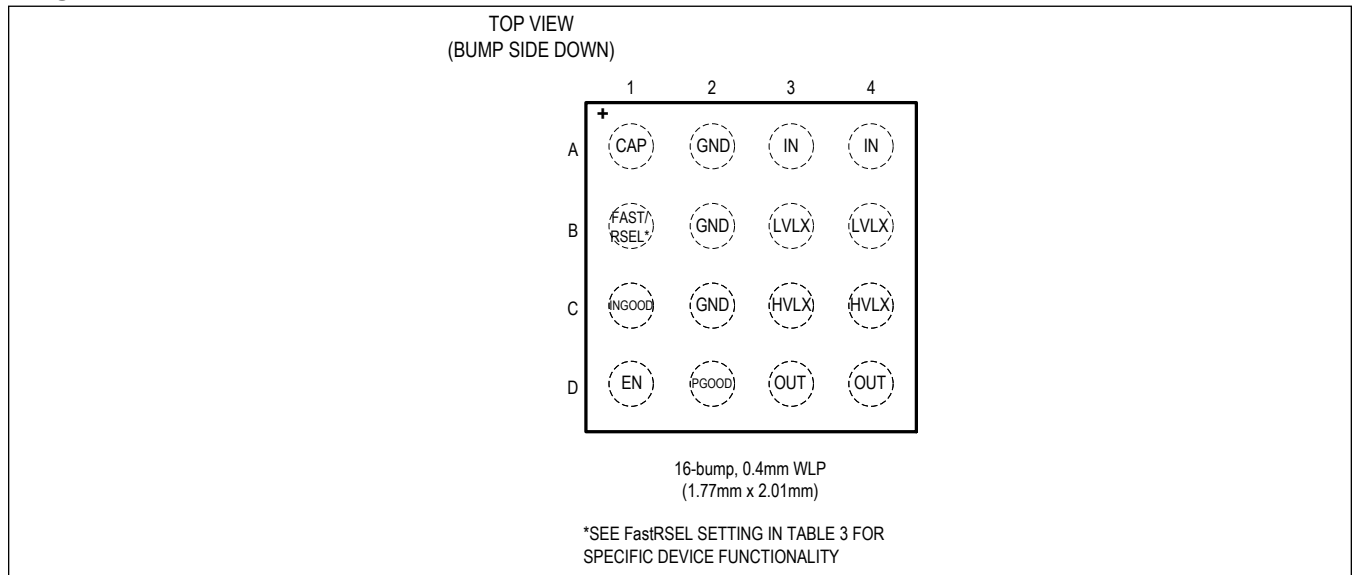


Pin Configurations

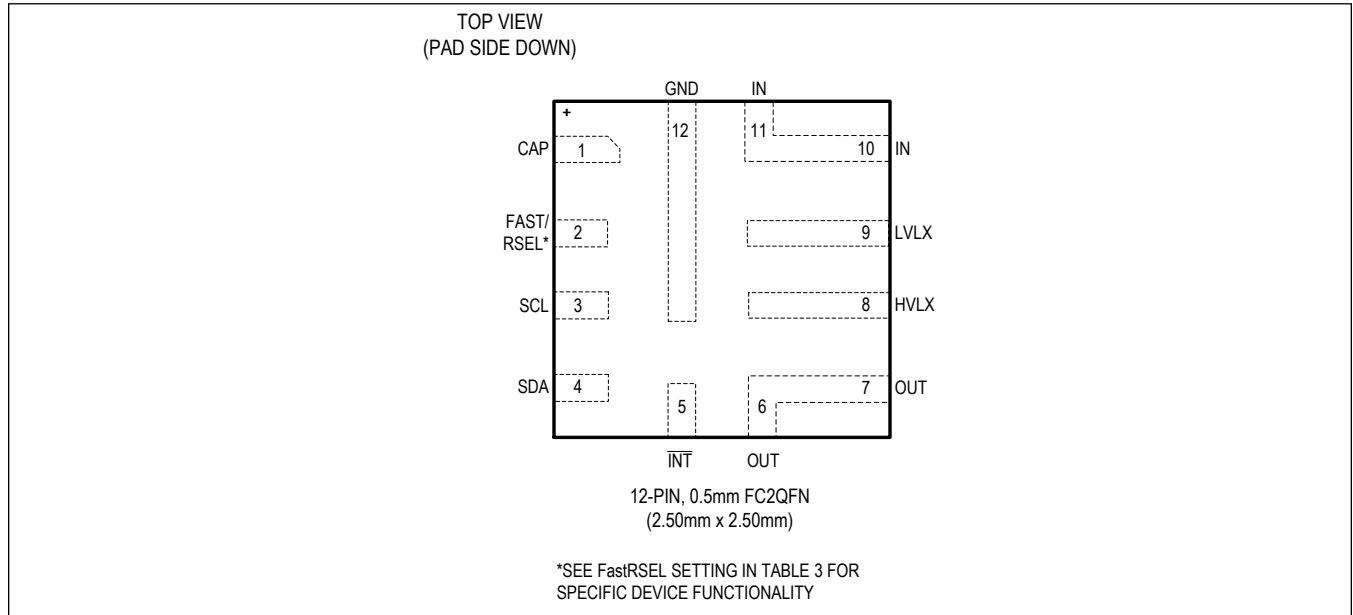
I²C-Controlled WLP



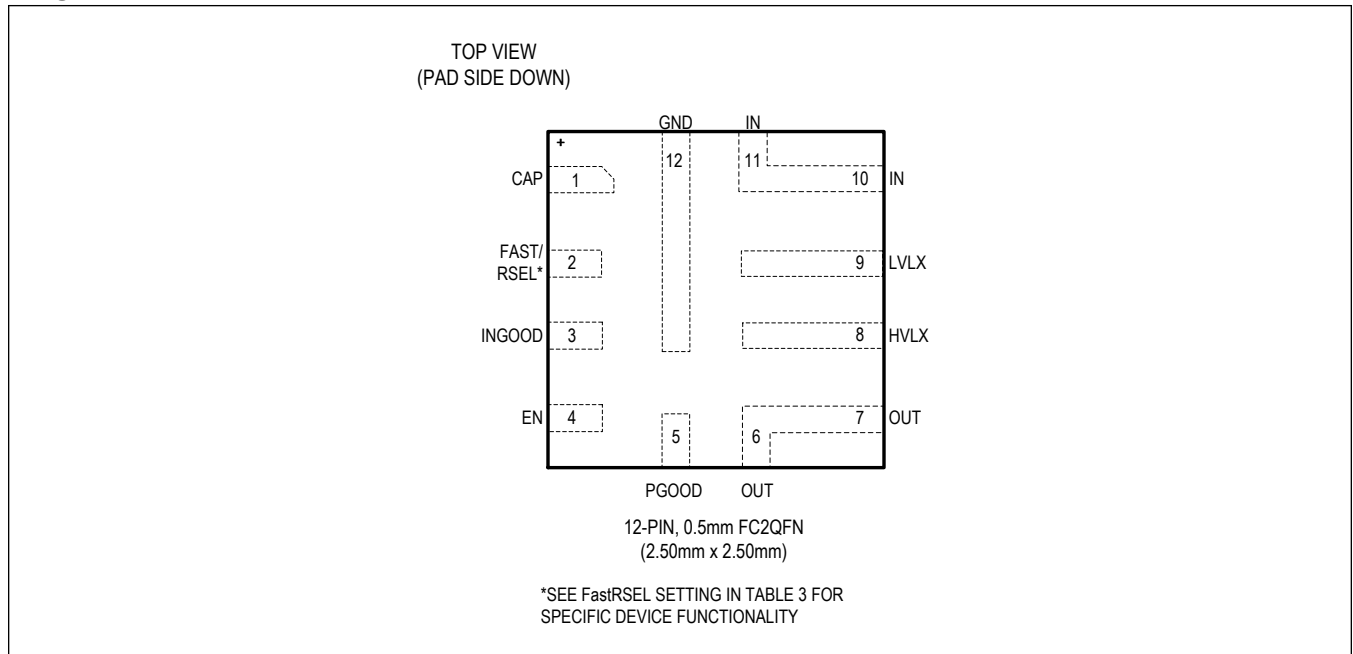
Single-Pin-Enabled WLP



I²C-Controlled FC2QFN



Single-Pin-Enabled FC2QFN



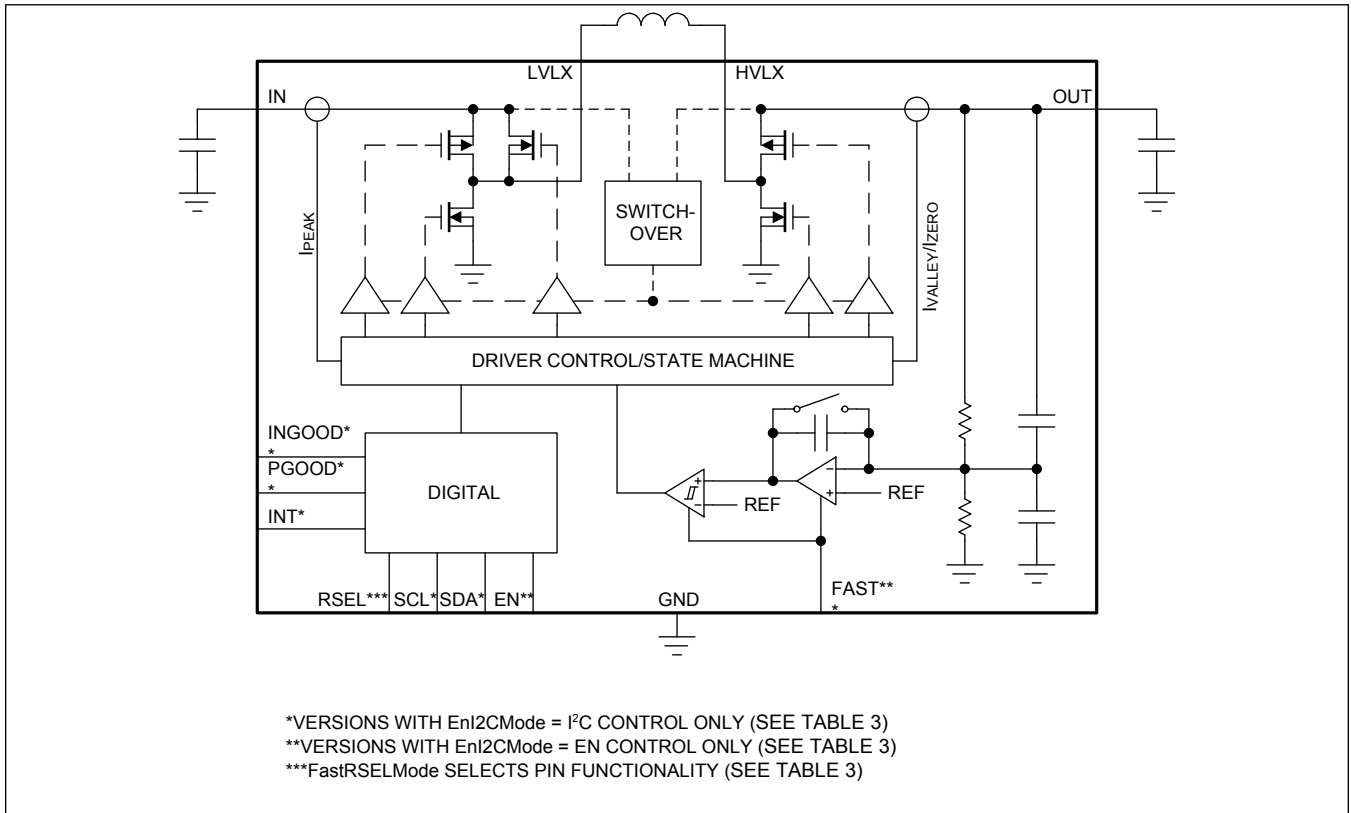
Pin Description

| PIN | | | | NAME | FUNCTION |
|--|-------------------------------|---|----------------------------------|--------|---|
| I ² C- Controlled WLP | Single-Pin- Enabled WLP | I ² C- Controlled FC2QFN | Single-Pin- Enabled FC2QFN | | |
| A1 | A1 | 1 | 1 | CAP | Bypass Capacitor Connection for Internal Supply. Connect through 470nF of capacitance to GND. |
| A2, B2, C2 | A2, B2, C2 | 12 | 12 | GND | Ground |
| A3, A4 | A3, A4 | 10, 11 | 10, 11 | IN | Input Supply. Bypass to GND with effective capacitance equal to the minimum of 5 μ F and the value of the derating curve (Figure 7) for a bias voltage V_{IN} placed as close to the device as possible. |
| B1 | B1 | 2 | 2 | FAST | Fast Transient Response. When FAST is high, the quiescent current of MAX20343/MAX20344 increases in order to improve response time to a load step. When FAST is low, the quiescent current is decreased to save power. The function of B1 is determined by the factory configuration of the device. See FastRSEL in Table 3 for the specific configuration of each device. |
| B1 | B1 | 2 | 2 | RSEL | Output Voltage Select. Connect a resistor from RSEL to GND based on the desired output voltage. See Figure 6. The function of B1 is determined by the factory configuration of the device. See FastRSEL in Table 3 for the specific configuration of each device. |
| B3, B4 | B3, B4 | 9 | 9 | LVLX | Switching Node. Connect to HVLX through a 1 μ H inductor if BBstFETScale = 0 or a 2.2 μ H inductor if BBstFETScale = 1. |
| C1 | — | 3 | — | SCL | I ² C Serial Clock Input. For I ² C versions, note the BBstEn setting. If a version is disabled by default an externally supplied source must be used for the I ² C interface to enable the output by I ² C command. |
| — | C1 | — | 3 | INGOOD | Input Power Good. LOW indicates that the CAP pin voltage is forced to V_{OUT} and the input voltage is below $V_{IN_UVLO_F}$ when $V_{OUT} \geq 3.3V$ and the soft-start period is complete. Power capabilities might be limited. If CAP is forced to V_{IN} , INGOOD does not function when $V_{IN} < V_{IN_UVLO_F}$. It is an open drain output and should be connected to an external logic supply using a pullup resistor. |
| C3, C4 | C3, C4 | 8 | 8 | HVLX | Switching Node. Connect to LVLX through a 1 μ H inductor if BBstFETScale = 0 or a 2.2 μ H inductor if BBstFETScale = 1. |
| D1 | — | 4 | — | SDA | I ² C Serial Data Input/Open-Drain Output. For I ² C versions, note the BBstEn setting. If a version is disabled by default an externally supplied source must be used for the I ² C interface to enable the output by I ² C command. |
| — | D1 | — | 4 | EN | Enable. Active-high. |

Pin Description (continued)

| PIN | | | | NAME | FUNCTION |
|--|-------------------------------|---|----------------------------------|-------------------------|--|
| I ² C- Controlled WLP | Single-Pin- Enabled WLP | I ² C- Controlled FC2QFN | Single-Pin- Enabled FC2QFN | | |
| D2 | — | 5 | — | $\overline{\text{INT}}$ | Interrupt Output. Open-drain, connect through pullup resistor to system logic supply. |
| — | D2 | — | 5 | PGOOD | Power Good Output. Indicates when output is ready for use. It is an open drain output and should be connected to an external logic supply using a pullup resistor. |
| D3, D4 | D3, D4 | 6, 7 | 6, 7 | OUT | Buck-Boost Output. If BBstFETScale = 0, bypass to GND with effective capacitance equal to twice the value of the derating curve (Figure 7) for a bias voltage V_{OUT} , placed as close to the device as possible. If BBstFETScale = 1, bypass to GND with effective capacitance equal to the value of the derating curve (Figure 7) for a bias voltage V_{OUT} , placed as close to the device as possible. |

Functional Diagram



Detailed Description

The MAX20343/MAX20344 is an ultra-low quiescent current, non-inverting buck-boost converter with 1A current capability at 3.5V intended for applications that require long run times while also demanding bursts of high current. A peak/valley current-controlled hysteretic architecture yields a fast transient response time with minimal settling time that allows the device to handle large load transients in high peak-power applications. The device has a unique control algorithm that seamlessly transitions between buck, buck-boost, and boost operation to minimize discontinuities and sub-harmonic noise in the output ripple.

The low, 1.9V startup voltage is compatible with a variety of power sources, and the near-zero minimum operating voltage extracts as much energy as possible from the source. Low inductance and capacitance requirements allow for a small total-solution size and make the MAX20343/MAX20344 well-suited for space-constrained applications. The device has a high efficiency and low noise that also makes it suitable for wireless and noise-sensitive applications such as LPWAN and optical sensor systems. It has an ultra-low, 3.5 μ A (typ) quiescent current and discontinuous conduction mode (DCM) to operate at low loads and extend run time in low average-power, battery-powered applications.

Startup Voltage

The MAX20343/MAX20344 is guaranteed to start up with a minimum input voltage of 1.9V. After device startup, an internal bootstrapping function allows the device to operate down to a 0.5V input. See the [Input Operating Voltage](#) section for more details.

Architectural Description

The MAX20343/MAX20344 buck-boost comprises a typical non-inverting buck-boost topology. [Figure 1](#) illustrates the basic structure of the regulator with arrows depicting the inductor current flow in each switching phase.

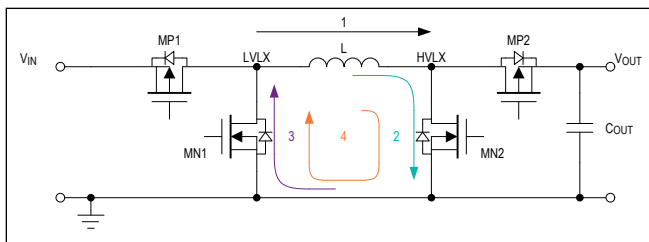


Figure 1. The Buck-Boost Regulator and Switching Phases

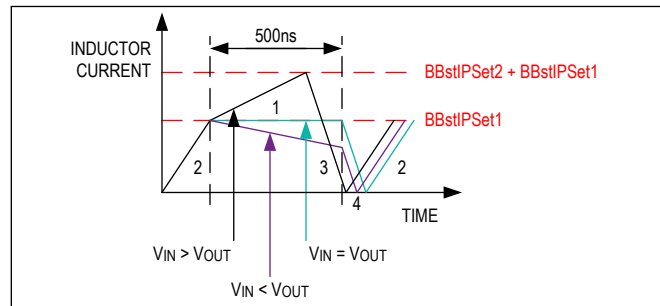


Figure 2. Buck-Boost Inductor Current in Buck-Boost Mode

Switching Phases

Depending on the buck-boost configurations, the topology enters different sequences of phases to generate the desired output voltage. Only two switches are on in each phase.

- Phase 1: MP1 on, MP2 on. Inductor charges.
- Phase 2: MP1 on, MN2 on. Inductor charges.
- Phase 3: MN1 on, MP2 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

Buck-Boost Mode

When `BBstMode = 0` (register 0x01[2]), the regulator operates in buck-boost mode. The inductor charges in Phase 2 up to `BBstIPSet1` (register 0x03[3:0]). The buck-boost then transitions to Phase 1. If $V_{IN} > V_{OUT}$, the inductor continues charging until either the current reaches `BBstIPSet1 + BBstIPSet2` (register 0x03[7:4]) or after a 500ns delay. If $V_{IN} \leq V_{OUT}$, the buck-boost waits for the 500ns timeout to elapse or until the current drops to the valley limit. Next, the regulator enters Phase 3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current

crossing threshold or falls below 0, the regulator freewheels in Phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters Phase 4 for approximately 30ns if $BBstZCCmpDis = 1$ (register 0x01[4]). The buck-boost skips Phase 4 when operating in CCM and $BBstZCCmpDis = 0$. The valley behavior is determined by $BBstZCCmpDis$. [Figure 2](#) shows the inductor current in buck-boost mode.

Buck-Only Mode

To maximize efficiency when $V_{IN} > V_{OUT}$, the buck-boost regulator has a buck-only mode. When $BBstMode = 1$, the regulator behaves as a synchronously rectified buck regulator. If the device is set to buck-only mode, the regulator never enters Phase 2. Instead, the inductor is always charged in Phase 1. The inductor charges until its current reaches $BBstIPSet1$ or the 500ns timeout elapses. The regulator then transitions to Phase 3 to provide a path to deliver the inductor current to the output. [Figure 3](#) shows the inductor current in buck-only mode.

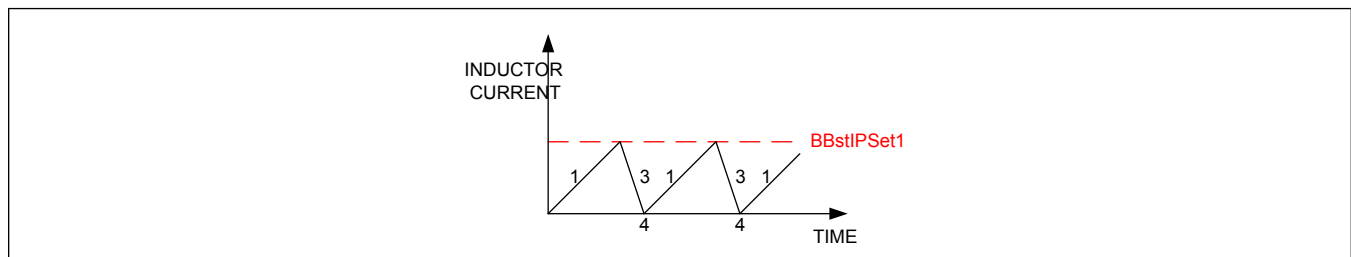


Figure 3. Buck-Boost Inductor Current in Buck-Only Mode

Buck-only mode reduces switching losses present in buck-boost mode. Buck-only mode should be used when V_{OUT} is always less than V_{IN} to maximize efficiency.

Inductor Peak and Valley Current Limits

The buck-boost regulator monitors the maximum and minimum values of the inductor current. If $BBstIPAdptDis = 1$ (register 0x04[1]), the peak currents are fixed to the values in $BBstIPSet$ (register 0x03) and the valley current is fixed to 0mA. If $BBstAdptDis = 0$, the peak and valley currents are allowed to change based on load requirements.

Peak currents are set in the $BBstIPSet$ register. $BBstIPSet1$ controls the peak current when $V_{IN} < V_{OUT}$ and begins the timeout period for Phase 1. $BBstIPSet2$ sets a secondary current limit in buck-boost mode when $V_{IN} > V_{OUT}$. The total inductor current limit when $V_{IN} > V_{OUT}$ is $BBstIPSet1 + BBstIPSet2$. The buck-boost regulator transitions from Phase 1 to Phase 3 if the inductor current reaches $BBstIPSet1 + BBstIPSet2$ or if the 500ns timeout has elapsed. Minimizing the difference between $BBstIPSet1$ and $BBstIPSet2$ reduces the output ripple, but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. [Figure 4](#) presents the safe operating area of $BBstIPSet2$ with respect to $BBstIPSet1$. Selecting values outside of the limits shown in [Figure 4](#) can cause unwanted behavior. [Figure 5](#) is a graphical guide to selecting combinations of $BBstIPSet1$ and $BBstIPSet2$ to balance efficiency for specific $BBstVSet$ values.

In order to control inrush current during startup, the MAX20343/MAX20344 forces discontinuous conduction mode during startup (valley current is always 0) and overrides the peak current settings with $BBstIP1SS$ and $BBstIP2SS$. Once the output reaches its final voltage, continuous conduction mode is allowed and the $BBstIPSet1$ and $BBstIPSet2$ settings are restored. See $BBstIP1SS$ and $BBstIP2SS$ ([Table 3](#)) for device-specific values.

The MAX20343/MAX20344 behavior when $BBstIPAdptDis = 0$ can be further defined with a zero current comparator. The device transitions to Phase 4 when its control loop detects a zero current crossing.

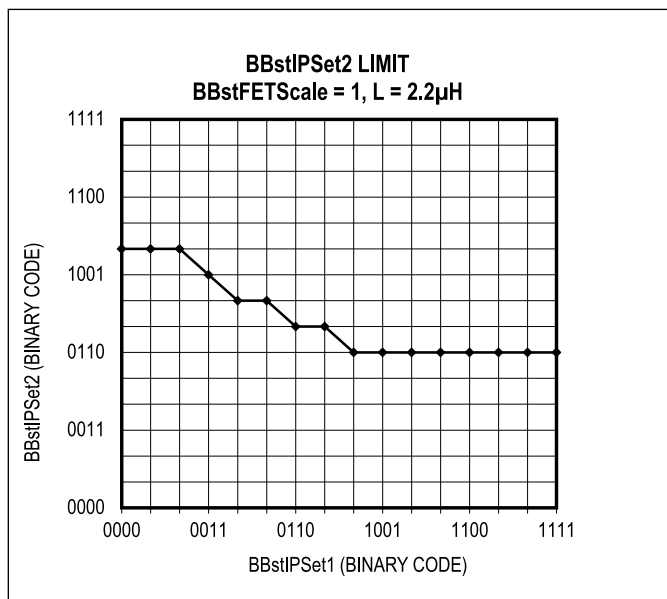


Figure 4. Minimum BBstIPSet2 Limit for Given BBstIPSet1 Setting

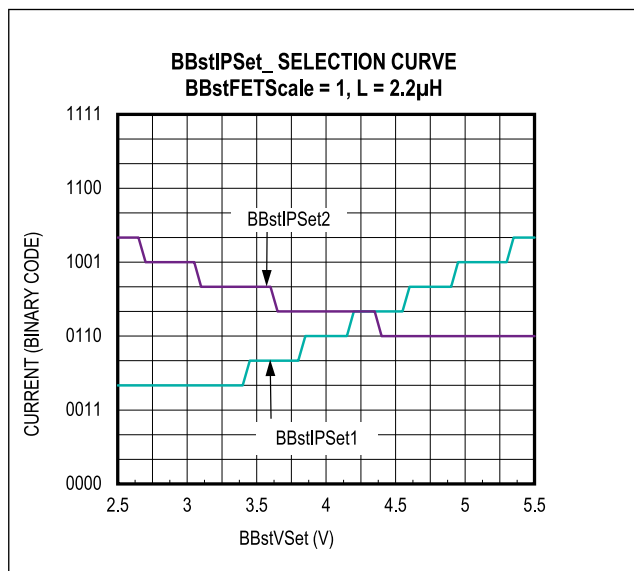


Figure 5. Recommended BBstIPSet1 and BBstIPSet2 Settings

When $BBstZCCmpDis = 1$ (register 0x01[4]), the zero crossing comparator is disabled and the buck-boost operates with only peak and valley current limits. In this configuration, the valley current limit acts as the zero crossing limit. In DCM, the valley limit is 0mA and is a true zero current crossing. In CCM, the peak and valley limits are automatically adjusted by the adaptive current control, so the effective zero current point might be larger than 0mA. This causes the MAX20343/MAX20344 to briefly enter Phase 4 each time the inductor current reaches the valley current threshold before transitioning to an inductor-charging phase. Setting $BBstZCCmpDis = 0$ enables the zero current comparator and the buck-boost operates with peak, valley, and zero crossing current limits. While the adaptive current loop adjusts the peak and valley currents, the zero crossing limit is fixed at 0mA. In DCM, the regulator functions similarly to when $BBstZCCmpDis = 1$. However, in CCM, the valley current is greater than the zero crossing current, so the regulator bypasses Phase 4 and directly enters an inductor-charging phase when the inductor current reaches the valley current threshold.

Disabling the zero current crossing comparator reduces the buck-boost output ripple. Enabling the comparator improves efficiency in CCM by removing the Phase 4 stage in CCM that is otherwise present when $BBstZCCmpDis = 1$.

Integrator Control Loop Disable

The MAX20343/MAX20344 contains an integrator in its control loop for normal operation. This integrator improves the load regulation for larger loads, but increases the transient response time. For applications where the output must quickly settle to a final regulation value to prevent noise injection during sensitive measurements (such as in PPG measurements), the integrator can be disabled so the regulator operates with a proportional-only control loop. The $BBstIntegEn$ bit (register 0x04[2]) enables and disables the integrator to speed response time on load transients (integrator off) or to increase the load capacity (integrator on). Note that when the integrator is disabled output stability is only guaranteed up to the maximum output power for input voltages down to 2.5V. To operate at lower input voltages, the output capacitance must be increased.

Input Operating Voltage

Operating at low input voltages enables a system to extract as much energy as possible from its energy source before shutting down. After startup and with $SwoFrIn = 0$, and $V_{OUT} \geq 3.2V$, the MAX20343/MAX20344 can operate to very low input voltages limited only by the amount of current that can be drawn effectively from the input. This allows a system to run the MAX20343/MAX20344 well below the minimum startup voltage, albeit at a reduced power capability.

When the input voltage is low, the R_{ON} of the input p-channel MOSFET increases. To offset the inherent increase in resistance, an n-channel MOSFET is present in parallel with the input MOSFET. The n-channel MOSFET is only enabled when the input voltage falls below $V_{IN_UVLO_F}$ to reduce switching losses at higher input voltages. In order to provide sufficient overdrive for the n-channel device, it is necessary to keep $V_{OUT} \geq 3.2V$. Therefore, high power operation below $V_{IN_UVLO_F}$ is only guaranteed if the output voltage is set to 3.2V or above.

Output Operating Power and Other Optimizations

The MAX20343/MAX20344 is a highly flexible device with many operating modes that allows the user to optimize the performance for their application. For applications like driving an LED for on the wrist PPG, settling time to a steady-state voltage during a load transient is critical. In such cases, the user benefits from a proportional-only output response (BBstIntegEn = 0, disabled), which trades an increased steady-state load regulation error for speed of settling. On the other hand, some applications are not as sensitive to response time, but benefit from the lower steady-state load regulation error provided when the integrator is enabled (BBstIntegEn = 1, enabled).

The efficiency can also be optimized by selecting the BBstFETScale setting according to which load region should be the focus for efficiency. If the application should primarily be optimized for light-load efficiency, the BBstFETScale = 1 (enabled) setting is preferable and vice-versa. Note that the improvement in efficiency at light loads with BBstFETScale = 1 comes with the tradeoff of lower maximum output power, which should be a consideration when configuring the setting. A comparison of performances for each setting can be found in the [Typical Operating Characteristics](#) section.

Finally, the MAX20343/MAX20344 features an internal switchover circuit (configured by SwoFrcIN), which manages the supply from which the internal circuitry of the buck-boost is driven. For applications where quiescent current is important and the primary operating mode is to boost the output, the switchover should be forced to the input (SwoFrcIN = 1). This is because the quiescent current when SwoFrcIN = 0 is drawn from the output, meaning that the input current is increased by the boost ratio and the efficiency of the conversion. However, in cases where a low input operating voltage must be supported, the SwoFrcIN = 0 setting allows the input voltage to drop much lower since the output voltage can be used to enhance the switching FETs of the buck-boost, keeping the on-resistance low. Note that when SwoFrcIN = 1, the buck-boost output automatically shuts down when V_{IN} falls below $V_{IN_UVLO_F}$ (1.782V typ). Instead when SwoFrcIN = 0 and $V_{OUT} \geq 3.2V$, the output continues to run even when V_{IN} falls very low and is only disabled when the output voltage falls below $V_{OUT_UVLO_F}$ or when the user disables the device. In this operating mode, the output power capabilities begin to decrease as the input voltage falls. To indicate that the input voltage has fallen to a critical level, the device generates an In UVLO status and interrupt for the system, which means that V_{IN} has dropped below $V_{IN_UVLO_F}$ and the source might be in a critical state. A comparison of performances for each setting can be found in the [Typical Operating Characteristics](#) section. For each combination of the above settings, there are tradeoffs to consider. [Table 2](#) below gives a general outline of the basic characteristics to expect with a given configuration.

Device Control

I²C-Controlled

The I²C-controlled versions of MAX20343/MAX20344 enable system flexibility by providing an interface between the device and a host microcontroller. Different parameters of the regulator, such as output voltage the inductor peak current levels, FET scaling, etc., can be optimized in real time for any application. While default values are programmed by the factory, new values can be set in the I²C registers. For device versions with I²C control take special care to observe the default setting of BBstEn in [Table 3](#). Versions with BBstEn = disabled by default need to have another power supply present that allows the system to wake the buck-boost by I²C command. In versions of the MAX20343/MAX20344 with an I²C interface and an RSEL voltage selection pin, the default voltage selected by the RSEL resistor can be overwritten over I²C after the OutGood (register 0x05[1]) status goes high.

The full configuration settings and status information provided through this interface are detailed in the register descriptions. The slave address information for I²C-controlled versions of MAX20343/MAX20344 can be found in the [Applications Information](#) section.

Single-Pin-Enabled

In the single-pin-enabled, fixed-programming versions of MAX20343/MAX20344, all configuration settings excluding the output voltage are programmed by the factory and cannot be modified in an application. Setting EN high turns on the buck-boost output and setting EN low turns off the buck-boost output. The BBstEn bit is ineffective in the Single-Pin-Enabled version. Two status pins, INGOOD and PGOOD, signal that the input and output voltages are ready to support the full system power requirements, respectively.

When the FAST/RSEL pin of a single-pin-enabled MAX20343/MAX20344 is configured to RSEL, the output voltage is set by the the RSEL resistor at startup. When the FAST/RSEL pin is configured to FAST, the output voltage is set by the factory.

Dynamic Voltage Scaling (DVS)

The output voltage of I²C-controlled MAX20343/MAX20344 devices can be changed at any point while the device is enabled without restarting the device. This feature is known as dynamic voltage scaling. DVS enables systems to operate at different voltage rails when the voltage or power requirements of the system change in different operating modes. By decreasing the voltage to the minimum value required by an operating mode, the overall system efficiency increases. The output voltage is set in BBstVSet[5:0] (register 0x02[5:0]).

RSEL Voltage Setting

RSEL is a unique, single-resistor output voltage selection method that minimizes quiescent current. Once power is applied at V_{IN} and the enable pin is brought high, the MAX20343/MAX20344 starts up and regulates to the minimum programmable voltage (2.5V). Once an internal PGOOD signal indicates that the voltage has reached an acceptable level, the device begins drawing up to 200 μ A from V_{IN} in order to read the resistor value on RSEL. This current is only present during the RSEL resistor detection time, typically 750 μ s. After the detection and output voltage programming period, the output increases to the set value. The output rise time is determined by the BBstRampEn setting. [Figure 6](#) illustrates this startup sequence.

RSEL has many benefits, including lower cost and smaller size. Only one resistor is needed versus the two resistors required in typical feedback connections. Another benefit of RSEL is that one regulator can be used in multiple projects with different output voltages just by changing a single standard 1% resistor. Lastly, RSEL eliminates wasting current continuously through feedback resistors for ultra-low power, battery-operated products. Select the RSEL resistor value by choosing the desired output voltage in [Table 1](#). Leaving RSEL open sets the output to the default voltage of the device (see [Table 3](#) for device configurations).

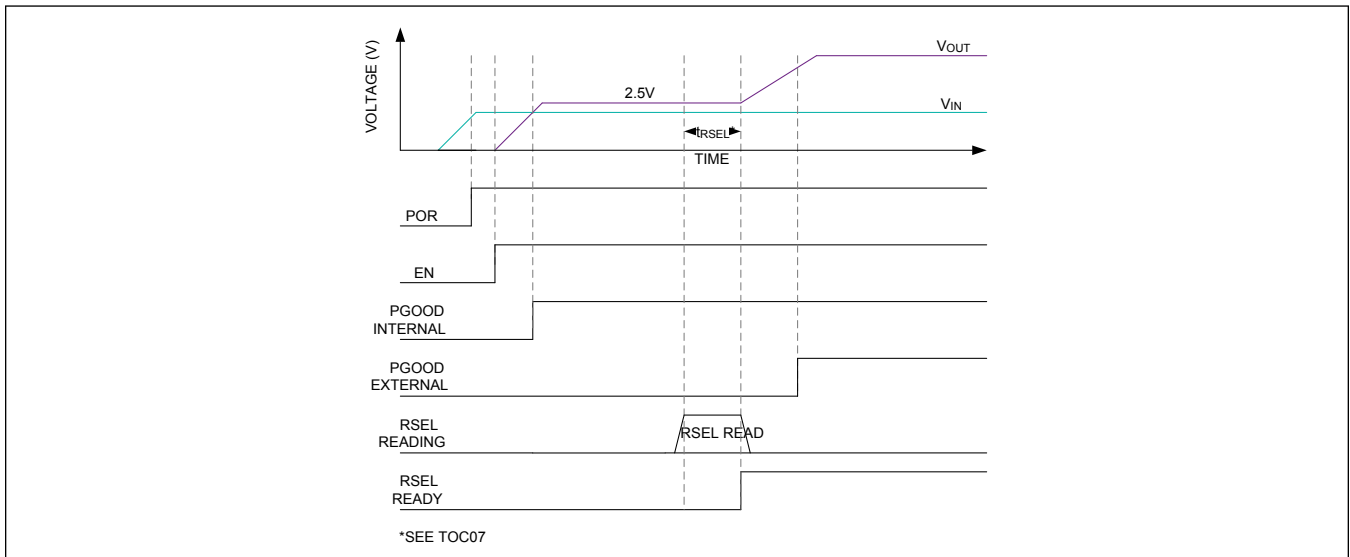


Figure 6. MAX20343/MAX20344 RSEL Startup Sequence

Table 1. RSEL SELECTION TABLE

| OUTPUT VOLTAGE (V) | STD RES 1% (kΩ) |
|--------------------|-----------------|
| Default | OPEN |
| 2.5 | 590 |
| 2.7 | 422 |
| 3.0 | 301 |
| 3.2 | 210 |
| 3.3 | 150 |
| 3.4 | 105 |
| 3.5 | 75 |
| 3.6 | 53.6 |
| 3.7 | 37.4 |
| 3.8 | 26.7 |
| 4.0 | 18.7 |
| 4.2 | 13.3 |
| 4.5 | 9.31 |
| 5.0 | 6.65 |
| 5.5 | SHORT |

Table 2. Characteristics and Device Settings

| CHARACTERISTICS | | | | | DEVICE SETTINGS | | |
|---|-------------------------------|--|---|---|-----------------|-------------|----------|
| MAX OUTPUT POWER ($V_{IN} = V_{OUT} \geq 3.2V$) (W) | QUIESCENT CURRENT | OPTIMIZED FOR: STEADY- STATE LOAD REGULATION ERROR OR LOAD-TRANSIENT SETTLING TIME | EFFICIENCY OPTIMIZED CURRENT RANGE | INPUT OPERATING VOLTAGE < $V_{IN_UVLO_F}$ | BBSTFETSCALE | BBSTINTEGEN | SWOFRGIN |
| ≥ 3.2 | INCREASED IN BOOST MODE | SETTLING TIME | HIGH | YES ($V_{OUT} \geq 3.2V$) | 0 | 0 | 0 |
| ≥ 3.2 | LOWEST | SETTLING TIME | HIGH | NO | 0 | 0 | 1 |
| ≥ 3.5 | INCREASED IN BOOST MODE | LOAD REGULATION | HIGH | YES ($V_{OUT} \geq 3.2V$) | 0 | 1 | 0 |
| ≥ 3.5 | LOWEST | LOAD REGULATION | HIGH | NO | 0 | 1 | 1 |
| ≥ 1.75 | INCREASED IN BOOST MODE | SETTLING TIME | LOW/ MEDIUM | YES ($V_{OUT} \geq 3.2V$) | 1 | 0 | 0 |
| ≥ 1.75 | LOWEST | SETTLING TIME | LOW/ MEDIUM | NO | 1 | 0 | 1 |
| ≥ 1.75 | INCREASED IN BOOST MODE | LOAD REGULATION | LOW/ MEDIUM | YES ($V_{OUT} \geq 3.2V$) | 1 | 1 | 0 |
| ≥ 1.75 | LOWEST | LOAD REGULATION | LOW/ MEDIUM | NO | 1 | 1 | 1 |

Register Map

MAX20343/MAX20344

| ADDRESS | NAME | MSB | | | | | | | LSB |
|-------------|---------------------------------|-----------------|------------|---------------|--------------|-----------------|-------------|---------------|--------------|
| USER | | | | | | | | | |
| 0x00 | ChipID[7:0] | ChipID[7:0] | | | | | | | |
| 0x01 | BBstCfg0[7:0] | BBstEn | BBstRampEn | BBstFast | BBstZCCmpDis | BBstLowEMI | BBstMode | BBstActDsc | BBstPsvDsc |
| 0x02 | BBstVSet[7:0] | BBFHighSh[1:0] | | BBstVSet[5:0] | | | | | |
| 0x03 | BBstIPSet[7:0] | BBstIPSet2[3:0] | | | | BBstIPSet1[3:0] | | | |
| 0x04 | BBstCfg1[7:0] | FstCmpEn | PasThrMode | SwoFrclN | - | - | BBstIntegEn | BBstIPAdptDis | BBstFETScale |
| 0x05 | Status[7:0] | - | - | - | - | - | - | OutGood | InUVLO |
| 0x06 | Int[7:0] | - | - | - | - | - | - | OutGoodInt | InUVLOInt |
| 0x07 | Mask[7:0] | - | - | - | - | - | - | OutGoodIntM | InUVLOIntM |
| 0x50 | LockMsk[7:0] | - | - | - | - | - | - | - | BBLck |
| 0x51 | LockUnlock[7:0] | PASSWD[7:0] | | | | | | | |

Register Details

[ChipID \(0x00\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field | ChipID[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---|
| ChipID | 7:0 | ChipID[7:0] indicates the version of the device in use. |

[BBstCfg0 \(0x01\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|-------------|
| Field | BBstEn | BBstRampEn | BBstFast | BBstZCCmpDis | BBstLowEMI | BBstMode | BBstActDsc | BBstPsvDsc |
| Reset | | | | | | | | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| BBstEn | 7 | Buck-Boost Enable 0 = Buck-boost disabled 1 = Buck-boost enabled |

| BITFIELD | BITS | DESCRIPTION |
|--------------|------|---|
| BBstRampEn | 6 | Buck-Boost Ramp Enable 0 = Output voltage setting transition is performed without intermediate steps 1 = Output voltage setting increases are performed with a digital ramp of 50mV every 50µs |
| BBstFast | 5 | Buck-Boost Pretrigger Mode Setting Increases the quiescent current of the buck-boost to improve output regulation during load transients. 0 = Normal, low quiescent current operation 1 = Fast response mode enabled. Quiescent current increased to 35µA (typ). |
| BBstZCCmpDis | 4 | Buck-Boost Zero-Crossing Comparator Disable. Latched internally, it can only be changed when BBstEn = 0 0 = Enabled 1 = Disabled |
| BBstLowEMI | 3 | Buck-Boost Low EMI Mode Increases the rise/fall time of HVLX/LVLX to reduce EMI, at the cost of efficiency. 0 = Normal operation 1 = Increase rise/fall time on HVLX/LVLX by 3x |
| BBstMode | 2 | Buck-Boost Operating Mode Configures the regulator to operate in buck-boost or buck-only mode. Latched internally, can only be changed while BBstEn = 0. 0 = Buck-boost mode 1 = Buck-only mode |
| BBstActDsc | 1 | Buck-Boost Active Discharge Control 0 = Buck-boost not actively discharged 1 = Buck-boost actively discharged on shutdown |
| BBstPsvDsc | 0 | Buck-Boost Passive Discharge Control 0 = Buck-boost not passively discharged 1 = Buck-boost passively discharged on shutdown |

BBstVSet (0x02)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---------------|---|---|---|---|---|
| Field | BBFHighSh[1:0] | | BBstVSet[5:0] | | | | | |
| Reset | | | | | | | | |
| Access Type | Write, Read | | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-----------|------|---|
| BBFHighSh | 7:6 | Buck-Boost f_{HIGH} Thresholds Selects the switching frequency threshold f_{HIGH} . If the buck-boost switching frequency exceeds the f_{HIGH} rising threshold, all the blocks are kept ON (I_Q is higher) until the frequency reaches the f_{HIGH} falling threshold. A small glitch on V_{OUT} can be present at the f_{HIGH} crossover. 00 = 25kHz rising / 6.125kHz falling 01 = 35kHz rising / 8.25kHz falling 10 = 50kHz rising / 12.5kHz falling 11 = 100kHz rising / 25kHz falling |
| BBstVSet | 5:0 | Buck-Boost Output Voltage Setting 2.5V to 5.5V, Linear Scale, 50mV increments 000000 = 2.5V 000001 = 2.55V ... ≥111100 = 5.5V |

BBstIPSet (0x03)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|---|-----------------|---|---|---|
| Field | BBstIPSet2[3:0] | | | | BBstIPSet1[3:0] | | | |
| Reset | | | | | | | | |
| Access Type | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION |
|------------|------|---|
| BBstIPSet2 | 7:4 | <p>Buck-Boost Nominal Maximum Peak Current Setting See buck-boost operation section for a description of the peak current settings. 0mA (minimum t_{ON}) to 618.75mA, linear scale, 41.25mA increments for BBstFETScale = 0. 0mA (minimum t_{ON}) to 375mA, linear scale, 25mA increments for BBstFETScale = 1.</p> <p>BBstFETScale = 0: 0000 = 0mA (minimum t_{ON}) 0001 = 50mA ... 1111 = 750mA</p> <p>Recommended settings $V_{OUT} \leq 2.65V$: 500mA(1010) $2.65V < V_{OUT} \leq 3.05V$: 450mA(1001) $3.05V < V_{OUT} \leq 3.60V$: 400mA(1000) $3.60V < V_{OUT} \leq 4.35V$: 350mA(0111) $V_{OUT} > 4.35V$: 300mA(0110)</p> <p>BBstFETScale = 1: 0000 = 0mA (minimum t_{ON}) 0001 = 25mA ... 1111 = 375mA</p> <p>Recommended settings $V_{OUT} \leq 2.65V$: 250mA(1010) $2.65V < V_{OUT} \leq 3.05V$: 225mA(1001) $3.05V < V_{OUT} \leq 3.60V$: 200mA(1000) $3.60V < V_{OUT} \leq 4.35V$: 175mA(0111) $V_{OUT} > 4.35V$: 150mA(0110)</p> |

| BITFIELD | BITS | DESCRIPTION |
|------------|------|---|
| BBstIPSet1 | 3:0 | <p>Buck-boost nominal peak current setting 1 Nominal peak current when charging inductor between V_{IN} and GND. See buck-boost operation section for a description of the peak current settings. 0mA (minimum t_{ON}) to 618.75mA, linear scale, 41.25mA increments for BBstFETScale = 0. 0mA (minimum t_{ON}) to 375mA, linear scale, 25mA increments for BBstFETScale = 1.</p> <p>BBstFETScale = 0: 0000 = 0mA (minimum t_{ON}) 0001 = 50mA ... 1111 = 750mA Recommended settings $V_{OUT} \leq 3.40V$: 200mA $3.40V < V_{OUT} \leq 3.80V$: 250mA(0101) $3.80V < V_{OUT} \leq 4.15V$: 300mA(0110) $4.15V < V_{OUT} \leq 4.55V$: 350mA(0111) $4.55V < V_{OUT} \leq 4.90V$: 400mA(1000) $4.90V < V_{OUT} \leq 5.30V$: 450mA(1001) $V_{OUT} > 5.30V$: 500mA(1010) BBstFETScale = 1: 0000 = 0mA (minimum t_{ON}) 0001 = 25mA ... 1111 = 375mA Recommended settings $V_{OUT} \leq 3.40V$: 100mA(0100) $3.40V < V_{OUT} \leq 3.80V$: 125mA(0101) $3.80V < V_{OUT} \leq 4.15V$: 150mA(0110) $4.20V < V_{OUT} \leq 4.55V$: 175mA(0111) $4.60V < V_{OUT} \leq 4.90V$: 200mA(1000) $4.95V < V_{OUT} \leq 5.30V$: 225mA(1001) $V_{OUT} > 5.30V$: 250mA(1010)</p> |

BBstCfg1 (0x04)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|-------------|-------------|-------------|---|---|-------------|---------------|--------------|
| Field | FstCmpEn | PasThrMode | SwoFrcIN | - | - | BBstIntegEn | BBstIPAdptDis | BBstFETScale |
| Reset | | | | - | - | | | |
| Access Type | Write, Read | Write, Read | Write, Read | - | - | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|------------|------|--|
| FstCmpEn | 7 | <p>FAST Comparator Enable The FAST mode comparator is enabled by the logical AND of the FAST pin and FstCmpEn. 0 = FAST pin does not control FAST mode 1 = FAST pin can set the device into FAST mode</p> |
| PasThrMode | 6 | <p>Pass Through Mode Bypasses the regulator to connect V_{OUT} to V_{IN}. This can only be enabled when BBstEn = 0 (register 0x01). 0 = Pass Through Mode disabled 1 = Pass Through Mode enabled. Enable only when BBstEn = 0.</p> |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|--|
| SwoFrcIN | 5 | Force Switch-Over Controls how the device powers the internal circuitry. 0 = Switch-over supply forced to V_{OUT} when $V_{OUT} > V_{OUT_UVLO_R}$. 1 = Switch-over supply forced to V_{IN} . |
| BBstIntegEn | 2 | Buck-Boost Integrator Enable The Integrator can be disabled to improve settling time on load transients at the cost of load regulation error. Latched internally, it can only be changed when BBstEn = 0. 0 = Integrator disabled 1 = Integrator enabled |
| BBstIPAdptDis | 1 | Adaptive Peak/Valley Current Adjustment Disable 0 = Enabled 1 = Disabled, peak current fixed to the values set by BBstIPSet1 and BBstIPSet2. Valley current is fixed to 0mA. This setting is equivalent to forcing discontinuous conduction mode and greatly diminishes the output power capability of the part. Generally this is not a recommended setting. |
| BBstFETScale | 0 | FET Scale Reduces FET sizes by a factor of 2. This setting can be used to optimize efficiency for lighter loads if it is acceptable to support lower maximum output power. If BBstFETScale = 0, the part requires a 1 μ H inductor and at least twice the derated capacitance in Figure 9. If BBstFETScale = 1, the part requires a 2.2 μ H inductor and at least the derated capacitance in Figure 9. Latched internally, it can only be changed when BBstEn = 0. 0 = FET scaling disabled 1 = FET scaling enabled |

Status (0x05)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|-----------|-----------|
| Field | – | – | – | – | – | – | OutGood | InUVLO |
| Reset | – | – | – | – | – | – | | |
| Access Type | – | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---|
| OutGood | 1 | Status of Output Voltage 0 = Output has not reached full power capability 1 = Output voltage is high enough to support full power capability |
| InUVLO | 0 | Status register showing whether input voltage is low enough to enable parallel input NMOS. 0 = V_{IN} high enough for full power operation 1 = Power may be limited due to low V_{IN} |

Int (0x06)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|------------|-----------|
| Field | – | – | – | – | – | – | OutGoodInt | InUVLOInt |
| Reset | – | – | – | – | – | – | | |
| Access Type | – | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|------------|------|---------------------------------------|
| OutGoodInt | 1 | Change in OutGood caused an interrupt |
| InUVLOInt | 0 | Change in InUVLO caused an interrupt |

Mask (0x07)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|-----------------|-------------|
| Field | - | - | - | - | - | - | OutGoodInt M | InUVLOIntM |
| Reset | - | - | - | - | - | - | | |
| Access Type | - | - | - | - | - | - | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|-------------|------|---|
| OutGoodIntM | 1 | OutGoodIntM masks the OutGoodInt interrupt. 0 = Not masked 1 = Masked |
| InUVLOIntM | 0 | InUVLOIntM masks the InUVLOInt interrupt. 0 = Not masked 1 = Masked |

LockMsk (0x50)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|-------------|
| Field | - | - | - | - | - | - | - | BBLck |
| Reset | - | - | - | - | - | - | - | 0x1 |
| Access Type | - | - | - | - | - | - | - | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| BBLck | 0 | Lock Mask for Buck-Boost Registers 0 = Buck-Boost Registers not masked from locking/unlocking 1 = Buck-Boost Registers masked from locking/unlocking |

LockUnlock (0x51)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field | PASSWD[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| PASSWD | 7:0 | Lock/Unlock Password Write 0xAA with BBLck unmasked to lock the BBstVSet[5:0] field Write 0x55 with BBLck unmasked to unlock the BBstVSet[5:0] field |

Applications Information

Input and Output Capacitance

The MAX20343/MAX20344 is designed to be compatible with small case-size ceramic capacitors. As such, the device has low-input and low-output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) capacitors. The sample derating curve for a 22 μ F nominal value capacitor in [Figure 7](#) presents the minimum capacitance required at IN and OUT. To ensure stability and low noise, the capacitance value under bias on IN should be the minimum of 5 μ F and the value of [Figure 7](#) at the lowest expected V_{IN} . The minimum capacitance value under bias on OUT should be equal to the value of [Figure 7](#) at the lowest expected V_{OUT} for BBstFETScale = 1 and twice that value for BBstFETScale = 0. Note that the derating curve in [Figure 7](#) is a sample only, refer to the manufacturer's derating curve of the actual capacitor selected to ensure that the minimum capacitance values under bias are met.

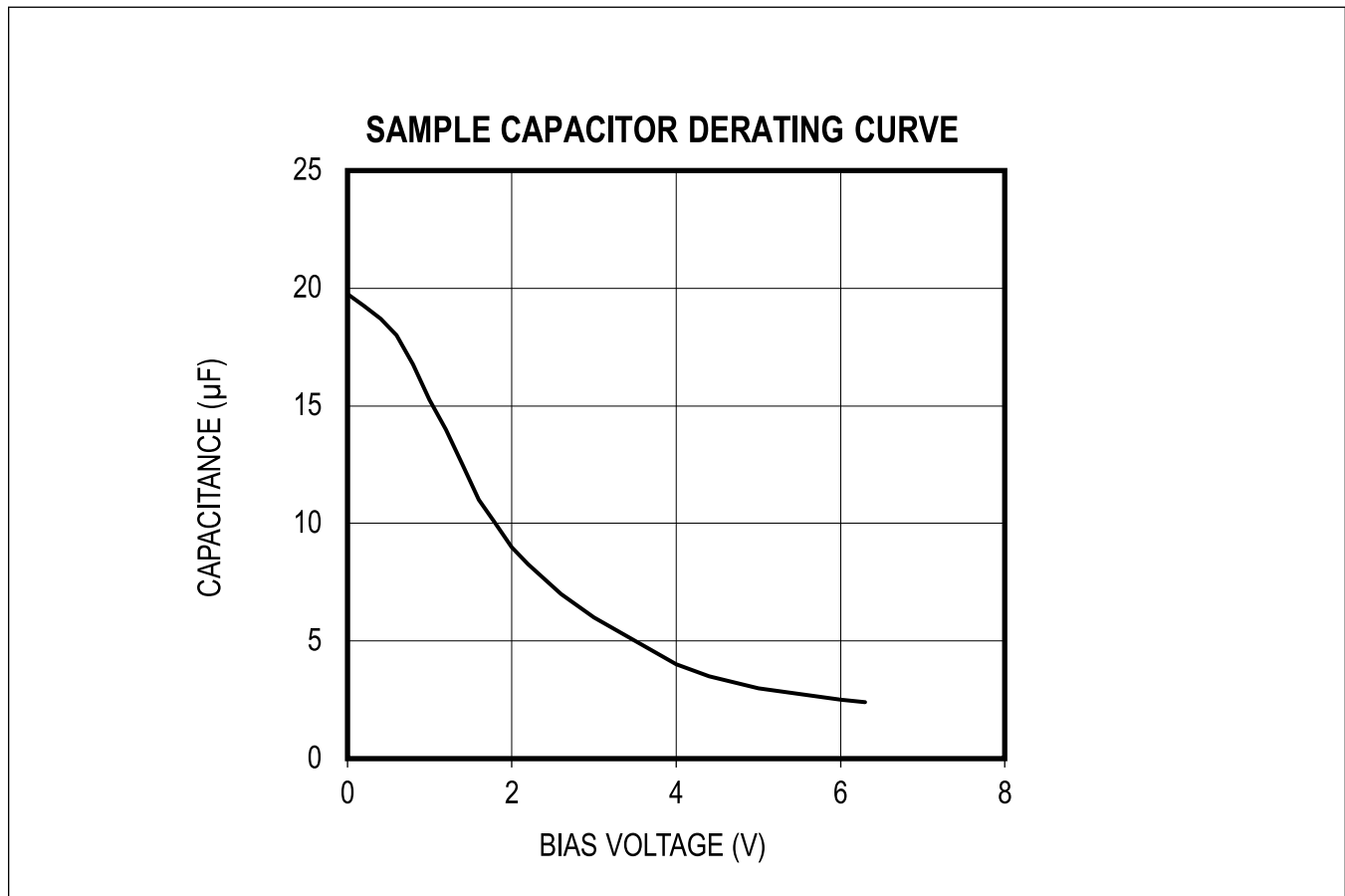


Figure 7. Buck-Boost Required Minimum Input/Output Capacitance

Inductor Selection

Inductor selection for the MAX20343/MAX20344 should be optimized for the intended application. A 2.2µH inductor value is required when FET scaling is enabled (BBstFETScale = 1) while 1µH is required when FET scaling is disabled (BBstFETScale = 0). Aside from the inductor value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is obtained using the following equation:

$$I_{L_MAX} = \frac{V_{OUT_MAX} \times I_{OUT_MAX}}{\eta \times V_{IN_MIN}}$$

Where,

V_{OUT_MAX} is the maximum expected operating voltage,

I_{OUT_MAX} is the maximum expected output current,

V_{IN_MIN} is the minimum expected operating input voltage,

η is the expected worst case efficiency in the minimum input voltage and maximum output power case (see the [Typical Operating Characteristics](#) for help in estimating efficiency).

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. In order to determine the required inductor saturation current, the peak current must be calculated. The peak current for this converter can be calculated as:

$$I_{L_PEAK} = I_{L_MAX} + (1.1 \times \text{BBstIPSet1})$$

Where BBstIPSet1 is the peak current setting described in register 0x03. When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases ferrite inductors should be avoided as they tend to exhibit poor AC characteristics especially in discontinuous conduction mode (DCM).

Soft-Start

Current at startup is limited by forcing DCM. This allows startup of the system with input voltages down to 1.9V.

I²C Interface

The MAX20343/MAX20344 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The MAX20343/MAX20344 can support I²C frequencies from 0kHz to 680kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Slave Address

In the MAX20343/MAX20344, the slave address is configured at the factory by the SlaveAddr bit to be either 0b1101000 (0x68) plus the Read/Write bit or 0b1101100 (0x6C) plus the Read/Write bit. For versions with the 7-bit slave address 0x68 Set the Read/Write bit high to configure the MAX20343 to read mode (0xD1) or set the Read/Write bit low to configure the MAX20343/MAX20344 to write mode (0xD0). For versions with the 7-bit slave address 0x6C Set the Read/Write bit high to configure the MAX20343/MAX20344 to read mode (0xD8) or set the Read/Write bit low to configure the MAX20343/MAX20344 to write mode (0xD9). See SlaveAddr in [Table 3](#) for the slave address for a given part number. The address is the first byte of information sent to the MAX20343/MAX20344 after the START condition.

Start, Stop, and Repeated Start Conditions

When writing to the MAX20343/MAX20344 using I²C, the master sends a START condition (S) followed by the MAX20343/MAX20344 I²C write address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See [Figure 8](#).

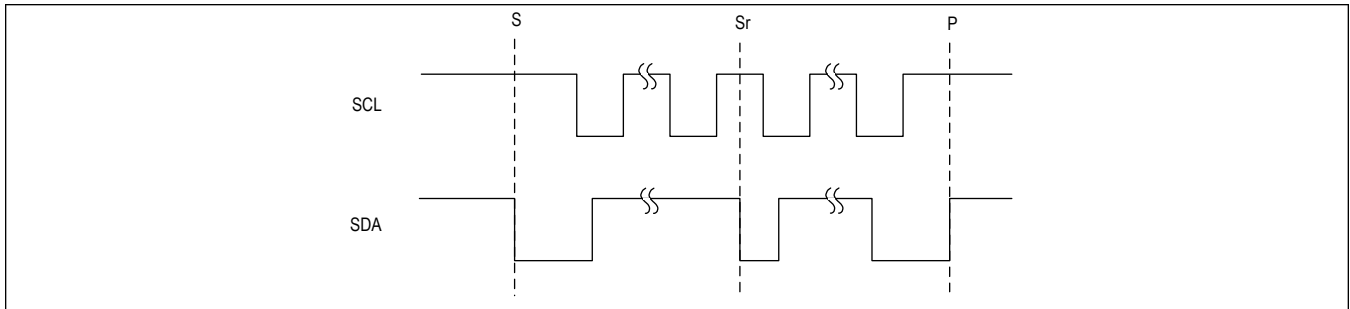


Figure 8. I²C START, STOP, and REPEATED START Conditions

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the [Start, Stop, and Repeated Start Conditions](#) section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 9). The following procedure describes the single byte write operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends 8 data bits.
- The slave asserts an ACK on the data line.
- The master generates a STOP condition.

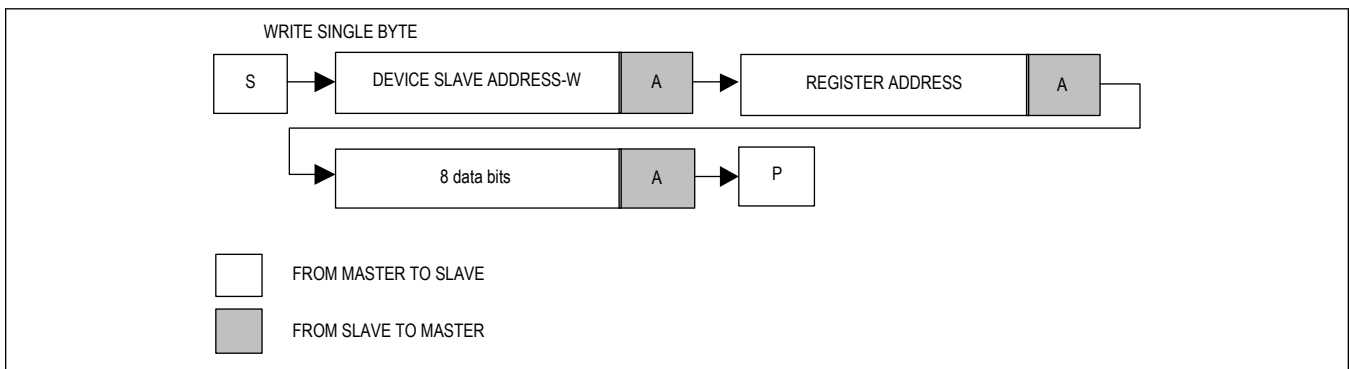


Figure 9. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 10). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).

- The master sends 8 data bits.
- The slave asserts an ACK on the data line.
- Repeat 6 and 7 N-1 times.
- The master generates a STOP condition.

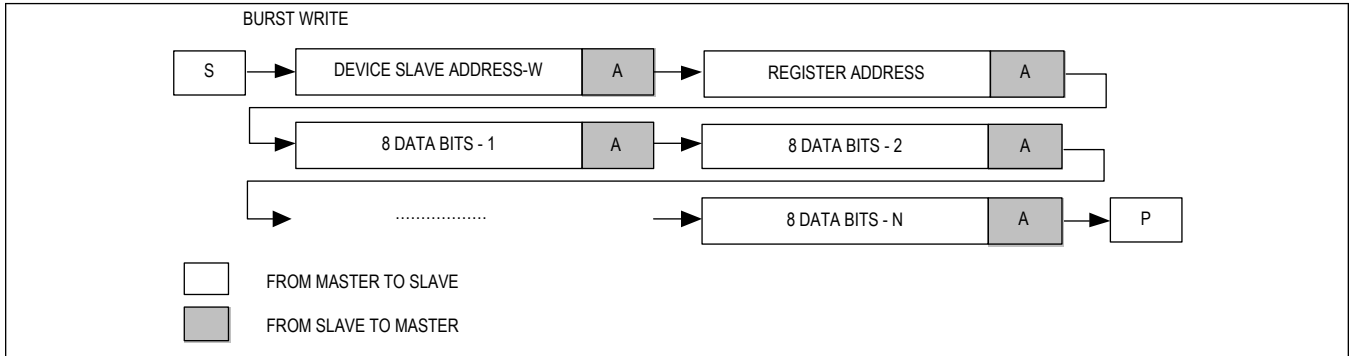


Figure 10. Burst Write Sequence

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 11). The following procedure describes the single byte read operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends a REPEATED START condition.
- The master sends the 7-bit slave address plus a read bit (high).
- The addressed slave asserts an ACK on the data line.
- The slave sends 8 data bits.
- The master asserts a NACK on the data line.
- The master generates a STOP condition.

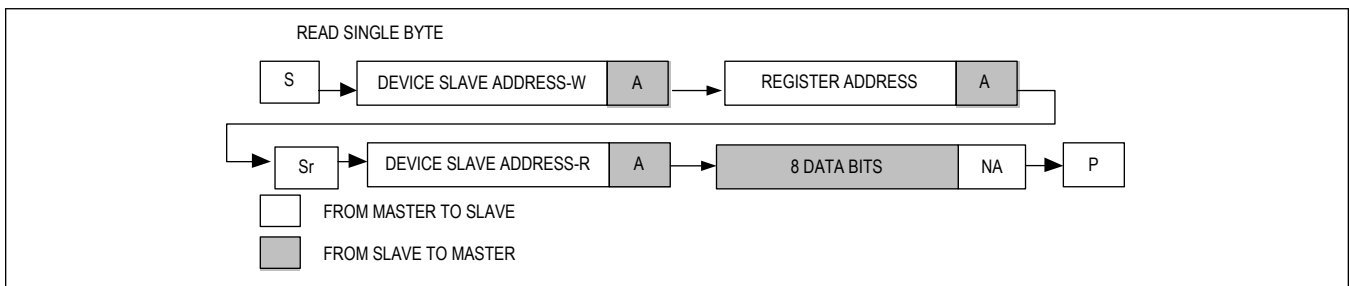


Figure 11. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 12). The following procedure describes the burst byte read operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.

- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends a REPEATED START condition.
- The master sends the 7-bit slave address plus a read bit (high).
- The slave asserts an ACK on the data line.
- The slave sends 8 data bits.
- The master asserts an ACK on the data line.
- Repeat 9 and 10 N-2 times.
- The slave sends the last 8 data bits.
- The master asserts a NACK on the data line.
- The master generates a STOP condition.

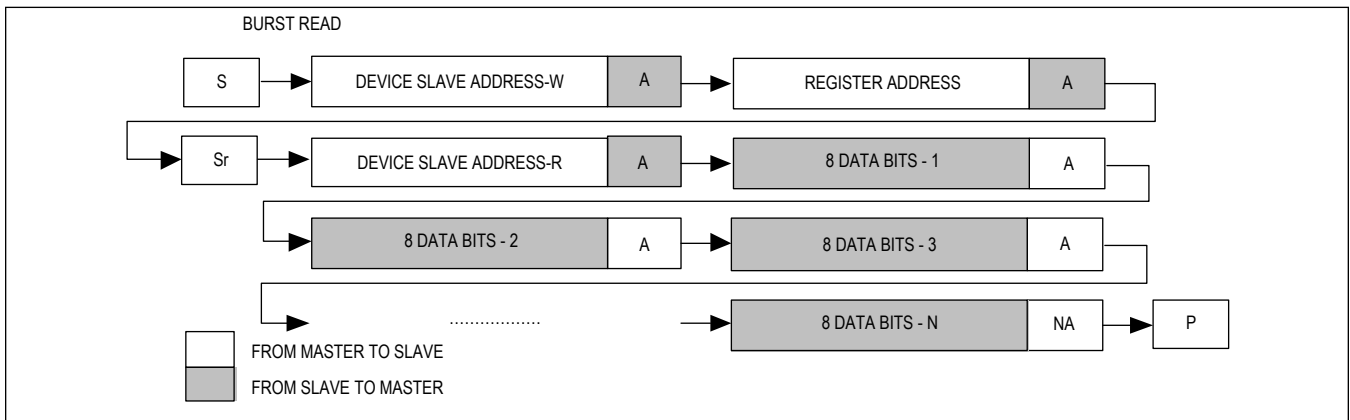


Figure 12. Burst Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20343/MAX20344 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (Figure 13). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

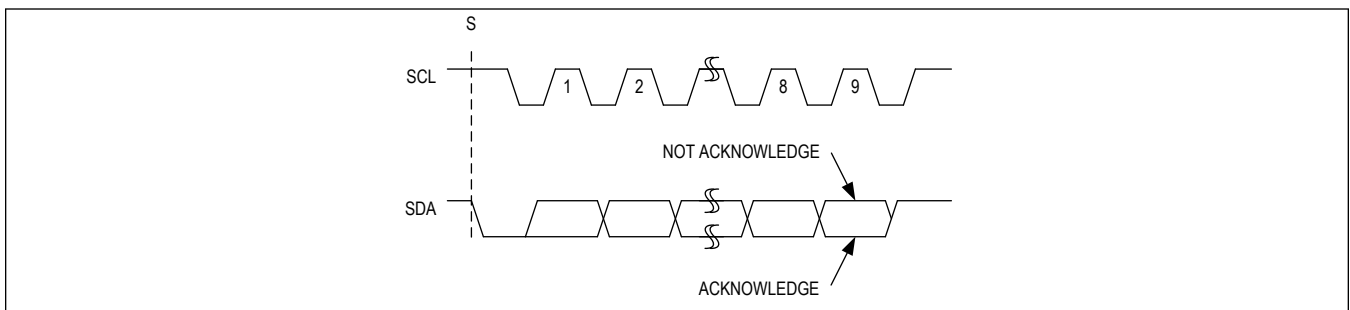


Figure 13. Acknowledge Bits

Register Values

The following tables provide the device and register bit default values for the various available parts.

Table 3. Register Bit Default Values

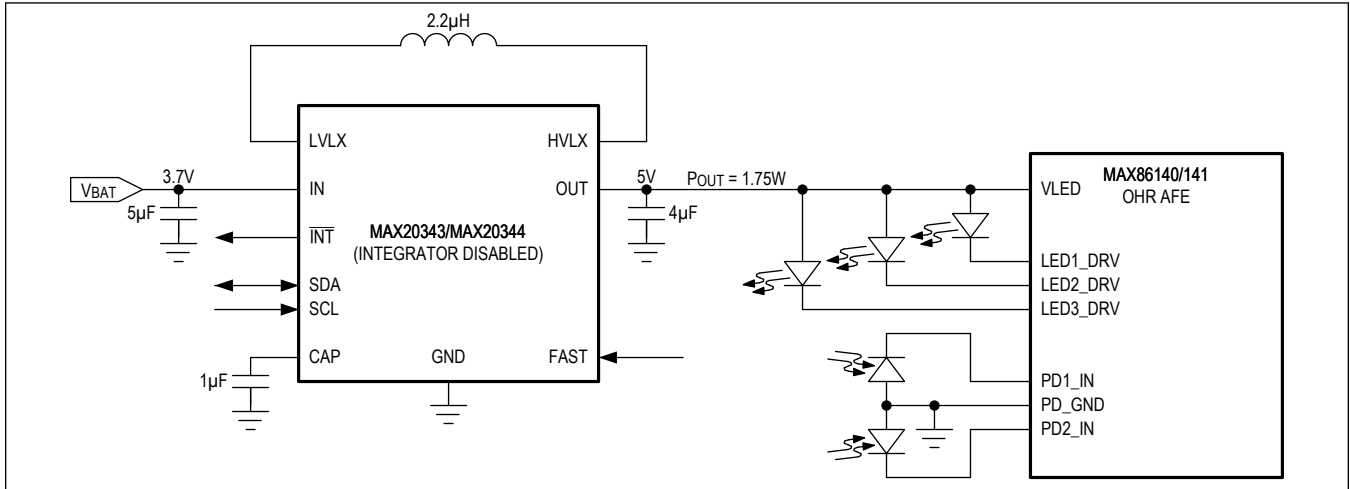
| REGISTER BITS | DEVICE | | | | | | | |
|-----------------|---|---------------------------------------|---|---|---|---|---------------------------------------|---------------------------------------|
| | MAX20343B | MAX20343E/ MAX20344E | MAX20343F | MAX20343G/ MAX20343K | MAX20343H | MAX20343I | MAX20343J | MAX20343N |
| BBstEn | Disabled | Disabled | Enabled | Disabled | Disabled | Disabled | Disabled | Enabled |
| BBstRampEn | Single Step | Single Step | Single Step | Single Step | Single Step | Single Step | Single Step | Single Step |
| BBstFast | Low I _Q Mode | Low I _Q Mode | Low I _Q Mode | Low I _Q Mode | Low I _Q Mode | Low I _Q Mode | Low I _Q Mode | Low I _Q Mode |
| BBstZCCmpDis | ZCC Disabled | ZCC Disabled | ZCC Disabled | ZCC Disabled | ZCC Disabled | ZCC Disabled | ZCC Disabled | ZCC Disabled |
| BBstLowEMI | High Efficiency | High Efficiency | High Efficiency | High Efficiency | High Efficiency | High Efficiency | High Efficiency | High Efficiency |
| BBstMode | Buck-Boost | Buck-Boost | Buck-Boost | Buck-Boost | Buck-Boost | Buck-Boost | Buck-Boost | Buck-Boost |
| BBstActDsc | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) | Active Discharge on Shutdown (50ms) |
| BBstPsvDsc | Passive Discharge in Shutdown | Passive Discharge in Shutdown | Passive Discharge in Shutdown | Passive Discharge in Shutdown | Passive Discharge in Shutdown | No Passive Discharge | Passive Discharge in Shutdown | Passive Discharge in Shutdown |
| BBstFHighSh | 100kHz/ 25kHz | 100kHz/ 25kHz | 100kHz/ 25kHz | 100kHz/ 25kHz | 100kHz/ 25kHz | 100kHz/ 25kHz | 100kHz/ 25kHz | 100kHz/ 25kHz |
| SwoFrcIn | Switch-Over Forced to V _{OUT} when OutGood = 1 | Switch-Over Forced to V _{IN} | Switch-Over Forced to V _{OUT} when OutGood = 1 | Switch-Over Forced to V _{OUT} when OutGood = 1 | Switch-Over Forced to V _{OUT} when OutGood = 1 | Switch-Over Forced to V _{OUT} when OutGood = 1 | Switch-Over Forced to V _{IN} | Switch-Over Forced to V _{IN} |
| BBstVSet[5:0] | 3.20V | 5.00V | 3.30V | 3.20V | 3.30V | 4V | 2.85V | 5.00V |
| BBstIntegEn | Disable Integrator | Disable Integrator | Enable Integrator | Disable Integrator | Enable Integrator | Enable Integrator | Disable Integrator | Disable Integrator |
| BBstIPAdptDis | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled | Adaptive Peak Current Enabled |
| BBstFETScale | FET Scaling Enabled | FET Scaling Enabled | FET Scaling Disabled | FET Scaling Enabled | FET Scaling Disabled | FET Scaling Disabled | FET Scaling Enabled | FET Scaling Disabled |
| FastRSELMode | FAST | FAST | FAST | FAST | RSEL | RSEL | RSEL | RSEL |
| EnI2CMode | I ² C Control | I ² C Control | I ² C Control | I ² C Control | EN Mode | EN Mode | EN Mode | EN Mode |
| BBstIPSet1[3:0] | 100mA | 225mA | 400mA | 100mA | 400mA | 300mA | 100mA | 450mA |
| BBstIPSet2[3:0] | BBstIPSet1 + 200mA | BBstIPSet1 + 150mA | BBstIPSet1 + 600mA | BBstIPSet1 + 200mA | BBstIPSet1 + 600mA | BBstIPSet1 + 350mA | BBstIPSet1 + 225mA | BBstIPSet1 + 300mA |
| BBstIP1SS[3:0] | 375mA | 375mA | 750mA | 375mA | 750mA | 350mA | 375mA | 375mA |
| BBstIP2SS[3:0] | BBstIPSet1 + 75mA | BBstIPSet1 + 75mA | BBstIPSet1 + 150mA | BBstIPSet1 + 75mA | BBstIPSet1 + 150mA | BBstIPSet1 + 100mA | BBstIPSet1 + 75mA | BBstIPSet1 + 75mA |
| Slave_Addr | 0xD0/0xD1 | 0xD0/0xD1 | 0xD0/0xD1 | 0xD0/0xD1 | 0xD0/0xD1 | 0xD0/0xD1 | 0xD0/0xD1 | 0xD0/0xD1 |

Table 4. Register Default Values

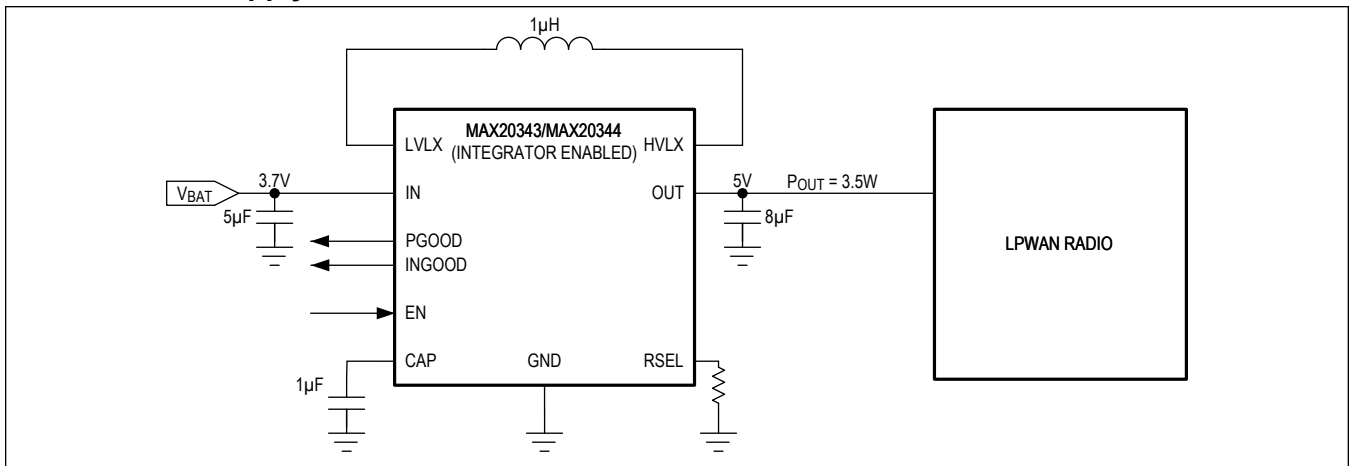
| REGISTER | NAME | DEVICE | | | | | | | | |
|----------|------------|-----------|-------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| | | MAX20343B | MAX20343E/ MAX20344E | MAX20343F | MAX20343G | MAX20343H | MAX20343I | MAX20343K | MAX20343J | MAX20343N |
| 0x00 | ChipID | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 | 0x02 | 0x03 | 0x03 | 0x03 |
| 0x01 | BBstCfg0 | 0x13 | 0x13 | 0x93 | 0x13 | 0x13 | 0x12 | 0x13 | 0x13 | 0x93 |
| 0x02 | BBstVSet | 0xCE | 0xF2 | 0xD0 | 0xCE | 0xD0 | 0xDE | 0xCE | 0xC7 | 0xF2 |
| 0x03 | BBstISet | 0x84 | 0x69 | 0xC8 | 0x84 | 0xC8 | 0x76 | 0x84 | 0x94 | 0x69 |
| 0x04 | BBstCfg1 | 0x81 | 0xA1 | 0x84 | 0x81 | 0x84 | 0x84 | 0x81 | 0xA1 | 0xA0 |
| 0x05 | Status | 0x00 | 0x00 | 0x02 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0x06 | Int | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| 0x07 | Mask | 0x03 | 0x03 | 0x03 | 0x03 | 0x03 | 0x03 | 0x03 | 0x03 | 0x03 |
| 0x50 | LockMsk | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 |
| 0x51 | LockUnlock | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF | 0xFF |

Typical Application Circuits

Optical Heart Rate LED Supply



LPWAN Radio Supply



Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|-----------------|-----------------|-------------|
| MAX20343BEFC+* | -40°C to +85°C | 12 FC2QFN |
| MAX20343BEFC+T* | -40°C to +85°C | 12 FC2QFN |
| MAX20343EEFC+* | -40°C to +85°C | 12 FC2QFN |
| MAX20343EEFC+T* | -40°C to +85°C | 12 FC2QFN |
| MAX20343GEFC+* | -40°C to +85°C | 12 FC2QFN |
| MAX20343GEFC+T* | -40°C to +85°C | 12 FC2QFN |
| MAX20343HEFC+ | -40°C to +85°C | 12 FC2QFN |
| MAX20343HEFC+T | -40°C to +85°C | 12 FC2QFN |
| MAX20344EAFC+ | -40°C to +125°C | 12 FC2QFN |
| MAX20344EAFC+T | -40°C to +125°C | 12 FC2QFN |
| MAX20343BEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343BEWE+T | -40°C to +85°C | 16 WLP |
| MAX20343EEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343EEWE+T | -40°C to +85°C | 16 WLP |
| MAX20343FEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343FEWE+T | -40°C to +85°C | 16 WLP |
| MAX20343GEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343GEWE+T | -40°C to +85°C | 16 WLP |
| MAX20343IEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343IEWE+T | -40°C to +85°C | 16 WLP |
| MAX20343JEWE+ | -40°C to +85°C | 16 WLP |
| MAX20343JEWE+T | -40°C to +85°C | 16 WLP |
| MAX20343KEWE+* | -40°C to +85°C | 16 WLP |
| MAX20343KEWE+T* | -40°C to +85°C | 16 WLP |
| MAX20343NEWE+* | -40°C to +85°C | 16 WLP |
| MAX20343NEWE+T* | -40°C to +85°C | 16 WLP |

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

*Future product—contact factory for availability.

See [Table 3](#) for specific device settings and defaults to select a part.

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|--|
| 0 | 3/19 | Initial release | — |
| 1 | 3/19 | Corrected typos; updated BBstFETScale Bit Description (and corrected typo), and added future product designation to MAX20343EEWE+ and MAX20343EEWE+T in the <i>Ordering Information</i> | 19, 21, 25, 34 |
| 2 | 4/19 | Updated the <i>General Description, Benefits and Features, Absolute Maximum Ratings, Package Information, Pin Configuration, Pin Description, Buck-Boost Mode, and Inductor Peak and Valley Current Limits</i> sections, and <i>Register Map</i> and BBstCfg0 (0x01) tables; added MAX20343BEFC+ and MAX20343BEFC+T as future parts to the <i>Ordering Information</i> | 1, 3, 12–13, 16, 18, 20–21, 34 |
| 3 | 6/19 | Removed future part designation from MAX20343EEWE+ and MAX20343EEWE+T in the <i>Ordering Information</i> | 34 |
| 4 | 1/20 | Updated the <i>General Description, Benefits and Features, Electrical Characteristics, Typical Operating Characteristics, Pin Description, Startup Voltage, Architectural Design, Switching Phases, Buck-Boost Mode, Buck-Only Mode, Inductor Peak and Valley Current Limits, Integrator Control Loop Disable, Input Operating Voltage, I²C-Controlled, Input and Output Capacitance, I²C Interface, Slave Address, and Ordering Information</i> sections; updated the <i>Simplified Block Diagram, Pin Configurations, Functional Diagrams</i> , Figures 4–Figure 7, Table 1, BBstlSet (0x03), BBstCfg1 (0x04), and Table 4; replaced Table 3; added the <i>Inductor Selection and Output Operating Power and Other Optimization</i> sections | 1–2, 4–20, 23–25, 28, 32, 34 |
| 4.1 | | Corrected typo | 1 |
| 5 | 6/20 | Updated <i>Benefits and Features, Electrical Characteristics, and Ordering Information</i> section; removed mention of MAX20343E; replaced the <i>Input and Output Capacitance</i> section, Figure 9, Table 3, and Table 4; added the <i>Soft-Start</i> section | 1, 4–6, 18–20, 22, 26–27, 31–32, 35–37 |
| 6 | 9/20 | Added MAX20344 to the title, <i>General Description, Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics, Inductor Peak and Valley Current Limits, Input Operating Voltage, Output Operating Power and Other Optimizations, I²C Interface, Slave Address, Optical Heart Rate LED Supply (Typical Application Circuit), LPWAN Radio Supply (Typical Application Circuit), and Ordering Information</i> sections; updated Tables 2–4 and register 0x03; removed Figures 4 and 6, and renumbered remaining figures | 1, 3, 4–6, 17, 19–20, 22, 26–27, 31, 35–37 |
| 7 | 1/21 | Updated Single-Pin-Enabled FC2QFN figure in the <i>Pin Configurations</i> section, added details in the <i>Single-Pin-Enabled</i> section, added MAX20343I to Tables 3 and 4, and updated the <i>Ordering Information</i> by adding MAX20343I and removed future part designation from MAX20344EAFC+ and MAX20344EAFC+T | 17, 25, 39–40, 42 |
| 8 | 6/21 | Corrected Continuous Power Dissipation in the <i>Absolute Maximum Ratings</i> , updated Table 3 and Table 4, and updated <i>Ordering Information</i> by adding MAX20343KEWE+ and MAX20343KEWE+T as future products | 7, 10, 39–40, 42 |
| 9 | 8/21 | Updated Figure 7 caption, updated Table 3 and Table 4, and updated <i>Ordering Information</i> by adding MAX20343JEWE+, MAX20343JEWE+T, and MAX20343NEWE+, MAX20343NEWE+T as future products | 34, 39–40, 42 |

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