MAX20412

Automotive Low-Voltage, 2-Channel Step-Down Controller

General Description

The MAX20412 is a dual-output, high-efficiency, synchronous step-down controller IC that operates with a 3.0V to 5.5V input voltage range and provides a 0.25V to 1.275V output voltage range. The controller architecture enables up to 30A of load current per phase. Channel one has an option to operate with two phases to deliver higher load current, making this device ideal for automotive point-of-load (PoL) and post-regulation applications.

The IC achieves ±2% output error over load, line, and temperature ranges. The IC features a 2.2MHz/1.1MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions.

The MAX20412 is offered with factory-preset output voltages (see the *Selector Guide* for options). The I^2C interface supports dynamic voltage adjustment with programmable slew rates for each channel. Other features include programmable soft-start, overcurrent, and overtemperature protections.

Applications

- Automotive

Benefits and Features

- 2-Channel, High-Efficiency DC-DC Controller in a Small Solution Size
  - 3.0V to 5.5V Operating Supply Voltage
  - OUT1 Supports 60A (with Two Phases)
  - OUT2 Supports 30A
- High-Precision Regulator for Applications Processors
  - ±2% Output-Voltage Accuracy
  - Differential Remote-Voltage Sensing
  - I^2C-Controlled Output Voltage: 0.25V to 1.275V in 6.25mV Steps
  - Excellent Load-Transient Performance
  - Programmable Compensation
- Low-Noise Features Reduce EMI
  - 2.2MHz or 1.1MHz Operation
  - Spread-Spectrum Option
  - Frequency-Synchronization Input/Output
  - Current-Mode, Forced-PWM, and Skip Operation
- Robust for the Automotive Environment
  - Individual Enable Inputs and PGOOD Outputs
  - Low $R_{DS(ON)}$ External MOSFETs
  - Overtemperature and Short-Circuit Protection
  - 32-Pin (5mm x 5mm) TQFN with Exposed Pad
  - -40°C to +125°C Operating Temperature Range
  - AECQ-100 Qualified

***Ordering Information* appears at end of data sheet.**

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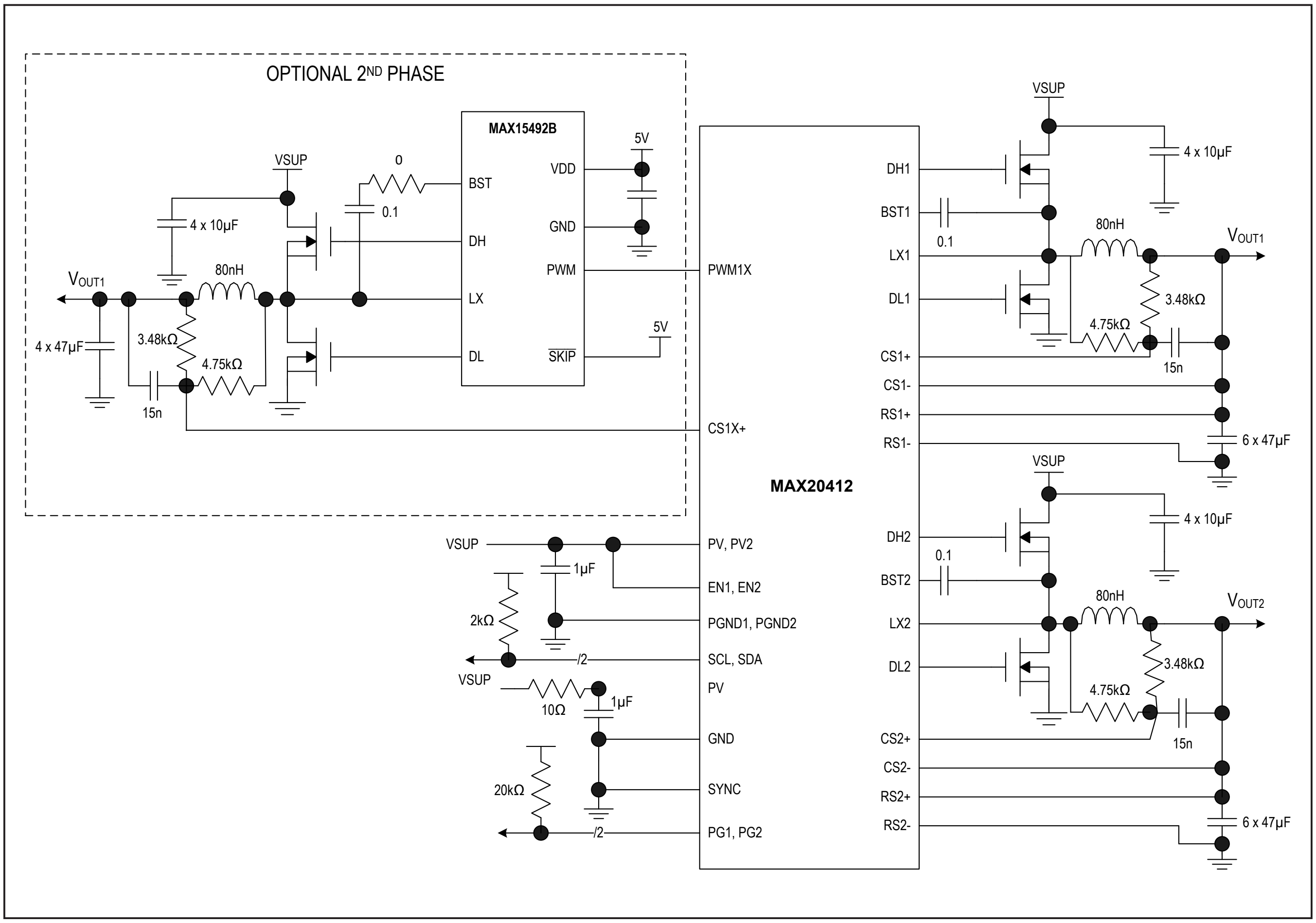
Typical Operating Circuit



Absolute Maximum Ratings

PV1, PV2 to PGND_ ....-0.3V to +6V
PV to GND..-0.3V to +6V
EN_, RS_+, RS_-, SYNC to GND................-0.3V to PV + 0.3V
PG_, ADDR, SDA, SCL to GND.............................-0.3V to +6V
DH_ to LX_..-0.3V to BST_ + 0.3V
DL_ to PGND_ ....-0.3V to PV_ + 0.3V
BST_ to LX_..-0.3V to +6V
LX_ to PGND_...-2V to +6V
CS1+ to CS1-, CS2+ to CS2- ....-0.3V to +0.3V
CS_-, CS1X+ to GND...................................-0.3V to PV + 0.3V
PWM1X to GND ....-0.3V to PV + 0.3V
GND to PGND_ ....-0.3V to +0.3V
Output Short-Circuit Duration ....Continuous
Continuous Power Dissipation (T_A = +70°C) (Multilayer Board)
32-Pin TQFN (derate 34.5mW/°C above +70°C)...2758.6mW
Operating Temperature Range......................... -40°C to +125°C
Junction Temperature..+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).....................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

32 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC})................3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+6C	21-0140	90-0603

Electrical Characteristics

(V_{PV} = $V_{PV\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	Fully operational	3.0		5.5	V
UVLO	V_{IN_UVLO}	Rising		2.9	3	V
		Falling	2.6	2.7		
UVLO Hysteresis	V_{IN_UVLOH}			200		mV
Supply Current (Skip Mode)	I_{IN_1}	EN1 = high, EN2 = low, CS1X+ = $V_{PV\_}$ (Note 3)		570		µA
	I_{IN_2}	EN1 = EN2 = high, CS1X+ = V_{PV} (Note 3)		1100		
Shutdown Supply Current	I_{SHDN}	EN1 = EN2 = low		5	10	µA
PWM Switching Frequency	f_{SW}	CONFIG.FSW = 0	2.0	2.2	2.4	MHz
	f_{SW11}	CONFIG.FSW = 1	1.0	1.1	1.2	
Spread Spectrum	SS	CONFIG.SS = 1		+3		%

Electrical Characteristics (continued)

(V_{PV} = $V_{PV\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Accuracy	$V_{OUT\_}$	$V_{CS\_}$ = 0 to 0.8 x V_{LIM} (Note 3), 3.0V ≤ $V_{PV\_}$ ≤ 5.5V, 0.80V to 1.275V	-2		+2	%
Voltage Accuracy	V_{OUT_L}	$V_{CS\_}$ = 0 to 0.8 x V_{LIM} (Note 3), 3.0V ≤ $V_{PV\_}$ ≤ 5.5V, 0.25V to 0.79V	-15		+15	mV
High-Side Output Drive Resistance	R_{HSD_HS}	Rising		2.0		Ω
High-Side Output Drive Resistance	R_{HSD_LS}	Falling		1.5		Ω
Low-Side Output Drive Resistance	R_{LSD_HS}	Rising		1.5		Ω
Low-Side Output Drive Resistance	R_{LSD_LS}	Falling		1.3		Ω
Peak Current-Limit Threshold	V_{LIM1}	Measured across $V_{CS\_}$, DCR gain = 16	69	71	74	mV
		Measured across $V_{CS\_}$, DCR gain = 32	43	45	47	
Peak Current-Limit Threshold	V_{LIM2}	Measured across $V_{CS\_}$, DCR gain = 32	35	37	39	mV
Peak Current-Limit Threshold	V_{LIM4}	Measured across $V_{CS\_}$, DCR gain = 16	81	83	87	mV
Skip Current Threshold	V_{SKIP}	Measured across $V_{CS\_}$ (Note 3), DCR gain = 32, 4 options		10		mV
				8		
		Measured across $V_{CS\_}$ (Note 3), DCR gain = 16, 4 options		6		
				4		
Maximum Duty Cycle	DC_{MAX}	PWM mode	90			%
Minimum On-Time	t_{MINON}			35		ns
LX Leakage Current	I_{LKG_LX}	V_{IN} = 6V, LX = PGND or PV, T_A = +25°C		0.1		µA
OUT2 Phase Shift	PH_{OUT2}	OUT1 in single phase		180		Degrees
CS_- Pulldown Resistance	R_{CS_PD}	$V_{EN\_}$ = 0V		5		Ω
THERMAL OVERLOAD						
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising		165		°C
Hysteresis	T_{HYS_SHDN}			15		°C

Electrical Characteristics (continued)

(V_{PV} = $V_{PV\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER GOOD						
PG_ OV Threshold	T_{HOVR}	Rising, percentage of nominal output, blanked during slewing	104	108	112	%
PG_ OV Threshold	T_{HOVF}	Falling, percentage of nominal output, blanked during slewing	102	108	111	%
PG_ UV Threshold	T_{HUVR}	Rising, percentage of nominal output, blanked during slewing	88	92	96	%
PG_ UV Threshold	T_{HUVF}	Falling, percentage of nominal output, blanked during slewing	89	92	95	%
Active Timeout Period	t_{HOLD}			256		Cycles
UV/OV Propagation Delay	t_{FILT}			5		µs
Output High-Leakage Current	I_{LKG_PG}				1	µA
PG_ Output Low Level	$V_{OL\_PG\_}$	3.0V ≤ V_{PV} ≤ 5.5V, sinking -2mA			0.2	V
DIGITAL INPUT (ADDR, EN_)						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis	V_{IHYS}			0.1		V
EN_ Input Leakage Current	$I_{LKG\_EN\_}$	0V ≤ V_{IN} ≤ 5.5V		1		µA
PWM1X						
Output High	V_{OH_PWM}	V_{PV} = 5.0V, I_{SOURCE} = 3mA	4.2			V
Output Low	V_{OL_PWM}	I_{SINK} = 3mA			0.4	V
DIGITAL INPUT (SYNC)						
Input High Level	V_{IH_SYNC}		1.8			V
Input Low Level	V_{IL_SYNC}				0.4	V
SYNC Input Pulldown	R_{PD_SYNC}			100		kΩ
Sync Input Frequency Range	f_{SYNC}	CONFIG.FSW = 0	1.8		2.6	MHz
Sync Input Frequency Range	f_{SYNC11}	CONFIG.FSW = 1	0.9		1.3	MHz
SYNC OUTPUT (CONFIG.SO[1:0]=10)						
Output Low	V_{OL_SYNC}	I_{SINK} = 3mA			0.4	V
Output High	V_{OH_SYNC}	V_{PV} = 5.0V, I_{SOURCE} = 3mA	4.2			V

Electrical Characteristics (continued)

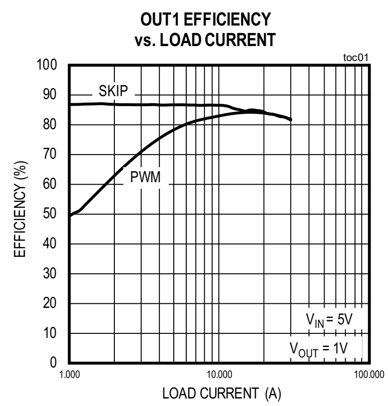
(V_{PV} = $V_{PV\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

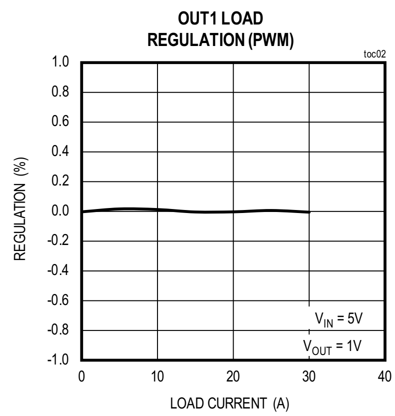
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT (SCL, SDA)						
Input High Level	V_{IH_I2C}		1.2			V
Input Low Level	V_{IL_I2C}				0.5	V
Input Hysteresis	V_{IHYS_I2C}			0.1		V
Input Leakage Current	I_{LKG_I2C}	0V ≤ V_{IN} ≤ 5.5V		0.1		µA
I²C INTERFACE						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time, Repeated START	$t_{SU:STA}$	(Note 3)	160			ns
Hold Time, Repeated START	$t_{HD:STA}$	(Note 3)	160			ns
SCL Low Time	t_{LOW}	(Note 3)	160			ns
SCL High Time	t_{HIGH}	(Note 3)	60			ns
Data Setup Time	$t_{SU:DAT}$	(Note 3)	10			ns
Data Hold Time	$t_{HD:DAT}$	(Note 3)	0		70	ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 3)	160			ns
Spike Suppression	t_{SS_I2C}			20		ns
SDA Output Low	V_{OL_SDA}	I_{SINK} = 13mA			0.4	V

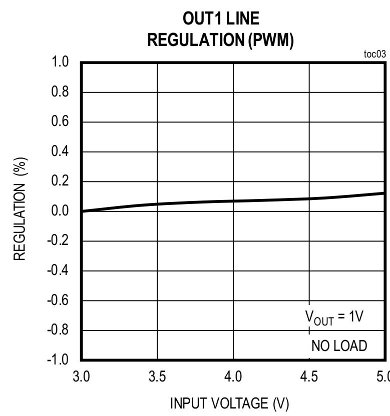
Note 2: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.
Note 3: $V_{CS\_}$ = (V_{CS_+}) - (V_{CS_-}).

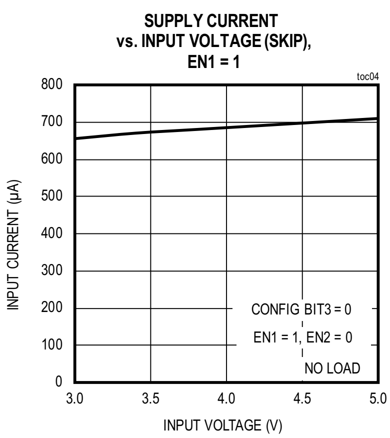
Typical Operating Characteristics

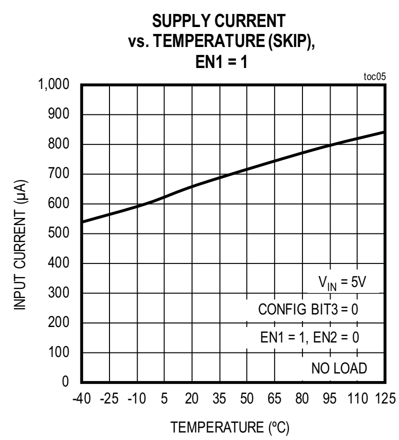
(T_A = +25°C, unless otherwise noted.)

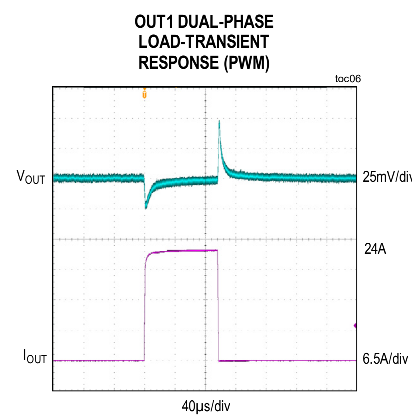


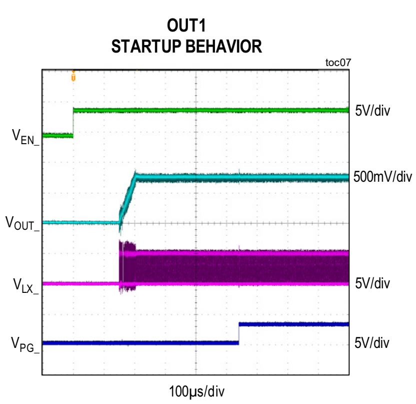


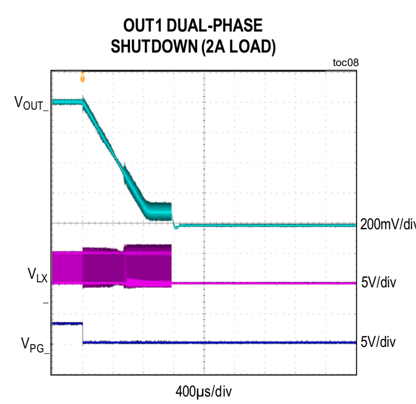


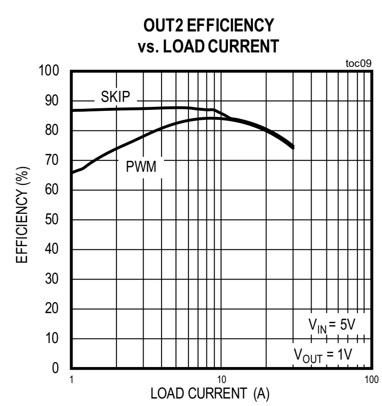








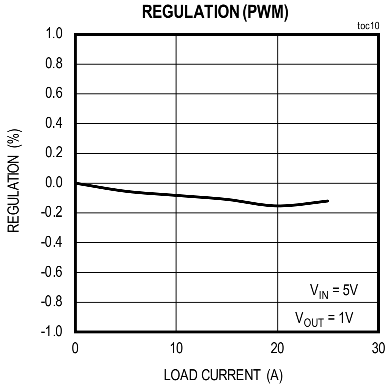




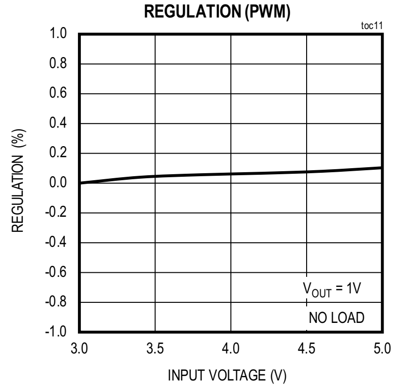
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

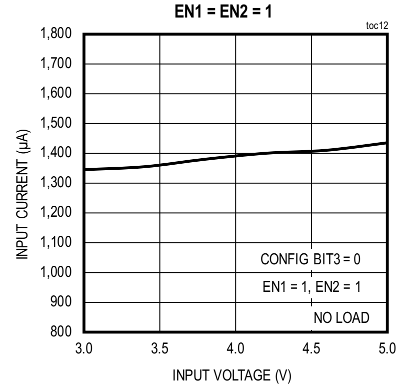
OUT2 LOAD REGULATION (PWM)



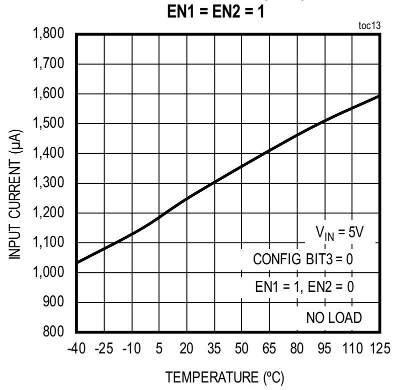
OUT2 LINE REGULATION (PWM)



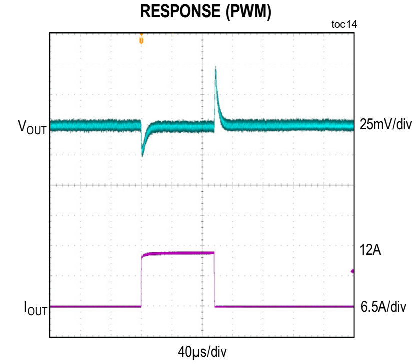
SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP), EN1 = EN2 = 1



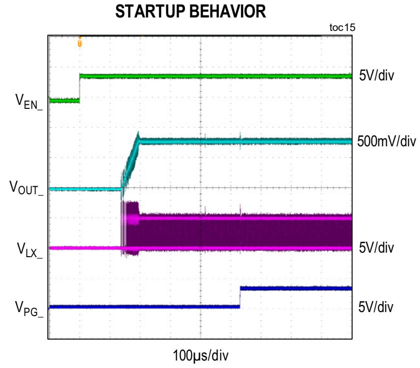
SUPPLY CURRENT vs. TEMPERATURE (SKIP), EN1 = EN2 = 1



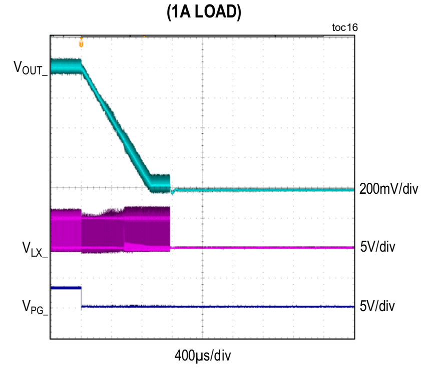
OUT2 LOAD-TRANSIENT RESPONSE (PWM)



OUT2 STARTUP BEHAVIOR

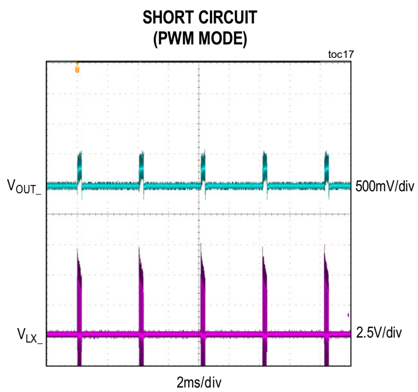


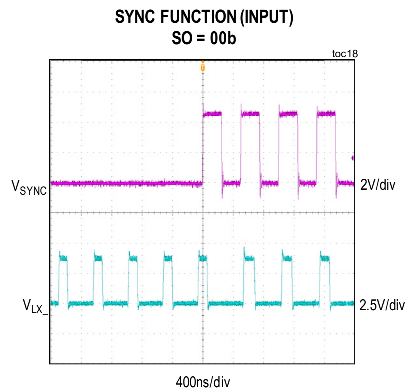
OUT2 SHUTDOWN (1A LOAD)

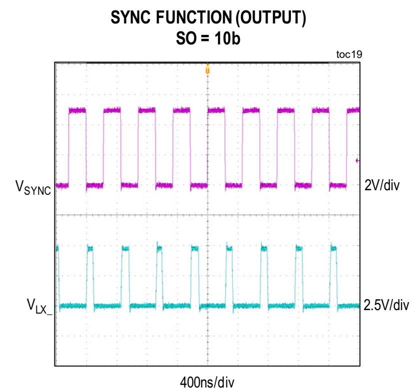


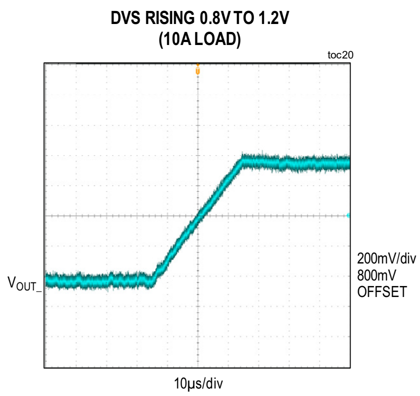
Typical Operating Characteristics

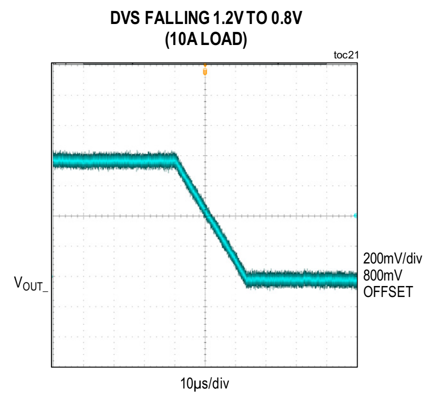
(T_A = +25°C, unless otherwise noted.)



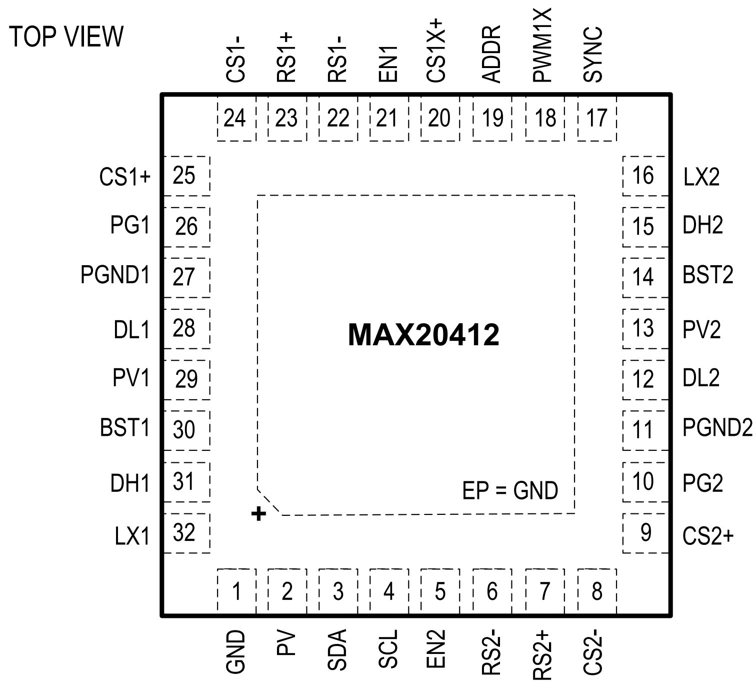








Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	FUNCTION
1	GND	Analog Ground
2	PV	Analog Input Supply. Connect a 1µF ceramic capacitor from PV to GND. Connect PV to PV1 and PV2 through a 10Ω resistor.
3	SDA	I^2C Data I/O
4	SCL	I^2C Clock Input
5	EN2	Active-High Digital Enable Input for DCDC2. Drive EN2 high for normal operation. Connect EN2 to GND if DCDC2 is not used.
6	RS2-	DCDC2 Remote Voltage-Sense Negative Input
7	RS2+	DCDC2 Remote Voltage-Sense Positive Input
8	CS2-	Current-Sense Negative Input for DCDC2. Connect CS2- to the negative side of the current-sense element.
9	CS2+	Current-Sense Positive Input for DCDC2. Connect CS2+ to the positive side of the current-sense element. See the *Current-Limit/Short-Circuit Protection* section.

Pin Description (continued)

PIN	NAME	FUNCTION
10	PG2	Open-Drain DCDC2 Reset Output. This output remains low for 120μs after the output has reached its regulation level (see the *Electrical Characteristics* table). To obtain a logic signal, pull up PG2 with an external resistor.
11	PGND2	Power Ground for DCDC2
12	DL2	Low-Side Gate Drive for DCDC2
13	PV2	Input-Voltage Pin for DCDC2. Bypass this pin with enough input capacitance to supply current to the buck controller. Connect PV1 and PV2 together externally. See the *Input Capacitor* section.
14	BST2	Bootstrap Capacitor for High-Side Driver of Buck 2. Connect a 0.1μF from LX2 to BST2.
15	DH2	High-Side Gate Drive for DCDC2
16	LX2	Inductor Connection for DCDC2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
17	SYNC	SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to PV or an external clock to enable fixed-frequency, forced-PWM mode operation. When configured as an output, connect SYNC to other devices' SYNC inputs.
18	PWM1X	PWM Output for Optional Second Phase of DCDC1. Connect to the MAX15492 PWM pin. If unused, leave PWM1X unconnected.
19	ADDR	I^2C Address Select. Connect to GND or PV to select between two different I^2C addresses. See the *Selector Guide* for default I^2C settings.
20	CS1X+	Current-Sense Positive Input for the 2nd Phase of DCDC1. Connect CS1X+ to the positive side of the current-sense element. To disable phase 2, short CS1X+ to PV.
21	EN1	Active-High, Digital Enable Input for DCDC1. Drive EN1 high for normal operation. Connect EN1 to GND if DCDC1 is not used.
22	RS1-	DCDC1 Remote Voltage-Sense Negative Input
23	RS1+	DCDC1 Remote Voltage-Sense Positive Input
24	CS1-	Current-Sense Negative Input for DCDC1. Connect CS1- to the negative side of the current-sense element.
25	CS1+	Current-Sense Positive Input for DCDC1. Connect CS1+ to the positive side of the current-sense element. See the *Current-Limit/Short-Circuit Protection* section.
26	PG1	Open-Drain DCDC1 Reset Output. This output remains low for 120μs after the output has reached its regulation level (see the *Electrical Characteristics* table). To obtain a logic signal, pull up PG1 with an external resistor.
27	PGND1	Power Ground for DCDC1
28	DL1	Low-Side Gate Drive for DCDC1
29	PV1	Input-Voltage Pin for DCDC1. Bypass this pin with enough input capacitance to supply current to the buck controller. Connect PV1 and PV2 together externally. See the *Input Capacitor* section.
30	BST1	Bootstrap Capacitor for High-Side Driver of DCDC1. Connect a 0.1μF from LX1 to BST1.
31	DH1	High-Side Gate Drive of DCDC1
32	LX1	Inductor Connection for DCDC1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
—	EP	Exposed Pad. Connect EP to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND1, PGND2, and GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

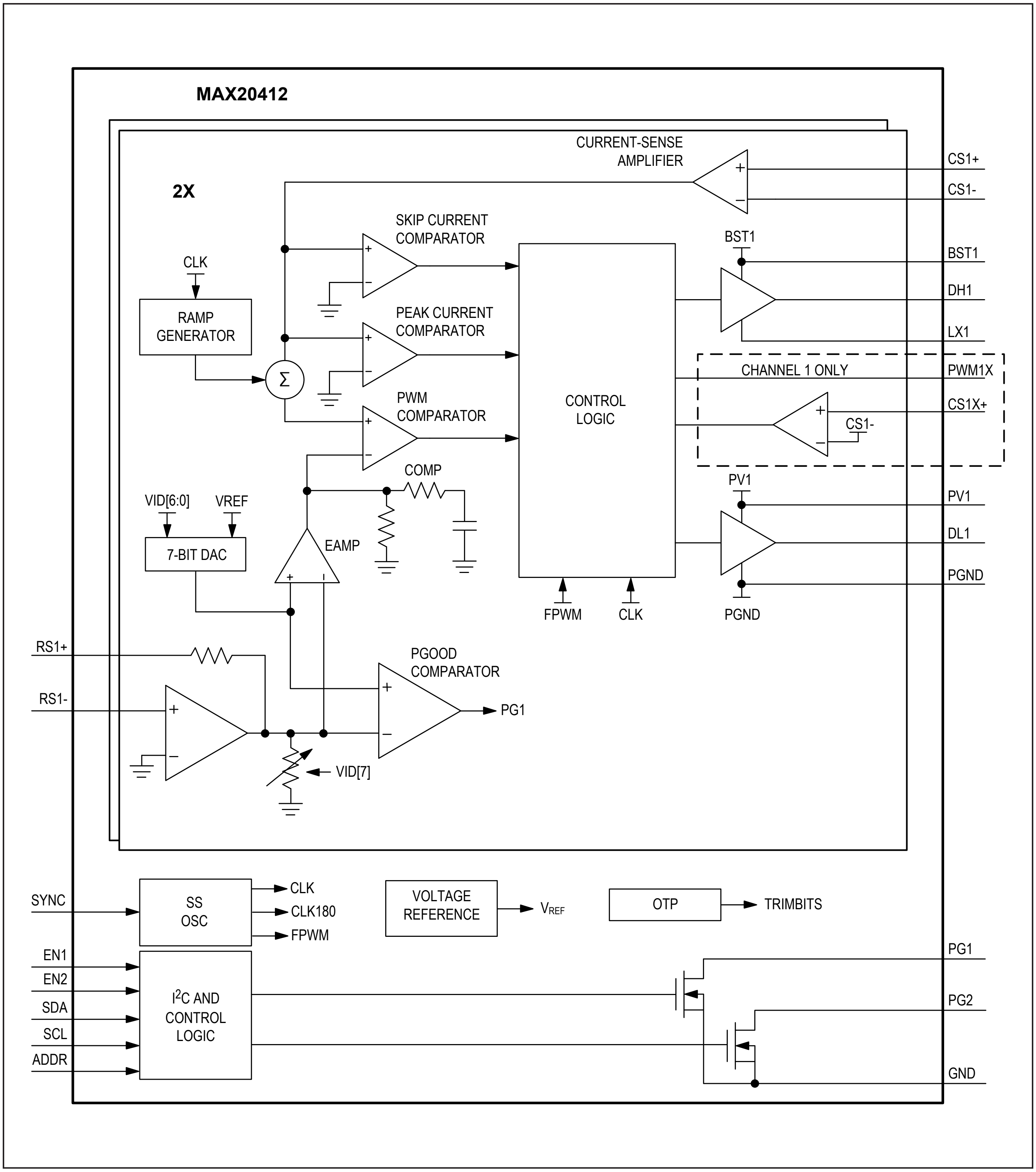


Figure 1. Internal Block Diagram

Detailed Description

The MAX20412 is a dual-output, high-efficiency synchronous step-down controller IC that operates with a 3.0V to 5.5V input voltage range and provides a 0.25V to 1.275V output voltage range. The IC delivers up to 30A of load current per channel and achieves ±2% output error over load, line, and temperature ranges. The IC can operate as a 2-phase controller to deliver currents of up to 60A.

The PWM input forces the IC into either a 2.2MHz fixed-frequency PWM mode, or a low-power pulse-frequency modulation mode (skip). Optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency. The I²C-programmable synchronization I/O (SYNC) enables system synchronization.

The IC is offered with a factory-preset output voltage that is dynamically adjustable through the I²C interface. The output voltage can be set to any desired value between 0.25V and 1.275V.

Additional features include fixed power-good delay, adjustable soft-start and DVS rate, overcurrent, and overtemperature protections (Figure 1).

I²C Interface

The IC features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 3.4MHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 2 shows the 2-wire interface timing diagram.

A master device communicates to the IC by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The IC's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus. The IC's SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SDA and SCL inputs suppress noise spikes to assure proper device operation, even on a noisy bus.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *STOP and START Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

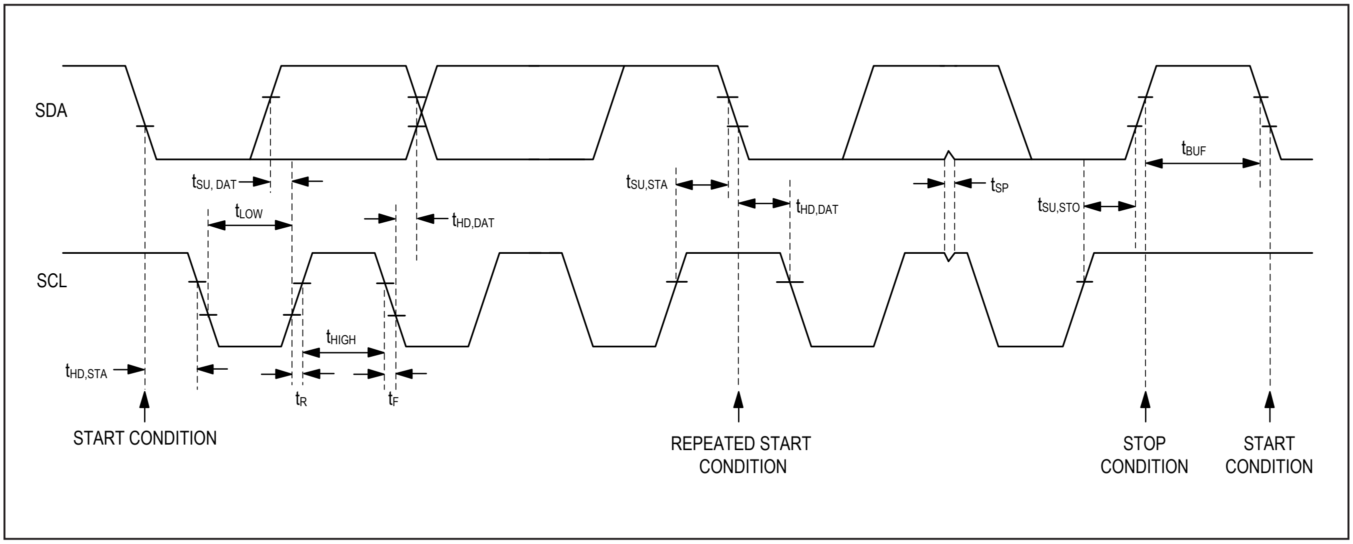


Figure 2. I²C Timing Diagram

STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 3). A START (S) condition from the master signals the beginning of a transmission to the device. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a Repeated START (Sr) condition is generated instead of a STOP condition.

The device recognizes a STOP condition at any point during data transmission, unless the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock-signal generation for the I^2C bus is the responsibility of the master device. The I^2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX20412 IC does not use any form of clock stretching to hold down the clock line.

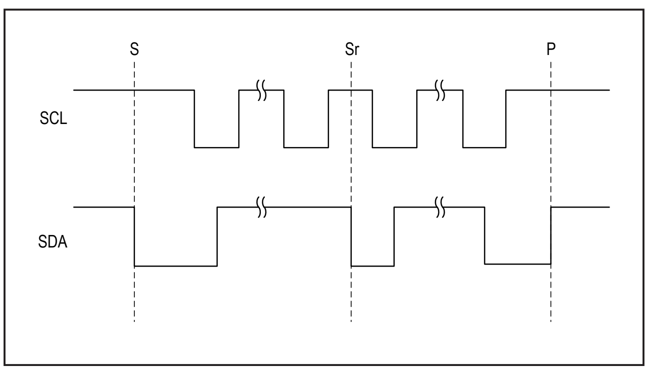


Figure 3. START, STOP, and Repeated START Conditions

I^2C General Call Address

The IC does not implement the I^2C specifications' "general call address." If the device sees the general call address (0b0000_0000), it does not issue an acknowledge.

Slave Address

Once the device is enabled, the I^2C slave address is set by the ADDR pin (Table 1). Each output channel has a unique slave address. The address is defined as the 7 most significant bits (MSBs), followed by the R/W bit. Set the R/W bit to 1 to configure the IC to read mode. Set the R/W bit to 0 to configure the IC to write mode. The address is the first byte of information sent to the devices after the START condition.

Table 1. I^2C Slave Addresses

ADDR PIN	A6	A5	A4	A3	A2*	A1*	A0	WRITE	READ
0	0	1	1	1	0	0	0	0x70	0x71
1	0	1	1	1	0	0	1	0x72	0x73
0	0	1	1	1	0	1	0	0x74	0x75
1	0	1	1	1	0	1	1	0x76	0x77
0	0	1	1	1	1	0	0	0x78	0x79
1	0	1	1	1	1	0	1	0x7A	0x7B

**See the Selector Guide for default settings.*

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 4). The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

Write Data Format

A write to the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to the register address, one byte of data to the command register, and a STOP condition. Figure 5 illustrates the proper format for one frame.

Read Data Format

A read from the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to the register address, a restart condition, the slave address with the read bit set to 1, one byte of data to the command register, and a STOP condition. Figure 5 illustrates the proper format for one frame.

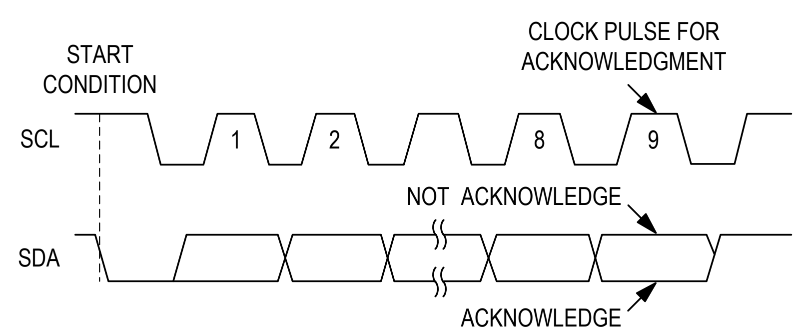


Figure 4. Acknowledge Condition

WRITE BYTE

S	SLAVE WRITE ADDRESS	A	REGISTER ADDRESS	A	DATA	NA	P

WRITE MULTIPLE BYTES

S	SLAVE WRITE ADDRESS	A	REGISTER ADDRESS	A	DATA 1	A	REGISTER ADDRESS	A	DATA 2	. . .	REGISTER ADDRESS	A	DATA 2	A	P

READ BYTE

S	SLAVE WRITE ADDRESS	A	REGISTER ADDRESS	A	Sr	SLAVE READ ADDRESS	A	DATA	NA	P

READ SEQUENTIAL BYTES

S	SLAVE WRITE ADDRESS	A	REGISTER ADDRESS	A	Sr	SLAVE READ ADDRESS	A	DATA 1	. . .	DATA N	NA	P

Figure 5. Data Format of I2C Interface

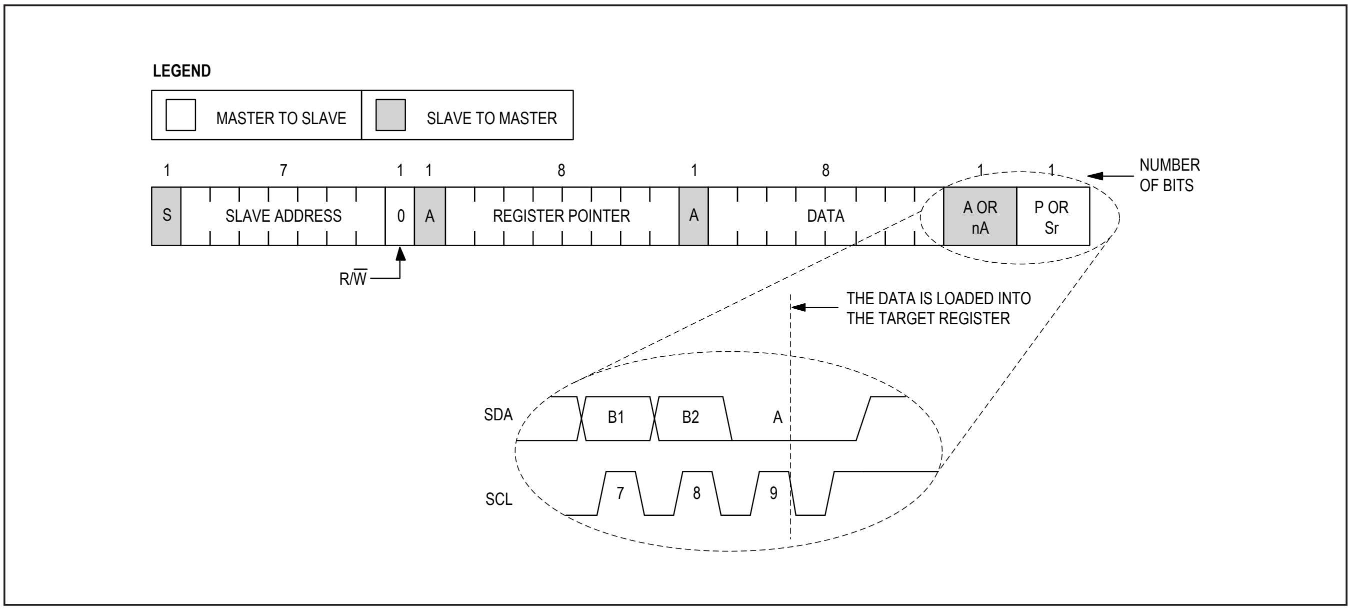


Figure 6. Write Byte Format

Writing to a Single Register

Figure 6 shows the protocol for the I2C master device to write one byte of data to the MAX20412. This protocol is the same as the SMBus specification's "write byte" protocol.

The "write byte" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9) The master sends a STOP condition (P) or a Repeated START condition (Sr).

Writing Multiple Bytes Using Register Data Pairs

Figure 7 shows the protocol for the I2C master device to write multiple bytes to the MAX20412 using register-data pairs. This protocol allows the I2C master device to address the slave only once and then send data to multiple registers in a random order. Registers can be written continuously until the master issues a STOP condition.

The "writing multiple bytes using register-data pairs" protocol is not supported by the RTC functional block.

The "multiple byte register-data pair" protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8) Steps 4–7 are repeated as many times as the master requires.
9) The master sends a STOP condition. During the rising edge of the stop-related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

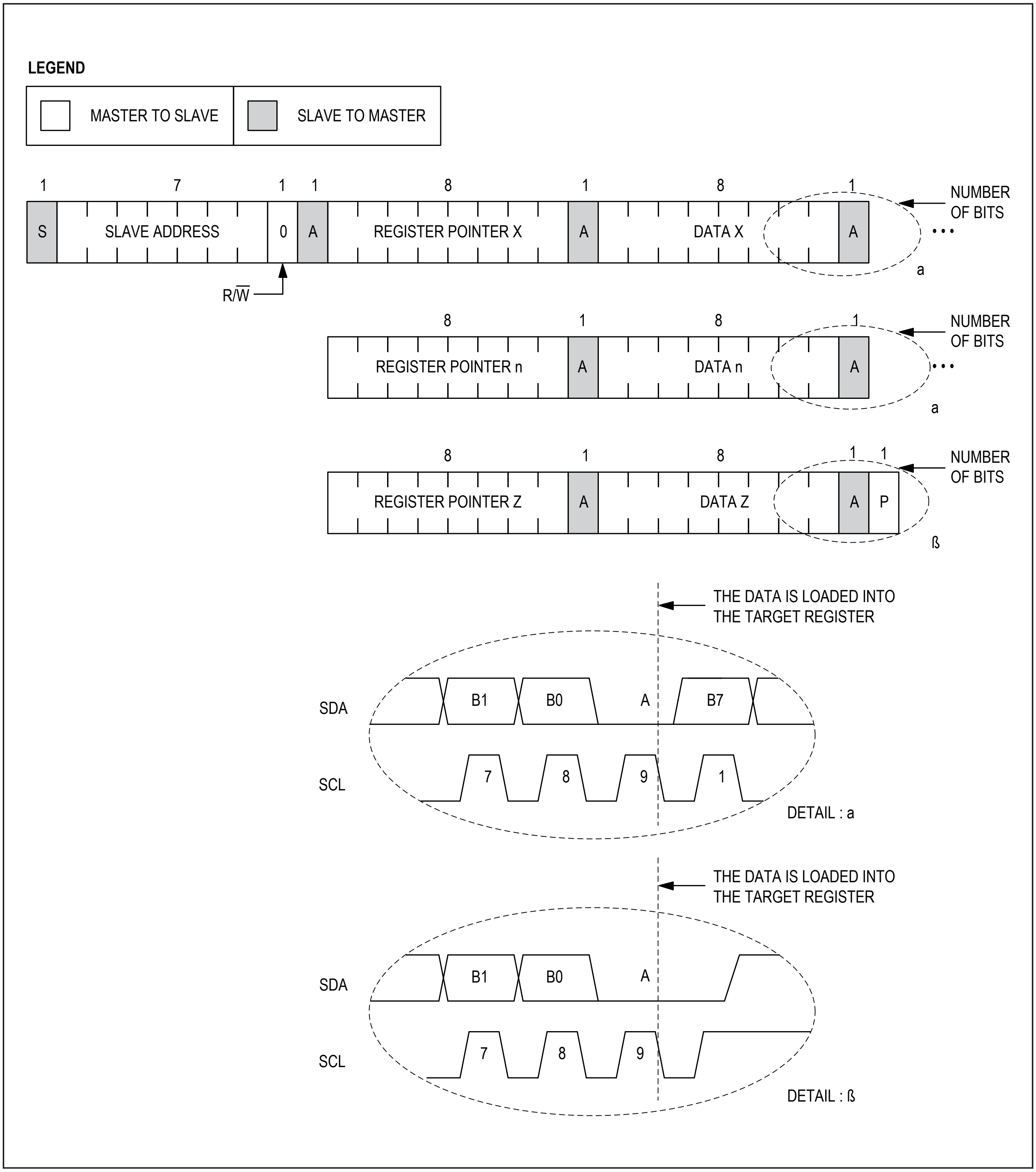


Figure 7. Write Register-Data-Pair Format

Table 2. Register Map

REG	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	CMD	R/W	POWER-ON RESET
ID	DEV3	DEV2	DEV1	DEV0	R3	R2	R1	R0	0x00	R	0x00
—	—	—	—	—	—	—	—	—	0x01	R/W	0x00
VIDMAX	VMAX7	VMAX6	VMAX5	VMAX4	VMAX3	VMAX2	VMAX1	VMAX0	0x02	R/W	OTP
CONFIG2	VSKIP1	VSKIP0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x03	R/W	OTP
STATUS	INTERR	—	VRHOT	UV	OV	OC	VMERR	0	0x04	R	0x00
CONFIG	—	FSW	—	—	FPWM	SS	SO1	SO0	0x05	R/W	OTP
SLEW	—	—	—	—	SR3	SR2	SR1	SR0	0x06	R/W	OTP
VID	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	0x07	R/W	OTP
COMP	ZEN	GM[1:0]		Z	RCOMP[3:0]				0x08	R/W	OTP

Note: Both outputs have an identical register set, as defined below. They are accessed individually by using each channel's unique I^{2}C address. Each channel has the same register set accessed through their individual I^{2}C address (see Table 1).

Table 3. Identification Register (ID, 0x00)

ID								
BIT NO.	7	6	5	4	3	2	1	0
NAME	DEV3	DEV2	DEV1	DEV0	R3	R2	R1	R0
OUT1 POR	0	1	0	0	0	0	1	0
OUT2 POR	0	1	0	1	0	0	1	0

BIT	BIT DESCRIPTION
DEV[3:0]	**Device ID:** MAX20412 OUT1 = 0x4 MAX20412 OUT2 = 0x5
R[3:0]	MAX20412 Pass 3 = 0x2

Table 4. Maximum Voltage-Settings Registers (VIDMAX, 0x02)

VIDMAX								
BIT NO.	7	6	5	4	3	2	1	0
NAME	VMAX7	VMAX6	VMAX5	VMAX4	VMAX3	VMAX2	VMAX1	VMAX0
POR	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

BIT	BIT DESCRIPTION
VMAX[7:0]	**Maximum Voltage Setting:** If VID[] > VMAX[], then a fault is set and the actual voltage is capped by VMAX[]. See Table 10 for VID output-voltage selections.

Table 5. Configuration Register (CONFIG2, 0x03)

CONFIG2								
BIT NO.	7	6	5	4	3	2	1	0
NAME	VSKIP[1:0]		RESERVED					
POR	OTP	OTP	0	1	0	0	0	0

BIT	BIT DESCRIPTION
VSKIP[1:0]	**Skip Current-Limit Configuration:** 00 = 4A 01 = 6A 10 = 8A 11 = 10A
CONFIG2[5:0]	Reserved

Table 6. Status Register (STATUS, 0x04)

STATUS								
BIT NO.	7	6	5	4	3	2	1	0
NAME	INTERR	—	VRHOT	UV	OV	OC	VMERR	0
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
INTERR	**Internal Hardware Error:** This bit is set to '1' when ATE trimming and testing is not complete.
VRHOT	**Thermal-Shutdown Indication:** A thermal shutdown has occurred since the last time this register was read.
UV	**V_{OUT} Undervoltage:** This bit indicates if the output is currently under the target voltage.
OV	**V_{OUT} Overvoltage:** This bit indicates if the output is currently over the target voltage.
OC	**V_{OUT} Overcurrent:** This bit indicates if an overcurrent event has occurred since the last time the STATUS register was read.
VMERR	V_{OUT_MAX} Error. Set to 1 if **VID[]** > **VOUTMAX[]**.

Table 7. Configuration Register (CONFIG, 0x05)

CONFIG								
BIT NO.	7	6	5	4	3	2	1	0
NAME	—	FSW	—	—	FPWM	SS	SO1	SO0
POR	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

BIT	BIT DESCRIPTION
FSW	**Switching Frequency (sets the nominal switching frequency):** 0 = 2.2MHz 1 = 1.1MHz
FPWM	**Forced-PWM Mode:** 0 = Mode controlled by SYNC pin. When SYNC is output, the device is always in FPWM mode. 1 = Forced-PWM Mode. Overrides the SYNC skip-mode setting when SYNC is an input.
SS	**Spread-Spectrum Clock Setting:** 0 = Disabled 1 = +3% spread
SO[1:0]	**SYNC I/O Select:** 00 = Master: Input, rising edge starts cycle 01 = Master: Input, falling edge starts cycle 10 = Master: Output, falling edge starts cycle 11 = Unused

Table 8. Slew-Rate Register (SLEW, 0x06)

SLEW								
BIT NO.	7	6	5	4	3	2	1	0
NAME	—	—	—	—	SR3	SR2	SR1	SR0
POR	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

SR[3:0]	SOFT-START SLEW RATE (mV/µs)	DVS SLEW RATE (mV/µs)
XXXX0000	14	14
XXXX0001	7	14
XXXX0010	3.4	14
XXXX0011	7	7
XXXX0100	3.4	7
XXXX0101	14	14
XXXX0110	14	14
XXXX0111	7	14
XXXX1000	3.4	14
XXXX1001	3.4	3.4
XXXX1010 – XXXX1111	Reserved	Reserved

***Note:** Falling DVS and power-down slew rate is -0.875mV/us.*

Table 9. Output-Voltage Register (VID, 0x07)

VID								
BIT NO.	7	6	5	4	3	2	1	0
NAME	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
POR	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

BIT	BIT DESCRIPTION
VID[7:0]	**Target Voltage Setting:** V_{OUT} ramps at the programmed DVS ramp rate until it reaches programmed the VID. See Table 10 for VID output-voltage selections. When VID[7:0] ! = 0, V_{OUT} = (VID[7:0] + 39) x 0.00625V.

Table 10. VID Output-Voltage Selection

VID	VOUT	VID	VOUT	VID	VOUT	VID	VOUT	VID	VOUT	VID	VOUT
0x00	OFF	0x20	0.44375	0x40	0.64375	0x60	0.84375	0x80	1.04375	0xA0	1.24375
0x01	0.25000	0x21	0.45000	0x41	0.65000	0x61	0.85000	0x81	1.05000	0xA1	1.25000
0x02	0.25625	0x22	0.45625	0x42	0.65625	0x62	0.85625	0x82	1.05625	0xA2	1.25625
0x03	0.26250	0x23	0.46250	0x43	0.66250	0x63	0.86250	0x83	1.06250	0xA3	1.26250
0x04	0.26875	0x24	0.46875	0x44	0.66875	0x64	0.86875	0x84	1.06875	0xA4	1.26875
0x05	0.27500	0x25	0.47500	0x45	0.67500	0x65	0.87500	0x85	1.07500	0xA5	1.27500
0x06	0.28125	0x26	0.48125	0x46	0.68125	0x66	0.88125	0x86	1.08125	—	—
0x07	0.28750	0x27	0.48750	0x47	0.68750	0x67	0.88750	0x87	1.08750	—	—
0x08	0.29375	0x28	0.49375	0x48	0.69375	0x68	0.89375	0x88	1.09375	—	—
0x09	0.30000	0x29	0.50000	0x49	0.70000	0x69	0.90000	0x89	1.10000	—	—
0x0A	0.30625	0x2A	0.50625	0x4A	0.70625	0x6A	0.90625	0x8A	1.10625	—	—
0x0B	0.31250	0x2B	0.51250	0x4B	0.71250	0x6B	0.91250	0x8B	1.11250	—	—
0x0C	0.31875	0x2C	0.51875	0x4C	0.71875	0x6C	0.91875	0x8C	1.11875	—	—
0x0D	0.32500	0x2D	0.52500	0x4D	0.72500	0x6D	0.92500	0x8D	1.12500	—	—
0x0E	0.33125	0x2E	0.53125	0x4E	0.73125	0x6E	0.93125	0x8E	1.13125	—	—
0x0F	0.33750	0x2F	0.53750	0x4F	0.73750	0x6F	0.93750	0x8F	1.13750	—	—
0x10	0.34375	0x30	0.54375	0x50	0.74375	0x70	0.94375	0x90	1.14375	—	—
0x11	0.35000	0x31	0.55000	0x51	0.75000	0x71	0.95000	0x91	1.15000	—	—
0x12	0.35625	0x32	0.55625	0x52	0.75625	0x72	0.95625	0x92	1.15625	—	—
0x13	0.36250	0x33	0.56250	0x53	0.76250	0x73	0.96250	0x93	1.16250	—	—
0x14	0.36875	0x34	0.56875	0x54	0.76875	0x74	0.96875	0x94	1.16875	—	—
0x15	0.37500	0x35	0.57500	0x55	0.77500	0x75	0.97500	0x95	1.17500	—	—
0x16	0.38125	0x36	0.58125	0x56	0.78125	0x76	0.98125	0x96	1.18125	—	—
0x17	0.38750	0x37	0.58750	0x57	0.78750	0x77	0.98750	0x97	1.18750	—	—
0x18	0.39375	0x38	0.59375	0x58	0.79375	0x78	0.99375	0x98	1.19375	—	—
0x19	0.40000	0x39	0.60000	0x59	0.80000	0x79	1.00000	0x99	1.20000	—	—
0x1A	0.40625	0x3A	0.60625	0x5A	0.80625	0x7A	1.00625	0x9A	1.20625	—	—
0x1B	0.41250	0x3B	0.61250	0x5B	0.81250	0x7B	1.01250	0x9B	1.21250	—	—
0x1C	0.41875	0x3C	0.61875	0x5C	0.81875	0x7C	1.01875	0x9C	1.21875	—	—
0x1D	0.42500	0x3D	0.62500	0x5D	0.82500	0x7D	1.02500	0x9D	1.22500	—	—
0x1E	0.43125	0x3E	0.63125	0x5E	0.83125	0x7E	1.03125	0x9E	1.23125	—	—
0x1F	0.43750	0x3F	0.63750	0x5F	0.83750	0x7F	1.03750	0x9F	1.23750	—	—

Table 11. Compensation Register (COMP, 0x08)

COMP								
BIT NO.	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	ZEN	GM[1:0]		Z	RCOMP[3:0]			
POR	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP

BIT	BIT DESCRIPTION
ZEN	**Zero Enable:** 0 = Disable feed-forward zero 1 = Enable feed-forward zero
GM[1:0]	**Feed-Forward GM Selection to Set Zero Position:** 00 = 100µS 01 = 188µS 10 = 265µS 11 = 335µS
Z	**Feed-Forward Zero Adjustment:** 0 = 300kΩ: Zero at lower frequency 1 = 80kΩ: Zero at higher frequency
RCOMP[3:0]	**Compensation-Resistor Selection:** 0 = 70kΩ 1 = 105kΩ 2 = 140kΩ 3 = 175kΩ 4 = 210kΩ 5 = 245kΩ 6 = 280kΩ 7 = 315kΩ 8 = 30kΩ 9 = 65kΩ 10 = 105kΩ 11 = 140kΩ 12 = 170kΩ 13 = 205kΩ 14 = 240kΩ 15 = 310kΩ

PG Output

The IC features an open-drain PGOOD output that asserts when the output voltage is between the PG_UV and PG_OV thresholds. PG_ is asserted after the power-good active-timeout period. An additional 220µs (typ) PG_ delay exists following soft-start or DVS slewing. PG_ is deasserted after a UV/OV propagation delay if the output voltage is outside the PG_ UV/OV thresholds. Connect PG_ to a pullup supply with a 20kΩ resistor.

Soft-Start

The IC includes a programmable soft-start rate. Soft-start limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Dynamic Voltage Scaling

The step-down regulators feature dynamic voltage scaling (DVS) to allow loads to margin their supply voltage. DVS registers for OUT1 and OUT2 are programmed with VID[6:0]. The slew rate during DVS is adjustable with SR[3:0] (see Table 8). The PG_ comparator is masked to prevent false PG_ interrupts during the DVS period. I^2C DVS commands should only be issued when the output voltage is no longer slewing and is in a stable state.

Shutdown

During shutdown, the output voltage is ramped down at the 0.875mV/µs slew rate. The CS- pulldown is enabled as needed to assist in the ramp down. When powering down in skip mode under light load, the falling ramp may be based on the RC discharge curve based on C_{OUT} and the 5Ω pulldown resistance.

Spread-Spectrum Option

The IC features spread-spectrum (SS) operation by varying the internal operating frequency down by 3%, relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to external sync.

Synchronization (SYNC)

SYNC is an I^2C-programmable I/O. When configured as an input and the FPWM bit = 0, driving SYNC low or unconnected places the converter in skip mode. Forcing SYNC logic-high places the IC in forced-PWM (FPWM) mode. Input triggering on the rising edge or falling edge is determined by the setting of registers SO[1:0], see Table 7. When SO[1:0] = 2, SYNC is configured as an output. The output clock is 180° out-of-phase with the internal clock.

Current-Limit/Short-Circuit Protection

The current-limit circuit uses differential current-sense inputs (CS_+ and CS_-) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold (VLIM_ = 45mV (typ)), the PWM controller turns off the high-side MOSFET.

The high side turns on again once the inductor current drops below the valley current limit. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT}/V_{IN}). See Figure 8 for current-sense configurations.

If the inductor current exceeds the maximum current limit programmed at CS_+ and CS_-, the respective driver turns off. In an overcurrent mode, this results in shorter and shorter high-side pulses. A hard short results in a minimum on-time pulse every clock cycle. During a hard short, the IC turns off and repeats soft-start every 4ms (at 2.2MHz switching frequency) until the short is removed. For an example, see the short-circuit (PWM mode) waveform (TOC20) in the *Typical Operating Characteristics* section.

PWM/Skip Modes

The IC features a SYNC input that puts both converters either in skip mode or forced-PWM mode of operation. See the *Pin Description* table for mode details. In PWM mode of operation, the converter switches at a constant frequency with variable on-time. In skip mode of operation, the converter's switching frequency is load-dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often is the case in PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode. VID updates while the IC is in skip mode are delayed until the next LX_ switching pulse, which is load-dependent. If immediate VID update response is required, switch the IC to PWM mode when updating the VID.

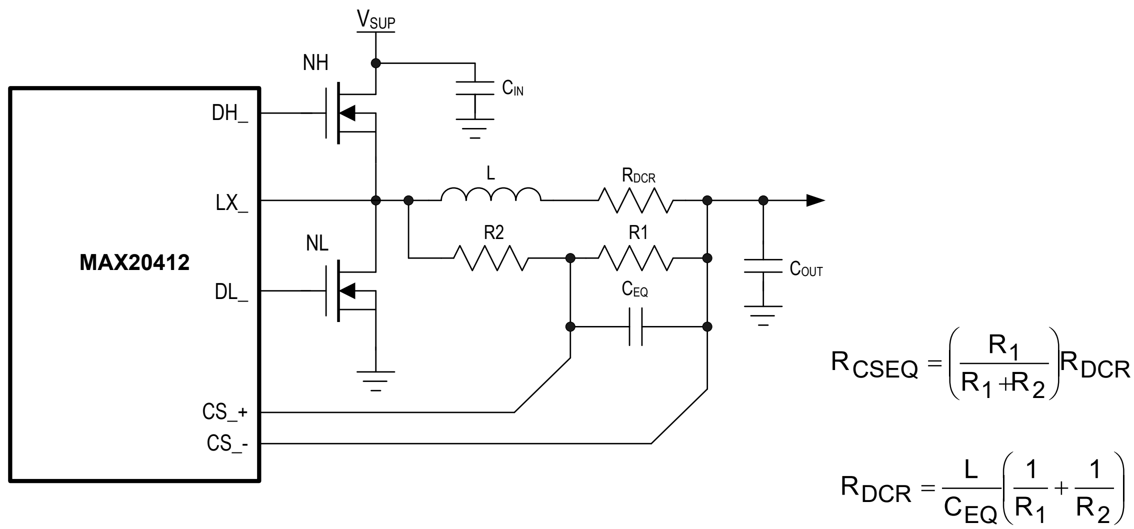


Figure 8. Current-Sense Configurations

Dual-Phase Operation

With the addition of a MAX15492 gate-driver IC connected to PWM1X and CS1X+, OUT1 of the MAX20412 can support two phases to increase the output current by a factor of two. The same inductor, MOSFETs, and current-limit network must be used on both phases to ensure proper current balancing. A total of 200µF to 600µF of ceramic output capacitance is required per phase, depending on load-transient requirements.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the IC. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Lossless Inductor DCR Sensing

High-power applications that do not require highly accurate current-limit protection can reduce the overall power dissipation by connecting a series RC circuit across the inductor with an equivalent time constant

Equations 1:

$$R_{CSEQ} = \left(\frac{R1}{R_1 + R_2}\right) R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

where R_{CSEQ} is the required current-sense resistor and R_{DCR} is the inductor's series DC resistance. Use the inductance and R_{DCR} values provided by the inductor manufacturer.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CS_+ and CS_-. Place the sense network close to the device with short, direct traces, making a Kelvin-sense connection to the current-sense network.

High-Side Gate-Drive Supply (BST1)

The high-side MOSFET is turned on by closing an internal switch between BST1 and DH1 and transferring the bootstrap capacitor's (at BST1) charge to the gate of the high-side MOSFET. This charge refreshes when the high-side MOSFET turns off and the LX1 voltage drops down to ground potential, taking the negative terminal of the capacitor to the same potential. At this time, the bootstrap diode recharges the positive terminal of the bootstrap capacitor. The selected n-channel high-side MOSFET determines the appropriate boost-capacitance values ($C_{BST\_}$ in the *Typical Operating Circuit*) according to the following equation.

Equation 2:

$$C_{BST\_} = \frac{Q_G}{\Delta V_{BST1}}$$

where Q_G is the total gate charge of the high-side MOSFET and ΔV_{BST1} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST1} such that the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST1} = 100mV to 300mV) when determining $C_{BST\_}$.

The boost capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF works in most cases. C_{BST2} is calculated using the same method described for C_{BST1}.

Applications Information

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation.

Equation 3:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{PV\_} - V_{OUT})}}{V_{PV\_}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{PV\_} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input-voltage ripple using the following equations

Equations 4:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{PV\_} - V_{OUT}) \times V_{OUT}}{V_{PV\_} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

and:

$$D = \frac{V_{OUT}}{V_{PV\_}}$$

I_{OUT} is the maximum output current, D is the duty cycle.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20412: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use the following formula to determine the minimum inductor value:

Equation 5:

$$L_{MIN} = 1.3 \times \left[\frac{(V_{PVMAX} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{PVMAX}} \right)}{f_{SW} \times I_{OUTMAX} \times K_{INDMAX}} \right]$$

where f_{SW1} is the operating frequency and 1.3 is a coefficient that accounts for inductance initial precision. K_{INDMAX} is the maximum inductor current ripple. A good initial maximum inductor current ripple is 30% peak to peak (K_{INDMAX} = 0.3).

For proper operation, the chosen inductor value must be ≥ L_{MIN}. The maximum inductor value recommended is twice the chosen value from the above formula.

MOSFET Selection

The gate drivers drive two external logic-level n-channel MOSFETs as the circuit switch elements. To choose these MOSFETs, the key selection parameters are:

- Drain-to-Source On-Resistance ($R_{DS(ON)}$)
- Maximum Drain-to-Source Voltage ($V_{DS(MAX)}$)
- Minimum Threshold Voltage ($V_{TH(MIN)}$)
- Total Gate Charge (Q_G)
- Reverse Transfer Capacitance (C_{RSS})
- Power Dissipation

Both n-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. The conduction losses at minimum input voltage should not exceed the MOSFET package thermal limits or violate the overall thermal budget. Also ensure that the conduction losses, plus switching losses at the maximum input voltage, do not exceed package ratings or violate the overall thermal budget. In particular, check that the dV/dt caused by DH_ turning on does not pull up the DL_ gate through its drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET; therefore, the power dissipation in the IC due to drive losses must be checked. Both MOSFETs must be selected so that their total gate charge is low enough; thus, P_V/V_{OUT} can power both drivers without overheating the IC.

Equation 6:

$$P_{DRIVE} = V_{OUT} \times (Q_{GTOTH} + Q_{GTOTL}) \times f_{SW1}$$

Where Q_{GTOTL} is the low-side MOSFET total gate charge and Q_{GTOTH} is the high-side MOSFET total gate charge. Select MOSFETs with a Q_{G_TOTAL} of less than 15nC.

The n-channel MOSFETs must deliver the average current to the load and the peak current during switching. Dual MOSFETs in a single package can be an economical solution. To reduce switching noise for smaller MOSFETs, use a series resistor in the DH_ path and additional gate capacitance. Contact the factory for guidance using gate resistors.

Output Capacitor

Use low-ESR ceramic capacitors on the output. Other capacitor types should be verified with a gain and phase analysis. The MAX20412's programmable compensation (Table 11) allows a wide range of capacitor values to meet different requirements. A good starting point for selecting the value is with the formula. below.

Equation 7:

$$C(\mu F) = 10 \times \frac{I_{OUT}}{V_{OUT}}$$

Selector Guide

OPTION SUFFIX	V_{OUT1} (V)						V_{OUT2} (V)					
	VMAX	CONFIG	VID	SLEW	COMP	I^2C	VMAX	CONFIG	VID	SLEW	COMP	I^2C
A/V+	0x71 0.95V	0x08	0x5D 0.825V	0x00	0xE0	0x74	0x71 0.95V	0x08	0x5D 0.825V	0x00	0xE0	0x70
C/V+	0x69 0.90V	0x08	0x51 0.75V	0x00	0xE9	0x74	0x71 0.95V	0x08	0x5D 0.825V	0x00	0xE0	0x70
D/V+	0x7E 1.03V	0x0C	0x79 1.00V	0x03	0xE6	0x70	0x7E 1.03V	0x0C	0x79 1.00V	0x03	0xE6	0x74

For variants with different options, contact factory.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20412ATJ_/V+	-40°C to +125°C	32 TQFN-EP*

Note: *Insert the desired option suffix from the Selector Guide into the blank.*

/V Denotes an automotive-qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	9/18	Added future product D/V+ variant to *Selector Guide*	28
2	10/18	Replaced V_{OUT1} and V_{OUT2} content for future product D/V+ variant in *Selector Guide*	28
3	11/18	Removed future-product designation from D/V+ variant in *Selector Guide*	28
4	2/20	Updated the land pattern number in *Package Information*	3