Click here for production status of specific part numbers.

MAX20416

2.2MHz Dual-Output, Low-Voltage Step-Down Converters

General Description

The MAX20416 is a high-efficiency, dual-output, low-voltage DC-DC converter. The synchronous step-down converters operate from a 3.0V to 5.5V input voltage range and provide a 0.8V to 3.8V output voltage range at up to 3A. The buck converters achieve ±1.5% output error over load, line, and temperature range.

The IC features a 2.2MHz fixed-frequency pulse-width modulation (PWM) mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for use of all-ceramic capacitors, minimizing the external component footprint. Programmable spread-spectrum-frequency modulation minimizes radiated electromagnetic emissions. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

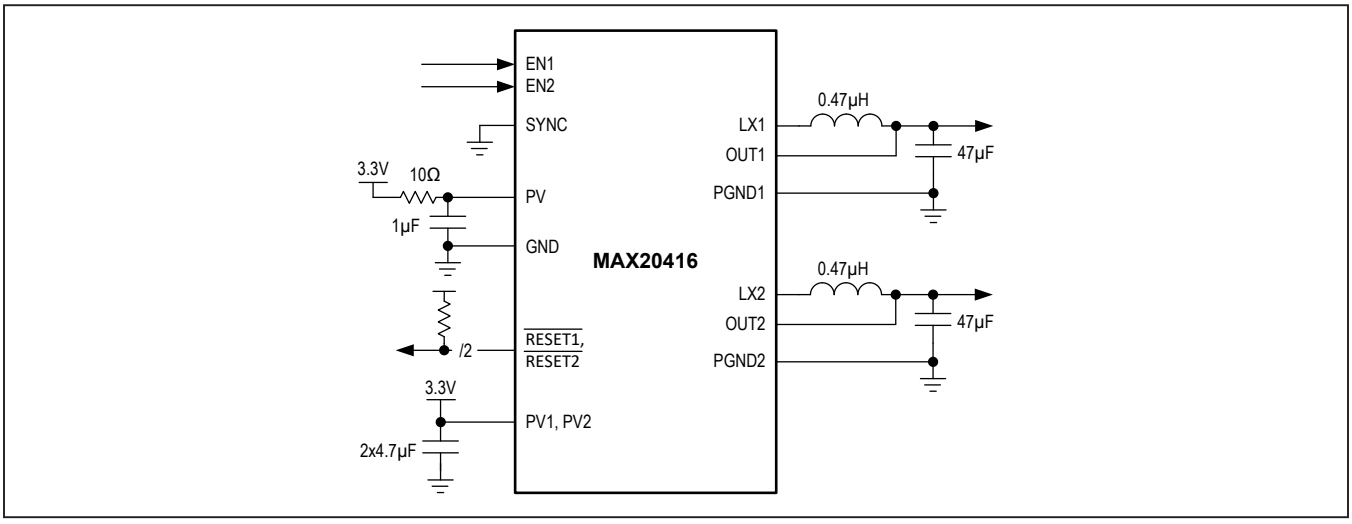
The IC is offered with factory-preset or resistor-adjustable output voltages. Additional features include soft-start ramping, overcurrent limiting, and overtemperature protection. The MAX20416 is available in a lead(Pb)-free, 24-pin TQFN package (see the *Ordering Information/Selector Guide* for available options).

Benefits and Features

- Multiple Functions for Small Size
  - Dual Synchronous Buck Converters Up to 3A
    - Fixed Output Voltage from 0.8V to 3.8V
    - Resistor-Adjustable Output Voltage
  - 3.0V to 5.5V Operating Supply Voltage
  - 2.2MHz Operation
  - 93% ±3% Undervoltage Threshold
  - 107% ±3% Overvoltage Threshold
  - Individual EN Inputs and $\overline{\text{RESET}}$_ Outputs
- High Precision
  - ±1.5% Output-Voltage Accuracy
  - Good Load-Transient Performance for Buck Converters
- Robust for the Automotive Environment
  - Current-Mode, Forced-PWM, and Skip Operation
  - Overtemperature and Short-Circuit Protection
  - 4mm x 4mm 24-Pin TQFN
  - -40°C to +125°C Automotive Temperature Range

***Ordering Information/Selector Guide* appears at end of data sheet.**

Typical Operating Circuit



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Absolute Maximum Ratings

PV1, PV2 to PGND_ .....-0.3V to +6V
PV to GND.....-0.3V to +6V
GND to PGND_.....-0.3V to +0.3V
EN1, EN2, SYNC to GND .....-0.3V to V_{PV} + 0.3V
$\overline{RESET1}$, $\overline{RESET2}$ to GND .....-0.3V to +6V
OUT1 to PGND1 .....-0.3V to V_{PV1} + 0.3V
OUT2 to PGND2 .....-0.3V to V_{PV2} + 0.3V
LX1 to PGND1.....-0.3V to V_{PV1} + 0.3V
LX2 to PGND2.....-0.3V to V_{PV2} + 0.3V
LX1, LX2 Continuous RMS Current 3A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-pin TQFN-EP (derate 30.3mW/°C > +70°C) 2222mW
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 24-PIN TQFN	
Package Code	T2444+4C
Outline Number	**21-0139**
Land Pattern Number	**90-0022**
THERMAL RESISTANCE, SINGLE-LAYER BOARD:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	36°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{PV} = V_{PV1} = V_{PV2} = 3.3V, V_{EN1} = V_{EN2} = 3.3V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	Fully operational	3.0		5.5	V
Undervoltage Lockout (UVLO)	V_{UVLOR}	Rising		2.7	2.9	V
	V_{UVLOF}	Falling	2.4	2.6		
Shutdown Supply Current	I_{IN_SHDN1}	EN1, EN2 = low	1	2.2	5	µA
Supply Current	I_{IN1}	EN1 = high, I_{OUT1} = 0mA, skip, V_{OUT1} 2% above regulation point	40	80	160	µA
	I_{IN2}	EN2 = high, I_{OUT2} = 0mA, skip, V_{OUT2} 2% above regulation point	40	80	160	
PWM Switching Frequency	f_{SW}	Internally generated	2.0	2.2	2.4	MHz
Spread Spectrum	SS	Factory option enabled		±3		%

Electrical Characteristics (continued)

(V_{PV} = V_{PV1} = V_{PV2} = 3.3V, V_{EN1} = V_{EN2} = 3.3V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT1 SYNCHRONOUS STEP-DOWN CONVERTER						
Voltage Accuracy	V_{OUT1}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, PWM mode selected	-1.5		+1.5	%
pMOS On-Resistance	R_{HS1}	V_{PV} = V_{PV1} = 3.3V, I_{LX1} = 0.2A	35	75	150	mΩ
nMOS On-Resistance	R_{LS1}	V_{PV} = V_{PV1} = 3.3V, I_{LX1} = 0.2A	20	50	100	mΩ
pMOS Current-Limit Threshold	I_{LIM1_1}	Option 1 (1A)	1.4	1.9		A
	I_{LIM1_2}	Option 2 (2A)	2.8	3.8		
	I_{LIM1_3}	Option 3 (3A)	4.5	5.8		
	I_{LIM1_4}	Option 4 (3.6A)	5.1	6.5		
nMOS Zero-Crossing Threshold	I_{ZX1}			150		mA
Maximum Duty Cycle	DC_{MAX1}				100	%
Minimum On-Time	$t_{MINTON1}$		25	44	68	ns
LX1 Discharge Resistance	R_{DIS1}	V_{EN1} = 0V (connected to LX1)	20	40	80	Ω
Switching Phase	PH_{LX1}	Respect to LX2 rising edge		180		degree
Skip Threshold	TH_{SKIP1}	Percentage of pMOS current-limit threshold	4	12	20	%
Soft-Start Time	t_{SS1_0}	Factory option selected (default)		2.5		ms
	t_{SS1_1}	Factory option selected		1.25		
OUT2 SYNCHRONOUS STEP-DOWN CONVERTER						
Voltage Accuracy	V_{OUT2}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, PWM mode selected	-1.5		+1.5	%
pMOS On-Resistance	R_{HS2}	V_{PV} = V_{PV2} =3.3V, I_{LX2} = 0.2A	35	75	150	mΩ
nMOS On-Resistance	R_{LS2}	V_{PV} = V_{PV2} = 3.3V, I_{LX2} = 0.2A	20	50	100	mΩ
pMOS Current-Limit Threshold	I_{LIM2_1}	Option 1 (1A)	1.4	1.9		A
	I_{LIM2_2}	Option 2 (2A)	2.8	3.8		
	I_{LIM2_3}	Option 3 (3A)	4.5	5.8		
	I_{LIM2_4}	Option 4 (3.6A)	5.1	6.5		
nMOS Zero-Crossing Threshold	I_{ZX2}			150		mA
Maximum Duty Cycle	DC_{MAX2}				100	%
Minimum On-Time	$t_{MINTON2}$		25	44	68	ns
LX2 Discharge Resistance	R_{DISCH2}	V_{EN2} = 0V	20	40	80	Ω
Switching Phase	PH_{LX2}	Respect to LX2 rising edge		0		degree
Skip Threshold	TH_{SKIP2}	Percentage of pMOS current-limit threshold	4	12	20	%
Soft-Start Time	t_{SS2_0}	Factory option selected		2.5		ms
	t_{SS2_1}	Factory option selected		1.25		

Electrical Characteristics (continued)

(V_{PV} = V_{PV1} = V_{PV2} = 3.3V, V_{EN1} = V_{EN2} = 3.3V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

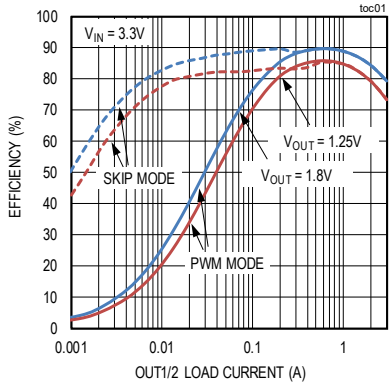
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL OVERLOAD						
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising		165		°C
Hysteresis	T_{HYST}			15		°C
OUT1, OUT2 OPEN-DRAIN $\overline{\text{RESET}}$ OUTPUTS ($\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$)						
Overvoltage-Threshold Accuracy	OV_{ACC}	Rising, % of nominal output	-3		+3	%
Undervoltage-Threshold Accuracy	UV_{ACC}	Falling, % of nominal output	-3		+3	%
Active Hold Period	t_{HOLD}			7.4		ms
Undervoltage-Propagation Delay	t_{UVDEL}	10% below threshold		10		µs
Overvoltage-Propagation Delay	t_{OVDEL}	10% above threshold		50		µs
$\overline{\text{RESET}}$[1:2]-High Leakage Current	I_{ROZH}	$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$ = 5.5V	-0.5	0.1	+0.5	µA
Output Low Level	V_{ROL}	3.0V ≤ V_{PV} ≤ 5.5V, sinking 2mA			0.2	V
EN1, EN2, SYNC INPUTS						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis	V_{ENHYST}			0.1		V
EN1, EN2 Pulldown Current	I_{ENPD}	V_{PV} = 5.0V, T_A = 25°C	0.2	0.5		µA
SYNC Input Pulldown	R_{SYNCPD}		50	100	200	kΩ
SYNC Input Frequency Range	f_{SYNC}		1.8		2.6	MHz
SYNC OUTPUT						
Output Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Output High	V_{OH}	V_{PV} = 3.3V, I_{SOURCE} = 2mA	2.7			V

Note 1: All units are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.

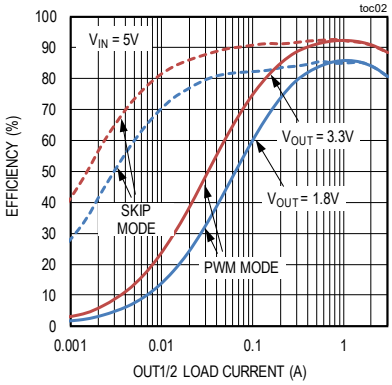
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

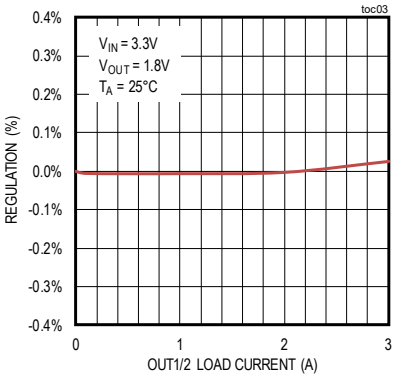
OUT1/2 EFFICIENCY



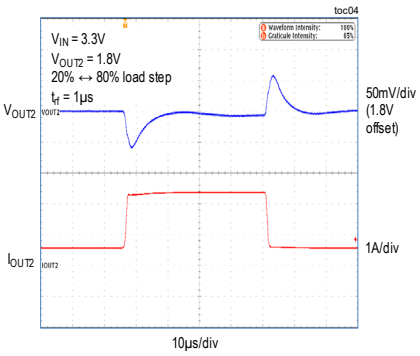
OUT1/2 EFFICIENCY



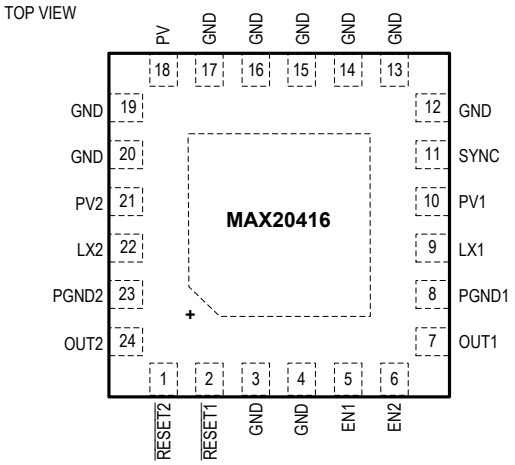
OUT1/2 LOAD REGULATION



OUT1/2 LOAD TRANSIENT (PWM MODE)



Pin Configurations



TQFN
(4mm x 4mm)

Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{RESET2}}$	Open-Drain $\overline{\text{RESET}}$ Output for OUT2. To obtain a logic signal, pull up $\overline{\text{RESET2}}$ with an external resistor.
2	$\overline{\text{RESET1}}$	Open-Drain $\overline{\text{RESET}}$ Output for OUT1. To obtain a logic signal, pull up $\overline{\text{RESET1}}$ with an external resistor.
3, 4, 12, 14–16, 19, 20	GND	Ground. Connect all GND and PGND pins together
5	EN1	Active-High Enable Input for OUT1. Drive EN1 high for normal operation.
6	EN2	Active-High Enable Input for OUT2. Drive EN2 high for normal operation.
7	OUT1	OUT1 Voltage-Sense Input/Feedback Pin
8	PGND1	Power Ground for OUT1. Connect all GND and PGND pins together.
9	LX1	Inductor Connection. Connect LX1 to the switched side of the inductor.
10	PV1	Power Input Supply for OUT1. Connect a 4.7µF ceramic capacitor from PV1 to PGND1.
11	SYNC	SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skip mode of operation under light loads. Connect SYNC to PV or an external clock to enable fixed-frequency forced-PWM mode of operation. When configured as an output (factory configured), connect SYNC to other devices' SYNC inputs.
13	PGND	Power Ground. Connect all GND and PGND pins together.
17	GND	Analog Ground. Connect all GND and PGND pins together
18	PV	Analog Input Supply. Connect a 1µF or larger ceramic capacitor from PV to GND with a 10Ω resistor in series to the supply voltage.
21	PV2	Power Input Supply for OUT2. Connect a 4.7µF ceramic capacitor from PV2 to PGND2.
22	LX2	Inductor Connection. Connect LX2 to the switched side of the inductor.

Pin Description (continued)

PIN	NAME	FUNCTION
23	PGND2	Power Ground for OUT2. Connect all GND and PGND pins together.
24	OUT2	OUT2 Voltage-Sense Input/Feedback
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX20416 is a high-efficiency, dual-output, low-voltage DC-DC converter. The two synchronous step-down converters (OUT1/OUT2) operate from a 3.0V to 5.5V input voltage and provide a 0.8V to 3.8V output voltage at up to 3A. OUT1/OUT2 can be set to resistor adjustable or to a fixed voltage. The buck converters achieve ±1.5% output error over load, line, and temperature range.

The IC features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency-modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. The spread modulation can be factory set to be pseudorandom. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

The IC contains high-accuracy overvoltage/undervoltage thresholds for each output mapped to the $\overline{RESET1}$ and $\overline{RESET2}$ pins.

In light-load applications, a logic input (SYNC) allows the IC to operate either in skip mode for reduced current consumption, or fixed-frequency, forced-PWM mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery.

Enable Inputs (EN1, EN2)

The enable control inputs (EN1, EN2) activate the device channel from its low-power shutdown state. EN1/EN2 have an input threshold of 1.0V (typ), with hysteresis of 100mV (typ). EN1 and EN2 are fully independent with no timing restrictions between each other. When an enable input goes high, the associated output voltage ramps up with the programmed soft-start time.

$\overline{RESET1}$/$\overline{RESET2}$ Outputs

The IC features individual open-drain reset outputs for each output that asserts low when the corresponding output voltage is outside of the undervoltage/overvoltage window. $\overline{RESET1}$/$\overline{RESET2}$ remain asserted for a fixed timeout period after the output rises up to its regulated voltage. The fixed timeout period is set to 7.4ms. See the *Ordering Information/Selector Guide* for available options. To obtain a logic signal, place a pullup resistor between the $\overline{RESET1}$/$\overline{RESET2}$ pins to the system I/O voltage.

Internal Oscillator

The IC has a spread-spectrum oscillator that varies the internal operating frequency up by ±3% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally applied oscillation frequency. The spread frequency generated is pseudorandom with a repeat rate well below the audio band.

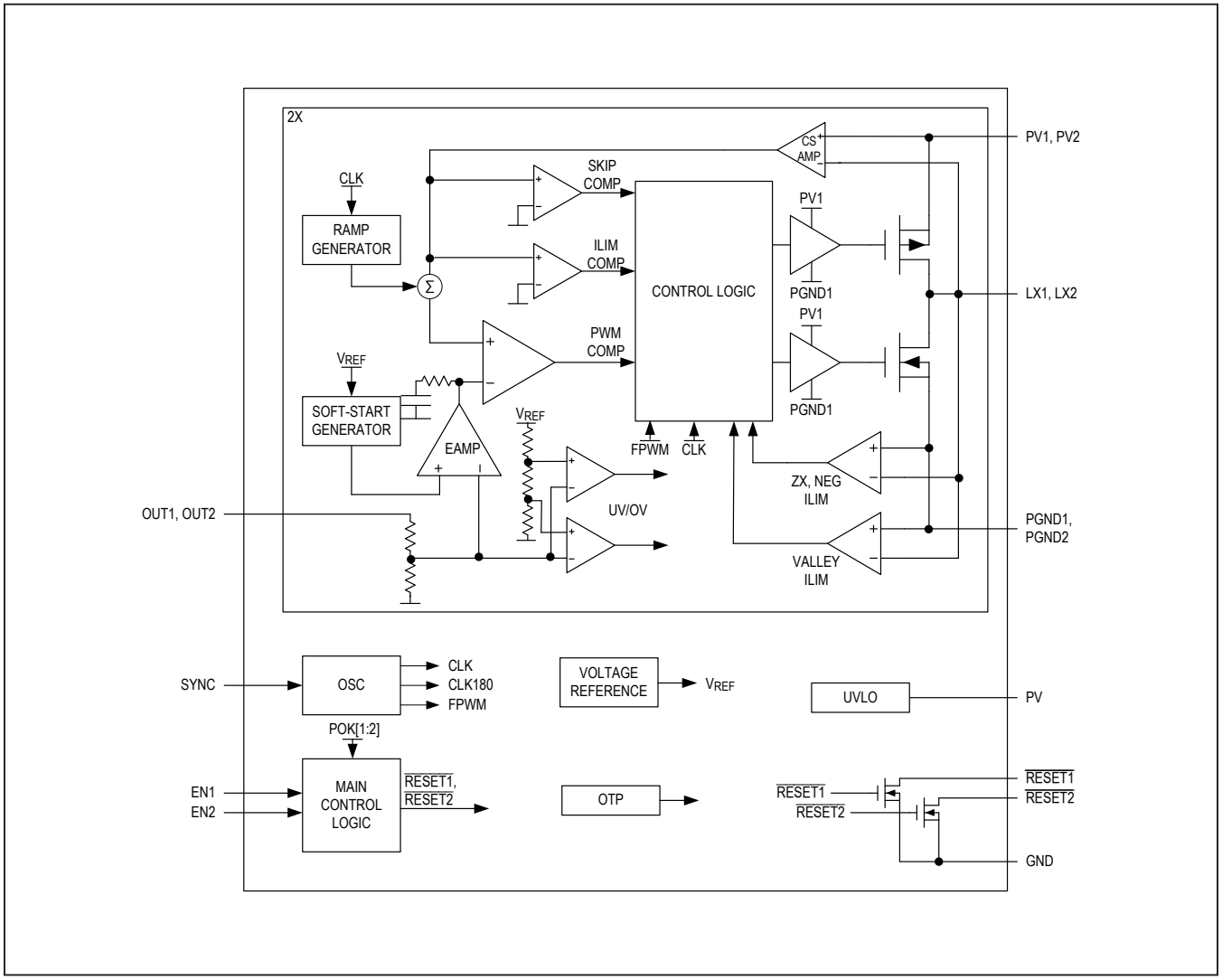
Synchronization (SYNC)

SYNC is factory-programmable I/O. See the *Ordering Information/Selector Guide* for available options. When configured as an input (default), a logic-high on SYNC enables the fixed-frequency, forced-PWM mode. Apply an external clock on the SYNC input to synchronize the internal oscillator to an external clock. The SYNC input accepts 1.8MHz < f_{SYNC} < 2.6MHz signal frequencies. When the pin is open or logic-low, the SYNC input enables the device to enter a low-power skip mode under light-load conditions. When configured as an output, SYNC outputs the internally generated 2.2MHz clock that switches from PV to GND. All converters operate in forced-PWM mode when SYNC is configured as an output.

Soft-Start

The IC includes a fixed soft-start time of 1.25ms or 2.5ms (factory configured). Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Internal Block Diagram



Current Limit/Short-Circuit Protection

The IC features current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

PWM/Skip Modes

The IC features a SYNC input that puts the converter in either skip mode or forced-PWM mode of operation. See the *Pin Description* table for more details. In PWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often is the case in PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the IC. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the device to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Applications Information

Input Capacitors

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. 4.7µF X7R ceramic capacitors are recommended for the PV1 and PV2 pins. A 1.0µF X7R ceramic capacitor is recommended for the PV pin, with PV connected to PV1/PV2 through a 10Ω resistor.

Inductor Selection

Three key inductor parameters must be specified for operation with the IC: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output-current capability of the output. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple-current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. The MAX20416 is designed for ΔI_{P-P} equal to ~30% of the full load current. Use Equation 1 to calculate the inductance.

Equation 1:

$$L_{MIN1} = \frac{(V_{IN} - V_{OUT\_}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times 30\%}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is 2.2MHz. The maximum output capability (I_{MAX}) is 1A, 2A, or 3A based on the specific part number of the device. See the *Output Capacitor* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during continuous output short circuits.

Equation 2 ensures that the inductor current downslope is less than the internal slope compensation. For this to be the case, Equation 2 needs to be satisfied.

Equation 2:

$$-m \geq \frac{m2}{2}$$

where:

m2	The inductor current downslope. $\frac{V_{OUT}}{L} \times R_{CS}$
-m	Slope Compensation: $\left[0.940 \frac{V}{\mu s}\right]$ for V_{OUT} > 3.2V fixed output $\left[0.535 \frac{V}{\mu s}\right]$ for V_{OUT} ≤ 3.2V fixed output or adjustable output version
R_{CS}	0.378Ω for 1A channel 0.263Ω for 2A channel 0.176Ω for 3A channel

Solving for L and adding a 1.3 multiplier to account for tolerances in the system (see Equation 3).

Equation 3:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.3$$

To satisfy both, L_{MIN1} and L_{MIN2} must be set to the larger of the two:

$$L_{MIN} = \max (L_{MIN1}, L_{MIN2})$$

The maximum inductor value recommended is 2 times the chosen value from the above formula:

$$L_{MAX} = 2 \times L_{MIN}$$

Select a nominal inductor value based on the following formula. For optimal performance, select the first standard inductor value greater than L_{MIN}:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

Output Capacitor

The IC is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The following output capacitor calculations are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify proper stability is achieved, as shown in Equation 4.

Equation 4:

$$C_{OUT12\_MIN} = 10.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT12\_NOM} = 27.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

With C_{OUT12_MIN} defining the minimum fully derated output capacitance required for a stable output and C_{OUT12_NOM} defining the nominal output capacitance for maximum phase margin. I_{MAX} is the maximum DC current capability of the associated output, as defined in the *Ordering Information/ Selector Guide*). V_{OUT} is the output voltage for the associated channel.

Adjustable Output-Voltage Option

The MAX20416 adjustable output-voltage version allows the customer to set the outputs to any voltage between 0.5V and approximately PV - 0.5V (see the *Ordering Information/ Selector Guide*). The actual maximum output-voltage setting is limited by the specific application conditions and components. Connect a resistive divider from the output capacitor (V_{OUT}) to OUT to GND to set the output voltage (Figure 1). Select R_2 (OUT to GND resistor) ≤ 100kΩ. Calculate R_1 (V_{OUT} to OUT resistor) with Equation 5.

Equation 5:

$$R_1 = R_2 \left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where V_{FB} = 800mV (see the *Electrical Characteristics*).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across R_1 in the resistive-divider network. Use Equation 6 to determine the value of the capacitor.

Equation 6:

$$C_1 = 50 \frac{R_2}{R_1} pF$$

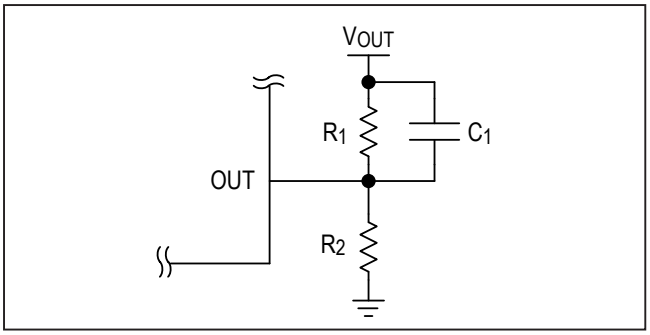


Figure 1. Adjustable Output-Voltage Configuration

Ordering Information/Selector Guide

PART	V_{OUT1} (V)	I_{OUT1} (A)	UV1/OV1 (%)	V_{OUT2} (V)	I_{OUT2} (A)	UV2/OV2 (%)	t_{HOLD} (ms)	SS	SYNC
MAX20416ATGA/V+	1.5	3	93/107	1.2	3	93/107	7.4	Off	Input
MAX20416ATGB/V+	1.5	3	93/107	1.4	3	93/107	0.5	Off	Input
MAX20416ATGD/V+	ADJ	3	93/107	ADJ	3	93/107	7.4	Off	Input
MAX20416ATGE/V+**	3.8	3	93/107	3.3	3	93/107	7.4	On	Input
MAX20416ATGF/V+**	1.175	3	93/107	1.8	3	93/107	7.4	On	Input

Note: *For variants with different options, contact factory.*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/17	Initial release	—
1	5/18	Updated the *Absolute Maximum Ratings* section, *Electrical Characteristics* table and the *Ordering Information/Selector Guide* table, and added MAX20416ATGE/V+ and MAX20416ATGF/V+ as future parts.	2–4, 11
2	6/18	Updated the *Electrical Characteristics* table, *Synchronization (SYNC)* section, and the *Ordering Information/Selector Guide* table.	3–4, 7, 11

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