Click here for production status of specific part numbers.

MAX20419

High-Efficiency, 3-Output, Low-Voltage DC-DC Converter

General Description

The MAX20419 is a high-efficiency, 3-output, low-voltage DC-DC converter IC. OUT1 boosts the input supply to 5V at up to 750mA, while two synchronous step-down converters operate from a 3.0V to 5.5V input voltage range and provide a 0.8V to 3.8V output voltage range at up to 3.6A. The boost converter achieves ±1.9% and the buck converters achieve ±1.4% output error over load, line, and temperature range. The IC features a 2.2MHz fixed-frequency pulse-width modulation (PWM) mode for better noise immunity and load-transient response, and a pulse-frequency-modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads, and make the layout a much simpler task with respect to discrete solutions.

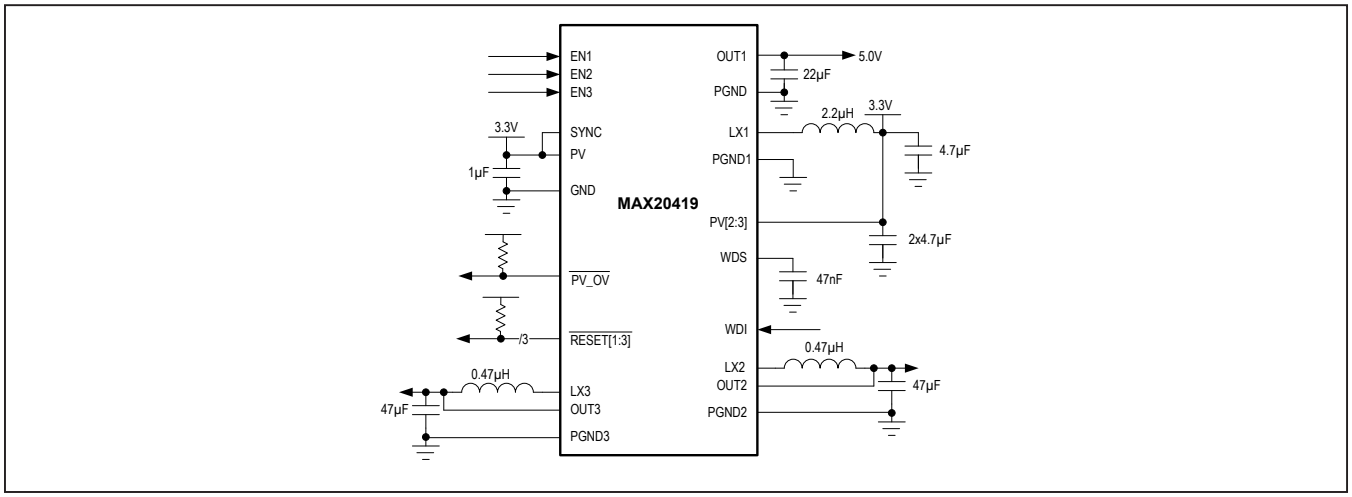
The IC is offered with factory-preset output voltages (see the *Ordering Information/Selector Guide* for available options). Other features include soft-start, overcurrent, and overtemperature protections. The MAX20419 also has several redundancy and diagnostic features for compatibility with ASIL-rated applications.

***Ordering Information/Selector Guide* appears at end of data sheet.**

Benefits and Features

- Multiple Functions for Small Size
  - Synchronous 750mA Boost Converter
  - Fixed at 5V Output
  - Dual Synchronous Buck Converters Up to 3.6A
    - Factory Configurable from 0.8V to 3.8V in 25mV Steps
  - Programmable Windowed Watchdog
  - 3.0V to 5.5V Operating Supply Voltage
  - 2.2MHz Operation
  - Individual $\overline{\text{RESET\_}}$ Outputs
  - High-Precision Performance
    - ±1.9% Output-Voltage Accuracy (OUT1) and ±1.4% Output-Voltage Accuracy (OUT2, OUT3)
    - ±1.3% OV/UV Monitoring (OUT1–OUT3, PV)
    - Excellent Load-Transient Performance
- Diagnostics and Redundant Circuits
  - ASIL-C Compliant
  - Redundant Reference
  - Fail Safe on Open Pins
  - Shorted Pin Detection on $\overline{\text{RESET1}}$–$\overline{\text{RESET3}}$
  - Input Overvoltage Detection
- Robust for the Automotive Environment
  - Current Mode, Forced-PWM, and Skip Operation
  - Overtemperature and Short-Circuit Protection
  - 24-Pin (4mm x 4mm) TQFN with Exposed Pad
  - -40°C to +125°C Automotive Temperature Range

Typical Operating Circuit



Absolute Maximum Ratings

PV2, PV3 to PGND_ .....-0.3V to +6V
PV to GND.....-0.3V to +6V
EN1–EN3, SYNC to GND .....-0.3V to V_{PV} + 0.3V
$\overline{RESET1}$–$\overline{RESET3}$, WDI, WDS to GND.....-0.3V to +6V
$\overline{PV\_OV}$ to GND ..... -0.3V to +6V
OUT1 to PGND1 .....-0.3V to +6V
OUT2 to PGND2 ..... -0.3V to V_{PV2} + 0.3V
OUT3 to PGND3 ..... -0.3V to V_{PV3} + 0.3V
LX1 to PGND1.....-0.3V to V_{OUT1} + 0.3V
LX2 to PGND2..... -0.3V to V_{PV2} + 0.3V
LX3 to PGND3..... -0.3V to V_{PV3} + 0.3V
GND to PGND.....-0.3V to +0.3V
LX1 Continuous RMS Current 2A
LX2, LX3 Continuous RMS Current 3A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN-EP (derate 30.3mW/°C > +70°C)..... 2222mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature Range.....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 24-PIN TQFN	
Package Code	T2444+4C
Outline Number	**21-0139**
Land Pattern Number	**90-0022**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{PV} = V_{PV2} = V_{PV3} = 3.3V, EN1 = EN2 = EN3 = 3.3V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C (Notes 1 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	Fully operational	3.0		5.5	V
Undervoltage Lockout (UVLO)	$UVLO_R$	Rising		2.7	2.9	V
	$UVLO_F$	Falling	2.4	2.6		
Shutdown Supply Current	I_{IN}	EN1–EN3 = low	15	45	70	µA
Supply Current (IN1)	I_{IN1}	EN1 = high, I_{OUT1} = 0mA, skip, watchdog disabled	70	150	230	µA
Supply Current (IN2)	I_{IN2}	EN2 = high, I_{OUT2} = 0mA, skip, watchdog disabled	50	125	200	µA
Supply Current (IN3)	I_{IN3}	EN3 = high, I_{OUT3} = 0mA, skip, watchdog disabled	50	125	200	µA
PWM Switching Frequency	f_{SW}	Internally generated	2.0	2.2	2.4	MHz
Spread Spectrum	SS	Factory option enabled		±3		%

Electrical Characteristics (continued)

(V_{PV} = V_{PV2} = V_{PV3} = 3.3V, EN1 = EN2 = EN3 = 3.3V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C (Notes 1 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT1 SYNCHRONOUS DC-DC BOOST CONVERTER						
Output Voltage				5.0		V
Voltage Accuracy	V_{OUT1}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{IN} ≤ 3.6V	-1.9		+1.9	%
pMOS On-Resistance	R_{HS1}	V_{PV} = V_{PV2} = 3.3V, I_{LX1} = 0.1A	60	125	250	mΩ
nMOS On-Resistance	R_{LS1}	V_{PV} = V_{PV2} = 3.3V, I_{LX1} = 0.1A	75	150	300	mΩ
nMOS Current-Limit Threshold	I_{LIM1}		1.6	2	2.6	A
pMOS Turn-Off Threshold	I_{ZX1}		15	50	90	mA
LX1 Leakage Current	I_{LX1LKG}	V_{PV} = V_{PV2} = 6V, LX1 = PGND1 or OUT1, T_A = +25°C	-1	0.1	+1	µA
Maximum Duty Cycle	DC_{MAX1}			75		%
Discharge Resistance	R_{DIS1}	V_{EN1} = 0V, V_{OUT1} = 1V	200	500	750	Ω
Switching Phase	PH_{LX1}	With respect to LX3 rising edge		20		Degrees
Skip Threshold	$SKIP_1$	Percentage of nMOS current-limit threshold	5	15	30	%
Soft-Start Time	t_{SS1}			1.9		ms
OUT2 SYNCHRONOUS STEP-DOWN CONVERTER						
Voltage Accuracy	V_{OUT2}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, PWM mode selected	-1.4		+1.4	%
pMOS On-Resistance	R_{HS2}	V_{PV} = V_{PV2} = 3.3V, I_{LX2} = 0.2A	35	75	150	mΩ
nMOS On-Resistance	R_{LS2}	V_{PV} = V_{PV2} = 3.3V, I_{LX2} = 0.2A	20	50	90	mΩ
pMOS Current-Limit Threshold	I_{LIM2-1}	Option 1 (1A)	2.5	3.2	4.0	A
	I_{LIM2-2}	Option 2 (2A)	3.2	4.3	5.3	
	I_{LIM2-3}	Option 3 (3A)	5.0	6.5	8.5	
	I_{LIM2-4}	Option 4 (3.6A)	5.5	7.3	9.0	
nMOS Zero-Crossing Threshold	I_{ZX2}			150		mA
LX2 Leakage Current	I_{LX2LKG}	V_{PV} = V_{PV2} = 6V, LX2 = PGND or PV, T_A = 25°C	-1	0.1	+1	µA
Maximum Duty Cycle	DC_{MAX2}				100	%
Minimum On-Time	$t_{MINTON2}$		25	48	71	ns
LX2 Discharge Resistance	R_{DIS2}	V_{EN2} = 0V	20	40	80	Ω
Switching Phase	PH_{LX2}	With respect to LX3 rising edge		180		Degrees
Skip Threshold	$SKIP_2$	Percentage of pMOS current-limit threshold	4	12	28	%
Soft-Start Time	t_{SS2}			2.5		ms

Electrical Characteristics (continued)

(V_{PV} = V_{PV2} = V_{PV3} = 3.3V, EN1 = EN2 = EN3 = 3.3V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C (Notes 1 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT3 SYNCHRONOUS STEP-DOWN CONVERTER						
Voltage Accuracy	V_{OUT3}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, PWM mode selected	-1.4		+1.4	%
pMOS On-Resistance	R_{HS3}	V_{PV} = V_{PV3} = 3.3V, I_{LX3} = 0.2A	35	75	150	mΩ
nMOS On-Resistance	R_{LS3}	V_{PV} = V_{PV3} = 3.3V, I_{LX3} = 0.2A	20	50	90	mΩ
pMOS Current-Limit Threshold	I_{LIM3-1}	Option 1 ($1A_{DC}$)	2.5	3.2	4.0	A
	I_{LIM3-2}	Option 2 ($2A_{DC}$)	3.2	4.3	5.3	
	I_{LIM3-3}	Option 3 ($3A_{DC}$)	5.0	6.5	8.5	
	I_{LIM3-4}	Option 3 ($3.6A_{DC}$)	5.5	7.4	9.0	
nMOS Zero-Crossing Threshold	I_{ZX3}			150		mA
LX3 Leakage Current	I_{LX3LKG}	V_{PV} = V_{PV3} = 6V, LX3 = PGND or PV, T_A = 25°C	-1	0.1	+1	µA
Maximum Duty Cycle	DC_{MAX3}				100	%
Minimum On-Time	$t_{MINTON3}$			44	74	ns
LX3 Discharge Resistance	R_{DIS3}	V_{EN3} = 0V (connected to LX3)	20	40	80	Ω
Switching Phase	PH_{LX3}	With respect to LX3 rising edge		0		Degrees
Skip Threshold	$SKIP_3$	Percentage of pMOS current-limit threshold	4	21	28	%
Soft-Start Time	t_{SS3}			2.5		ms
THERMAL OVERLOAD						
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising (Note 2)		165		°C
Hysteresis	T_{HYST}	(Note 2)		15		°C
OUT1–OUT3 OPEN-DRAIN RESET OUTPUTS ($\overline{RESET1}$–$\overline{RESET3}$)						
Overvoltage-Threshold Accuracy	OV_{ACC}	Rising threshold, factory programmed, percentage of actual output	-1.3		+1.3	%
Undervoltage-Threshold Accuracy	UV_{ACC}	Falling threshold, factory programmed, percentage of actual output	-1.3		+1.3	%
Active Hold Period	t_{HOLD}			7.4		ms
Undervoltage-Propagation Delay	t_{UVDEL}	10% below threshold		50		µs
OUT1 Overvoltage-Propagation Delay	t_{OV1DEL}	10% above threshold		50		µs
OUT2 Overvoltage-Propagation Delay	t_{OV2DEL}	10% above threshold		50		µs
OUT3 Overvoltage-Propagation Delay	t_{OV3DEL}	10% above threshold		50		µs
RESET[1:3] High-Leakage Current	I_{ROZH}	T_A = +25°C		0.1		µA
Output Low Level	V_{ROL}	3.0V ≤ V_{PV} ≤ 5.5V, sinking 2mA			0.2	V

Electrical Characteristics (continued)

(V_{PV} = V_{PV2} = V_{PV3} = 3.3V, EN1 = EN2 = EN3 = 3.3V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C (Notes 1 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-GOOD OUTPUT ($\overline{PV\_OV}$)						
PV Overvoltage Threshold	V_{PV_OV}			3.422		V
PV Undervoltage Threshold	V_{PV_UV}			3.178		V
PV Overvoltage/Undervoltage-Threshold Accuracy	V_{PV_TH}	Absolute rising/falling threshold, factory programmed, percentage of supply	-1.3		+1.3	%
Active Hold Period	t_{HOLD1}	Factory option 1		0.47		ms
	t_{HOLD2}	Factory option 2		3.7		
	t_{HOLD3}	Factory option 3 (default)		7.4		
	t_{HOLD4}	Factory option 4		14.8		
OV/UV Delay Filter	t_{PVDEL}	10% below/above threshold		50		µs
PV_OV High-Leakage Current	$I_{PVOVLKG}$	$\overline{PV\_OV}$ = 5.5V		0.1		µA
Output Low Level	V_{PVOL}	3.0V ≤ V_{PV} ≤ 5.5V, sinking 2mA			0.2	V
SYNC INPUTS (EN1–EN3)						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis	V_{ENHYST}			0.1		V
EN1–EN3 Pulldown Current	I_{EN_PD}	V_{PV} = 5.0V, T_A = 25°C	0.1	0.6		µA
EN[1:3] Leakage Current	I_{ENLKG}	0V ≤ V_{PV} ≤ 5.5V, T_A=25°C		0.1		µA
SYNC Input Pulldown	R_{SYNCPD}			100		kΩ
SYNC Input-Frequency Range	f_{SYNC}		1.8		2.6	MHz
SYNC OUTPUT						
Output Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Output High	V_{OH}	V_{PV} = 3.3V, I_{SOURCE} = 2mA	2.7			V
WATCHDOG (WDS, WDI)						
WDS Source Current	I_{WDS}		118	125	133	µA
WDS Ramp Threshold	V_{WDSTH}	Rising	1.2	1.25	1.3	V
WDI Input High Level	V_{WDIH}		1.5			V
WDI Input Low Level	V_{WDIL}				0.5	V
Minimum WDI Pulse Width	t_{WDIMIN}		50	150	300	ns

Note 1: Limits are 100% production tested at TA = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization.

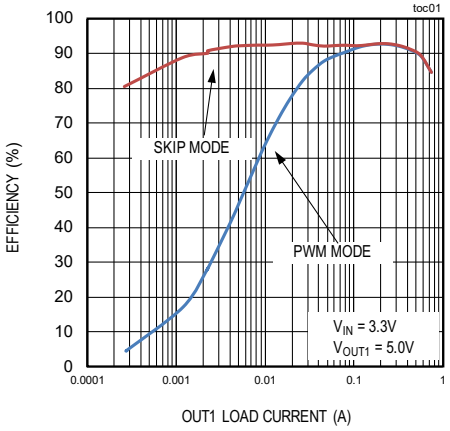
Note 2: Guaranteed by design. Not production tested.

Note 3: The device is designed for continuous operation up to TJ = +125°C for 95,000 hours and TJ = +150°C for 5,000 hours.

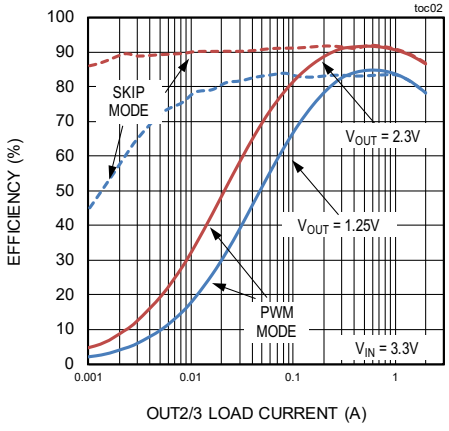
Typical Operating Characteristics

(T_A = +25°C under normal conditions, unless otherwise noted.)

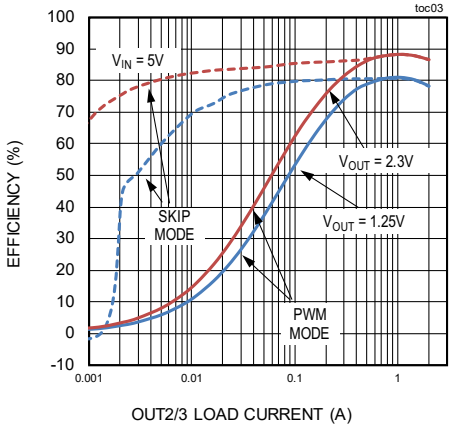
OUT1 EFFICIENCY



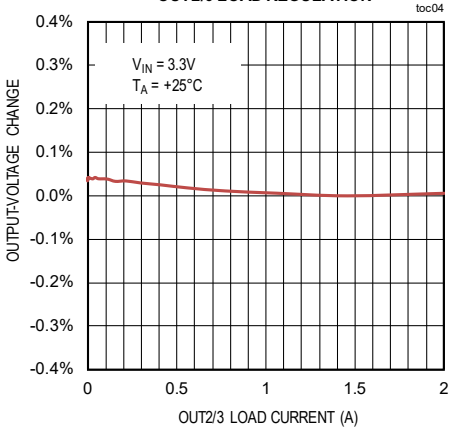
OUT2/3 EFFICIENCY



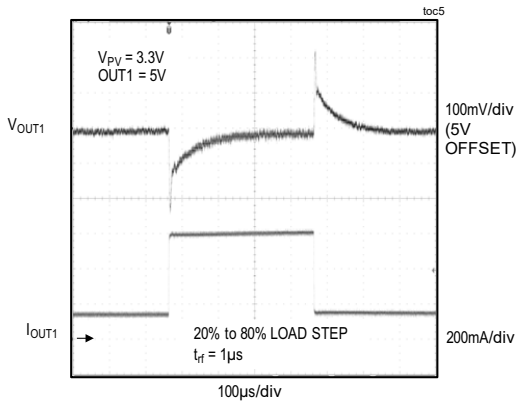
OUT2/3 EFFICIENCY



OUT2/3 LOAD REGULATION



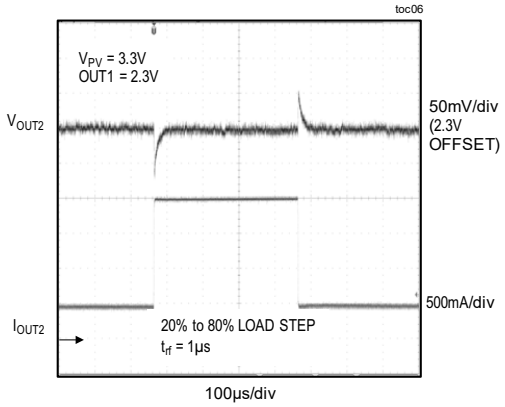
OUT1 LOAD TRANSIENT (PWM MODE)



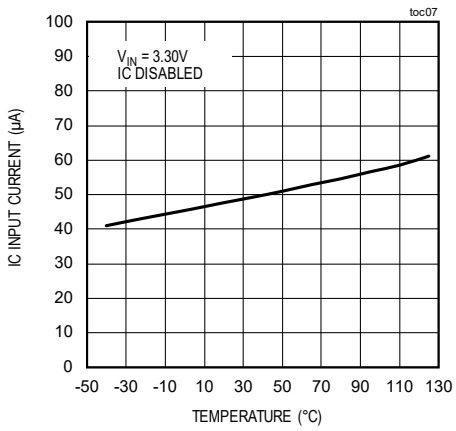
Typical Operating Characteristics (continued)

(T_A = +25°C under normal conditions, unless otherwise noted.)

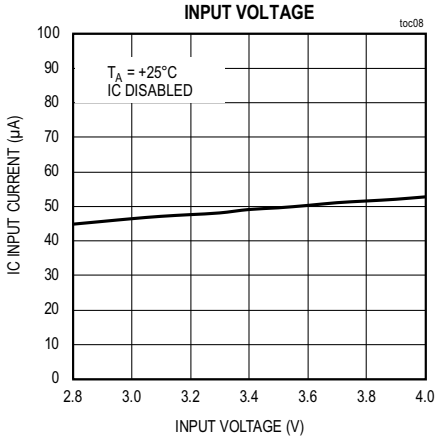
OUT2/3 LOAD TRANSIENT (PWM MODE)



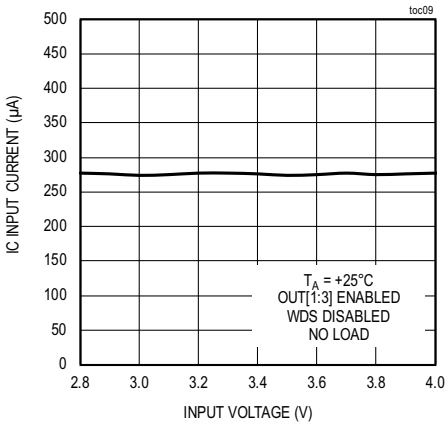
SHUTDOWN CURRENT vs. TEMP



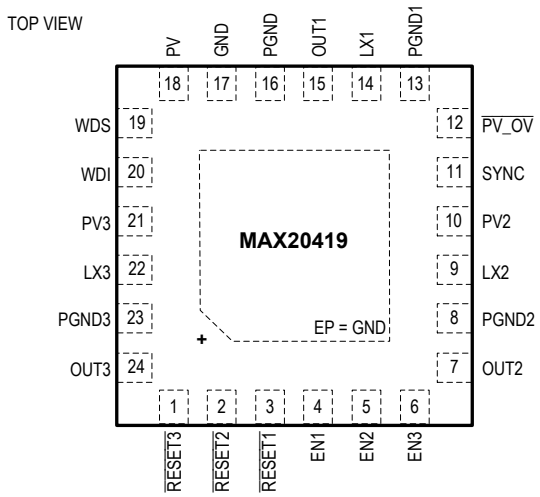
SHUTDOWN CURRENT vs. INPUT VOLTAGE



OPERATING CURRENT vs. INPUT VOLTAGE



Pin Configurations



TQFN
(4mm x 4mm)

Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{RESET3}}$	Open–Drain RESET Output for OUT3. To obtain a logic signal, pull up $\overline{\text{RESET3}}$ with an external resistor.
2	$\overline{\text{RESET2}}$	Open–Drain RESET Output for OUT2. To obtain a logic signal, pull up $\overline{\text{RESET2}}$ with an external resistor.
3	$\overline{\text{RESET1}}$	Open–Drain RESET Output for OUT1. To obtain a logic signal, pull up $\overline{\text{RESET1}}$ with an external resistor.
4	EN1	Active-High Enable Input for OUT1. Drive EN1 high for normal operation.
5	EN2	Active-High Enable Input for OUT2. Drive EN2 high for normal operation.
6	EN3	Active-High Enable Input for OUT3. Drive EN3 high for normal operation.
7	OUT2	OUT2 Voltage-Sense Input/Feedback Pin
8	PGND2	Power Ground for OUT2. Connect all PGND pins together.
9	LX2	Inductor Connection. Connect LX2 to the switched side of the inductor.
10	PV2	Power Input Supply for OUT2. Connect a 4.7µF ceramic capacitor from PV2 to PGND2.
11	SYNC	SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skip mode under light loads. Connect SYNC to PV or an external clock to enable fixed-frequency forced-PWM mode. When configured as an output (factory-configured), connect SYNC to other devices' SYNC inputs.
12	$\overline{\text{PV\_OV}}$	Open-Drain Power-Good Output. To obtain a logic signal, pull up $\overline{\text{PV\_OV}}$ with an external resistor.
13	PGND1	Power Ground. Connect all PGND pins together.
14	LX1	Inductor Connection. Connect LX1 to the switched side of the inductor.
15	OUT1	OUT1 Voltage Output
16	PGND	Power Ground. Connect all PGND pins together.
17	GND	Analog Ground. Connect to PGND pin.
18	PV	Analog Input Supply. Connect a 1µF ceramic capacitor from PV to GND with a 10Ω resistor in series to the supply voltage.

Pin Description (continued)

PIN	NAME	FUNCTION
19	WDS	Watchdog Time Set. Connect a capacitor to GND to set the watchdog timeout window.
20	WDI	Watchdog Refresh Input Pin
21	PV3	Power Input Supply for OUT3. Connect a 4.7µF ceramic capacitor from PV3 to PGND3.
22	LX3	Inductor Connection. Connect LX3 to the switched side of the inductor.
23	PGND3	Power Ground for OUT3. Connect all PGND pins together.
24	OUT3	OUT3 Voltage-Sense Input/Feedback Pin
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX20419 is a high-efficiency, 3-output, low-voltage DC-DC converter IC. OUT1 is a 750mA (typ) synchronous DC-DC boost converter that boosts the 3.0V to 5.5V input supply to a 5V output voltage. The boost converter has True Shutdown™ so the output voltage is 0V when off. The two synchronous step-down converters (OUT2, OUT3) operate from a 3.0V to 5.5V input voltage and provide a 0.8V to 3.80V output voltage at up to 3.6A. OUT2/OUT3 are factory set to a fixed voltage. The boost converter achieves ±1.9% and the buck converters achieve ±1.4% output error over load, line, and temperature ranges.

The IC features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency-modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. The spread modulation can be factory set to pseudorandom. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads, and make the layout a much simpler task with respect to discrete solutions.

The IC contains high-accuracy, factory-programmable overvoltage/undervoltage (OV/UV) thresholds for each output, which are mapped to the $\overline{RESET1}$–$\overline{RESET3}$ pins, along with fixed OV/UV monitoring of the input voltage mapped to the $\overline{PV\_OV}$ pin. There are diagnostics on the $\overline{RESET1}$–$\overline{RESET3}$ and OUT1–OUT3 pins to guarantee high reliability and fail-safe operation.

In light-load applications, a logic input (SYNC) allows the device to operate in either skip mode for reduced current consumption, or fixed-frequency, forced-PWM mode to eliminate frequency variation and help minimize EMI. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery.

Enable Inputs (EN1–EN3)

The enable control inputs (EN1–EN3) activate the IC channels from their low-power shutdown state. EN1–EN3 have an input threshold of 1.0V (typ) with hysteresis of 100mV (typ). EN1–EN3 are fully independent with no timing restrictions between one another. When an enable input goes high, the associated output voltage ramps up with the programmed soft-start time.

Reset Outputs ($\overline{RESET1}$–$\overline{RESET3}$)

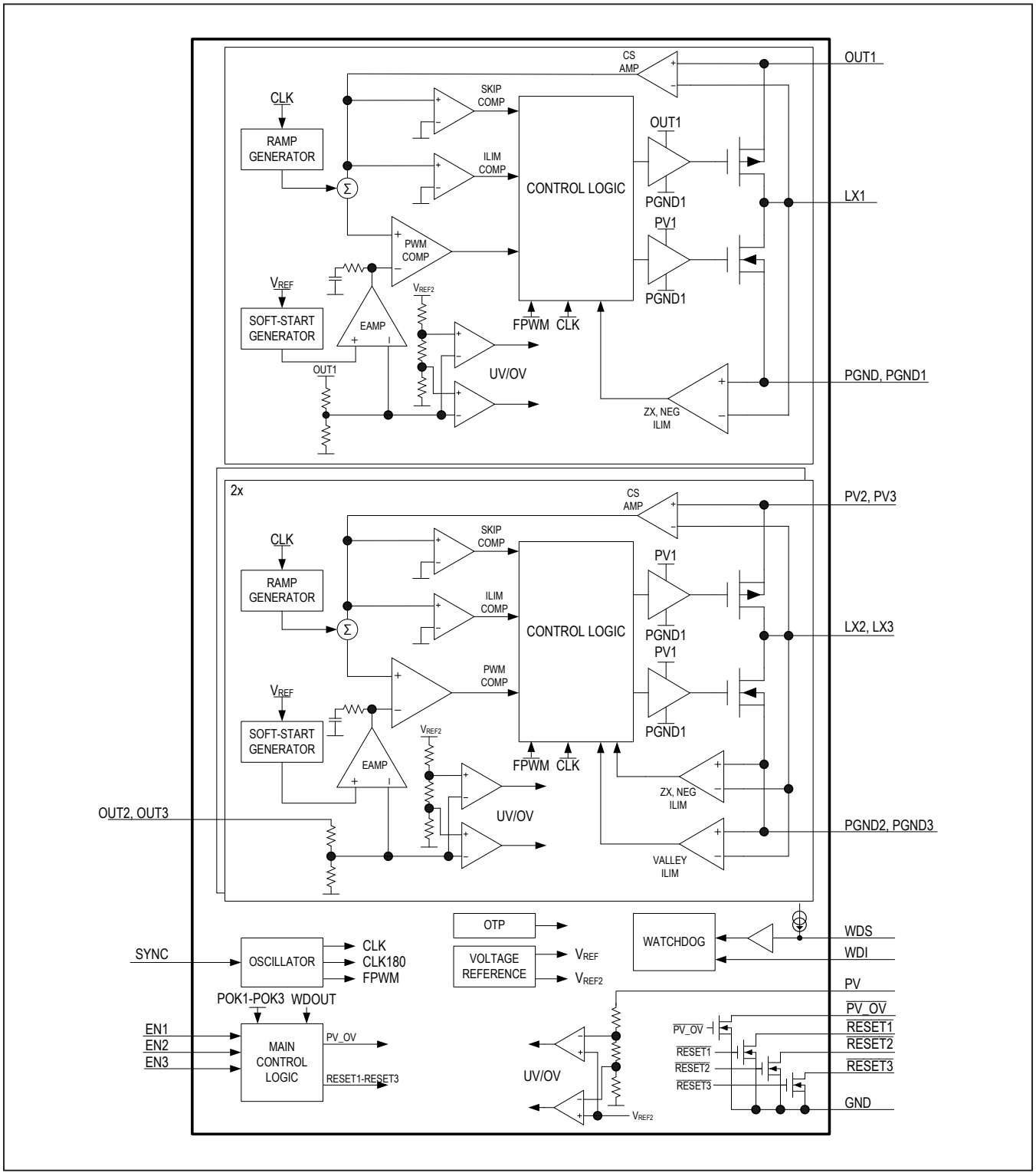
The IC features individual open-drain reset outputs for each output that asserts low when the corresponding output voltage is outside the OV/UV window. The OV/UV comparators run from a separate reference to provide drift detection on the outputs. If one of the reset outputs is shorted high, the associated output does not turn on to prevent startup without a valid reset signal. $\overline{RESET1}$–$\overline{RESET3}$ remain asserted for a fixed 7.4ms timeout period after the output rises up to its regulated voltage. To obtain a logic signal, place a resistor pullup between the $\overline{RESET1}$–$\overline{RESET3}$ pins to the system I/O voltage.

Feedback Pins (OUT1–OUT3)

The output voltage is fed back to the corresponding OUT_ feedback pin to close the regulation loop. If this connection is open, the output turns off to prevent open-loop operation that would normally result in the output being driven to the input supply voltage. Connect OUT_ directly to the output.

True Shutdown is a trademark of Maxim Integrated Products, Inc.

Internal Block Diagram



Internal Oscillator

The IC has a spread-spectrum oscillator that varies the internal operating frequency up by ±3%, relative to the internally generated 2.2MHz (typ) operating frequency. This function does not apply to the externally applied oscillation frequency. The spread frequency generated is pseudorandom, with a repeat rate well below the audio band.

Synchronization (SYNC)

SYNC is factory-programmable I/O (see the *Ordering Information/Selector Guide* for available options). When configured as an input, a logic-high on SYNC enables fixed-frequency, forced-PWM mode. Apply an external clock on the SYNC input to synchronize the internal oscillator to an external clock. The SYNC input accepts signal frequencies in the 1.8MHz < f_{SYNC} < 2.6MHz range. When the pin is open or logic-low, the SYNC input enables the device to enter a low-power skip mode under light-load conditions. When configured as an output, SYNC outputs the internally generated 2.2MHz clock that switches from PV to GND. All converters operate in forced-PWM mode when SYNC is configured as an output.

Watchdog

The IC features a programmable windowed watchdog that asserts all $\overline{\text{RESET\_}}$ lines for outputs on which the watchdog is activated, if the internal counter expires. The watchdog operates only if all the watchdog-activated output channels are enabled.

Table 1. Factory Settings for Watchdog

OTP OPTIONS	COMMENTS
WD5 0: 8 (default) 1: 16	**WRATIO** — Sets the ratio of lower-to-upper window: $t_{WD2} = t_{WD1}$ x (WRATIO + 1)
WD4 0: 16 (default) 1: 64	**WDCNT** — Sets the number of WDS counts per t_{WD1}: $t_{WD1} = t_{WDCLK}$ x WDCNT
WD3 0: 64 (default) 1: 128	**1STUPDATE** — Sets the number of extra counts added to the first t_{WD2} window after POR: $t_{1STWD2} = t_{WD1}$ x (WRATIO + 1STUPDATE)
WD2 0: Disabled 1: Enabled	**WDEN3** — Enables/disables the watchdog function on OUT3: When enabled, the watchdog operates when EN3 is high. An update violation results in $\overline{\text{RESET3}}$ being activated.
WD1 0: Disabled 1: Enabled	**WDEN2** — Enables/disables the watchdog function on OUT2: When enabled, the watchdog operates when EN2 is high. An update violation results in $\overline{\text{RESET2}}$ being activated.
WD0 0: Disabled 1: Enabled	**WDEN1** — Enables/disables the watchdog function on OUT1: When enabled, the watchdog operates when EN1 is high. An update violation results in $\overline{\text{RESET1}}$ being activated.

EXAMPLE	TIMING
CWDS = 68nF WRATIO = 0 1STUPDATE = 0 WDCNT = 0	t_{WD1} = 10.9ms t_{WD2} = 97.9ms t_{1STWD2} = 783.6ms
CWDS = 47nF WRATIO = 0 1STUPDATE = 0 WDCNT = 1	t_{WD1} = 30.1ms t_{WD2} = 270.8ms t_{1STWD2} = 2165ms

The WDS pin has a 125µA (typ) current source on the pin. When the WDS capacitor charges to 1.25V (typ), the pin discharges the capacitor and increments the internal counter. Connect a capacitor between WDS and GND to set the clock count rate (see Equation 1).

Equation 1:

$$t_{WDCLK} = C_{WDS} \times 1.25/(1.25 \times 10^{-4})$$

The first window (t_{WD1} counts) masks any signals on the WDI pin. Apply a logic pulse (low-high-low) to the WDI pin after the t_{WD1} window expires and before the second window (t_{WD2} counts after t_{WD1}) expires to reset the internal counter. On startup of the watchdog (typically after a POR event), the first mask window is eliminated and the first update window is extended (t_{1STWD2}) to allow for longer power-up routines to complete without requiring rigorous timing for the boot sequence. See Table 1 for possible factory settings.

Input Power-Good Output ($\overline{PV\_OV}$)

The IC features an open-drain $\overline{PV\_OV}$ output that asserts when the input supply voltage is more than 5% (max) above or below the target input voltage. The available target input voltages are 3.3V and 5.0V.

In order for the PV_OV detection to be active, at least one of the EN pins must be high. When the IC is in shutdown state, PV_OV will be pulled low.

Soft-Start

The IC includes a fixed 1.9ms soft-start for OUT1 and 2.5ms for OUT2/OUT3. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Current Limit/Short-Circuit Protection

The MAX20419 features current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

PWM and Skip Modes

The IC features a SYNC input that puts the converter either in skip mode or forced-PWM (FPWM) mode. See the *Pin Description* table for mode details. In PWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off, as often is the case in PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds 165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the DC-DC controllers, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Applications Information

Input Capacitors

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 4.7µF X7R ceramic capacitor is recommended for the PV2 and PV3 pins, as well as the supply side pin of the boost inductor. A 1.0µF X7R ceramic capacitor is recommended for the PV pin.

Boost Inductor Selection and Output Current

Proper choice of inductor for the boost converter is based on ripple current and slope compensation. Ripple current (I_{PK-PK}) is usually specified as a percentage of the average input current. 33% peak-to-peak ripple provides

a reasonable balance between inductor size, DCR, and core losses.

The peak boost input current limit is 1.6A (min), so the average current as a function of I_{PK-PK} is shown below.

Equation 2:

$$I_{IN} = 1.6/(1 + I_{PK-PK}/2)$$

For 33% ripple, this equates to 1.37A for I_{IN} and 0.45A ripple current (denoted as I_{Δ}, which has a unit of A, as opposed to I_{PK-PK}, which is a percentage). With the maximum average current I_{IN} known, the maximum output current for a given duty cycle (D) is shown in Equation 3.

Equation 3:

$$I_{OUT\_MAX} = (1-D) \times I_{IN}$$

where (see Equation 4).

Equation 4:

$$D = 1 - \eta \times V_{IN}/V_{OUT}$$

If η (efficiency) is not known, it must be measured, or estimated. A good efficiency estimate is 0.9 (90%) for V_{OUT}/V_{IN} ratios of 1.5 or less, and 0.8 for V_{OUT}/V_{IN} ratios near 2.5.

The approximate minimum inductance necessary to achieve a given ripple current (I_{Δ}) is shown below.

Equation 5:

$$L_{MIN1} = (V_{IN} \times D)/(f_{SW} \times I_{\Delta})$$

The second factor in inductor selection is slope compensation. The inductor current down-slope (m2) must be less than twice the internal slope compensation down-ramp (m1) to dampen oscillations in the inductor current waveform. Perfect deadbeat control occurs when the two downslopes are equal. The inductor current downslope is given by (Equation 6):

Equation 6:

$$m2 = (V_{OUT} - V_{IN})/L$$

The internal slope compensation ramp for the boost channel is set at 0.630 V/µs, and the R_{CS} for the boost channel is fixed at 0.330Ω. This provides a compensation ramp downslope of (Equation 7):

Equation 7:

$$m1 = 0.630/R_{CS}$$

Setting the inequality, adding in a margin factor of 1.3 for device and component variation, and rearranging for inductance gives the results shown below.

Equation 8:

$$L_{MIN2} \geq 1.3 \cdot R_{CS} \times (V_{OUT} - V_{IN})/(0.630 \times 2)$$

This gives the minimum inductance necessary to satisfy slope compensation (half-inductor downslope). The minimum inductance acceptable for use is the greater of the two calculated minimum values (see Equation 9).

Equation 9:

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

The maximum recommended inductance is twice the minimum value (see Equation 10).

Equation 10:

$$L_{MIN} < L_{NOM} < 2 \times L_{MIN}$$

Soft-saturation type inductors are recommended, as they maintain a measure of effective inductance even when driven past their saturation points during fault conditions. If a ferrite-based inductor is used, the saturation current must be higher than the maximum current limit to protect the part during continuous output short-circuit events.

Buck-Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20419: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output current capability of the output. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple-current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. The device is designed for ΔI_{P-P} equal to ~30% of the full load current. Follow Equation 11 to calculate the inductance.

Equation 11:

$$L_{MIN1} = \frac{\left(V_{IN} - V_{OUT\_}\right) \times V_{OUT\_}}{V_{IN} \times f_{SW} \times I_{MAX} \times 30\%}$$

V_{IN}:	The nominal input voltage, 3.3V or 5V (typ).
$V_{OUT\_}$:	The nominal output voltage.
I_{MAX}:	1A, 2A, or 3A depending on part number and channel. Use the maximum output capability of the output channel for the channel being used.
f_{SW}:	The operating frequency. This value is 2.2MHz unless externally synchronized to a different frequency.

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency is 2.2MHz. The maximum output capability is 1A, 2A, or 3A based on the specific part number of the device. The inductor saturation current is also important to avoid runaway current during continuous-output short circuits.

The next equation ensures that the inductor current downslope is less than twice the internal slope compensation. For this to be the case, the following equation needs to be satisfied.

Equation 12:

$$\frac{-m}{R_{CS}} \geq \frac{m2}{2}$$

m2:	The inductor current downslope. $\frac{V_{OUT}}{L} \times R_{CS}$
-m:	Slope Compensation: $\left[0.940 \frac{V}{\mu s}\right]$ for V_{OUT} > 3.2V fixed output. $\left[0.535 \frac{V}{\mu s}\right]$ for V_{OUT} ≤ 3.2V fixed-output or adjustable-output version.
R_{CS}:	0.378Ω for 1A channel. 0.263Ω for 2A channel. 0.176Ω for 3A channel.

Solving for L and adding a 1.3 multiplier to account for tolerances in the system (Equation 13).

Equation 13:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times -m} \times 1.3$$

To satisfy both L_{MIN1} and L_{MIN2}, L_{MIN} must be set to the larger of the two (Equation 14):

Equation 14:

$$L_{MIN} = \max (L_{MIN1}, L_{MIN2})$$

The maximum inductor value recommended is 2 times the chosen value from the above formula and is shown below.

Equation 15:

$$L_{MAX} = 2 \times L_{MIN}$$

Select a nominal inductor value based on the following formula (Equation 16). For optimal performance, select the first standard inductor value greater than L_{MIN}.

Equation 16:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

Boost Output Capacitor

The IC is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output-capacitor calculations in Equation 17 are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify proper stability is achieved.

Equation 17:

$$C_{OUT1\_MIN} = \frac{50 \times A \times \mu s}{V_{OUT}}$$

$$C_{OUT1\_NOM} = \frac{100 \times A \times \mu s}{V_{OUT}}$$

Buck Output Capacitors

The IC is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output-capacitor calculations in Equation 18 are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify that proper stability is achieved.

Equation 18:

$$C_{OUT23\_MIN} = 10.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT23\_NOM} = 27.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

C_{OUT23_MIN}:	The minimum fully derated output capacitance needed for a stable output.
C_{OUT23_NOM}:	The nominal output capacitance.
I_{MAX}:	The maximum DC current capability. Either 1A, 2A, or 3A. depending on the part number (see the *Ordering Information/ Selector Guide*).
V_{OUT}:	Nominal output voltage.

With C_{OUT23_MIN} defining the minimum fully derated output capacitance required for a stable output, and C_{OUT23_NOM} defining the nominal output capacitance for maximum phase margin. I_{MAX} is the maximum DC current capability of the associated output, as defined in the *Ordering Information/Selector Guide*. V_{OUT} is the output voltage for the associated channel.

PCB Layout Guidelines

For each converter, place the capacitor with the highest current ripple closest to the IC. For a buck converter, this is the input capacitor; for the boost converter, it is the output capacitor. Route the LX trace out from the IC underneath that capacitor (use a larger-package capacitor, such as 3.2mm x 1.6mm). Lastly, place the other capacitors close by with their ground pins very close to both the IC's ground pins and the other capacitor's ground pins. This configuration results in a closely routed DC-DC converter that helps maintain performance and reduces EMI.

The layer directly below the IC and power components should be a continuous ground plane. Use multiple vias to provide good connections between that plane and component ground pins/pads. Split grounding should not be used.

The exposed pad (EP) of the IC is attached to the die with epoxy, thus providing the means to dissipate thermal energy from the die. Connect the EP to all available ground planes below it using a grid of small vias in the EP land (3 x 3 grid of 0.3mm diameter vias is recommended).

Ordering Information/Selector Guide

PART	$\overline{PV\_OV}$ (V)	V_{OUT1} (V)	UV1/OV1 (%)	V_{OUT2} (V)	I_{OUT2} (A)	UV2/OV2 (%)	V_{OUT3} (V)	I_{OUT3} (A)	UV3/OV3 (%)	WD[5:0]	t_{HOLD} (ms)	SS
MAX20419ATGB/V+	3.3*	5.0	96.3/103.7	2.3	2	96.3/103.7	1.25	2	97.1/103.5	0x0C	7.4	Off
MAX20419ATGC/V+	3.3*	5.0	96.3/103.7	1.83	2	96.3/103.7	1.23	2	96.3/103.7	0x3C	7.4	On
MAX20419ATGD/V+	3.3*	5.0	96.3/103.7	1.8	2	96.3/103.7	1.25	2	96.3/103.7	0x0F	7.4	Off
MAX20419ATGE/V+	3.3*	5.0	96.3/103.7	1.1	1	96.3/103.7	1.8	1	96.3/103.7	0x0C	7.4	On
MAX20419ATGF/V+**	3.3*	5.0	96.3/103.7	2.3	2	96.3/103.7	1.25	3	96.3/103.7	0x0C	7.4	On
MAX20419ATGG/V+	3.3*	5.0	96.3/103.7	1.0	2	96.3/103.7	1.25	2	96.3/103.7	0x0C	7.4	On
MAX20419ATGH/V+	3.3*	5.0	96.3/103.7	1.1	1	96.3/103.7	1.8	1	96.3/103.7	0x09	7.4	On
MAX20419ATGI/V+**	3.3*	5.0	96.3/103.7	1.8	2	96.3/103.7	1.2	3	96.3/103.7	0x0C	7.4	Off

**3.3V, 5.0V, or disabled.*
For variants with different options, contact factory.
/V denotes an automotive-qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
*** Future product—contact factory for availability*

Chip Information

BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—
0.1		Added future product status to MAX20419ATGC/V, MAX20419ATGD/V, MAX20419ATGE/V	17
1	5/18	Updated *Absolute Maximum Ratings* and *Ordering Information/Selector Guide* table	2, 16
1.1		Added future product status to MAX20419ATGC/V, MAX20419ATGD/V, MAX20419ATGE/V	16
2	6/18	Removed future product status from MAX20419ATGC/V and MAX20419ATGE/V	16
2.1		Added future product status to MAX20419ATGE/V	16
3	7/18	Removed future product status from MAX20419ATGD/V+	16
4	10/18	Removed future product status from MAX20419ATGE/V+	16
5	2/19	Updated factory settings for watchdog table, added future part MAX20419ATGF/V+**	11, 16
6	6/19	Updated Benefits and Features, Electrical Characteristics, and *Ordering Information* (added future parts MAX20419ATGH/V+** and MAX20419ATGI/V+**)	1, 2–5, 16
7	8/19	Updated *Detailed Description*	12, 14
8	3/20	Updated *Ordering Information* to add MAX20419ATGG/V+	16
9	4/20	Updated *Ordering Information* to remove future-product notation from MAX20419ATGH/V+	16

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at **https://www.maximintegrated.com/en/storefront/storefront.html**.

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