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Automotive 4-Channel, 130mA Backlight Driver with Boost/SEPIC Controller and I²C Interface

MAX20444C

General Description

The MAX20444C is a 4-channel backlight driver IC with boost controller for automotive displays. The integrated current outputs can sink up to 130mA LED current each. The device accepts a wide 4.5V to 36V input voltage range and withstands direct automotive load-dump events.

The internal current-mode switching DC-DC controller supports boost or SEPIC topologies and operates in the 400kHz to 2.2MHz frequency range. Integrated spread spectrum helps reduce EMI. An adaptive output-voltage-control scheme minimizes power dissipation in the LED current-sink paths.

The device features I²C-controlled pulse-width-modulation (PWM) dimming and hybrid dimming. In either case, the minimum pulse width is 500ns. Phase-shifted dimming of the strings is incorporated for lower EMI.

Comprehensive diagnostic information is also available through the I²C interface, while stand-alone operation is also supported.

The MAX20444C is available in a 24-pin TQFN or 24-pin side-wettable TQFN (SWTQFN) package and operates over the -40°C to +125°C temperature range.

Applications

- Infotainment Displays
- Central Information Displays
- Instrument Clusters

Benefits and Features

- Wide Voltage-Range Operation
  - Operates Down to 4V Supply After Startup
  - Survives Load Dumps Up to 52V
- High Integration
  - Complete 4-Channel Solution Including Boost Controller
  - I²C Control for Minimum Parts Count
- Robust and Low EMI
  - Spread-Spectrum Oscillator
  - Phase Shifting
  - 400kHz to 2.2MHz Switching-Frequency Range
  - Fail-Safe Operation Mode Using the FSEN Pin
- Versatile Dimming Scheme Allows Hybrid or PWM-Only Dimming Using DIM Input or I²C
  - Dimming Ratio > 10,000:1 Using Hybrid Dimming
  - 10,000:1 Dimming Ratio at 200Hz Using PWM Dimming
- Complete Diagnostics
  - LED Open/Short Detection and Protection
  - Boost Output Undervoltage and Overvoltage
  - Boost-Voltage Measurement
  - LED-Current Measurement
  - Thermal Shutdown
- Compact (4mm x 4mm) 24-Pin TQFN and SWTQFN Packages

***Ordering Information** appears at end of data sheet.*

19-101244; Rev 0; 9/21

One Analog Way, Wilmington, MA 01887 U.S.A. | Tel: 781.329.4700 |

Absolute Maximum Ratings

IN, EN, OUT_, BSTMON, PGATE to GND .....-0.3V to +52V
PGND, LEDGND to GND.....-0.3V to +0.3V
V_{CC} to GND .....-0.3V to +6V (min) of (V_{IN} + 0.3V)
FLTB, SCL/IRANGE, I2CDIS/RSDT,
SDA/PSEN, DIM to GND.....-0.3V to +6V
FSEN/ISET, CS, RT, COMP,
NDRV, IREF to GND .....-0.3V to V_{CC} + 0.3V
HDSET to GND .....-0.3V to V_{CC} + 0.3V
NDRV Peak Current (< 100ns) ..... -5A to +5A
NDRV Continuous Current ..... -100mA to +100mA
OUT_ Continuous Current..... -150mA to +150mA
Continuous Power Dissipation
Multilayer Board (T_A = +70°C) 2.857W
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Package Thermal Resistance (θ_{JC}) .....3°C/W
Operating Temperature ..... -40°C to +125°C
Junction Temperature..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range.....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN/SWTQFN

	TQFN	SWTQFN
Package Code	T2444+4C	T2444Y+4C
Outline Number	21-0139	21-100290
Land Pattern Number	90-0022	90-0022
Thermal Resistance, Four-Layer Board:		
Junction to Ambient (θ_{JA})	36°C/W	41.27°C/W
Junction to Case (θ_{JC})	3°C/W	3.44°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 2.2µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT						
Input Voltage Range			4.5		36	V
Input Voltage Range After Startup			4.2		36	V
Input Voltage Range		IN pin connected to V_{CC}	4.5		5.5	V
Quiescent Supply Current		V_{DIM} = 5V; V_{BSTMON} = 1.3V, OUT1–OUT4 are unconnected		7.5	11	mA
Standby Supply Current		V_{IN} = 12V, V_{EN} = 0V		0.1	1	µA
Undervoltage Lockout, Rising			3.8	4.15	4.45	V
Undervoltage Lockout, Falling			3.1	3.7	4	V
Startup Delay		From EN high to I²C ready			2	ms
V_{CC} REGULATOR						
V_{CC} Output Voltage		5.75V < V_{IN} < 36V, I_{VCC} = 1mA to 10mA	4.75	5	5.25	V
Dropout Voltage		V_{IN} = 4.5V, I_{VCC} = 5mA			0.2	V
Short-Circuit Current Limit		V_{CC} shorted to GND		60		mA
V_{CC} Undervoltage-Lockout Threshold, Rising			4.05	4.2	4.35	V
V_{CC} Undervoltage-Lockout Threshold, Falling			3.75	3.9	4.04	V
RT OSCILLATOR						
Switching-Frequency Range	f_{SW}	Frequency dithering disabled	400		2200	kHz
Maximum Duty Cycle		f_{SW} = 400kHz	90	94.5	98.5	%
		f_{SW} = 2200kHz	86	90.5	95	
Oscillator-Frequency Accuracy		f_{SW} = 400kHz to 2200kHz, frequency dither disabled	-10		+10	%
Frequency Dither	SS	SSL bit = 1		±3		%
RT Output Voltage	V_{RT}	R_{RT} = 76.8kΩ or R_{RT} = 13.3kΩ	1.22	1.25	1.28	V
Sync Rising Threshold			3			V
Sync-Frequency Duty-Cycle Range				50		%
Sync-Frequency Range			1.2 x f_{SW}		1.5 x f_{SW}	kHz

Electrical Characteristics (continued)

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 2.2µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MOSFET DRIVER							
NDRV On-Resistance, High Side		I_{SINK} = 30mA			1.5	3	Ω
NDRV On-Resistance, Low Side		I_{SOURCE} = 30mA			0.8	1.6	Ω
NDRV Rise Time		C_{LOAD} = 1nF			8		ns
NDRV Fall Time		C_{LOAD} = 1nF			8		ns
SLOPE COMPENSATION							
Peak Slope-Compensation Current-Ramp Magnitude		Current ramp added to CS		42	50	58	µA
CURRENT-SENSE COMPARATOR							
Current-Limit Threshold	V_{CL_MAX}	Includes internal slope-ramp magnitude, V_{CL} = V_{CS} + slope-compensation voltage		390	420	450	mV
ERROR AMPLIFIER							
OUT_ Regulation, High Threshold		$V_{OUT\_}$ falling		0.95	1.03	1.1	V
OUT_ Regulation, Low Threshold		$V_{OUT\_}$ rising		0.7	0.78	0.85	V
Transconductance				420	600	840	µS
COMP Sink Current		V_{COMP} = 2V		200	480	800	µA
COMP Source Current		V_{COMP} = 1V		200	480	800	µA
LED CURRENT SINKS							
IREF Voltage	V_{IREF}	R_{IREF} = 49.9kΩ		1.22	1.25	1.28	V
OUT_ Output Current		R_{IREF} = 49.9kΩ	120mA setting	115	120	125	mA
		R_{IREF} = 49.9kΩ	100mA setting	96	100	104	
		R_{IREF} = 49.9kΩ	50mA setting	48	50	52	
		R_{IREF} = 45.3kΩ	130mA setting	126	132	138	
Channel-to-Channel Matching		$I_{OUT\_}$ = 120mA		-2		+2	%
		$I_{OUT\_}$ = 50mA		-2.5		+2.5	
Total OUT_ Leakage Current to IN	$I_{OUTLEAK}$	$V_{OUT\_}$ = 48V, V_{DIM} = 0V, all OUT_ are shorted together			8	15	µA
OUT_ Current, Rise Time		10% to 90% $I_{OUT\_}$			150		ns
OUT_ Current, Fall Time		90% to 10% $I_{OUT\_}$			50		ns
DIM Sampling Frequency					20		MHz

Electrical Characteristics (continued)

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 2.2µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUT AND OUTPUTS						
EN, SDA/PSEN, SCL/IRANGE, DIM Input, Logic-High			2.1			V
EN, SDA/PSEN, SCL/IRANGE, DIM Input, Logic-Low					0.8	V
EN Input Current		V_{EN} = 5V		3	5	µA
SDA/PSEN, SCL/IRANGE Input Current		$V_{SDA/PSEN}$ = $V_{SCL/IRANGE}$ = 5V	-1		+1	µA
HDSET Input Current		R_{IREF} = 49.9kΩ	14.75	15	16.25	µA
DIM Frequency Range			90			Hz
DIM Input Pullup Current				5		µA
FSEN/ISET Input, Logic High		FSEN/ISET rising	2.2			V
FSEN/ISET Input Current	I_{FSEN}	$V_{FSEN/ISET}$ = 1V	14.5	15	16	µA
I2CDIS/RSDT Disable LED-Short Threshold	V_{RSDTH}	$V_{I2CDIS/RSDT}$ rising	2.3	2.5	2.7	V
I2CDIS/RSDT I²C Enable Threshold	V_{RSDTLO}	$V_{I2CDIS/RSDT}$ falling	0.2	0.3	0.4	V
SDA/PSEN, FLTB Output Low Voltage		Sinking 3mA			0.4	V
FLTB Output-Leakage Current		V_{FLTB} = 5.5V	-1		+1	µA
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
BSTMON Overvoltage-Trip Threshold		V_{BSTMON} rising	1.18	1.23	1.28	V
BSTMON Hysteresis				70		mV
BSTMON Input Bias Current		0V < V_{BSTMON} < 1.3V	-500		+500	nA
BSTMON Undervoltage-Detection Threshold		BSTMON falling, PGATE latched off	0.4	0.43	0.46	V
Boost Undervoltage-Blanking Time		After ENA is written to '1' or EN pin is taken high in stand-alone mode	47.8	52	56.2	ms
BSTMON Undervoltage-Detection Delay		BSTMON falling	4	10	18	µs
PGATE Pulldown Current			170	200	230	µA
PGATE Start Delay		Delay between PGATE going low and the boost converter starting		2	2.2	ms
PGATE Leakage Current		V_{PGATE} = 12V, V_{EN} = 0V		0.1	1	µA

Electrical Characteristics (continued)

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 2.2µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED FAULT DETECTION						
LED Short-Detection Threshold		SLDET[1:0] = 11 or $V_{I2CDIS/RSDT}$ = 2V	7.5	8	8.5	V
		SLDET[1:0] = 10	5.6	6	6.4	
		SLDET[1:0] = 01	2.8	3	3.25	
Short-Detection Comparator Delay				9		µs
OUT_ Check LED Source Current			50	60	70	µA
OUT_ Short to GND Detection Threshold		Before boost converter startup	250	300	365	mV
OUT_ Unused-Detection Threshold			1.15	1.25	1.35	V
OUT_ Open-LED Detection Threshold		During operation	250	300	365	mV
ANALOG-TO-DIGITAL CONVERTER						
ADC Measurement Resolution				8		Bits
Total Measurement Error, Current		$I_{OUT\_}$ = 120mA	-12		+6	mA
Total Measurement Error, Voltage		V_{BSTMON} = 1V	-60		80	mV
ADC Gain Error		$I_{OUT\_}$ = 120mA	-5.5		+4.5	%
ADC Offset Error		$I_{OUT\_}$ = 120mA			±4	LSB
Measurement Resolution, Current		R_{IREF} = 49.9kΩ		0.5		mA
		R_{IREF} = 45.3kΩ		0.55		
Measurement Resolution, Voltage				5.1		mV
THERMAL SHUTDOWN						
Thermal Warning				125		°C
Thermal-Shutdown Threshold				165		°C
Thermal-Shutdown Hysteresis				15		°C

Electrical Characteristics (continued)

(V_{IN} = 12V, R_{RT} = 76.8kΩ, C_{VCC} = 2.2µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

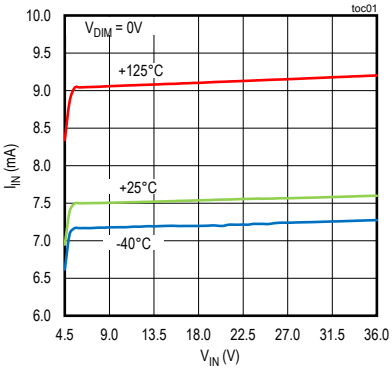
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C INTERFACE						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	Measured from 50% point on SCL falling edge to SDA edge	0			µs
Pulse Width of Spike Suppressed	t_{SP}			50		ns

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

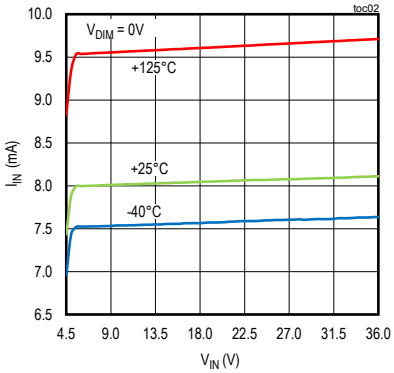
Typical Operating Characteristics

(V_{IN} = V_{EN} = +12V, 4x6 LED load at 100mA, T_A = +25°C, unless otherwise noted.)

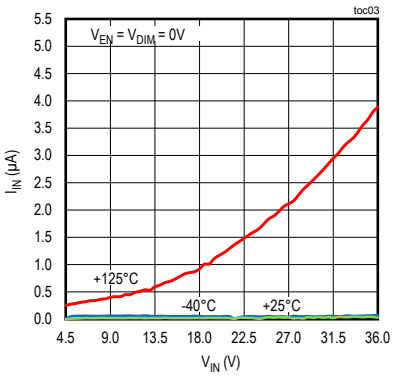
SUPPLY CURRENT vs. SUPPLY VOLTAGE (400kHz SWITCHING FREQUENCY)



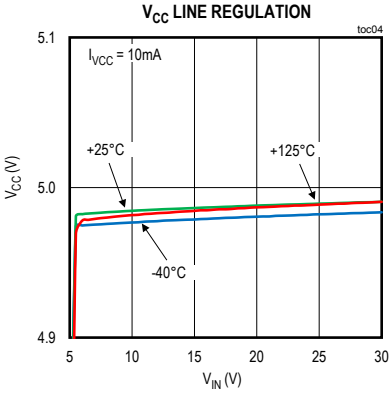
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2.2MHz SWITCHING FREQUENCY)



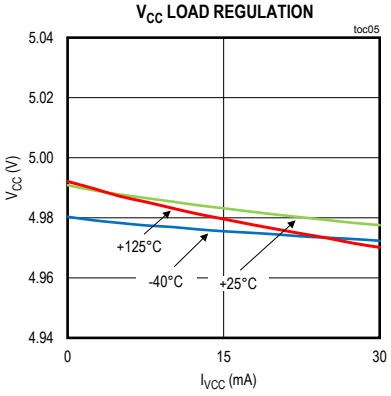
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



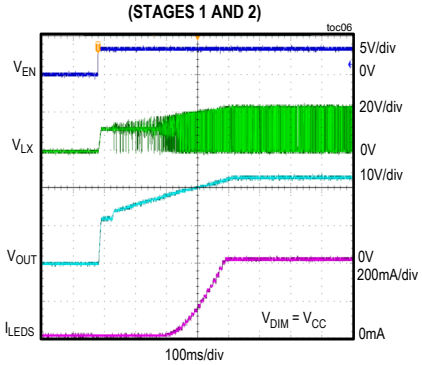
V_{CC} LINE REGULATION



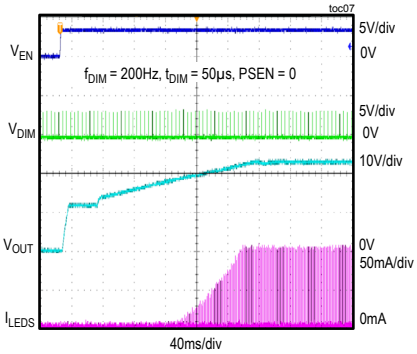
V_{CC} LOAD REGULATION



STARTUP WAVEFORM (STAGES 1 AND 2)



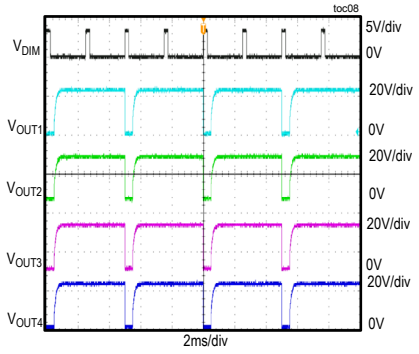
STARTUP WAVEFORM (STAGES 1 AND 2)



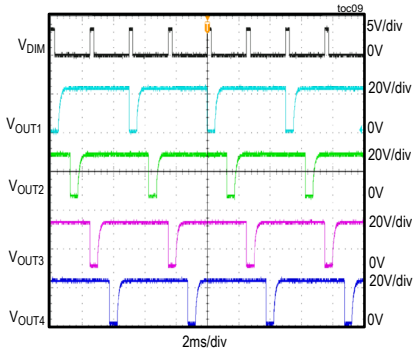
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = +12V, 4x6 LED load at 100mA, T_A = +25°C, unless otherwise noted.)

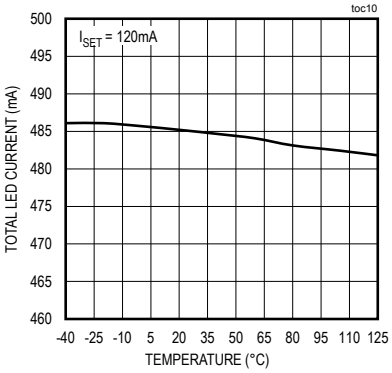
DIMMING WAVEFORM (PSEN = 0)
f_{DIM} = 200Hz, t_{DIM} = 0.5ms



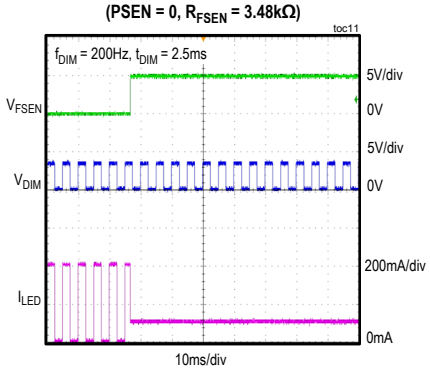
DIMMING WAVEFORM (PSEN = 1)
f_{DIM} = 200Hz, t_{DIM} = 0.5ms



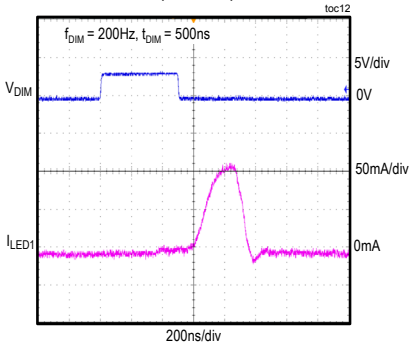
TOTAL LED CURRENT vs. TEMPERATURE
(400kHz SWITCHING FREQUENCY)



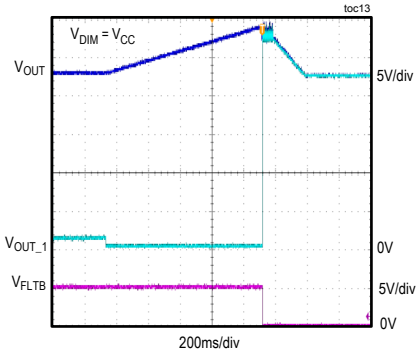
NORMAL OPERATION TO FSEN HIGH
(PSEN = 0, R_{FSEN} = 3.48kΩ)



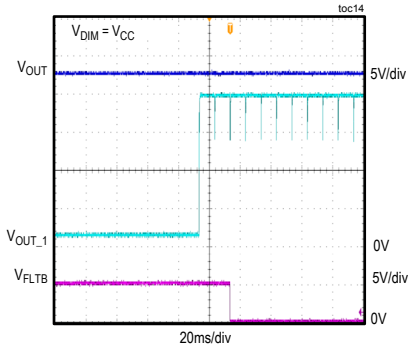
LED CURRENT WITH DIMMING t_{ON} = 500ns
(PSEN = 1)



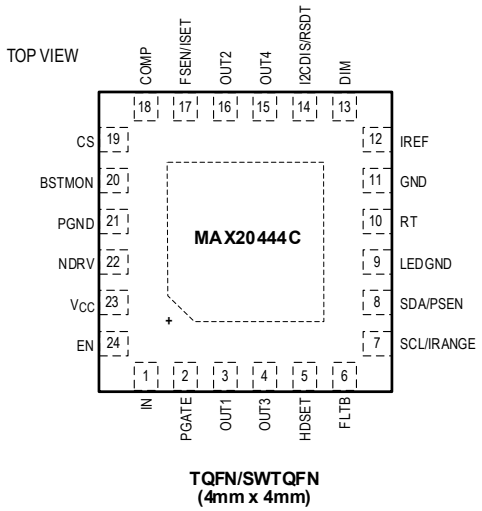
LED OPEN FAULT ON OUT_1



LED SHORT FAULT ON OUT_1



Pin Configuration



TQFN/SWTQFN (4mm x 4mm)

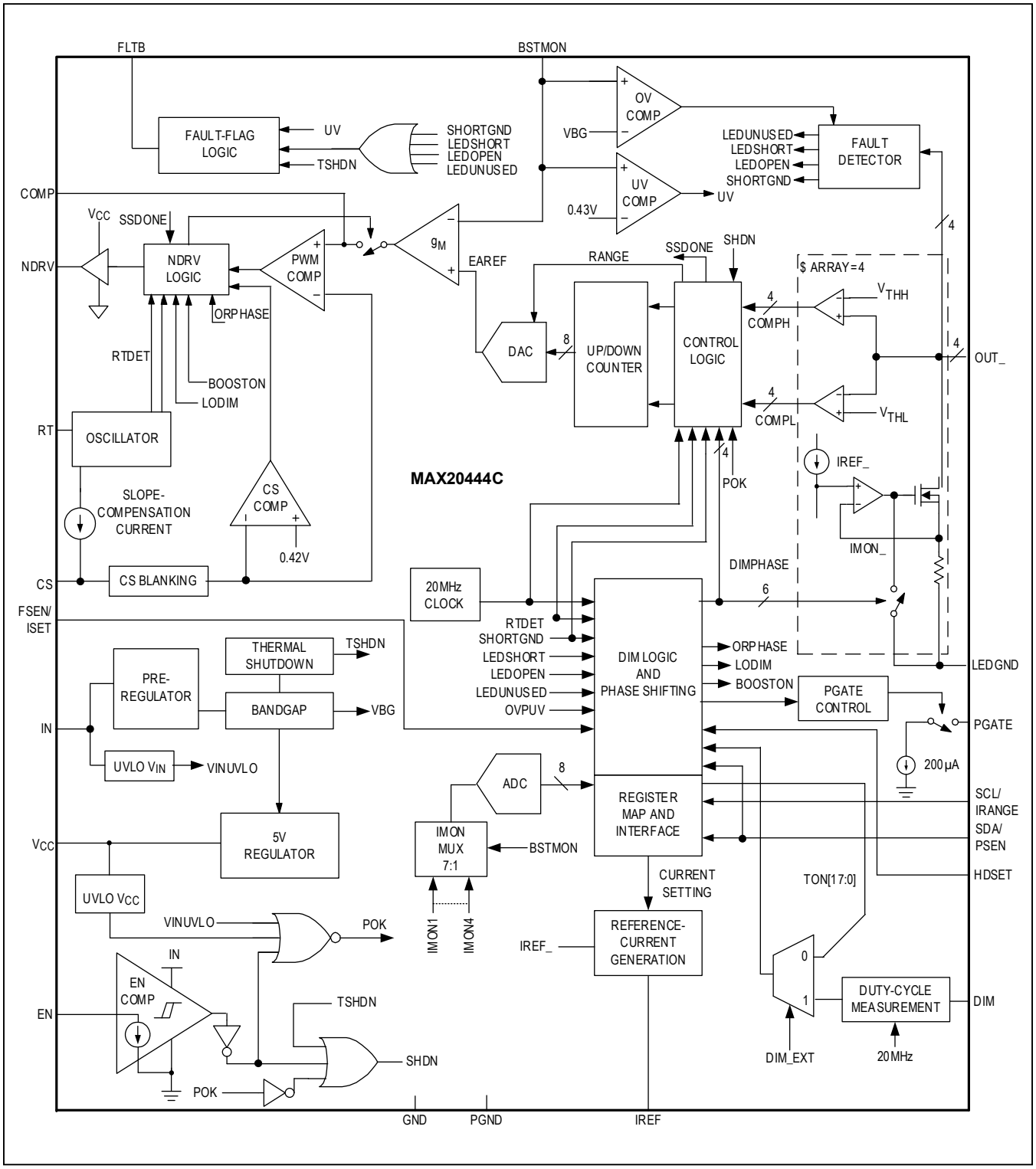
Pin Description

PIN	NAME	FUNCTION
1	IN	Bias Supply Input. Connect a 4.5V to 36V supply to IN. Bypass IN to GND with a 2.2µF ceramic capacitor.
2	PGATE	Gate Connection for External Series pMOSFET
3	OUT1	LED String Cathode Connection 1. OUT1 is the open-drain output of the linear current sink, which controls the current through the LED string connected to OUT1. OUT1 sinks up to 132mA.
4	OUT3	LED String Cathode Connection 3. OUT3 is the open-drain output of the linear current sink, which controls the current through the LED string connected to OUT3. OUT3 sinks up to 132mA.
5	HDSET	Hybrid Dimming-Setting Pin. Connect a resistor from HDSET to ground to set the crossover point from analog to PWM dimming. The crossover point is defined as a percentage of the current set by the resistor on the FSEN/ISET pin, and the voltage on the SCL/IRANGE pin. The crossover point options are: 6.25%, 12.5%, 25%, and 50%. Connect HDSET to V_{CC} to disable hybrid dimming. When using the I²C interface, connect HDSET to GND.
6	FLTB	Open-Drain Fault Output. FLTB asserts low when any diagnostic bit that is not masked is asserted. See the *Fault Protection* section for more details. Connect a pullup resistor from FLTB to V_{CC} or to a logic supply of 5V (max).
7	SCL/IRANGE	In I²C mode, this is the I²C clock input. Connect a pullup resistor from SCL to the logic supply. In stand-alone mode, this is the current-range input. Connect to GND to set the lower current range (45mA to 80mA). Connect to V_{CC} to select the higher current range (85mA to 120mA). Use the ISET pin to set the exact LED current. The state of the IRANGE pin is read once at power-up, and the current cannot be changed subsequently.
8	SDA/PSEN	In I²C mode, this is the I²C data I/O pin. Connect a pullup resistor from SDA to the logic supply. In stand-alone mode, PSEN enables or disables phase shifting between the LED strings; when high, phase shifting is enabled. The state of this pin is read and latched at startup.
9	LEDGND	LED Ground. LEDGND is the return-path connection for the linear current sinks. Connect GND, LEDGND, and PGND at a single point.

Pin Description (continued)

PIN	NAME	FUNCTION
10	RT	Oscillator-Timing Resistor Connection. Connect a timing resistor (R_{RT}) from RT to GND to program the switching frequency. Also connect a 100pF capacitor from RT to GND. To synchronize the switching frequency with an external clock, apply an AC-coupled external clock at RT. When the oscillator is synchronized with the external clock, spread spectrum is disabled.
11	GND	Signal Ground. GND is the current return-path connection for the low-noise analog signals. Connect GND, LEDGND, and PGND at a single point.
12	IREF	LED Current-Reference Input. Connect a resistor (R_{IREF} = 49.9kΩ or 45.3kΩ) from IREF to GND to set the reference current.
13	DIM	PWM Dimming Input. Apply a PWM signal to DIM for LED dimming control unless I²C dimming is used. Connect DIM to V_{CC} if dimming control is not used (100% brightness). Connect DIM to GND if dimming will be controlled through I²C.
14	I2CDIS/RSDT	I²C Disable and LED Short-Detection Threshold-Adjust Input. Connect to GND to enable I²C communication. When not using I²C, connect a resistive divider from V_{CC} to I2CDIS/RSDT and GND (setting a voltage higher than 1.3V on RSDT) to program the LED short-detection threshold. Connect I2CDIS/RSDT directly to V_{CC} to disable LED short detection.
15	OUT4	LED String Cathode Connection 4. OUT4 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT4. OUT4 sinks up to 132mA.
16	OUT2	LED String Cathode Connection 2. OUT2 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT2. OUT2 sinks up to 132mA.
17	FSEN/ISET	In I²C Mode, this is the Fail-Safe Enable Pin. When FSEN/ISET is taken high, the boost converter is enabled and the outputs (OUT1–OUT4) enabled at 100% duty cycle, independently of all register settings. Connect a resistor from FSEN/ISET to GND to set the LED current; FSEN/ISET sets both the LED current (when the pin is active or high) and the device's I²C address (see the *FSEN/ISET Pin Function* section). If the fail-safe function is not needed, connect the pin directly to GND. In stand-alone mode, this pin is the LED Current-Adjust Input. Connect a resistor (R_{ISET}) from ISET to GND to set the current through each LED string. The state of the FSEN/ISET pin is read once at power-up and the current cannot be changed subsequently. See the *Stand-Alone Mode* section for further details.
18	COMP	Switching-Converter Compensation Input. Connect the compensation network from COMP to GND for current-mode control (see the *Feedback Compensation* section).
19	CS	Current-Sense Input for the Switching Regulator. A sense resistor connected from the source of the external power MOSFET to PGND sets the switching current limit. A resistor connected between the source of the power MOSFET and CS sets the slope-compensation ramp rate (see the *Slope Compensation and Current-Sense Resistor* section).
20	BSTMON	Overvoltage Threshold-Adjust Input. Connect a resistor-divider from the switching converter output to BSTMON and GND. The OVP comparator reference is internally set to 1.23V.
21	PGND	Power Ground. PGND is the switching current-return-path connection. Connect GND, LEDGND, and PGND at a single point.
22	NDRV	Switching nMOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching-power nMOSFET using a small 10Ω to 22Ω resistor. This decreases the slew rate of the gate driver and reduces switching noise.
23	VCC	5V Regulator Output. Bypass V_{CC} to GND with a 1µF (min) ceramic capacitor as close as possible to the device.
24	EN	Enable Input. Connect EN to ground to shut down the device. Connect EN to logic-high or IN for normal operation. EN has an internal clamp at 3.9V; when EN is above this voltage, an input current of (V_{EN} - 3.9V)/1.2MΩ will flow.
—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP must be connected to GND.

Functional Diagrams



Detailed Description

The MAX20444C high-efficiency, high-brightness LED driver IC integrates all the necessary features to implement a high-performance backlight driver to power LEDs in medium-to-large-sized displays for automotive as well as general applications. The IC provides load-dump voltage protection up to 52V in automotive applications and incorporates three major blocks: 1) DC-DC controller with peak current-mode control to implement a boost or SEPIC-type switched-mode power supply, 2) 4-channel LED driver with 45mA to 132mA constant-current sink capability per channel, and 3) control block with I²C interface. Operation is also possible in stand-alone mode without using the I²C interface.

Enable

The internal regulator is enabled when the EN pin is high, and an I²C interface is enabled if the I2CDIS/RSDT pin is low. To shut down the device, drive EN low and the current consumption is reduced to 1µA (max). In stand-alone mode, the boost converter and current sinks are enabled when EN goes high.

Undervoltage Lockout

The IC features two undervoltage lockouts (UVLOs) that monitor the input voltage at IN and the output of the internal LDO regulator at V_{CC}. The device turns on when EN is taken high if both IN and V_{CC} are higher than their respective UVLO thresholds.

Current-Mode DC-DC Controller

The IC has a constant-frequency, current-mode controller designed to drive the LEDs in a boost, SEPIC, or coupled-inductor buck-boost configuration. To minimize power dissipation, the IC features multi-loop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks.

The switching frequency can be programmed over the 400kHz to 2.2MHz range using a resistor connected from RT to GND.

Adjustable slope compensation is provided to compensate for subharmonic oscillations that occur at above 50% duty cycles in continuous-conduction mode.

The external MOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until it is turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor (R_{CS}) connected from the source of the external MOSFET to ground, with the addition of the slope-compensation voltage due to R_{SC}.

The IC features leading-edge blanking to suppress the MOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the MOSFET when the voltage at CS exceeds the error amplifier's output voltage, which is also the voltage on the COMP pin. This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the IC has two other feedback loops for control. The converter output voltage is sensed through the BSTMON input, which goes to the inverting input of the error amplifier; the other feedback comes from the OUT_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation, while still ensuring accurate LED current matching. Each current sink has a window comparator with a low threshold of 0.78V and a high threshold of 1.03V. The outputs of these comparators control an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives an 8-bit DAC that sets the reference to the error amplifier. When dimming is set to 100%, the counter is updated at intervals of 10ms.

Output Undervoltage Protection

At the end of the boost converter soft-start, an undervoltage threshold is activated on the output of the DC-DC converter, which is set at 430mV. If the BSTMON pin is below 430mV after the soft-start period of the DC-DC converter, the converter is turned off and the PGATE output is switched to high impedance (thus turning off the optional external pMOSFET). The FLTB pin is asserted low whenever undervoltage protection is activated. The ENA bit in the ISET (0x02) register must be toggled to start up again once the fault condition has been removed. Alternatively, the EN pin or power supply can be toggled.

8-Bit Digital-to-Analog Converter

The error amplifier's reference input is controlled with an 8-bit digital-to-analog converter (DAC). The DAC output is ramped up slowly during startup to implement a soft-start function (see the *Startup Sequence* section). During normal operation, the DAC output range is limited to 0.6V to 1.25V. Because the DAC output is limited to no less than 0.6V during normal operation, the overvoltage threshold for the output should be set to a value less than twice the minimum LED forward voltage. The DAC LSB determines the minimum step-in output voltage according to the equation below.

Equation 1:

$$V_{STEP\_MIN} = V_{DAC\_LSB} \times A_{OVP}$$

where:

V_{STEP_MIN} = Minimum output-voltage step

V_{DAC_LSB} = DAC least significant bit size (2.5mV)

A_{OVP} = BSTMON resistor-divider gain (1 + R6/R7)

FSEN/ISET Pin Function

The FSEN/ISET pin is active when the I2CDIS/RSDT pin is connected to GND, and can be used to enable the device in situations where I²C control is temporarily impossible or the interface has stopped functioning. When FSEN/ISET is taken high, the boost converter is turned on and the current sinks are enabled at 100% duty cycle. When FSEN/ISET returns low, the values programmed in the I²C registers are applied at the beginning of the next dimming cycle.

The OUT_ current, when FSEN/ISET is high, is set by a resistor from FSEN/ISET to GND (Table 1).

The resistor value is read at power-up and the set OUT_ current value and I²C address cannot subsequently be changed.

If FSEN/ISET is not used, connect the pin to GND unless an I²C address other than 0x68 is desired.

In stand-alone mode, the FSEN/ISET pin sets the LED current, as described in the *LED Current Control* section.

PWM Dimming

Dimming can be performed using either an external PWM signal applied to the DIM pin, or by programming the desired dimming level through I²C.

When using the DIM pin as an input, set the DIM_EXT bit in the IMODE register (0x03) to 1 (this is also the default value; in stand-alone mode the DIM pin is always the dimming input). The signal on the DIM pin is sampled with a 20MHz internal clock.

The DIM input accepts a PWM signal greater than 100Hz to control the current and the luminous intensity of the LEDs. The DIM input detects the dimming frequency based on the first two pulses applied to the DIM input after EN goes high. The dimming frequency cannot be changed during normal operation. If a change of dimming frequency is desired, the EN input should be set low, and the DIM frequency changed; then the EN signal can be set high again. The DIM signal can be applied before or after the device is enabled, but the DIM signal needs to power on smoothly (no high-frequency pulses). If the DIM signal turn-on is inconsistent, the DIM signal should be applied first. Once the DIM signal is stable, the EN signal can be applied.

Table 1. FSEN/ISET Resistor Values

FSEN/ISET RESISTOR VALUE (kΩ)	OUT_ CURRENT (mA)	7-BIT I²C ADDRESS
0	Fail-safe disabled	0x68
3.48	25	0x68
7.15	25	0x6E
12	50	0x68
18.7	50	0x6E
27.4	75	0x68
39	75	0x6E
59	100	0x68
84.5	100	0x6E

Hybrid Dimming

In hybrid-dimming mode, the external LEDs are dimmed by first reducing their current as the dimming duty-cycle decreases from 100% (see Figure 1). At the crossover level set by the HDIM_THR_1_0[1:0] bits or the HDSET input, dimming transitions to PWM dimming where the LED current is chopped. To select hybrid dimming, set the HDIM bit in the IMODE (0x03) register and select the desired crossover level between analog and PWM dimming using the HDIM_THR_1_0[1:0] bits in the same register. See the *Stand-Alone Mode* section on how to implement hybrid dimming when using the device in stand-alone mode. Depending on the DIM_EXT bit, the device functions in one of two ways:

1) (DIM_EXT=1 or stand-alone mode) measures the duty cycle on the DIM pin and translates it into a combined LED current value and PWM setting.
2) (DIM_EXT=0) takes the 18-bit value from the TON__ registers and translates it into a combined LED current value and PWM setting.

Note: When hybrid dimming is used with an internal dimming setting (DIM_EXT=0), only the value TON1[17:0] is used. It is not possible to have individual dimming settings for each of the channels in this mode but the TON_ settings for all the channels must be non-zero.

In summary, there are four possible dimming modes:

1) External PWM dimming.
2) Internal PWM dimming, with the pulse width set through I2C and the PWM frequency generated internally.
3) External hybrid dimming with a PWM signal applied to the DIM pin; the pulsed current on the OUT_ pins follows the DIM frequency.
4) Internal hybrid dimming with the dimming ratio set through I2C and the PWM frequency generated internally.

Only modes one and three are available in stand-alone mode.

Figure 2 illustrates the difference between standard and hybrid dimming with phase-shifting enabled.

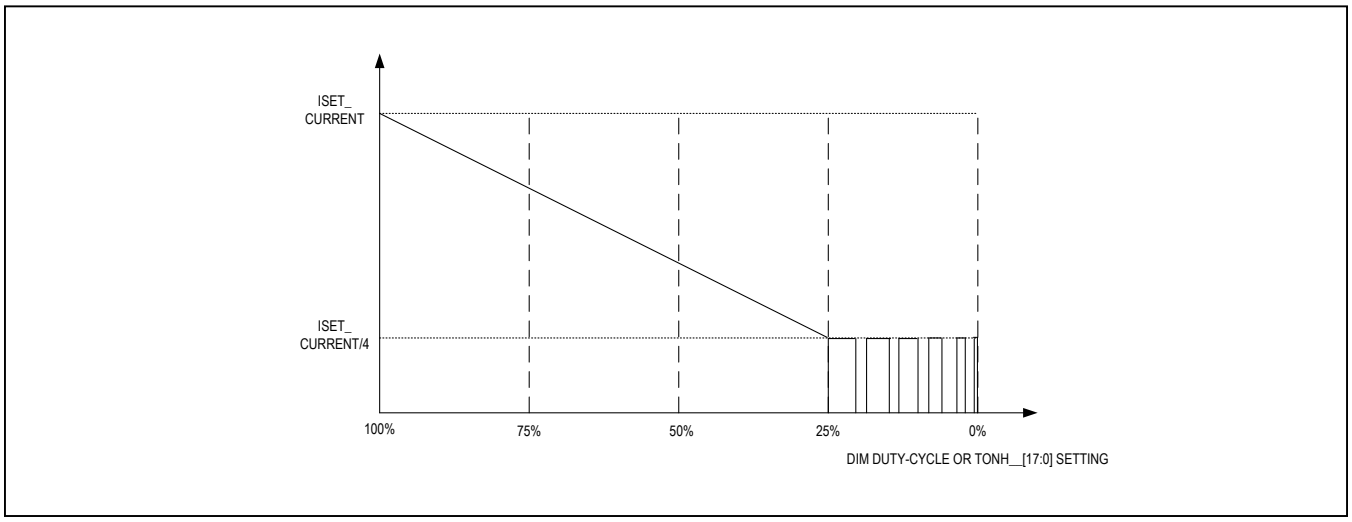


Figure 1. Hybrid Dimming Operation with HDIM[1:0] = 10 (25%) or R_{HDSET} = 27.4kΩ

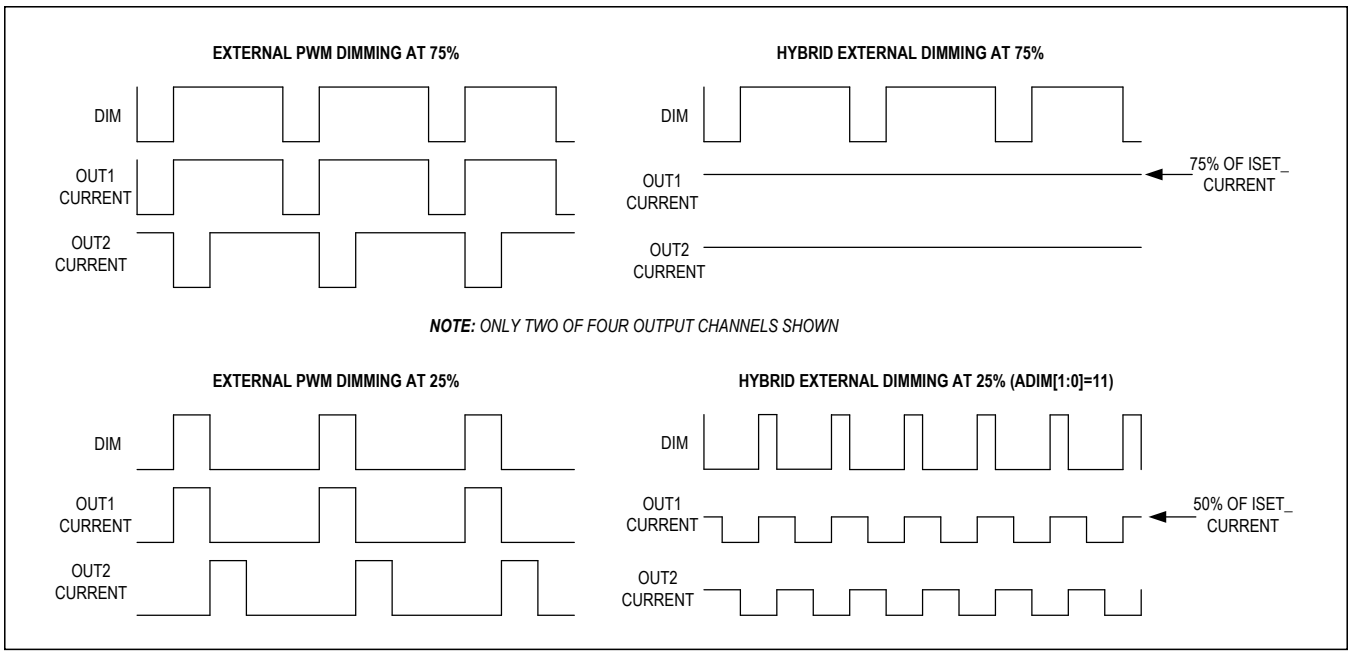


Figure 2. Hybrid Dimming Operation Modes

Low-Dimming Mode

The IC's operation changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. If the dimming on-time (from either the DIM input or the TON_ value, depending on which is selected) is lower than 50µs (typ), the device enters low-dimming mode. In this state, the converter switches continuously and LED short detection is disabled. When the DIM input is greater than 51µs (typ) the device goes back into normal operation, enabling the short-LED detection and switching the power FET only when the effective dimming signal is high. OUT_ current monitoring does not operate in low-dim mode although the BSTMON voltage can still be measured.

When the device is used in I2C mode with internal dimming some channels may be in low-dim mode while others are not. If any channel is in low-dim mode, the boost converter runs continuously.

Phase-Shift Dimming

When the PSEN bit in register 0x02 is set (or the SDA/PSEN pin is high in stand-alone mode), phase shifting of the LED strings is enabled. The device automatically sets the phase shift between strings to 90°, 120°, or 180° depending on the number of strings enabled.

Disabling Individual Strings

To disable an unused LED string, connect the unused OUT_ to ground through a 12kΩ resistor, or set the corresponding DIS_ bit to 1 in the DISABLE (0x13) register before the ENA bit is set. During startup, the device sources 60µA (typ) current through the OUT_ pins and measures the corresponding voltage. For the string to be properly disabled, the OUT_ voltage should measure between 365mV and 1.15V during this check. 365mV is the maximum threshold for the OUT_ short-to-ground check and 1.15V is the minimum unused string-detection threshold.

Note: When disabling unused strings, it is necessary to start by disabling the highest numbered current sinks first (e.g., if two strings need to be disabled, disable OUT4 and OUT3. Do not disable any two strings at random). During normal operation, strings can be selectively turned off by changing the corresponding TON_ setting to 0. This is only possible when internal dimming is used (not when using the DIM input pin).

Startup Sequence

When the EN pin is taken high (assuming the IN voltage is above its undervoltage-lockout value), the internal regulator and the I²C interface are turned on (if I2CDIS/RSDT is connected to GND) and the device checks the OUT_ channels. If any of the OUT_ pins are detected as shorted to GND, the boost converter does not start (to avoid possible damage) and the corresponding OUT_SG bit(s) are set. The device also detects and disconnects any unused current-sink channels connected to GND by means of a 12kΩ resistor. Alternatively, when using the I²C interface, individual channels can be disabled using the DIS[4:1] bits. The total duration of this phase of the startup is 2ms (max). After this phase, the I²C interface can be used and the device registers can be written (in stand-alone mode the boost converter and current-sinks are enabled after this phase). When using I²C, the ENA bit should be set to 1 to enable the boost and subsequently the OUT_ current sinks. When the ENA bit is set high, the startup sequence occurs in three stages:

Stage 1

Once the ENA bit is high (or the EN pin is in stand-alone mode), the controller begins the soft-start of the boost. First, the driver of the external pMOSFET is turned on. A constant current of 200µA (typ) flows into the PGATE pin of the device. This current in the PGATE resistor pulls down the gate of the external pMOSFET turning it on. After the external pMOSFET is turned on and a 2ms timeout expires, stage 2 of the startup begins.

Stage 2

After the checks in stage 1 have been performed, the converter starts switching and the output begins to ramp. The DAC reference to the error amplifier is stepped up 1 bit at a time until the voltage at BSTMON reaches 600mV. This stage duration is fixed at approximately 50ms (typ). The BSTMON pin is then sampled, and if its voltage is less than 430mV (typ), FLTB is asserted low, the power converter is turned off, the external pMOSFET is turned off, and they all remain off until the ENA bit, input power, or EN pin is toggled.

Stage 3

The third stage begins once stage 2 is complete and the DIM input goes high (with DIM_EXT=1), or internal dimming is enabled by setting a PWM value greater than 0 on any of the channels. During stage 3, the output of the converter is adjusted until the minimum OUT_ voltage falls within 0.78V (typ) and 1.03V (typ) comparator limits. The output adjustment is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input pin (or internal dimming signal). If the DIM input (or the internal dimming signal when DIM_EXT=1) is at 100% duty cycle (DIM = high), the DAC output is updated once every 10ms.

The total soft-start time can be calculated using Equation 3.

Equation 3:

$$t_{SS} = 52ms + \frac{(V_{LED} + 0.91) - (0.6 \times A_{OVP})}{f_{DIM} \times 0.01 \times A_{OVP}}$$

where:

t_{SS} = Total soft-start time

52ms = Fixed stage 1 + stage 2 duration

V_{LED} = Total forward voltage of the LED strings

0.91V = Midpoint of the window comparator

f_{DIM} = Dimming frequency (use 100Hz for f_{DIM} when input duty cycle is 100%)

0.01V = 4 times the 2.5mV LSB of the DAC, and

A_{OVP} = Gain of the BSTMON resistor-divider or 1 + R6/R7

After the soft-start period, a fault is detected whenever the BSTMON pin falls below 430mV (typ). When this occurs, the power converter is latched off and the PGATE output goes high impedance, disconnecting the input voltage from the boost converter. The FLTB pin is asserted low whenever the undervoltage protection is activated. Cycling the ENA bit, EN pin, or the supply is required to start up again, once the fault condition has been removed.

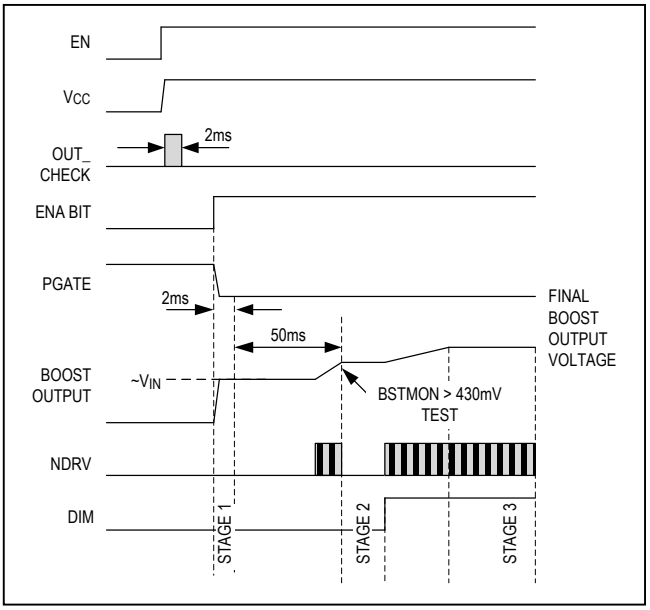


Figure 3. Boost Startup (I²C Operation)

Oscillator Frequency/ External Synchronization

The internal oscillator frequency is programmable between 400kHz and 2.2MHz using a timing resistor (R_{RT}) connected from the RT pin to GND. Use Equation 4 to calculate the value of R_{RT} for the desired switching frequency (f_{SW}).

Equation 4:

$$R_{RT} = \frac{29260 + (2200 - f_{SW}) \times 0.81}{f_{SW}}$$

where R_{RT} is in kΩ and f_{SW} is in kHz.

Synchronize the oscillator with an external clock by AC-coupling the external clock to the RT input. The value of the capacitor used for AC-coupling is C_{SYNC} = 10pF and the duty cycle of the external clock should be 50%.

Spread-Spectrum Mode

The IC includes a spread-spectrum mode that reduces peak electromagnetic interference (EMI) at the switching frequency and its harmonics.

The spread spectrum uses a pseudorandom dithering technique where the switching frequency is varied in the 97% range (or 94% when the SSL bit is 1) of the programmed switching frequency, to 103% (or 106% when the SSL bit is 1) of the programmed switching frequency set through the external resistor from RT to GND. When spread spectrum is used, the total energy at the fundamental and each harmonic is spread over a wider bandwidth, reducing the peak energy at the relevant frequency.

Spread spectrum is disabled if external synchronization is used. Optionally, spread spectrum can also be disabled by setting the SS_OFF bit in the SETTING (0x12) register to 1. The amount of spread spectrum can also be varied between ±3% and ±6% using the SSL bit in the same register.

5V LDO Regulator (V_{CC})

The internal LDO regulator converts the input voltage at IN to a 5V output voltage at V_{CC}. The LDO regulator supplies current to the internal control circuitry and the gate driver. Bypass V_{CC} to GND with a 1µF (min) ceramic capacitor as close as possible to the device.

LED Current Control

The full-scale sink current for the outputs (OUT1–OUT4) is set using the four ISET[3:0] bits in the ISET register (0x02), or by the resistor on the FSEN/ISET pin (along with the state of the IRANGE pin). The OUT_ current value is also directly related to the reference current in the resistor on the IREF pin (R_{IREF}). If the R_{IREF} value is not in the 40kΩ to 70kΩ range, the device will not operate and an IREFOOR error is indicated (see the *Register Map*).

When PWM dimming is used, the current in the OUT_ channels switches between zero and the full-scale sink current at the set duty cycle.

The maximum LED current can be increased to 132mA by reducing the value of R_{IREF} to 45.3kΩ. With this value of R_{IREF}, the current settings are as shown in Table 2.

When hybrid dimming is used, the sink current in OUT1–OUT4 is reduced linearly from the full-scale value until the level set by HDIM_THR_1_0[1:0] or HDSET is reached; dimming at lower levels is then accomplished using PWM (see Figure 1).

Table 2. ISET Currents with 45.3kΩ IREF Resistor

ISET[3:0]	NOMINAL OUT_ CURRENT (mA)
0000	50
0001	55
0010	61
0011	66
0100	72
0101	77
0110	83
0111	88
1000	94
1001	99
1010	105
1011	110
1100	116
1101	121
1110	127
1111	132

Fault Protection

Fault protection in the IC includes cycle-by-cycle current limiting in the PWM controller, DC-DC converter output-undervoltage protection, output-overvoltage protection, open-LED detection, short-LED detection and protection, and overtemperature shutdown. The open-drain fault flag output (FLTB) goes low when an open-LED string is detected, a short-LED string is detected, an output undervoltage, or during thermal shutdown. When using the I²C interface, certain faults can be inhibited from causing FLTB to go low. FLTB is cleared when the fault condition is removed during thermal shutdown and shorted LEDs. FLTB is latched low for an open-LED and can be reset by cycling power or by toggling the EN pin or the ENA bit in the ISET register (0x02). The thermal-shutdown threshold is +165°C and has +15°C hysteresis.

Open-LED Management and Overvoltage Protection

After the soft-start of the boost converter, the IC detects open-LED strings and disconnects any such strings from the internal minimum OUT_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency. The current in strings that have been detected open is not measured by the ADC and reads as zero.

During normal operation, the DC-DC converter output-regulation loop uses the minimum OUT_ voltage as the feedback input. If any LED string is open, the voltage at the opened OUT_ goes to V_{LEDGND}. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, the BSTMON input, and GND. The overvoltage-protection threshold at the DC-DC converter output is determined using the equation below.

Equation 5:

$$V_{OUT\_BSTMON} = 1.23 \times \left(1 + \frac{R6}{R7}\right)$$

where: 1.23V (typ) is the overvoltage threshold on BSTMON (see the *Functional Diagrams*). Select V_{OUT_BSTMON} according to the formula below.

Equation 6:

$$1.1 \times (V_{LED\_MAX} + 1.04) < V_{OUT\_BSTMON} < 2 \times (V_{LED\_MIN} + 0.58)$$

where:

V_{LED_MAX} = Maximum expected LED string voltage

V_{LED_MIN} = Minimum expected LED string voltage

Select R6 and R7 such that the voltage at OUT_ does not exceed the absolute maximum rating. As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the internal MOSFET is switched off.

The overvoltage threshold should be set to less than twice the minimum LED voltage to ensure proper operation and so the BSTMON minimum regulation point of 600mV (typ) is not breached. Connect a 12kΩ resistor between OUT_ and LEDGND for each unused channel to avoid overvoltage triggering at startup. When an open-LED overvoltage condition occurs, FLTB is latched low. Any current-sink output with $V_{OUT\_}$ < 300mV (typ) is permanently disconnected from the minimum voltage detector.

Short-LED Detection

The IC checks for shorted LEDs after the current in any channel is turned on. A shorted-LED is detected at OUT_ if the condition below is met.

Equation 7:

$$V_{OUT\_} > RSDT$$

where:

RSDT = Programmable short-LED-detection threshold set by the SLDET[1:0] bits in the SETTING (0x12) register, or in stand-alone mode, 4 times the voltage on the I2CDIS/RSDT pin (at least 1.3V).

If a short is detected on any of the strings, the affected LED strings are disconnected and the FLTB output flag asserts low until the device detects that the shorts are removed. Disable short-LED detection by setting SLDET[1:0] to 0x0 or connecting I2CDIS/RSDT to V_{CC} in stand-alone mode. Short-LED detection is disabled in low-dimming mode. In external dimming mode with the DIM input connected continuously high, the OUT_ pins are periodically scanned to detect shorted LEDs. The scan frequency is 100Hz.

Similarly, when DIM_EXT=0 and internal dimming is being used, shorted LEDs are still detected by periodically scanning the OUT_ states at 100Hz.

Thermal Warning/Shutdown

The IC includes thermal protection that operates at a temperature of +165°C. When the thermal-shutdown temperature is reached, the device is immediately disabled so it can cool. When the junction temperature falls by 15°C, the device is re-enabled with the same settings as before (the boost converter performs a soft-start). When a thermal shutdown occurs, the FLTB pin goes low and the OT bit, if read through the I²C, is set to 1.

A thermal warning bit (OTW) is implemented in the DIAG (0x1F) register and indicates that the junction temperature has exceeded +125°C. The OTWMASK bit in the MASK (0x1E) register is used to control whether or not an active OTW bit causes the FLTB pin to go low. In stand-alone mode, FLTB does not assert low when the junction temperature exceeds +125°C.

Stand-Alone Mode

Connect I2CDIS/RSDT to V_{CC} or set a voltage of 1.3V or greater on RSDT to use the IC in stand-alone mode without the I²C interface. In this mode, the peak LED current is set using the FSEN/ISET and SCL/IRANGE pins, as shown in Table 3.

The OUT_ current value is also directly related to the reference current in the resistor on the IREF pin. If the IREF resistor value is not in the 40kΩ to 70kΩ range, the device will not operate.

Table 3. Current-Setting Resistors

R_{IREF} (kΩ)	IRANGE	R_{ISET} (Ω)	CURRENT SETTING (mA)
49.9	GND	3480	45
		7150	50
		12k	55
		18.7k	60
		27.4k	65
		39k	70
		59k	75
		84.5k	80
	V_{CC}	3480	85
		7150	90
		12k	95
		18.7k	100
		27.4k	105
		39k	110
		59k	115
		84.5k	120

R_{IREF} (kΩ)	IRANGE	R_{ISET} (Ω)	CURRENT SETTING (mA)
45.3	GND	3480	50
		7150	55
		12k	61
		18.7k	66
		27.4k	72
		39k	77
		59k	83
		84.5k	88
	V_{CC}	3480	94
		7150	99
		12k	105
		18.7k	110
		27.4k	116
		39k	121
		59k	127
		84.5k	132

Dimming in Stand-Alone Mode

The dimming modes available in stand-alone mode are:

1) External PWM dimming.
2) External hybrid dimming with a PWM signal applied to the DIM pin. In this mode, the device automatically determines whether the LED current is to be dimmed by reducing the LED current or by chopping the LED current (depending on the hybrid dimming threshold).

Hybrid Dimming in Stand-Alone Mode

Hybrid dimming can be used in stand-alone mode by connecting a resistor from HDSET to GND. The resistor sets the threshold where analog dimming transitions to PWM dimming according to Table 4. As shown in the table, if hybrid dimming is not used, connect HDSET to V_{CC}.

The state of the FSEN/ISET, SCL/IRANGE, and HDSET pins is read at startup and stored in the device. The resulting settings cannot subsequently be changed, unless the device is powered down and back up again.

Phase shifting of the output channels can be enabled and disabled using the SDA/PSEN pin when in stand-alone mode. With SDA/PSEN connected high (to V_{CC}) phase shifting is enabled.

Table 4. Setting the Hybrid-Dimming Threshold

HDSET	HYBRID-DIMMING THRESHOLD
Shorted to V_{CC}	Hybrid dimming disabled
59kΩ to GND	50% of ISET
27.4kΩ to GND	25% of ISET
12kΩ to GND	12.5% of ISET
3480Ω to GND	6.25% of ISET

Analog-to-Digital Converter

The analog-to-digital converter (ADC) is used to measure the current in each of the strings and the voltage on the BSTMON pin. A conversion cycle is started by setting the CONVERT bit in the ISET (0x02) register to 1. At the end of the cycle the CONVERT bit is reset to 0 to indicate a complete cycle, and the IOUT1–IOUT4 and BSTMON registers contain the updated values. The full-scale value of the current measurement is 127.5mA with an IREF resistor of 49.9kΩ or 140.4mA with R_{IREF} = 45.3kΩ. Values higher than these read as full scale or 0xFF. Current measurements are not performed on channels that are in low-dim mode; before performing a conversion, this can be checked by reading the LoDIM_ bits. If a conversion is attempted on a channel that is in low-dim mode, the current value returned will be 0x00. The duration of a complete conversion depends on whether or not phase shifting is enabled. With phase shifting enabled, a complete conversion can take up to two dimming cycles, worst-case. With phase shifting disabled, one dimming cycle is the worst-case latency (the conversion is initiated at the beginning of a DIM cycle and concluded < 50µs later).

Register Map

ADDRESS	NAME	MSB							LSB
I²C									
0x00	Dev_ID[7:0]	Device_ID[7:0]							
0x01	Rev_ID[7:0]	–	–	–	–	Revision_ID[3:0]			
0x02	ISET[7:0]	–	CONVERT	ENA	PSEN	ISET[3:0]			
0x03	IMODE[7:0]	LoDIM4	LoDIM3	LoDIM2	LoDIM1	DIM_EXT	HDIM	HDIM_THR_1_0[1:0]	
0x04	TON1H[7:0]	TON1H[7:0]							
0x05	TON1L[7:0]	TON1L[7:0]							
0x06	TON2H[7:0]	TON2H[7:0]							
0x07	TON2L[7:0]	TON2L[7:0]							
0x08	TON3H[7:0]	TON3H[7:0]							
0x09	TON3L[7:0]	TON3L[7:0]							
0x0A	TON4H[7:0]	TON4H[7:0]							
0x0B	TON4L[7:0]	TON4L[7:0]							
0x0C	TON1-4LSB[7:0]	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
0x12	SETTING[7:0]	–	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
0x13	DISABLE[7:0]	–	–	–	–	DIS4	DIS3	DIS2	DIS1
0x14	BSTMON[7:0]	VMON[7:0]							
0x15	IOUT1[7:0]	IOUT1[7:0]							
0x16	IOUT2[7:0]	IOUT2[7:0]							
0x17	IOUT3[7:0]	IOUT3[7:0]							
0x18	IOUT4[7:0]	IOUT4[7:0]							
0x1B	OPEN[7:0]	–	–	–	–	OUT4O	OUT3O	OUT2O	OUT1O
0x1C	SHORTGND[7:0]	–	–	–	–	OUT4SG	OUT3SG	OUT2SG	OUT1SG
0x1D	SHORTED LED[7:0]	–	–	–	–	OUT4SL	OUT3SL	OUT2SL	OUT1SL
0x1E	MASK[7:0]	–	–	–	BSTUVMASK	OMASK	SGMASK	OTWMASK	SLMASK
0x1F	DIAG[7:0]	–	–	IREFOOR	BSTUV	BSTOV	HW_RST	OTW	OT

Register Details

Dev_ID (0x00)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[7:0]							
Reset	0x44							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Device_ID	7:0		Device ID, reads 0x44.

Rev_ID (0x01)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Revision_ID[3:0]			
Reset	–	–	–	–	0x01			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
Revision_ID	3:0	Device revision ID, reads 0x01.

ISET (0x02)

BIT	7	6	5	4	3	2	1	0
Field	–	CONVERT	ENA	PSEN	ISET[3:0]			
Reset	–	0b0	0b0	0b1	0b1011			
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CONVERT	6	Write a 1 to this bit to start a conversion cycle of the ADC. When the cycle is finished, this bit is automatically reset to indicate that data is ready.	
ENA	5	Boost converter and LED outputs enable bit. Set to 1 to enable the device.	
PSEN	4	When 0, phase shifting is disabled. When 1, phase shifting is enabled.	
ISET	3:0	LED current setting (values with R_{IREF} = 49.9kΩ).	*default value

IMODE (0x03)

BIT	7	6	5	4	3	2	1	0
Field	LoDIM4	LoDIM3	LoDIM2	LoDIM1	DIM_EXT	HDIM	HDIM_THR_1_0[1:0]	
Reset	0x0	0x0	0x0	0x0	0b1	0b0	0b00	
Access Type	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
LoDIM4	7	When 1, indicates that channel 4 is in low-dim mode.
LoDIM3	6	When 1, indicates that channel 3 is in low-dim mode.
LoDIM2	5	When 1, indicates that channel 2 is in low-dim mode.
LoDIM1	4	When 1, indicates that channel 1 is in low-dim mode.
DIM_EXT	3	When 1, dimming through the DIM pin is enabled. When 0, dimming is controlled using the TON__ registers.
HDIM	2	When 1, hybrid dimming is enabled. Default value is 0.
HDIM_THR_1_0	1:0	Set hybrid-dimming threshold. Default value is 6.25% (00).

TON1H (0x04)

On-time setting for channel 1 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1H	7:0	High byte of 18-bit TON setting for channel 1.

TON1L (0x05)

On-time setting for channel 1 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1L	7:0	Middle byte of 18-bit TON setting for channel 1.

TON2H (0x06)

On-time setting for channel 2 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2H	7:0	High byte of 18-bit TON setting for channel 2.

TON2L (0x07)

On-time setting for channel 2 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2L	7:0	Middle byte of 18-bit TON setting for channel 2.

TON3H (0x08)

On-time setting for channel 3 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON3H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3H	7:0	High byte of 18-bit TON setting for channel 3.

TON3L (0x09)

On-time setting for channel 3 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON3L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3L	7:0	Middle byte of 18-bit TON setting for channel 3.

TON4H (0x0A)

On-time setting for channel 4 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON4H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4H	7:0	High byte of 18-bit TON setting for channel 4.

TON4L (0x0B)

On-time setting for channel 4 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON4L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4L	7:0	Middle byte of 18-bit TON setting for channel 4.

TON1-4LSB (0x0C)

LSbs of on-time setting for all channels with 50ns resolution.

BIT	7	6	5	4	3	2	1	0
Field	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
Reset	0b11		0b11		0b11		0b11	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
TON4LSB	7:6	2 least significant bits of 18-bit TON setting for channel 4.
TON3LSB	5:4	2 least significant bits of 18-bit TON setting for channel 3.
TON2LSB	3:2	2 least significant bits of 18-bit TON setting for channel 2.
TON1LSB	1:0	2 least significant bits of 18-bit TON setting for channel 1.

SETTING (0x12)

BIT	7	6	5	4	3	2	1	0
Field	–	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
Reset	–	0b001			0b0	0b0	0b00	
Access Type	–	Write, Read			Write, Read	Write, Read	Write, Read	

<table>
<tr><th>BITFIELD</th><th>BITS</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="10">FPWM</td><td rowspan="10">6:4</td><td colspan="4">These bits set the PWM frequency in internal PWM mode.</td></tr>
<tr><td>FPWM2</td><td>FPWM1</td><td>FPWM0</td><td>PWM FREQUENCY (Hz)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>153</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>203</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>305</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>610</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>980</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1220</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1401</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1634</td></tr>
<tr><td>SS_OFF</td><td>3</td><td colspan="4">When 1, spread-spectrum switching is disabled. Default value is 0.</td></tr>
<tr><td>SSL</td><td>2</td><td colspan="4">When spread spectrum is enabled, the SSL bit chooses the amount of spread: When 0, the spread is nominally ±6%, and when 1, the spread is ±3%.</td></tr>
<tr><td rowspan="5">SLDET</td><td rowspan="5">1:0</td><td colspan="4">Shorted-LED-Threshold Settings</td></tr>
<tr><td colspan="2">SLDET1</td><td>SLDET0</td><td>SETTING</td></tr>
<tr><td colspan="2">0</td><td>0</td><td>Disabled</td></tr>
<tr><td colspan="2">0</td><td>1</td><td>3V</td></tr>
<tr><td colspan="2">1</td><td>0</td><td>6V</td></tr>
<tr><td colspan="2">1</td><td>1</td><td>8V</td></tr>
</table>

DISABLE (0x13)

Channel-disable bits.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DIS4	DIS3	DIS2	DIS1
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DIS4	3	Set this bit to 1 to disable OUT4. This must be done before ENA is written to 1.
DIS3	2	Set this bit to 1 to disable OUT3. This must be done before ENA is written to 1.
DIS2	1	Set this bit to 1 to disable OUT2. This must be done before ENA is written to 1.
DIS1	0	Set this bit to 1 to disable OUT1. This must be done before ENA is written to 1.

BSTMON (0x14)

BSTMON pin-voltage readback.

BIT	7	6	5	4	3	2	1	0
Field	VMON[7:0]							
Reset	0b00000000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VMON	7:0	Voltage on BSTMON. Full-scale = 1.3V, 1 LSB = 5.1mV.

IOUT1 (0x15)

OUT1 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT1	7:0	OUT1 output current.Full scale is 127.5mA or 140.4mA, depending on the IREF resistor value.

IOUT2 (0x16)

OUT2 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT2	7:0	OUT2 output current, Full scale is 127.5mA or 140.4mA, depending on the IREF resistor value.

IOUT3 (0x17)

OUT3 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT3	7:0	OUT3 output current. Full scale is 127.5mA or 140.4mA, depending on the IREF resistor value.

IOUT4 (0x18)

OUT4 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT4	7:0	OUT4 output current. Full scale is 127.5mA or 140.4mA, depending on the IREF resistor value.

OPEN (0x1B)

Open-string diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4O	OUT3O	OUT2O	OUT1O
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4O	3	If 1, an open has been detected on channel 4.
OUT3O	2	If 1, an open has been detected on channel 3.
OUT2O	1	If 1, an open has been detected on channel 2.
OUT1O	0	If 1, an open has been detected on channel 1.

SHORTGND (0x1C)

Short-to-ground diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4SG	OUT3SG	OUT2SG	OUT1SG
Reset	–	–	–	–	0x0b0	0x0b0	0x0b0	0x0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4SG	3	If 1, a short-to-ground has been detected on channel 4 at startup.
OUT3SG	2	If 1, a short-to-ground has been detected on channel 3 at startup.
OUT2SG	1	If 1, a short-to-ground has been detected on channel 2 at startup.
OUT1SG	0	If 1, a short-to-ground has been detected on channel 1 at startup.

SHORTED LED (0x1D)

Shorted-LED diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4SL	OUT3SL	OUT2SL	OUT1SL
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4SL	3	If 1, a shorted-LED condition has been detected on channel 4.
OUT3SL	2	If 1, a shorted-LED condition has been detected on channel 3.
OUT2SL	1	If 1, a shorted-LED condition has been detected on channel 2.
OUT1SL	0	If 1, a shorted-LED condition has been detected on channel 1.

MASK (0x1E)

Mask register for the FLTB pin.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BSTUV MASK	OMASK	SGMASK	OTWMASK	SLMASK
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BSTUVMASK	4	When 1, a boost fault (undervoltage or overvoltage) does not cause the FLTB pin to assert low.
OMASK	3	When 1, an open-LED fault does not cause the FLTB pin to assert low.
SGMASK	2	When 1, a short-to-ground LED fault does not cause the FLTB pin to assert low.
OTWMASK	1	When 1, an overtemperature warning does not cause the FLTB pin to assert low.
SLMASK	0	When 1, a shorted-LED fault does not cause the FLTB pin to assert low.

DIAG (0x1F)

Boost state, overtemperature-warning/shutdown diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	IREFOOR	BSTUV	BSTOV	HW_RST	OTW	OT
Reset	–	–	0b0	0b0	0b0	0b1	0x0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
IREFOOR	5	When 1, this bit indicates that the IREF current is out of range. This is probably due to an incorrect resistor value on IREF. In this condition, the IC stops operation.
BSTUV	4	If 1, an undervoltage has been detected on the boost output and the boost was disabled.
BSTOV	3	If 1, the boost converter is at its overvoltage limit.
HW_RST	2	If 1, the device has just emerged from a hardware reset (power-up). This bit is reset after the first read from this register.
OTW	1	If 1, the junction temperature of the device is over +125°C.
OT	0	If 1, the junction temperature of the device exceeded +165°C and the device was shut down.

Applications Information

DC-DC Converter

Three different converter topologies are possible with the DC-DC converter in the MAX20444C that have the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string forward voltage is always greater than the input supply voltage range, use the boost-converter topology. If the LED string forward voltage falls within the supply voltage range, use a buck-boost converter topology. The possible buck-boost topologies are SEPIC or a coupled-inductor buck-boost topology. The latter is basically a flyback converter with 1:1 turns ratio. 1:1-coupled inductors are available with tight coupling suitable for this application.

The boost-converter topology provides the highest efficiency among the above-mentioned topologies. The coupled-inductor topology has the advantage of not using a coupling capacitor, but does require tightly coupled windings to avoid additional snubber components. The SEPIC configuration requires two inductors (or a coupled inductor) and a coupling capacitor. Furthermore, the feedback-loop compensation for SEPIC becomes complex if the coupling capacitor is not large enough.

Power-Circuit Design

First select a converter topology based on the factors listed in the *DC-DC Converter* section. Determine the required input supply voltage range, the maximum voltage needed to drive the LED strings, including the minimum 0.85V across the constant LED current sink (V_{LED}), and the total output current needed to drive the LED strings (I_{LED}), as shown below in Equation 8.

Equation 8:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

where I_{STRING} is the current per string and N_{STRING} is the number of strings used.

Next, calculate the maximum duty cycle (D_{MAX}) using one of the equations below, depending on the configuration.

Equation 9 (for the boost configuration)**:**

$$D_{MAX} = \frac{(V_{LED} + V_{D1} - V_{IN\_MIN})}{(V_{LED} + V_{D1} - V_{DS} - 0.3)}$$

Equation 10 (for SEPIC and coupled-inductor buck-boost configurations)**:**

$$D_{MAX} = \frac{V_{LED} + V_{D1}}{(V_{IN\_MIN} - V_{DS} - 0.3 + V_{LED} + V_{D1})}$$

where:

- V_{D1} = Forward drop of the rectifier diode in volts (approximately 0.6V)
- V_{IN_MIN} = Minimum input supply voltage
- V_{DS} = Drain-to-source voltage of the external MOSFET when it is on

Select the switching frequency (f_{SW}) depending on the space, noise, and efficiency constraints.

Boost and Coupled-Inductor Configurations

In all three converter configurations, the average inductor current varies with the input voltage; the maximum average current occurs at the lowest input voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current (ΔIL). The recommended maximum peak-to-peak ripple is 60% of the average inductor current, but lower and higher values of ripple are also acceptable.Use the following equations to calculate the maximum average inductor current (IL_{AVG}) and peak inductor current (I_{LP}) in amperes.

Equation 11:

$$IL_{AVG} = \frac{I_{LED}}{(1 - D_{MAX})}$$

Allowing the peak-to-peak inductor ripple (ΔIL) to be ±30% of the average inductor current:

Equations 12:

$$\Delta IL = IL_{AVG} \times 0.3 \times 2$$

and:

$$IL_P = IL_{AVG} + \frac{\Delta IL}{2}$$

Calculate the minimum inductance value (L_{MIN}), in henries (H), with the inductor current ripple set to the maximum value:

Equation 13:

$$L_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3) \times D_{MAX}}{f_{SW} \times \Delta IL}$$

Choose an inductor with a minimum inductance greater than the calculated L_{MIN} and current rating greater than IL_P. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration. For the coupled-inductor, the saturation limit of the inductor with only one winding conducting should be 10% higher than IL_P.

SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts. One of the inductors (L2) takes LED current as the average current, and the other (L1) takes input current as the average current.

Use the following equations to calculate the average inductor currents ($IL1_{AVG}$, $IL2_{AVG}$) and peak inductor currents ($IL1_P$, $IL2_P$) in amperes.

Equation 14:

$$I_{L1AVG} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a margin of 10% to account for the converter losses.

Equation 15:

$$IL2_{AVG} = I_{LED}$$

Assuming the peak-to-peak inductor ripple ΔIL is ±30% of the average inductor current.

Equations 16:

$$\Delta IL1 = IL1_{AVG} \text{ x } 0.3 \text{ x } 2$$

and:

$$IL1_P = IL1_{AVG} + \frac{\Delta IL1}{2}$$

and:

$$IL2 = IL2_{AVG} \text{ x } 0.3 \text{ x } 2$$

and:

$$IL2_P = IL2_{AVG} + \frac{\Delta IL2}{2}$$

Calculate the minimum inductance values ($L1_{MIN}$ and $L2_{MIN}$) in henries with the inductor current ripple set to the values previously calculated.

Equations 17:

$$L1_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3) \times D_{MAX}}{f_{SW} - \Delta IL1}$$

$$L2_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3) \times D_{MAX}}{f_{SW} - \Delta IL2}$$

Choose inductors with a minimum inductance greater than the calculated $L1_{MIN}$ and $L2_{MIN}$, and current rating greater than $IL1_P$ and $IL2_P$, respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

To simplify further calculations, consider L1 and L2 as a single inductor with L1 and L2 connected in parallel. The combined inductance value and current is calculated as shown below.

Equations 18:

$$L = \frac{L1 \times L2}{L1 + L2}$$

and:

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where IL_{AVG} represents the total average current through both the inductors in the SEPIC configuration. Use these values in the calculations in the following sections.

Select coupling-capacitor C_S so that peak-to-peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series-resonant circuit comprising L1, C_S, and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of C_S.

Equation 19:

$$C_S = \frac{I_{LED} \times D_{MAX}}{V_{IN\_MIN} \times 0.02 \times f_{SW}}$$

where:

- C_S = Minimum value of the coupling capacitor in farads
- 0.02 = 2% ripple factor

Slope Compensation and Current-Sense Resistor

The IC generates a current ramp for slope compensation. This ramp current is synchronized with the switching frequency and starts from zero at the beginning of every clock cycle, rising linearly to reach 50µA at the end of the clock cycle. The slope-compensating resistor (R_{SC}) is connected between the CS input and the source of the external switching MOSFET. This adds a programmable ramp voltage to the CS input voltage to provide slope compensation.

Use one of the the following equations to calculate the value of R_{SC}.

Equation 20 (for the boost configuration)**:**

$$R_{SC} = \frac{(V_{LED} - 2 \times V_{IN\_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

Equation 21 (for SEPIC and coupled-inductor configurations)**:**

$$R_{SC} = \frac{(V_{LED} - V_{IN\_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

where:

- V_{LED} and V_{IN_MIN} are in volts
- R_{SC} and R_{CS} are in ohms
- L_{MIN} is in henries
- f_{SW} is in hertz

The value of the switch current-sense resistor (R_{CS}) can be calculated as follows.

Equation 22 (for the boost configuration)**:**

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.39 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times (V_{LED} - 2 \times V_{IN\_MIN}) \times 3}$$

Equation 23 (for SEPIC and coupled-inductor configurations)**:**

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.39 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times (V_{LED} - V_{IN\_MIN}) \times 3}$$

where 0.39 is the minimum value of the peak current-sense threshold. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold of 0.39 is multiplied by 0.9 to take tolerances into account.

Output Capacitor Selection

For all three converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across the constant-current sink outputs because the LED-string voltages are stable due to the constant current. For the MAX20444C, limit peak-to-peak output-voltage ripple to 200mV to get stable output current.

The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESR and ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming, the amount of ceramic capacitors on the output is usually minimized. In this case, an additional electrolytic or aluminum organic polymer capacitor can provide most of the bulk capacitance.

External Switching-MOSFET Selection

The external switching MOSFET should have a voltage rating sufficient to withstand the maximum boost output voltage, together with the rectifier diode drop and any possible overshoot due to ringing caused by parasitic inductance and capacitance. The recommended MOSFET VDS voltage rating is 30% higher than the sum of the maximum output voltage and the rectifier diode drop.

The continuous-drain current rating of the MOSFET (ID), when the case temperature is at the maximum operating ambient temperature, should be greater than that calculated as follows.

Equation 24:

$$ID_{RMS} = \left(\sqrt{IL_{AVG}^{2} \times D_{MAX}}\right) \times 1.3$$

The MOSFET dissipates power due to both switching losses and conduction losses. Use the following equation to calculate the conduction losses in the MOSFET.

Equation 25:

$$P_{COND} = IL^{2}_{AVG} \times D_{MAX} \times R_{DS(ON)}$$

where $R_{DS(ON)}$ is the on-state drain-to-source resistance of the MOSFET. Use the following equation to calculate the switching losses in the MOSFET.

Equation 26:

$$P_{SW} = \frac{IL_{AVG} \times V_{LED}^2 \times C_{GD} \times f_{SW}}{2} \times \left(\frac{1}{I_{GON}} + \frac{1}{I_{GOFF}} \right)$$

where IGON and IGOFF are the gate currents of the MOSFET in amperes when it is turned on and turned off, respectively. C_{GD} is the gate-to-drain MOSFET capacitance in farads.

Rectifier Diode Selection

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than that shown in Equation 27.

Equation 27:

$$IL_{AVG} \times (1 - D_{MAX}) \times 1.2$$

Feedback Compensation

During normal operation, the feedback control loop regulates the minimum OUT_ voltage to fall within the window comparator limits of 0.78V and 1.03V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the previous boost output-voltage value for use during the next on cycle.

The switching converter small-signal-transfer function has a right-half plane (RHP) zero in the boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90º phase lag, which is difficult to compensate.

Equation 28 (worst-case RHP zero frequency (f_{ZRHP}) is calculated using)**:**

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED}}$$

Equation 29 (for SEPIC and coupled-inductor configurations)**:**

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED} \times D_{MAX}}$$

The standard way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determine the output pole frequency (f_{P1}) that is calculated for the boost configuration, as shown in the following equation.

Equation 30:

$$f_{P1} = \frac{I_{LED}}{\pi \times V_{LED} \times C_{OUT}}$$

Equation 31 (use this formula for SEPIC and coupled-inductor)**:**

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{\pi \times V_{LED} \times C_{OUT}}$$

Compensation components R_{COMP} and C_{COMP} perform two functions. C_{COMP} introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain. R_{COMP} flattens the gain of the error amplifier for frequencies above the zero formed by R_{COMP} and C_{COMP}. For compensation, this zero is placed at f_{P1} to provide a -20dB/decade slope for frequencies above f_{P1} to the combined modulator and compensator response.

The value of R_{COMP} needed to fix the total loop gain at f_{P1} so the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency is calculated for the boost configuration as follows.

Equation 32:

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX})}$$

Equation 33 (for SEPIC and coupled-inductor buck-boost configurations)**:**

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP} \times D_{MAX}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX})}$$

where:

- R_{COMP} = Compensation resistor in ohms
- A_{OVP} = BSTMON resistor-divider gain (a value << 1)
- R_{CS} = Current-sense resistor in ohms
- GM_{COMP} = Transconductance of the error amplifier (600µS)

The value of C_{COMP} is calculated as shown below.

Equation 34:

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{Z1} \times R_{COMP}}$$

where f_{Z1} is the compensation zero placed at 1/5 the crossover frequency, which is, in turn, set at 1/5 the f_{ZRHP}. If the output capacitors do not have low ESR, the ESR zero frequency could fall below the 0dB crossover frequency. An additional pole may be required to cancel out this zero placed at the same frequency. This can be added by connecting a capacitor from the COMP pin directly to GND with a value shown below.

Equation 35:

$$C_{PAR} = GM_{COMP} \times R_{ESR} \times C_{OUT}$$

where R_{ESR} is the capacitor ESR value and C_{OUT} is the output-capacitor value.

External Disconnect-MOSFET Selection

An external pMOSFET can be used to disconnect the boost output from the battery in the event of an output overload or short condition. In the case of the SEPIC or buck-boost, this protection is not necessary so there is no need for the pMOSFET. Connect the PGATE pin to ground in the case of the SEPIC and buck-boost. If it is necessary to have an output-short protection for the boost even at power-up, then the current through the pMOSFET (see the MAX20444 evaluation kit (EV kit) for a reference circuit) has to be sensed. Once the current-sense voltage exceeds a certain threshold, it should limit the input current to the programmed threshold. This threshold should be set at a sufficiently high level so it never trips at startup or under normal operating conditions. Check the safe operating area (SOA) of the pMOSFET so the current-limit-trip threshold and voltage on the MOSFET do not exceed the limits of the SOA curve of the pMOSFET at the highest operating temperature.

Connect a resistor from the PGATE output to the source of the pMOSFET, with the gate of the pMOSFET connected to PGATE. Calculate the resistor value using the following equation.

Equation 36:

$$R_{PGATE} = \frac{V_t}{170\mu A}$$

Where V_t is the minimum value of the pMOSFET gate threshold voltage. Choose an R_{PGATE} value larger than the value calculated using this equation. If the battery voltage can exceed 20V, it may be necessary to add an 18V zener diode across the gate source of the external pMOSFET to avoid damage to the gate.

V_{OUT} to OUT_ Bleed Resistors

The OUT_ pins have a leakage specification of 15µA (max) in cases where all OUT_ pins are shorted to 48V (see $I_{OUTLEAK}$ in the *Electrical Characteristics* table). This leakage current is dependent on the OUT_ voltage and is higher at higher voltages. Therefore, in cases where large numbers of LEDs are connected in series, a 100kΩ (or larger) bleed resistor can be placed in parallel with the LED string to prevent the OUT_ leakage current from very dimly turning on the LEDs, even when the DIM signal is low (see resistors R8–R11 in the *Typical Application Circuits*).

Thermal Considerations

The on-chip power dissipation of the MAX20444C comprises two main factors:

1) Current-sink power loss: $1.1V \times I_{LED}$
2) Device operating current power loss: $V_{IN} \times 15mA$
3) Gate-drive current for the external MOSFET: $V_{IN} \times Q_{GD} \times f_{SW}$, where Q_{GD} is the total gate charge of the selected MOSFET and f_{SW} is the switching frequency.

Calculate the total power dissipation by adding the two values calculated above. The junction temperature at the maximum ambient temperature can then be calculated as follows.

Equation 37:

$$T_J = T_A + P_{TOT} \times \theta_{JA}$$

where T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the package (36°C/W on a four-layer board). Ensure that the junction temperature does not exceed +150°C.

As an example, consider an application with an operating voltage of 14V and a total output current of 600mA. The selected MOSFET has a total gate charge of 5°C and the switching frequency is 400kHz. The total power dissipation is as follows.

Equation 38:

$$P_{TOT} = 1.1 \times 0.4 + 14 \times 0.011 + 14 \times 5nC \times 400000 = 0.622W$$

and the maximum junction temperature at an ambient temperature of +85°C is shown below.

Equation 39:

$$T_J = 85 + 0.622 \times 36 = 107°C$$

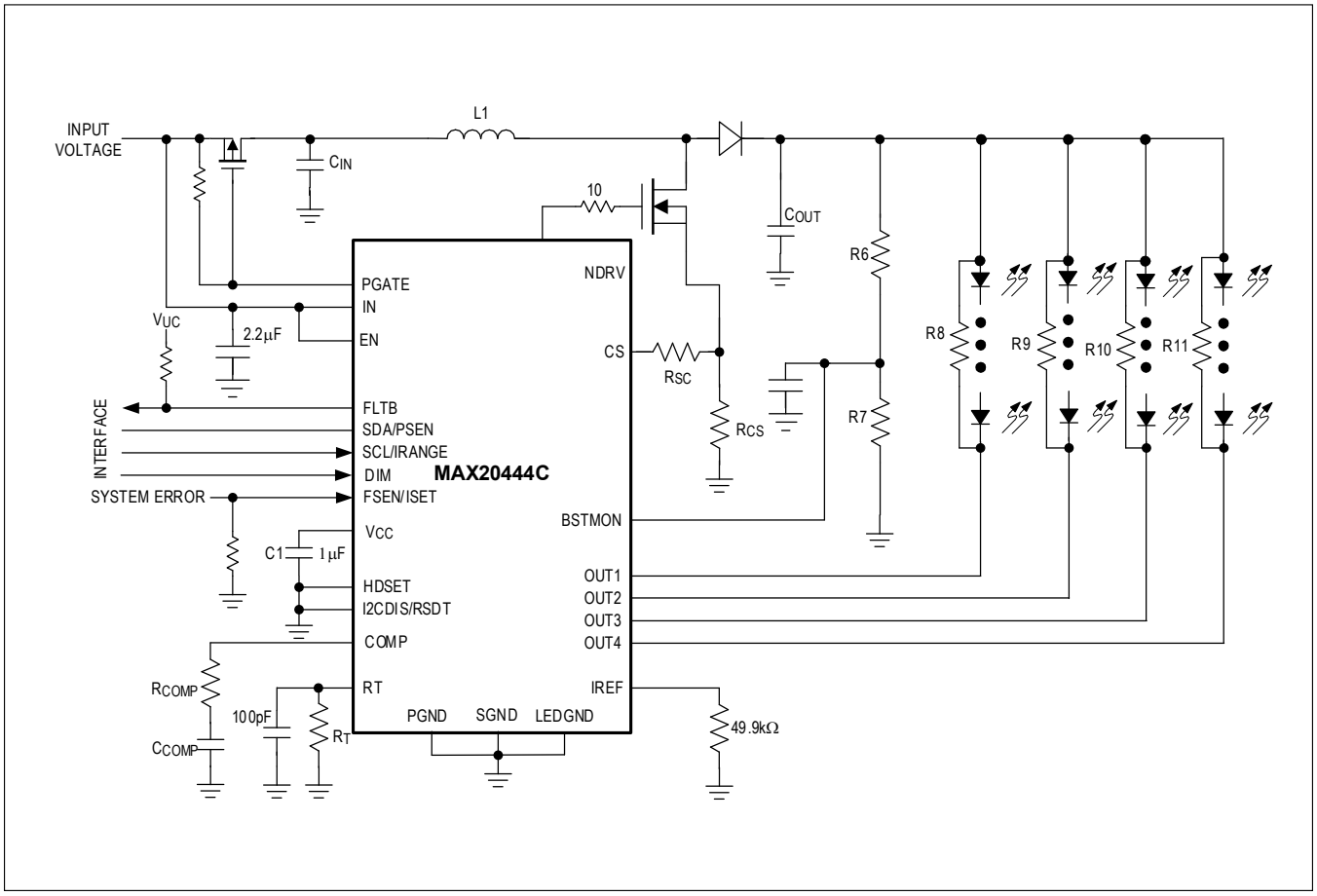
PCB Layout Considerations

LED driver circuits based on the MAX20444C use a high-frequency switching converter to generate the voltage for LED strings. Take proper care while laying out the circuit to ensure correct operation. The switching-converter portion of the circuit has nodes with very fast voltage changes that could lead to undesirable effects on the sensitive parts of the circuit. Follow the guidelines below to reduce noise as much as possible:

- Connect the bypass capacitor on V_{CC} as close as possible to the device and connect the capacitor ground to the analog ground plane using vias close to the capacitor terminal. Connect the GND of the device to the analog ground plane using a via placed close to GND. Lay the analog ground plane on the inner layer, preferably next to the top layer. Use the analog ground plane to cover the entire area under critical signal components for the power converter.
- Have a power-ground plane for the switching-converter power circuit under the power components (i.e., input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power-ground plane closest to PGND. Connect all other ground connections to the power ground plane using vias placed close to the terminals.
- There are two loops in the power circuit that carry high-frequency switching currents. One loop is when the MOSFET is on (from the input filter capacitor positive terminal, through the inductor, the internal MOSFET and the current-sense resistor, to the input capacitor negative terminal). The other loop is when the MOSFET is off (from the input capacitor positive terminal, through the inductor, the rectifier diode, output filter capacitor, to the input capacitor negative terminal). Analyze these two loops and make the loop areas as small as possible. Wherever possible, have a return path on the power ground plane for the switching currents on the top layer copper traces, or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also reduces radiation during switching.
- Connect the power-ground plane for the constant-current LED-driver portion of the circuit to LEDGND as close as possible to the device. Connect GND to PGND at the same point.
- Add a small bypass capacitor (22pF to 47pF) to the BSTMON input. Place the capacitor as close as possible to the pin to suppress high-frequency noise.
- Boost output voltage for the LED strings should be taken directly from the output capacitors and not from the boost diode anode.
- Input and output capacitors need good grounding with wide traces and multiple vias to the ground plane.
- Refer to the MAX20444 EV kit data sheet for an example layout.

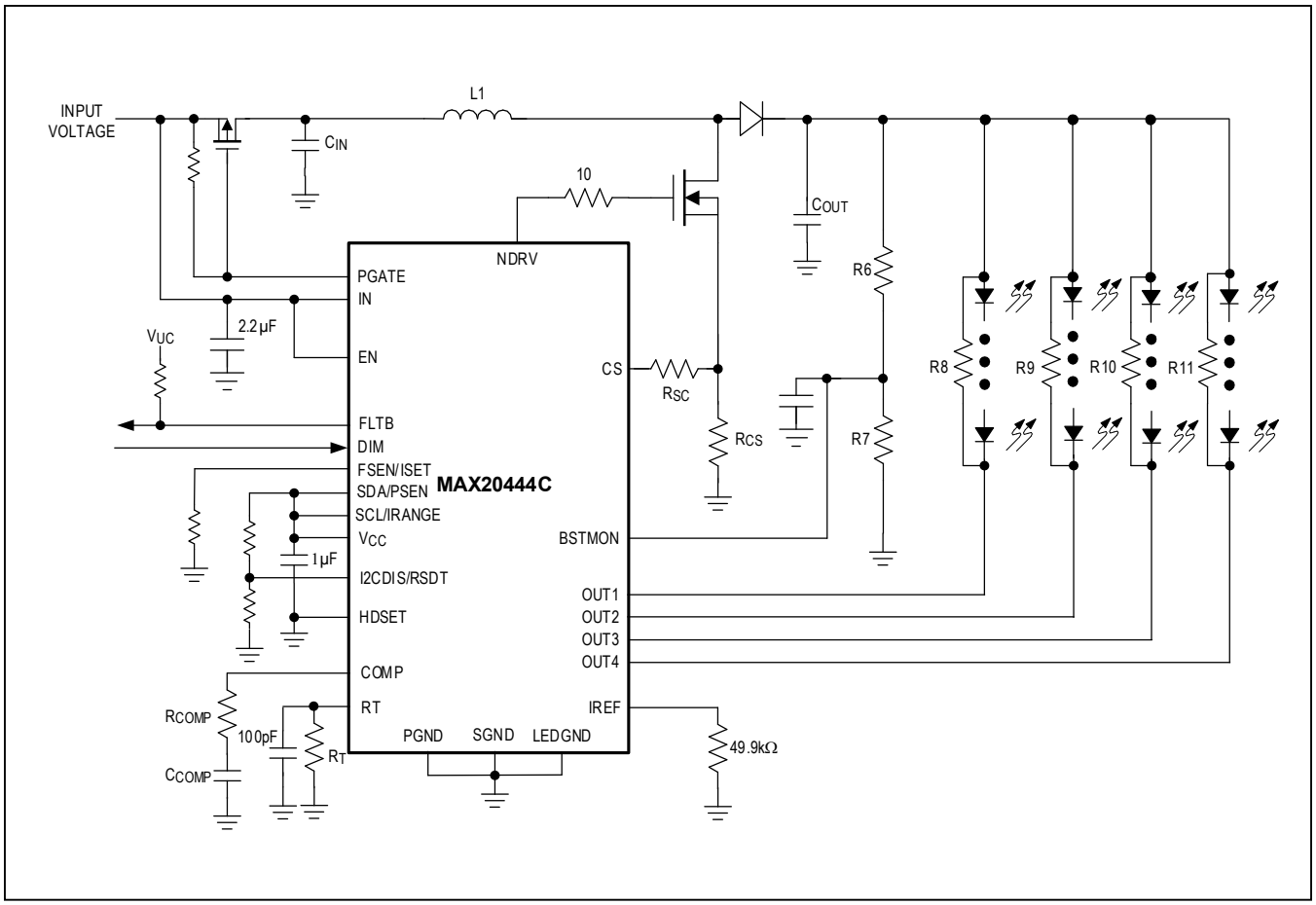
Typical Application Circuits

I²C Interface



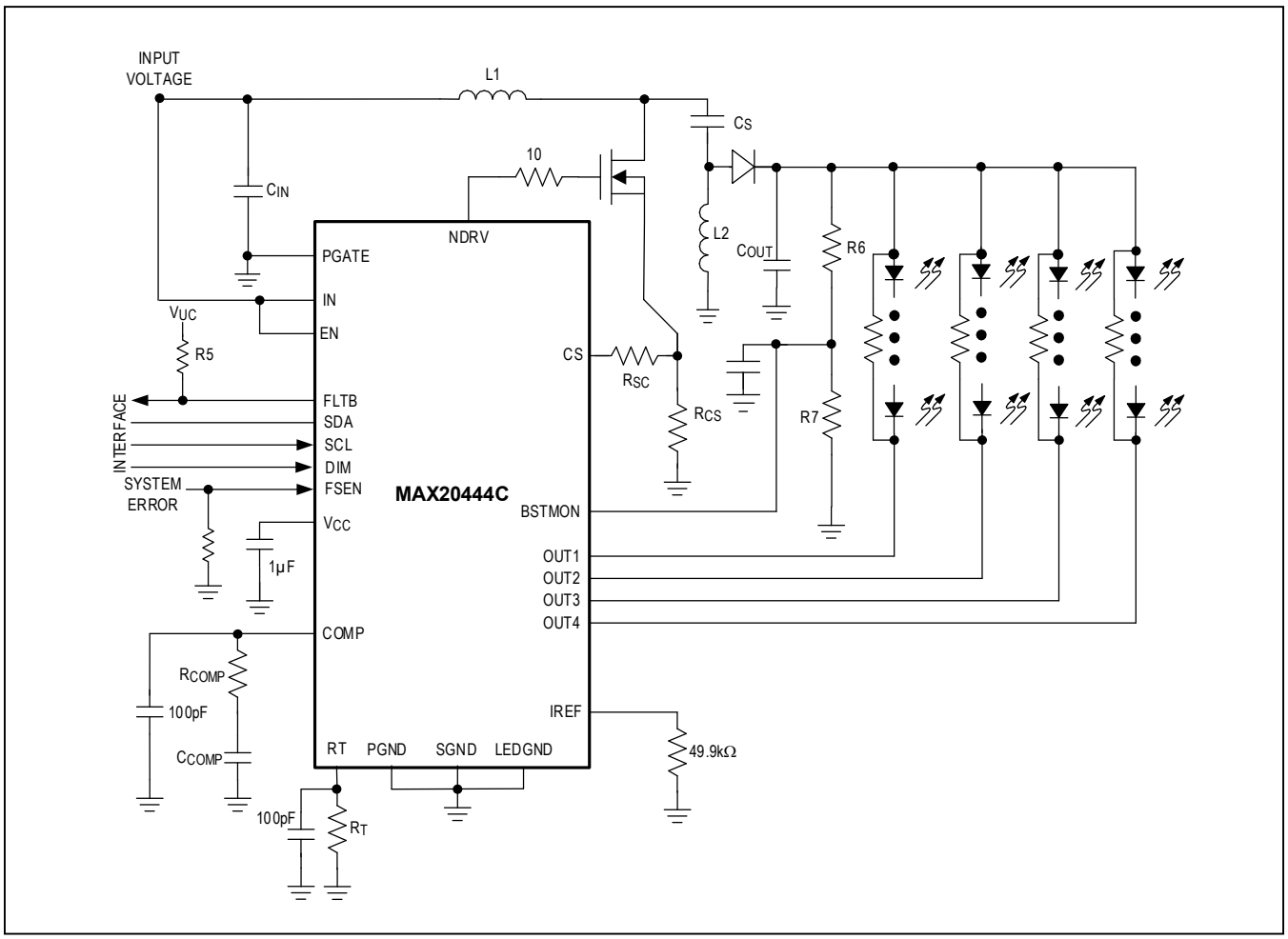
Typical Application Circuits (continued)

Stand-Alone Mode



Typical Application Circuits (continued)

SEPIC Topology



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20444CATG/V+**	-40°C to +125°C	24 TQFN-EP*
MAX20444CATG/V+T**	-40°C to +125°C	24 TQFN-EP*
MAX20444CATG/VY+	-40°C to +125°C	24 SWTQFN-EP*
MAX20444CATG/VY+T	-40°C to +125°C	24 SWTQFN-EP*

/V Denotes an AEC-Q100-qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape-and-reel package.
SW = Side-wettable package
**EP = Exposed pad.*
*** Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/21	Initial release	—

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