




1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

MAX2059

General Description

The MAX2059 high-linearity digital-variable-gain amplifier (DVGA) is designed to provide 56dB of total gain range and typical output IP3 and output P1dB levels of +31.8dBm and +18.4dBm, respectively. The device is ideal for a variety of applications, including single and multicarrier 1700MHz to 2200MHz DCS 1800/PCS 1900 EDGE, cdma2000®, WCDMA/UMTS, and TD-SCDMA base stations. The MAX2059 yields a high level of component integration, which includes two 5-bit digital attenuators, a two-stage driver amplifier, a loopback mixer, and a serial interface to control the attenuators.

The MAX2059 is pin compatible with the MAX2058 700MHz to 1200MHz DVGA, facilitating an easy design-in for applications where a common PC board layout is used for both frequency bands.

The MAX2059 is available in a 40-pin thin QFN package with an exposed paddle. Electrical performance is guaranteed over a -40°C to +85°C temperature range.

Applications

DCS 1800/PCS 1900 EDGE Base-Station Transmitters and Power Amplifiers
 cdmaOne™ and cdma2000 Base-Station Transmitters and Power Amplifiers
 WCDMA, TD-SCDMA, and Other 3G Base-Station Transmitters and Power Amplifiers
 Transmitter Gain Control
 Receiver Gain Control
 Broadband Systems
 Automatic Test Equipment
 Digital and Spread-Spectrum Communication Systems
 Microwave Terrestrial Links

cdma2000 is a registered trademark of Telecommunications Industry Association.
 cdmaOne is a trademark of CDMA Development Group.
 SPI is a trademark of Motorola, Inc.
 MICROWIRE is a trademark of National Semiconductor Corp.

Features

- ◆ +31.8dBm Typical Output IP3
- ◆ +18.4dBm Typical Output 1dB Compression Point
- ◆ 1700MHz to 2200MHz RF Frequency Range
- ◆ 700MHz to 1200MHz RF Frequency Range (MAX2058)
- ◆ 10.9dB Typical Small-Signal Gain
- ◆ Includes Two Independent 5-Bit Digital Attenuator Stages, Yielding 56dB of Total Gain-Control Range with 1dB Steps
- ◆ 3-Wire SPI™/MICROWIRE™ Compatible
- ◆ Integrated Loopback Mixer for Tx/Rx Self-Diagnostics
- ◆ +5V Single-Supply Operation
- ◆ External Current-Setting Resistors for Scalable Device Power
- ◆ Lead-Free Package Available

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|--------------|----------------|--------------------------------|----------|
| MAX2059ETL | -40°C to +85°C | 40 Thin QFN-EP* (6mm x 6mm) | T4066-3 |
| MAX2059ETL-T | -40°C to +85°C | 40 Thin QFN-EP* (6mm x 6mm) | T4066-3 |
| MAX2059ETL+ | -40°C to +85°C | 40 Thin QFN-EP* (6mm x 6mm) | T4066-3 |
| MAX2059ETL+T | -40°C to +85°C | 40 Thin QFN-EP* (6mm x 6mm) | T4066-3 |

*EP = Exposed paddle.

+Denotes lead-free package.

T = Tape-and-reel.

Pin Configuration/Functional Diagram appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| V _{CC} to GND | -0.3V to +5.5V |
| RSET1, RSET2 | +1.2V to +4.0V |
| LBBIAS | (V _{CC} - 1.5V) to +5.5V |
| LB_EN, DATA, $\overline{\text{CS}}$, CLK | -0.3V to (V _{CC} + 0.3V) |
| ATTEN_INA, ATTEN_INB, ATTEN_OUTA, ATTEN_OUTB | |
| Input Power | +24dBm |
| AMPIN, Differential LO Input Power | +12dBm |
| Continuous Power Dissipation (T _A = +70°C) | |
| 40-Pin TQFN (derated 26.3mW/°C above +70°C) |2100mW |

| | |
|--------------------------------------|-----------------|
| Operating Temperature Range (Note A) | -40°C to +85°C |
| Junction Temperature | +150°C |
| θ_{JC} | 10°C/W |
| θ_{JA} | 38°C/W |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

Note A: T_C is the temperature on the exposed paddle of the package.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2059 Typical Application Circuit, V_{CC} = +4.75V to +5.25V, R1 = 1.2k Ω , R2 = 2k Ω , R3 = 2k Ω , T_C = -40°C to +85°C. Typical values are at V_{CC} = +5.0V and T_C = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------|--|------|------|------|---------|
| Supply Voltage | V _{CC} | Reference to V _{CC} , VCCLB, VCCLOGIC, VCCBIAS1, VCCBIAS2, VCCAMP | 4.75 | 5.0 | 5.25 | V |
| Total Supply Current | I _{CC} | LB mixer disabled (LB_EN = 1) | | 189 | 241 | mA |
| | | LB mixer enabled (LB_EN = 0) | | 217 | 275 | |
| LOGIC INPUTS (DATA, $\overline{\text{CS}}$, CLK, LB_EN) | | | | | | |
| Input High Voltage | V _{IH} | | 2.4 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Input Current with Logic-High | I _{IH} | | | 0.01 | | μ A |
| Input Current with Logic-Low | I _{IL} | | | 0.01 | | μ A |

AC ELECTRICAL CHARACTERISTICS

(MAX2059 Typical Application Circuit, V_{CC} = +4.75V to +5.25V, digital attenuators set for maximum gain, 1700MHz \leq f_{RF} \leq 2200MHz, 40MHz \leq f_{LO} \leq 100MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, P_{IN} = 0dBm, f_{RF} = 1850MHz, P_{LO} = -6dBm, f_{LO} = 95MHz, f_{LBOUT} = f_{RF} - f_{LO}, and T_C = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------------|------------------|--|---------------------------------|--------|------|-------|
| RF Frequency (Note 2) | | MAX2058 | 700 | | 1200 | MHz |
| | | MAX2059 | 1700 | | 2200 | |
| Small-Signal Gain | A _V | f _{RF} = 1850MHz, T _C = +25°C | 8.0 | 10.9 | 13.3 | dB |
| Gain Variation vs. Temperature | | All attenuation settings | T _C = -40°C to +25°C | -0.024 | | dB/°C |
| | | | T _C = +25°C to +85°C | -0.032 | | |
| Output Power | P _{OUT} | P _{IN} = 0dBm, f _{RF} = 1850MHz, T _C = +25°C | 8.0 | 10.9 | 13.3 | dBm |
| Output Power Flatness | | P _{IN} = 0dBm | 1800MHz to 2000MHz | -0.77 | | dB |
| | | | 2000MHz to 2200MHz | -2 | | |
| Attenuation Range | | | | 56 | | dB |
| Output 3rd-Order Intercept Point | OIP3 | Two tones: f _{RF1} = 1850MHz, f _{RF2} = 1851MHz, P _{OUT1} = P _{OUT2} = +5dBm | | 31.8 | | dBm |

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2059 *Typical Application Circuit*, $V_{CC} = +4.75V$ to $+5.25V$, digital attenuators set for maximum gain, $1700MHz \leq f_{RF} \leq 2200MHz$, $40MHz \leq f_{LO} \leq 100MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = 5.0V$, $P_{IN} = 0dBm$, $f_{RF} = 1850MHz$, $P_{LO} = -6dBm$, $f_{LO} = 95MHz$, $f_{LBOUT} = f_{RF} - f_{LO}$, and $T_C = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|--|---------------|----------------|-----|-------|
| Output -1dB Compression Point | OP _{1dB} | (Note 3) | | 18.4 | | dBm |
| RMS Error Vector Magnitude | EVM | P _{OUT} = +12dBm, EDGE modulation | | 0.5 | | % |
| Spurious Emissions in 30kHz Bandwidth | | P _{OUT} = +12dBm, EDGE modulation (Note 4) | 200kHz offset | -39.1 | | dBc |
| | | | 400kHz offset | -72.5 | | |
| | | | 600kHz offset | -83.1 | | |
| | | | 1.2MHz offset | -85.7 | | |
| Noise Figure | NF | | | 8.1 | | dB |
| Input Return Loss | | 50Ω source, minimum attenuation setting | | 19 | | dB |
| Output Return Loss | | 50Ω load, minimum attenuation setting | | 24 | | dB |
| 5-BIT DIGITAL ATTENUATORS | | | | | | |
| Insertion Loss | | Attenuator measured separately Z _S = Z _L = 50Ω | | 5 | | dB |
| Input 3rd-Order Intercept Point | IIP3 | Attenuator measured separately Z _S = Z _L = 50Ω, two tones: f _{RF1} = 1850MHz, f _{RF2} = 1851MHz, P _{IN1} = P _{IN2} = +5dBm | | 40 | | dBm |
| Control Range | | (Note 5) | | 28 | | dB |
| Attenuation Step Size Variation vs. Frequency | | 1800MHz to 2000MHz | | ±0.17 | | dB |
| | | 2000MHz to 2200MHz | | ±0.29 | | |
| Attenuation Variation vs. Temperature | | 1800MHz to 2200MHz, T _C = -40°C to +25°C | | ±0.011 | | dB/°C |
| | | 1800MHz to 2200MHz, T _C = +25°C to +85°C | | ±0.023 | | |
| Step Size | | | | 1 | | dB |
| Relative Step Accuracy | | 1800MHz to 2000MHz, all states represented. For steps 0–23dB, accuracy is significantly improved. See <i>Typical Operating Characteristics</i> . | | +0.53 -0.97 | | dB |
| Absolute Step Accuracy | | 1800MHz to 2000MHz, all states represented. For steps 0–23dB, accuracy is significantly improved. See <i>Typical Operating Characteristics</i> . | | -3.5 +0.3 | | dB |
| Spurious Emissions in 300kHz Bandwidth | | No RF input, attenuator A stepped from 0 to 2dB, 7dB to 9dB, 15dB to 17dB, 0 to 31dB, 31dB to 0dB, with attenuator B at 0dB; attenuator B stepped from 0 to 2dB, 7dB to 9dB, 15dB to 17dB, 0 to 31dB, 31dB to 0dB, with attenuator A at 0dB (Note 6) | | -89 | | dBm |

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2059 *Typical Application Circuit*, $V_{CC} = +4.75V$ to $+5.25V$, digital attenuators set for maximum gain, $1700MHz \leq f_{RF} \leq 2200MHz$, $40MHz \leq f_{LO} \leq 100MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = 5.0V$, $P_{IN} = 0dBm$, $f_{RF} = 1850MHz$, $P_{LO} = -6dBm$, $f_{LO} = 95MHz$, $f_{LBOUT} = f_{RF} - f_{LO}$, and $T_C = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|---|--------------------|-------|-----------|---------|
| Switching Speed | | From chip select transitioning high to the output settling to within 1dB of steady state output | | 0.3 | | μs |
| LOOPBACK MIXER | | | | | | |
| LO Frequency | f_{LO} | (Note 2) | 40 | | 100 | MHz |
| LO Input Power | P_{LO} | | | -6 | 0 | dBm |
| Output Power | | $P_{IN} = +5dBm$, $f_{RF} = 1850MHz$, $T_C = +25^\circ C$ (Note 7) | -15.4 | -12.6 | -9.6 | dBm |
| Gain Accuracy | | $P_{IN} = +5dBm$, $T_C = -40^\circ C$ to $+85^\circ C$ | 1800MHz to 2000MHz | | ± 2.2 | dB |
| | | | 2000MHz to 2200MHz | | ± 2.2 | |
| Output 3rd-Order Intercept Point | OIP3 | Two tones: $f_{RF1} = 1850MHz$, $f_{RF2} = 1850.2MHz$, $P_{IN1} = P_{IN2} = +2dBm$, $T_C = +25^\circ C$ | | 6.2 | | dBm |
| Output Noise Floor | | $P_{IN} = +5dBm$ | | -137 | | dBc/Hz |
| ON/OFF Switching Time | | LB_EN enable time | | 0.12 | | μs |
| | | LB_EN disable time | | 0.12 | | |
| LBOU to ATTEN_OUTB Isolation | | Mixer enabled, attenuators A and B both set to 31dB, $P_{IN} = +5dBm$ | | 55 | | dB |
| ATTEN_OUTB to LBOU Isolation | | Mixer disabled, $P_{IN} = 0dBm$ | | 50 | | dB |
| Output Return Loss | | Mixer enabled, 50Ω load | | 20 | | dB |
| | | Mixer disabled, 50Ω load | | 13 | | |
| LO Port Return Loss | | 50Ω source | | 28 | | dB |
| SERIAL PERIPHERAL INTERFACE (SPI) | | | | | | |
| Maximum Clock Speed | | | | 38 | | MHz |
| Data to Clock Setup Time | t_{CS} | | | 1 | | ns |
| Data to Clock Hold Time | t_{CH} | | | 9 | | ns |
| Clock to \overline{CS} Setup Time | t_{ES} | | | 4 | | ns |
| \overline{CS} Positive Pulse Width | t_{EW} | | | 18 | | ns |
| \overline{CS} Negative Pulse Width | t_{EWN} | | | 24 | | ns |
| Clock Pulse Width | t_{CW} | | | 13 | | ns |

Note 1: All limits include external component losses. Output measurements taken at RFOU or LBOU ports of the *Typical Application Circuit*.

Note 2: Operating outside this range is possible, but with degraded performance of some parameters.

Note 3: Compression point characterized. It is advisable not to continuously operate the VGA RF input above +15dBm.

Note 4: Input RF source contribution to spurious emissions (Agilent ESG 4435B, PSA E4443A): 200kHz = -39.2dBc, 400kHz = -73.5dBc, 600kHz = -83.2dBc, 1.2MHz = -85.7dBc

Note 5: See the *Applications Information* section regarding effective attenuation range.

Note 6: No SPI clock input applied.

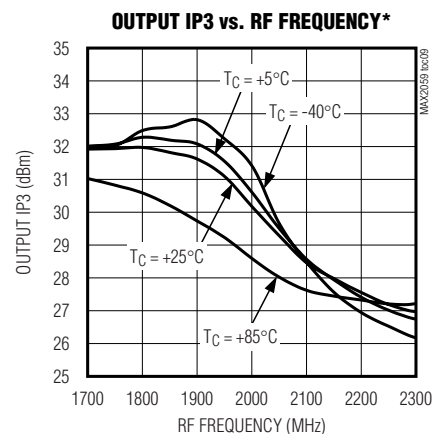
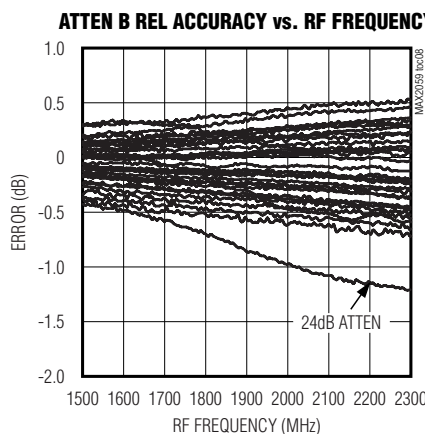
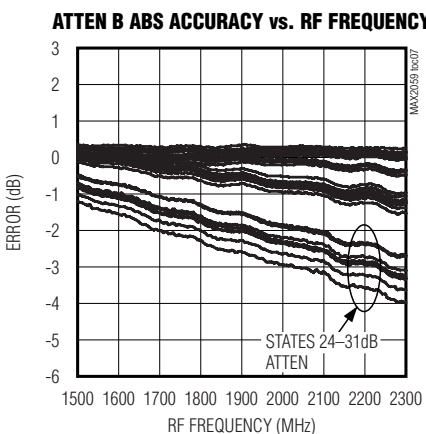
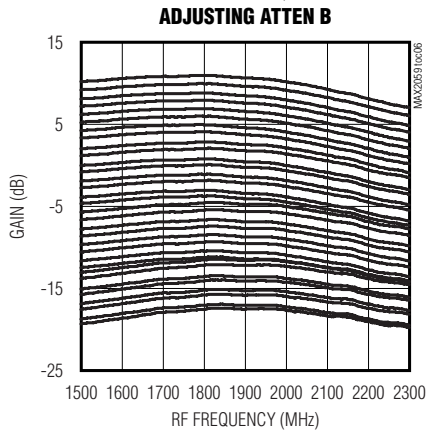
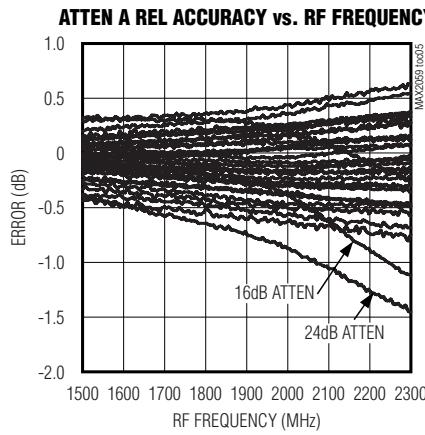
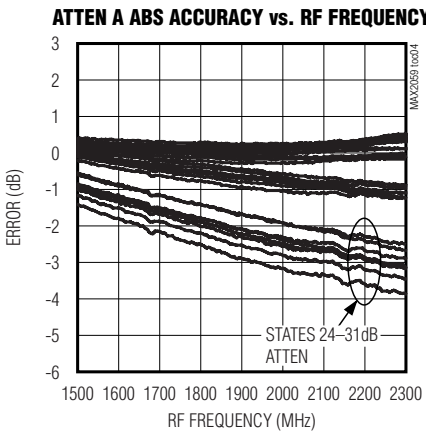
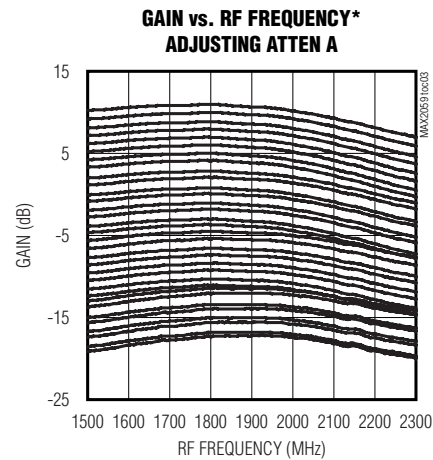
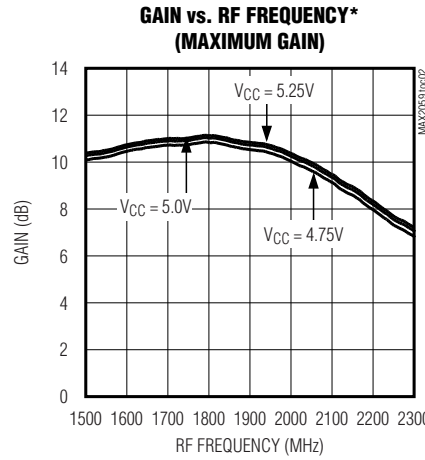
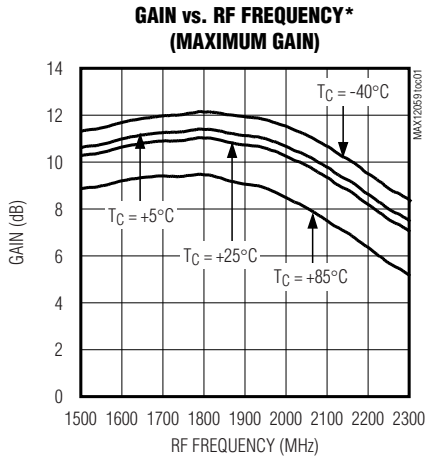
Note 7: Guaranteed by design and characterization.

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Typical Operating Characteristics

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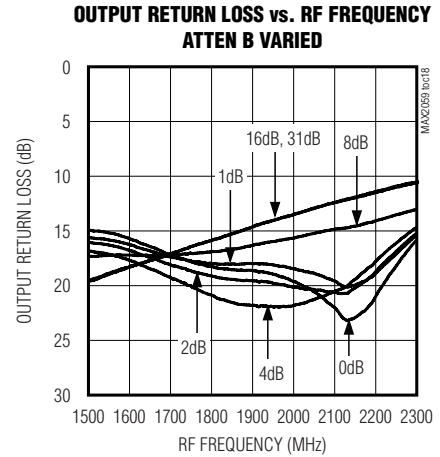
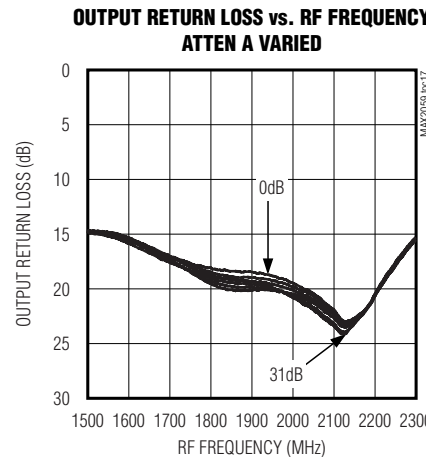
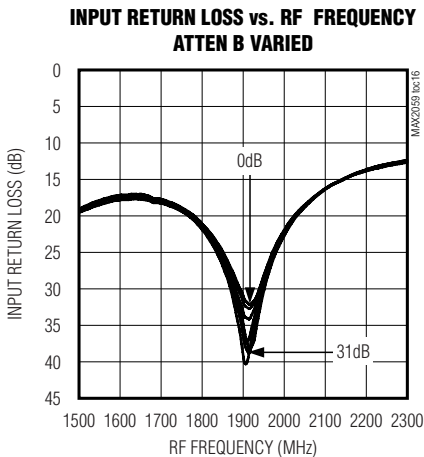
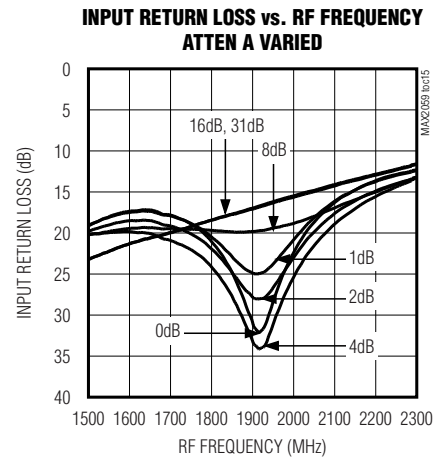
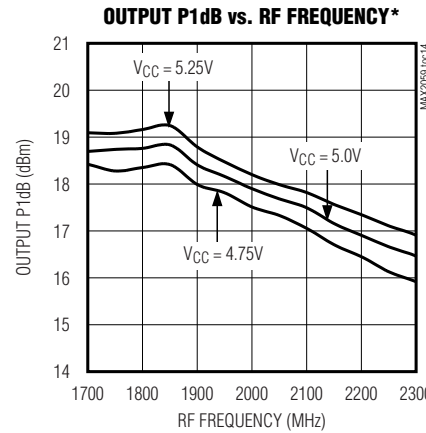
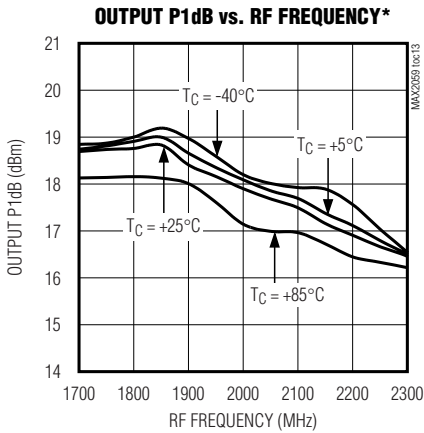
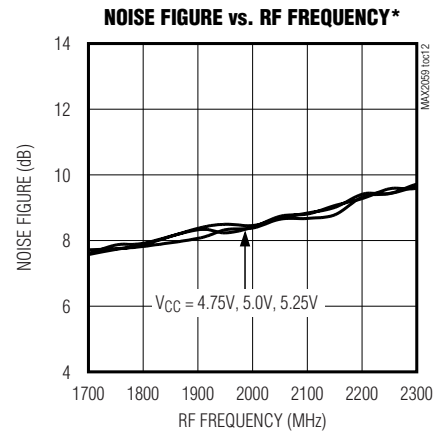
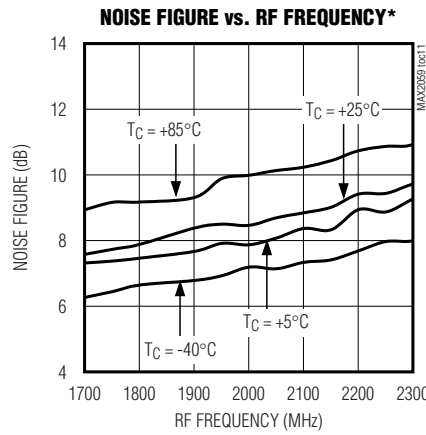
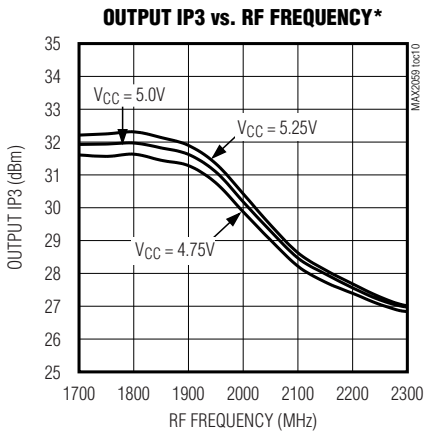


*Off-chip tuning can improve performance for applications beyond 2200MHz. Contact factory for details.

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Typical Operating Characteristics (continued)

(MAX2059 Typical Application Circuit, $V_{CC} = +4.75V$ to $+5.25V$, digital attenuators set for maximum gain, $1700MHz \leq f_{RF} \leq 2200MHz$, $40MHz \leq f_{LO} \leq 100MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = 5.0V$, $P_{IN} = 0dBm$, $f_{RF} = 1850MHz$, $f_{LO} = 95MHz$, $f_{LBOUT} = f_{RF} - f_{LO}$, and $T_C = +25^\circ C$, unless otherwise noted.)



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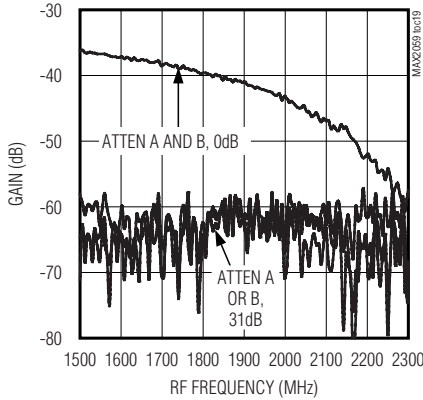
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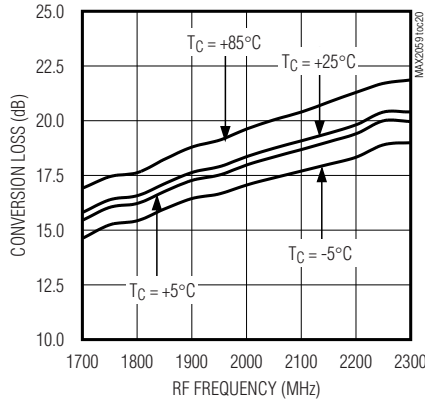
Typical Operating Characteristics (continued)

(MAX2059 Typical Application Circuit, $V_{CC} = +4.75V$ to $+5.25V$, digital attenuators set for maximum gain, $1700MHz \leq f_{RF} \leq 2200MHz$, $40MHz \leq f_{LO} \leq 100MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = 5.0V$, $P_{IN} = 0dBm$, $f_{RF} = 1850MHz$, $f_{LO} = 95MHz$, $f_{LBOUT} = f_{RF} - f_{LO}$, and $T_C = +25^\circ C$, unless otherwise noted.)

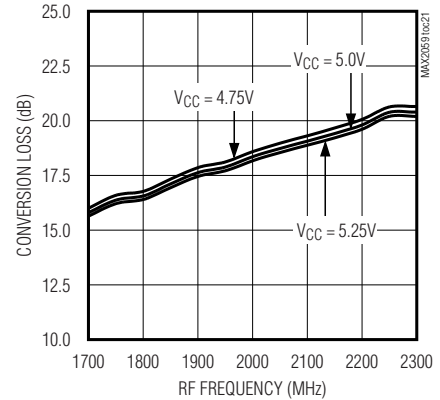
REVERSE GAIN vs. RF FREQUENCY
ADJUSTING ATTEN A AND B



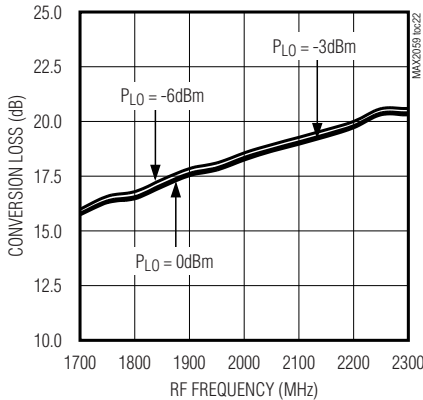
MIXER CONV LOSS vs. RF FREQUENCY



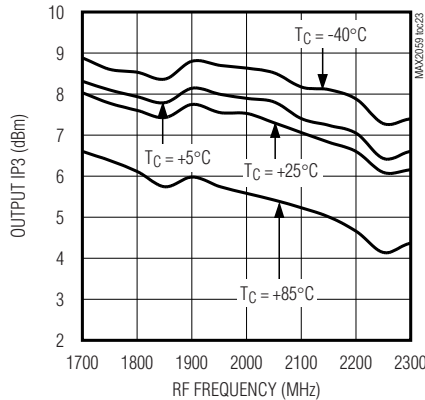
MIXER CONV LOSS vs. RF FREQUENCY



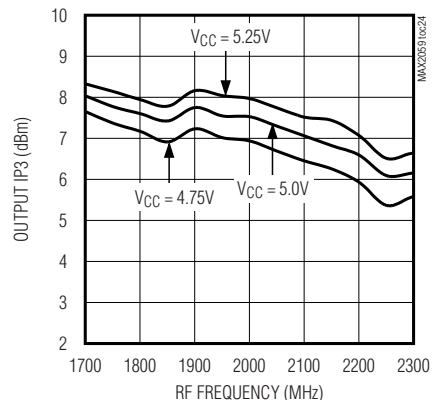
MIXER CONV LOSS vs. RF FREQUENCY



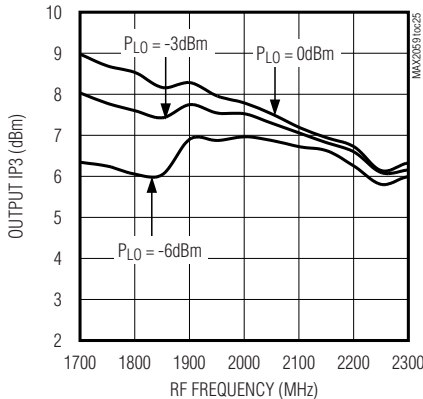
MIXER OUTPUT IP3 vs. RF FREQUENCY



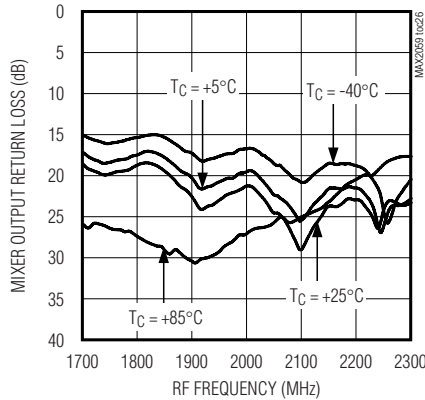
MIXER OUTPUT IP3 vs. RF FREQUENCY



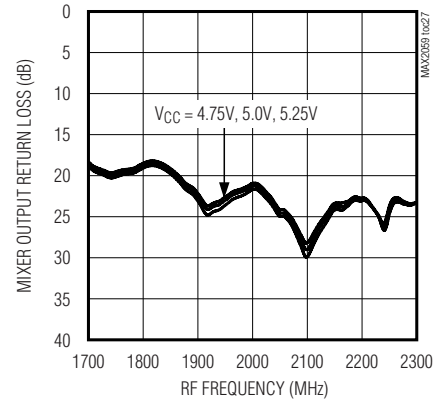
MIXER OUTPUT IP3 vs. RF FREQUENCY



MIXER OUTPUT RETURN LOSS vs. RF FREQUENCY (MIXER ENABLED)



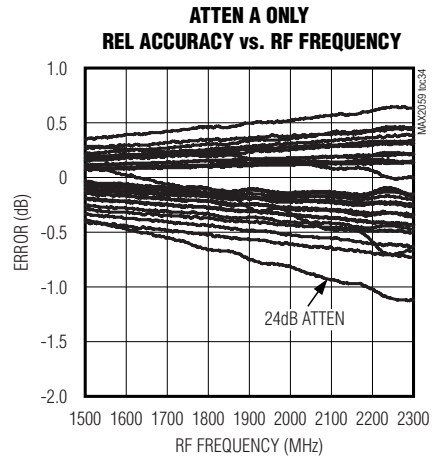
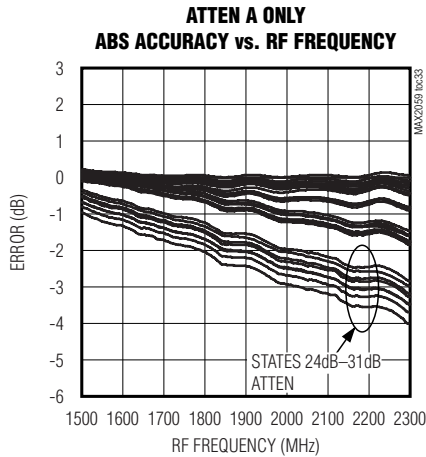
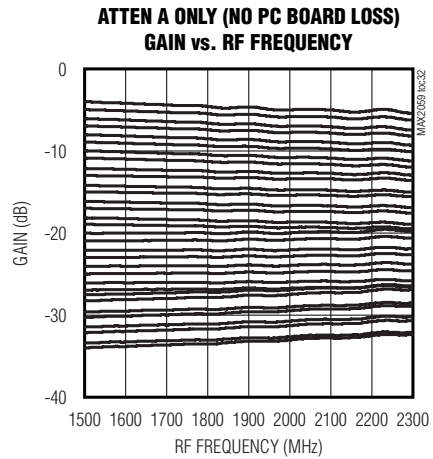
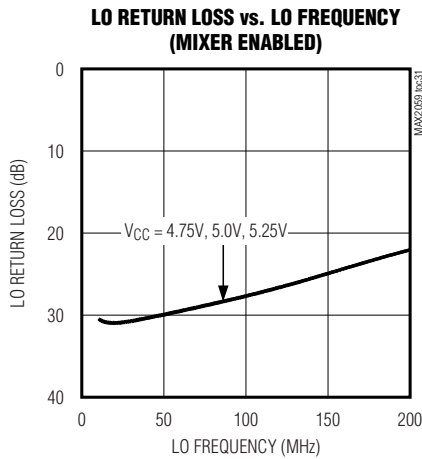
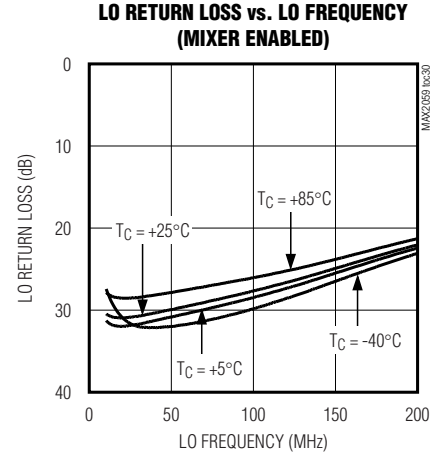
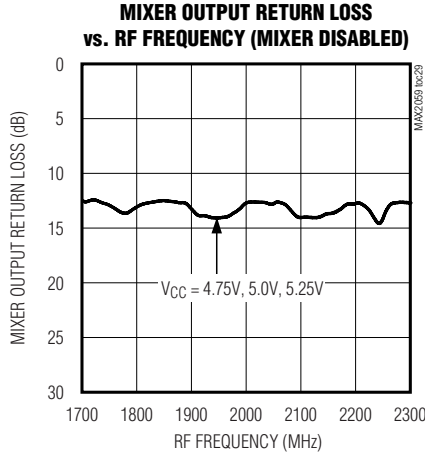
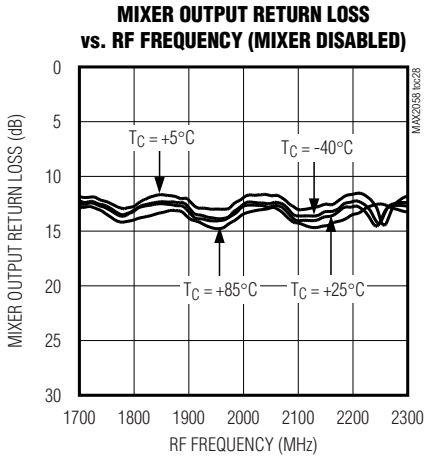
MIXER OUTPUT RETURN LOSS vs. RF FREQUENCY (MIXER ENABLED)



1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

Typical Operating Characteristics (continued)

(MAX2059 Typical Application Circuit, $V_{CC} = +4.75V$ to $+5.25V$, digital attenuators set for maximum gain, $1700MHz \leq f_{RF} \leq 2200MHz$, $40MHz \leq f_{LO} \leq 100MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = 5.0V$, $P_{IN} = 0dBm$, $f_{RF} = 1850MHz$, $f_{LO} = 95MHz$, $f_{LBOUT} = f_{RF} - f_{LO}$, and $T_C = +25^\circ C$, unless otherwise noted.)

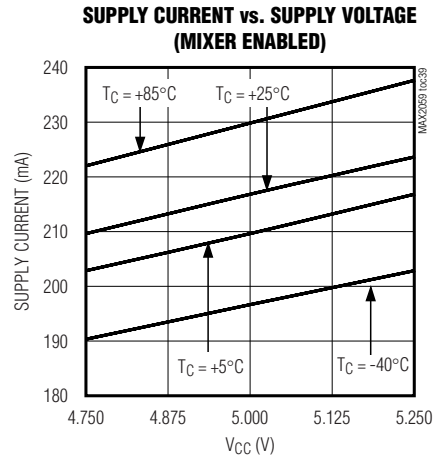
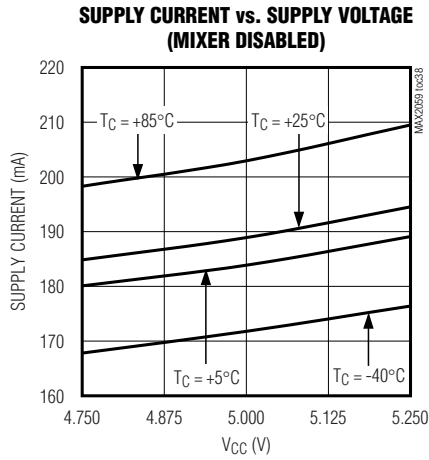
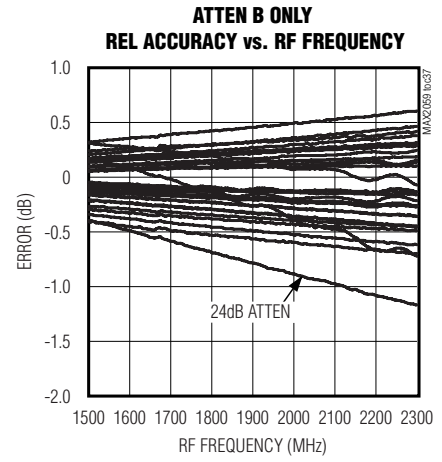
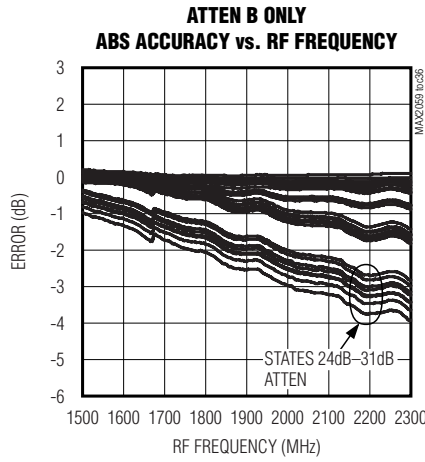
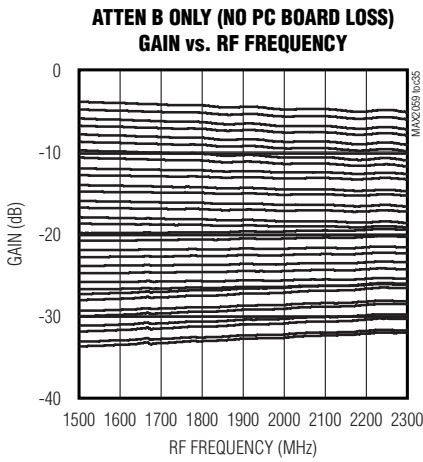


1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

MAX2059

Typical Operating Characteristics (continued)

(MAX2059 Typical Application Circuit, $V_{CC} = +4.75V$ to $+5.25V$, digital attenuators set for maximum gain, $1700MHz \leq f_{RF} \leq 2200MHz$, $40MHz \leq f_{LO} \leq 100MHz$, $T_C = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = 5.0V$, $P_{IN} = 0dBm$, $f_{RF} = 1850MHz$, $f_{LO} = 95MHz$, $f_{LBOUT} = f_{RF} - f_{LO}$, and $T_C = +25^\circ C$, unless otherwise noted.)



1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

Pin Description

| PIN | NAME | FUNCTION |
|---|-----------------|--|
| 1 | LO+ | Loopback Mixer Local Oscillator Positive Input |
| 2 | LO- | Loopback Mixer Local Oscillator Negative Input |
| 3 | VCCLB | Loopback Mixer Supply Voltage. +5V supply for the internal loopback mixer. Bypass to GND with 22pF and 0.1μF capacitors as close as possible to the pin. |
| 4 | LBOU | Loopback Mixer RF Output. Internally matched to 50Ω. AC-couple with a capacitor. |
| 5 | LB_EN | Loopback Mixer Logic Input. Set to logic-low 0 to enable the mixer. Set to logic-high 1 to disable the mixer. |
| 6 | DATA | SPI Digital Data Input |
| 7 | CLK | SPI Clock Input |
| 8 | \overline{CS} | SPI Chip-Select Input |
| 9 | VCCLOGIC | Logic Supply Voltage. +5V supply for the internal logic circuitry. Bypass to GND with 22pF and 0.1μF capacitors as close as possible to the pin. |
| 10, 11, 13, 14, 16, 17, 19, 22, 24, 25, 26, 30, 32, 34, 35, 37, 38 | GND | Ground |
| 12 | ATTEN_OUTB | Attenuator B Output. Internally matched to 50Ω. |
| 15 | VCC | Attenuator B Supply. +5V supply for attenuator B. Bypass to GND with 22pF and 0.01μF capacitors as close as possible to the pin. |
| 18 | ATTEN_INB | Attenuator B Input. Internally matched to 50Ω. |
| 20 | RSET2 | Output Amplifier Bias-Current-Setting Resistor. Sets the bias current for the output amplifier stage. Connect a 2kΩ resistor to ground. |
| 21 | VCCBIAS2 | Bias Circuit Supply Voltage. +5V supply for the internal bias circuitry. Bypass to GND with 1000pF and 0.1μF capacitors as close as possible to the pin. |
| 23 | AMPOUT | RF Amplifier Output. Internally matched to 50Ω. |
| 27 | VCCAMP | RF Amplifier Supply Voltage. +5V supply for the RF amplifier. Bypass to GND with 1000pF and 0.1μF capacitors as close as possible to the pin. |
| 28 | AMPIN | RF Amplifier Input. Internally matched to 50Ω. |
| 29 | VCCBIAS1 | Bias Circuit Supply Voltage. +5V supply for the internal bias circuitry. Bypass to GND with 1000pF and 0.1μF capacitors as close as possible to the pin. |
| 31 | RSET1 | Input Amplifier Bias-Current-Setting Resistor. Sets the bias current for the input amplifier stage. Connect a 1.2kΩ resistor to ground. |
| 33 | ATTEN_OUTA | Attenuator A Output. Internally matched to 50Ω. |
| 36 | VCC | Attenuator A Supply Voltage. +5V supply for attenuator A. Bypass to GND with 22pF and 0.01μF capacitors as close as possible to the pin. |
| 39 | ATTEN_INA | Attenuator A Input. Internally matched to 50Ω. |
| 40 | LBBIAS | Loopback Mixer Bias-Current-Setting Resistor. Sets the bias current for the mixer. Connect a 2kΩ resistor to ground. |
| EP | EP | Exposed Ground Paddle. Solder the exposed paddle to GND using multiple vias. |

1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

Detailed Description

The MAX2059 high-linearity DVGA consists of two 5-bit digital attenuators, a fixed-gain two-stage driver amplifier, a loopback mixer, and a serial interface to control the attenuators. This high level of component integration makes the MAX2059 ideal for base-station transmitter applications. The MAX2059 is designed to operate in the 1700MHz to 2200MHz frequency range. The overall cascaded performance of the MAX2059 produces a typical 10.9dB gain, a +31.8dBm OIP3, an 18.4dBm OP1dB, and a total 56dB gain-control range.

5-Bit Attenuators

The MAX2059 integrates two 5-bit digital attenuators to achieve a high dynamic range. Each attenuator is programmed with a 3-wire SPI interface, with a total effective range of 28dB and step size of 1dB. See the *Applications Information* section and Table 1 for attenuator programming details. The attenuators can be used for both static and dynamic power control.

Table 1. Attenuator Programming

| ATTENUATOR A (5 MSBs) | ATTENUATOR B (5 LSBs) |
|-----------------------|-----------------------|
| Bit 9 = 16dB step | Bit 4 = 16dB step |
| Bit 8 = 8dB step | Bit 3 = 8dB step |
| Bit 7 = 4dB step | Bit 2 = 4dB step |
| Bit 6 = 2dB step | Bit 1 = 2dB step |
| Bit 5 = 1dB step | Bit 0 = 1dB step |

Note: Due to finite circuit isolation, the total effective range of each attenuator is limited to 28dB.

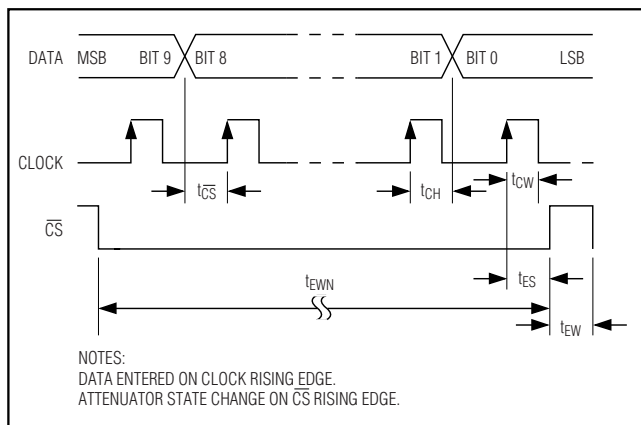


Figure 1. SPI Timing Diagram

Driver Amplifier

The MAX2059 includes a two-stage medium power amplifier with a fixed 18.5dB gain. The driver amplifier circuit is optimized for high linearity and medium output power capability for the 1800MHz to 2000MHz frequency range. The driver amplifier is intended to amplify a modulated signal and drive a high-power amplifier in base-station transmitters. In a typical application, the driver amplifier is cascaded in between the two digital attenuators. See the *Typical Application Circuit*.

The two-stage amplifier stage can be disabled for applications where only the digital attenuators and/or loopback mixer are used. To disable the two-stage amplifier, ground or leave unconnected the amplifier supplies VCCBIAS2, VCCAMP, VCCBIAS1, and also the inputs for setting the amplifier bias currents RSET1, RSET2. This reduces the supply current by approximately 187mA under typical conditions.

Loopback Mixer

The MAX2059 loopback mixer uses a double-balanced active architecture designed to operate with a 1700MHz to 2200MHz RF frequency range, and a 40MHz to 100MHz LO frequency range. The RF port of the mixer is connected internally (with an on-chip switch) to the input of the first attenuator stage. The mixer's IF port is matched for a single-ended 50Ω impedance, while the LO port requires a differential input impedance of 100Ω.

The loopback mixer facilitates a self-diagnostic mode for cellular transceivers, whereby the Tx band signal at the input of the mixer can be translated up or down to the corresponding Rx band. This translated signal can then be fed back to the radio's receiver for complete Tx/Rx loop diagnostics. The loopback mixer is enabled and disabled with LB_EN. Set LB_EN to a logic-low 0 to enable the mixer, set LB_EN to a logic-high 1 to disable the mixer.

The MAX2059 loopback mixer accepts a nominal -6dBm LO input power and exhibits a -12.6dBm output power and an output IP3 of 6.2dBm (PIN = +5dBm).

Applications Information

SPI Interface and Attenuator Settings

The two 5-bit attenuators are programmed with the 3-wire SPI/MICROWIRE-compatible serial interface using 10-bit words. Bit 9 of the 10-bit data is shifted in first, along with all remaining data bits, on the rising edge of the clock regardless of CS being high or low. Once all the data bits are shifted in, all will be sent to the attenuators on the rising edge of CS, thus changing the attenuation state. For standard SPI operation, pull CS low for the

1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

duration of a valid 10-bit data set (t_{EWN}). This \overline{CS} negative pulse width includes the setup time of the rising clock edge to \overline{CS} transitioning high (t_{ES}). See Figure 1.

The 5 MSBs of the 10-bit word program attenuator A, and the 5 LSBs of the 10-bit word program attenuator B. Each bit sets the attenuators to a corresponding attenuation level. For example, logic-low 0 for bit 5 and bit 0 of attenuator A and B, respectively, sets both attenuators at 1dB. 00000 configures both attenuators for maximum attenuation and 11111 sets for minimum attenuation. See Table 1 for programming details.

External Bias

Bias currents for the two-stage amplifier and the loopback mixer are set and optimized with external resistors. Resistor R1 (pin 31) sets the bias current for the input amplifier, R2 (pin 20) sets the bias current for the output amplifier, and R3 (pin 40) sets the bias for the loopback mixer. The external biasing resistor values can be increased for reduced current operation at the expense of performance. Contact the factory for details.

Board Layout

The pin configuration of the MAX2059 has been optimized to facilitate a very compact physical layout of the device and its associated discrete components.

The exposed paddle (EP) of the MAX2059's thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PC board on which the MAX2059 is mounted be designed to conduct heat

from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PC board, either directly or through an array of plated via holes.

Table 2. Component List Referring to the Typical Application Circuit

| COMPONENT | VALUE | DESCRIPTION |
|------------------------------------|---------------|--|
| C1, C4, C10, C13, C16 | 0.1 μ F | Microwave capacitors (0603) |
| C2, C3, C5, C8, C11, C14, C17, C24 | 22pF | Microwave capacitors (0402) |
| C6, C19 | 120pF | Microwave capacitors (0402) |
| C7, C18 | 0.01 μ F | Microwave capacitors (0402) |
| C9, C12, C15 | 1000pF | Microwave capacitors (0402) |
| C20, C21, C22 | 0.75pF | Microwave capacitors (0402) |
| C23 | 1pF | Microwave capacitor (0402) |
| R1 | 1.2k Ω | \pm 1% resistor (0402) |
| R2, R3 | 2.0k Ω | \pm 1% resistors (0402) |
| R4 | 110 Ω | \pm 1% resistor (0402) |
| T1 | 2:1 | RF transformer (100:50) Mini-Circuits TC2-1T |
| U1 | — | MAX2059 |

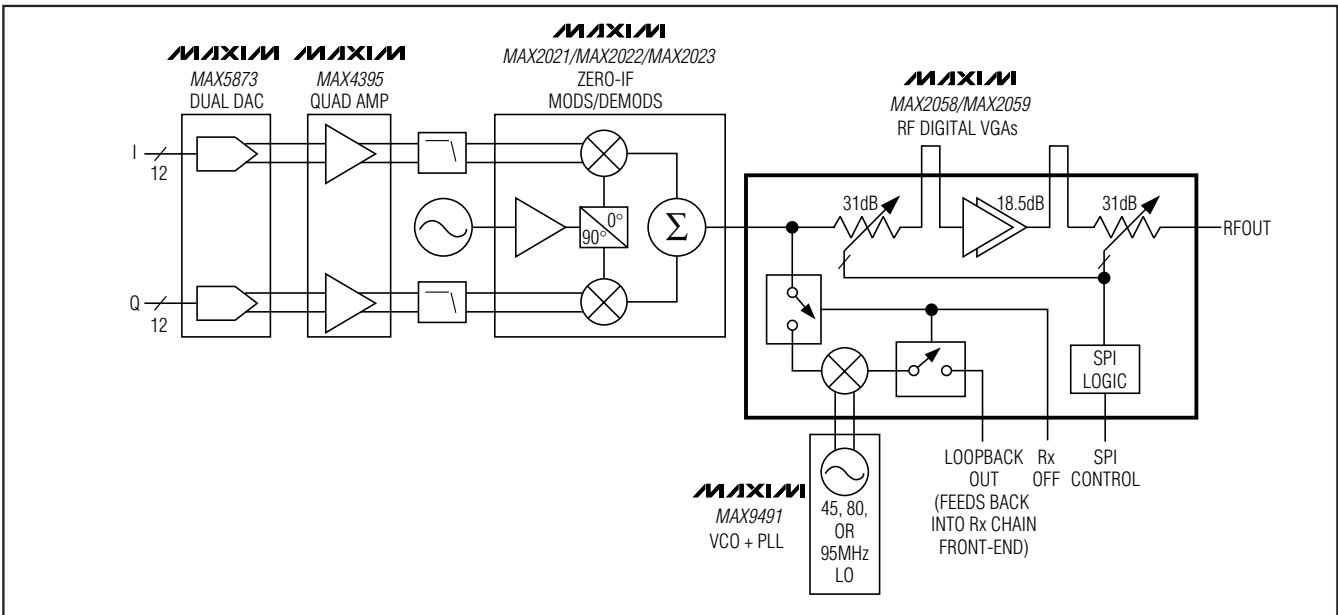


Figure 2. Direct Conversion Transmitter for GSM/EDGE Base Stations

1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

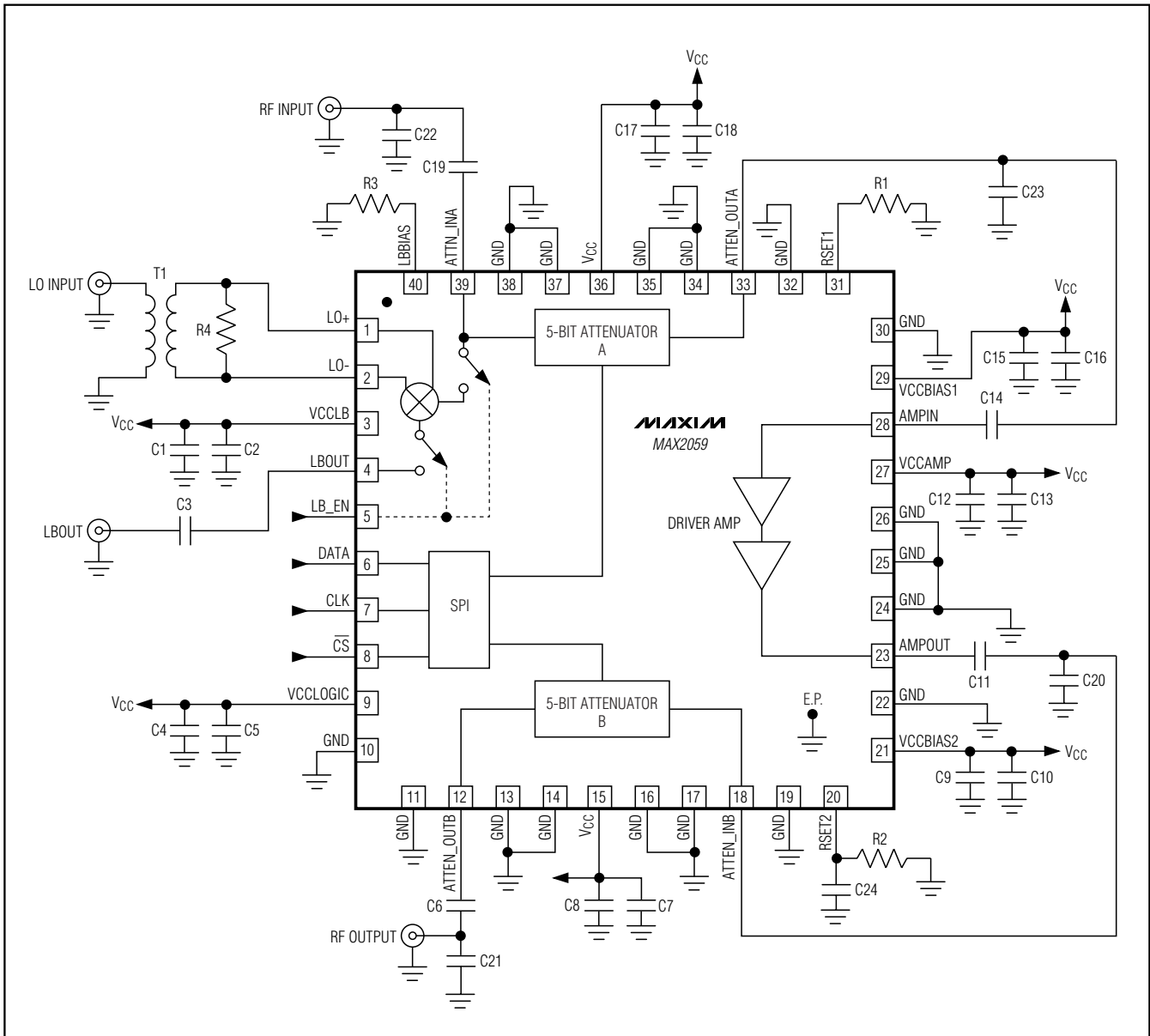
Direct-Conversion Base-Station Transmitter

The MAX2058/MAX2059 are designed to interface directly with Maxim's direct-conversion quadrature modulators and high-speed DACs to provide a complete solution for GSM/EDGE base-station transmitter applications. See Figure 2. The MAX2058/MAX2059,

together with the MAX2021/MAX2022/MAX2023 direct-conversion modulators/demodulators, the MAX5873 dual-channel DAC, and the MAX4395 quad amplifier, form an ideal total transmitter lineup. This overall system is highly efficient and low cost, while maintaining high linearity and low-noise performance.

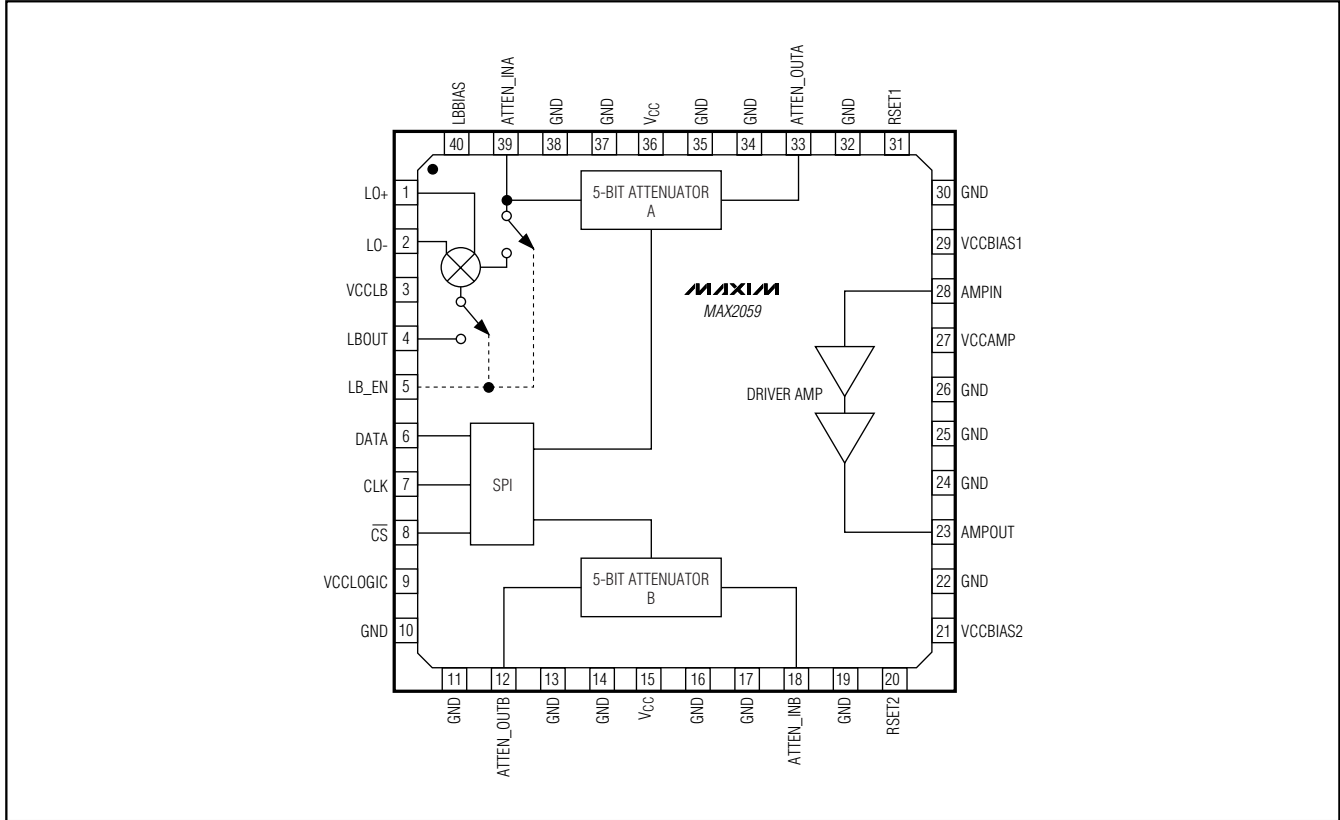
MAX2059

Typical Application Circuit



1700MHz to 2200MHz High-Linearity, SPI-Controlled DVGA with Integrated Loopback Mixer

Pin Configuration/Functional Diagram



Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

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