19-0699; Rev 0; 4/07

EVALUATION KIT AVAILABLE

Direct-Conversion to Low-IF Tuners for Digital Audio Broadcast

General Description

The MAX2170/MAX2171 direct-conversion to low-IF tuners are designed for Digital Audio Broadcast (DAB) and Terrestrial Digital Multimedia Broadcast (T-DMB) applications, covering an input frequency range of 168MHz to 240MHz (VHF-III), 1452MHz to 1492MHz (L-Band), and also 87MHz to 108MHz (FM). The MAX2170/MAX2171 achieve a high level of component integration, allowing low-power, tuner-on-board designs. The direct-conversion to low-IF architecture eliminates the need for an IF-SAW filter while providing a balanced 2.048MHz center frequency baseband output to the demodulator.

The MAX2170 provides a buffered reference clock at the crystal frequency, while the MAX2171 outputs a reference at 1/3rd of the crystal frequency.

A sigma-delta fractional-N synthesizer is incorporated to optimize both close-in and wideband phase noise performances for OFDM applications where sensitivity to both 1kHz phase noise and wideband phase noise related to strong adjacents can be a problem.

The MAX2170/MAX2171 are available in a 40-pin thin QFN package (6mm x 6mm) with an exposed paddle. Electrical performance is guaranteed over the extended -40°C to +85°C temperature range.

Applications

Fixed and Mobile Digital Audio Broadcast (DAB)

Terrestrial Digital Multimedia Broadcast (T-DMB)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2170ETL+	-40°C to +85°C	40 Thin QFN-EP* (6mm x 6mm)	T4066+2
MAX2171ETL+	-40°C to +85°C	40 Thin QFN-EP* (6mm x 6mm)	T4066+2

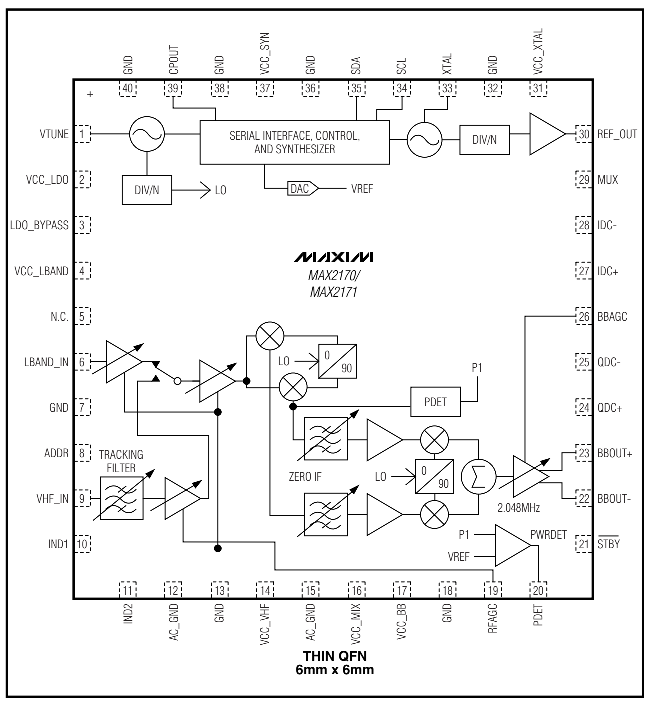
+Denotes lead-free package.
**EP = Exposed paddle.*

Features

- ♦ **+2.7V to +3.5V Supply Voltage Range**
- ♦ **Low-IF Output Eliminates IF-SAW Filter**
- ♦ **Integrated Low-IF Bandpass Filter**
- ♦ **Sigma-Delta Fractional-N Synthesizer**
- ♦ **+45dB Digital ACPR**
- ♦ **3.5dB Typical Noise Figure for VHF-III (Includes On-Chip Tracking Filter)**
- ♦ **3.1dB Typical Noise Figure for L-Band**
- ♦ **VHF-III Sensitivity of -100dBm**
- ♦ **L-Band Sensitivity of -99dBm**
- ♦ **Baseband Overload Detector Controls RF AGC**

Typical Application Circuit appears at end of data sheet.

Pin Configuration/ Functional Diagram



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +3.6V
VHF_IN ....-0.3V to +1.9V
LBAND_IN, IND1, IND2..-0.3V to +0.9V
Any Other Pins to GND..............................-0.3V to (V_{CC} + 0.3V)
BBOUT+, BBOUT- Short-Circuit Protection..................Indefinite
LBAND_IN, VHF_IN Input Power....................................+10dBm
Continuous Power Dissipation
(T_A = +70°C) (derated 35.7mW/°C above +70°C) 2857mW

Operating Temperature Range ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
θ_{JA} ....+28°C/W
θ_{JC} ....+1.5°C/W
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2170/MAX2171 *Typical Application Circuit*, V_{CC} = +2.7V to +3.5V, GND = 0V, BBAGC = RFAGC = +2.4V, RF input terminated into 50Ω, BBOUT+ and BBOUT- are open, default register settings, no input signal, VCO locked to default channel, f_{REF} = 24.576MHz, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Supply Voltage	V_{CC}		2.7	3.0	3.5	V
Supply Current	I_{CC}	Active mode, V_{CC} = 3V		62	77	mA
		Standby mode, $\overline{STBY}$ = 0V		3		mA
		Shutdown mode, $\overline{STBY}$ = 0V, SHDN_ALL bit set at logic-high		5		µA
RFAGC AND BBAGC						
RFAGC Input Bias Current		At 0.4V and 2.4V	-20		+10	µA
BBAGC Input Bias Current		At 0.4V and 2.4V	-20		+15	µA
RF and Baseband AGC Control Voltage		Minimum attenuation	2.4			V
		Maximum attenuation			0.4	V
SERIAL INTERFACE (SCL, SDA)						
Input Logic-Level Low					0.3 x V_{CC}	V
Input Logic-Level High			0.7 x V_{CC}			V
SDA, SCL Input Current			-10		+10	µA
Output Logic-Level Low		3mA sink current			0.4	V
SYSTEM TIMING						
Signal Path Settling Time		From standby mode to active, any band		0.02		ms
Adjacent Channel Change		Any mode, including VCO tuning		0.5		ms
Reference Oscillator Turn-On Time to 50ppm		Using the MAX2170 EV kit		0.6		ms

AC ELECTRICAL CHARACTERISTICS

(MAX2170/MAX2171 *Typical Application Circuit*, V_{CC} = 2.7V to 3.5V, GND = 0V. RFAGC = BBAGC = +2.4V, RF input terminated into 50Ω, BBOUT+ and BBOUT- terminated into balanced 2kΩ ll 10pF load, default register settings, VCO locked. T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency Range		FM band gain specification met across this frequency band, BAND_SEL = “10”	87		108	MHz
		VHF-III band gain specification met across this frequency band, BAND_SEL = “00”	168		240	
		L-band gain specification met across this frequency band, BAND_SEL = “01”	1452		1492	
Input Power per Channel Maximum Gain Mode (LNA_BYP = 0)		All bands, output signal of at least 100mV_{P-P} at minimum input level	-96			dBm
		VHF-III and FM band, output signal not to exceed 1V_{P-P} at maximum input level; RFAGC = BBAGC = 0.4V			-17	
Overall Voltage Gain, Maximum Gain Mode (LNA_BYP = 0)		All bands	80			dB
		RFAGC = BBAGC = 0.4V			21	
Input Power per Channel Low-Gain Mode (LNA_BYP = 1)		All bands, output signal of at least 100mV_{P-P} at minimum input level	-76			dBm
		VHF-III and FM band, output signal not to exceed 1V_{P-P} at maximum input level			3	
Overall Voltage Gain, Low-Gain Mode (LNA_BYP = 1)		All bands	60			dB
		RFAGC = BBAGC = 0.4V			1	
RF Gain Flatness		Over selected input frequency band, RFAGC = 2.4V	-3		+3	dB
Input Return Loss		Worst case across band selected (Note 1)	7	13		dB
Noise Figure (DSB) (LNA_BYP = 0) (Note 2)		FM band, BAND_SEL = “10”		3		dB
		VHF-III band, BAND SEL = “00”		3.5		
		L-band, BAND_SEL = “01”		3.1		
Noise Figure (DSB) (LNA_BYP = 1)		VHF-III band, BAND_SEL = “00”		15.3		dB
		L-band, BAND_SEL = “01”		12.8		
IIP2 (In-Band) (Note 3)		VHF_III, BAND_SEL = “00,” LNA_BYP = 0		16.7		dBm
		RFAGC = 2.4V, BAND_SEL = “00,” LNA_BYP = 1		27.8		
IIP3 (In-Band) (Note 4)		All bands, LNA_BYP = 0		-19.8		dBm
		VHF-III, BAND_SEL = “00,” LNA_BYP = 1		1.7		

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AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2170/MAX2171 *Typical Application Circuit*, V_{CC} = 2.7V to 3.5V, GND = 0V. RFAGC = BBAGC = +2.4V, RF input terminated into 50Ω, BBOUT+ and BBOUT- terminated into balanced 2kΩ ll 10pF load, default register settings, VCO locked. T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF 1dB Desense (Note 2)		$P_{DESIRED}$ = -90dBm and converted to f_{IF} = (2.048 + fo) MHz, tone 10MHz higher; any input frequency band; LNA_BYP = 1		-32.5		dBm
		$P_{DESIRED}$ = -75dBm and converted to (2.048 + fo) MHz, tone 10MHz higher; any input frequency band; LNA_BYP = 0		-11.5		
Adjacent Channel Protection Ratio		Adj. DAB (N ±1) (Note 5)		> +45		dBc
		Adj. DAB (N ± 2) (Note 6)		> +49		
Harmonic Rejection		FM, BAND_SEL = 01 and VHF-III, BAND_SEL = “00” (N = 3 and 5) (Note 1)	60			dBc
Beats within Output		Any input frequency, P_{IN} = -78.75dBm (Note 2)		< -22		dBc
Quadrature Accuracy		L-band		46		dB
Spurious at the RF Input (Note 1)		50MHz to 470MHz			-20	dBmV
		470MHz to 878MHz			-35	
		878MHz to 1732MHz			-20	
Phase Noise (Single-Sideband, Closed Loop) L-Band, BAND_SEL = “01,” 1472MHz, ICP = “0”		At 1kHz (Note 1)	-80	-90		dBc/Hz
		At 10kHz (Note 1)	-80	-90		
		At 100kHz		-105		
SIGMA-DELTA FRACTIONAL-N SYNTHESIZER						
REFERENCE OSCILLATOR						
Frequency				24.576		MHz
Load Capacitance		Present at XTAL to GND		18		pF
DIVIDERS						
N-Divider Ratio		To synthesizer	35		251	
R-Divider Ratio		To synthesizer	1		2	
Fractional-N Resolution		XTAL frequency / (2^{20})		23.4375		Hz
LO PHASE DETECTOR AND CHARGE PUMP						
f_{ϕ}		Phase-detector frequency	12.288	24.576		MHz
Charge-Pump Current		ICP = “0”		600		µA
		ICP = “1”		1200		
Charge-Pump Tri-State Current			-10		+10	µA
LOCAL OSCILLATOR						
Tune Range		Tank frequency	2688		3840	MHz
VCO Dividers		Directly to LO buffers driving the mixer	2	16	32	
VCO Tuning Gain		Tank oscillator gain, based on endpoint	40		410	MHz/V

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2170/MAX2171 *Typical Application Circuit*, V_{CC} = 2.7V to 3.5V, GND = 0V. RFAGC = BBAGC = +2.4V, RF input terminated into 50Ω, BBOUT+ and BBOUT- terminated into balanced 2kΩ ll 10pF load, default register settings, VCO locked. T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOW-IF STAGE						
Nominal Output Voltage		Differential output load = 2kΩ, differential output capacitance < 10pF		1		V_{P-P}
1dB Output Compression Point		Differential voltage at f_{IF} = 2.148MHz (Note 1)	1.4	2.3		V_{P-P}
Output Impedance		Balanced		27		Ω
Passband AGC Range		BBAGC = +2.4 to +0.4V		40		dB
Passband Cutoff Attenuation		f_{IF} = 2.048 ± 0.8MHz with nominal 3dB attenuation relative to 2.148MHz	1.3	3	4.0	dB
Passband Flatness		f_{IF} = 2.048 ± 0.4MHz		0.35		dB
Rejection Ratio		At -0.52MHz (RF tone at f_C - 2.568MHz) (Note 1)	50	57		dB
		At 4.616MHz (RF tone at f_C + 2.568MHz) (Note 1)	50	57		
		At > 21.7MHz		85		
DC Output Voltage		Common mode		V_{CC} / 2		V_{DC}
AGC Gain Slope		BBAGC = +0.4V to +2.4V	14		35	dB/V
Ratio of Passband to Stopband Noise		BBAGC = +2.4V, 2.048 ± 0.8MHz vs. 24.576 ± 0.8MHz		27		dB
MIXER OVERLOAD DETECTOR (RSSI)						
Attack-Point Accuracy		BAND_SEL = "00," f_{LO} = 210MHz, tone at 210.4MHz, P_{IN} = -52dBm		±1.5		dB
Detector Output Sink		Detector on, V_{OUT} < 0.5V	0.2			mA
		Detector off, V_{OUT} > 2.5V			5	µA
Detector Gain				36		
REFERENCE FREQUENCY OUTPUT BUFFER						
Output Level		REFOUT_VPP = 0, load impedance of 10kΩ and 10pF	500	760	1000	mV_{P-P}
		REFOUT_VPP = 1, load impedance of 10kΩ and 10pF		1500		
DC Voltage				1.9		V
Buffer Output Frequency		MAX2170		F_{REF}		
		MAX2171		F_{REF} / 3		
2-WIRE INTERFACE						
Clock Rate					400	kHz

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AC ELECTRICAL CHARACTERISTICS (continued)

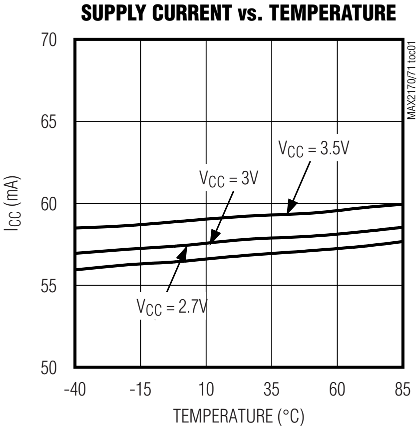
(MAX2170/MAX2171 *Typical Application Circuit*, V_{CC} = 2.7V to 3.5V, GND = 0V. RFAGC = BBAGC = +2.4V, RF input terminated into 50Ω, BBOUT+ and BBOUT- terminated into balanced 2kΩ ll 10pF load, default register settings, VCO locked. T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.)

Note 1: Guaranteed by design characterization, not production tested.
Note 2: BBAGC set at 1.4V and RFAGC set at 2.4V.
Note 3: f_{LO} at 177MHz. Desired tone at 177.1MHz at -70dBm with FM tones at 88.1MHz and 89.1MHz both at -35dBm. RFAGC = 1.4V for high-gain mode (LNA_BYP = 0) and RFAGC = 2.4V for low-gain mode (LNA_BYP = 1).
Note 4: Two tones at (f_O - 1.712) and (f_O - 3.024) MHz. Measured at 2.448MHz.
Note 5: Adjacent DAB channel with 1.712MHz channel spacing.
Note 6: Second adjacent DAB channel.

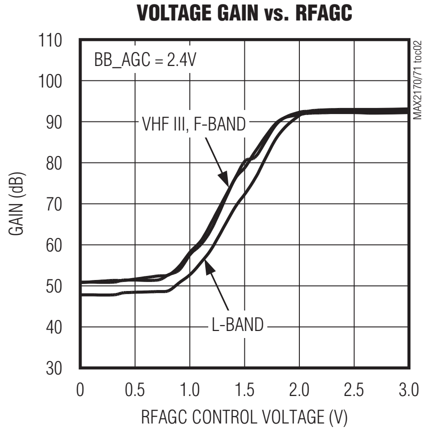
Typical Operating Characteristics

(MAX2170 EV kit, V_{CC} = +3.0V, FM = 108MHz, VHF band III = 239.2MHz, L-band = 1490.624MHz, IF = 2.148, RFAGC = BBAGC = 2.4V, $\overline{STBY}$ = V_{CC}, VCO running, f_{REF} = 24.576MHz, default register settings, T_A = +25°C, unless otherwise noted.)

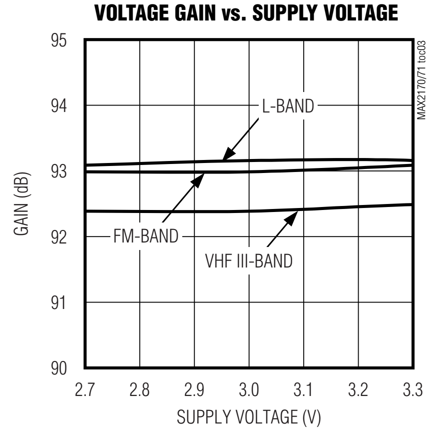
SUPPLY CURRENT vs. TEMPERATURE



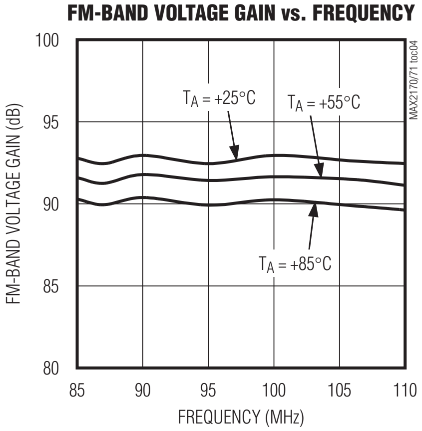
VOLTAGE GAIN vs. RFAGC



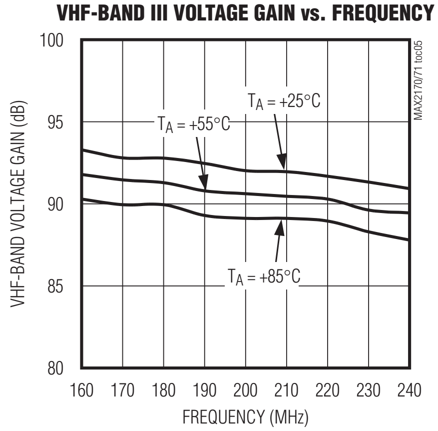
VOLTAGE GAIN vs. SUPPLY VOLTAGE



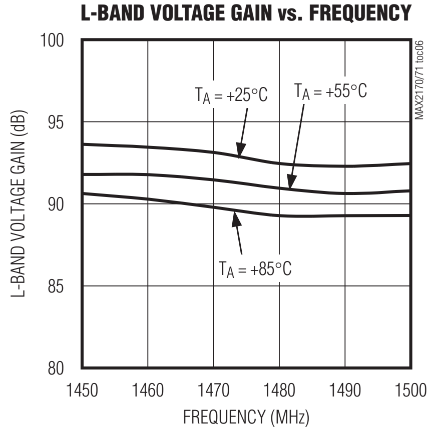
FM-BAND VOLTAGE GAIN vs. FREQUENCY



VHF-BAND III VOLTAGE GAIN vs. FREQUENCY



L-BAND VOLTAGE GAIN vs. FREQUENCY

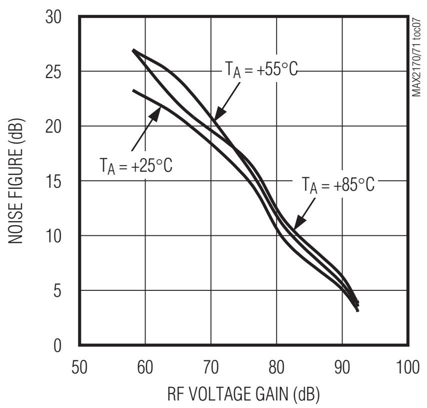


Direct-Conversion to Low-IF Tuners for Digital Audio Broadcast

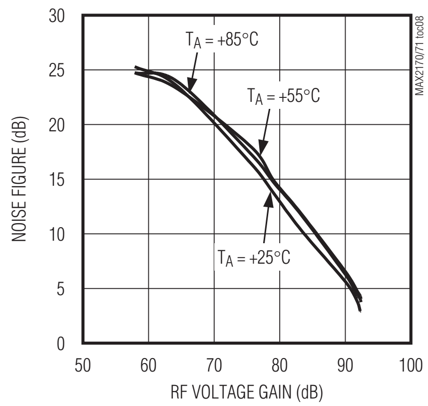
Typical Operating Characteristics (continued)

(MAX2170 EV kit, V_{CC} = +3.0V, FM = 108MHz, VHF band III = 239.2MHz, L-band = 1490.624MHz, IF = 2.148, RFAGC = BBAGC = 2.4V, $\overline{STBY}$ = V_{CC}, VCO running, f_{REF} = 24.576MHz, default register settings, T_A = +25°C, unless otherwise noted.)

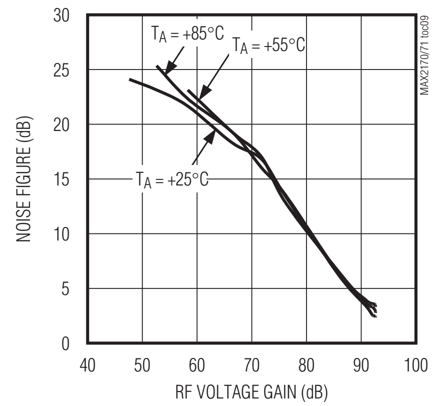
FM-BAND NOISE FIGURE vs. RF VOLTAGE GAIN



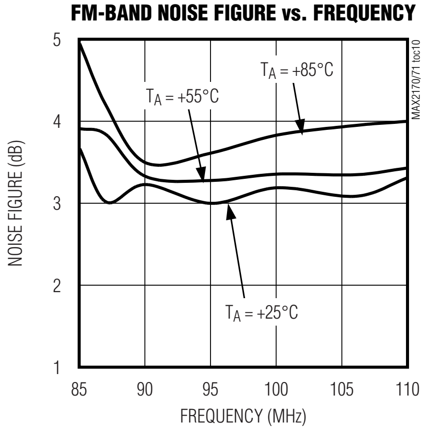
VHF-BAND III NOISE FIGURE vs. RF VOLTAGE GAIN



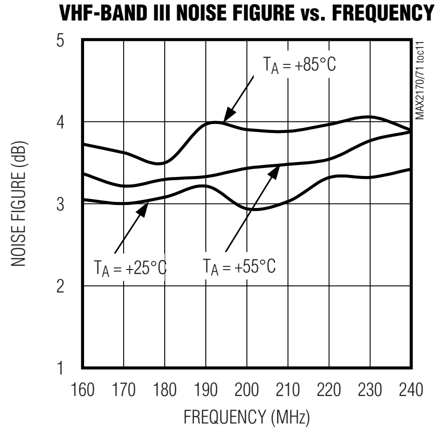
L-BAND NOISE FIGURE vs. RF VOLTAGE GAIN



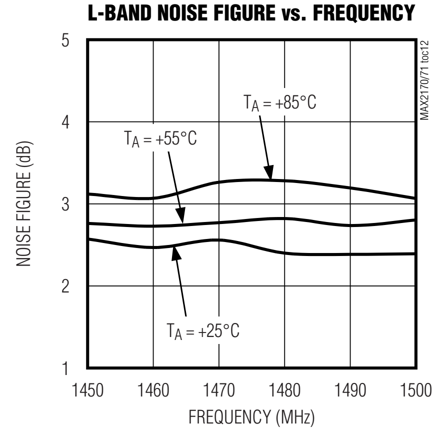
FM-BAND NOISE FIGURE vs. FREQUENCY



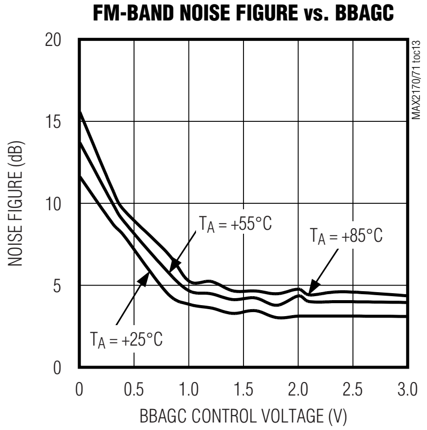
VHF-BAND III NOISE FIGURE vs. FREQUENCY



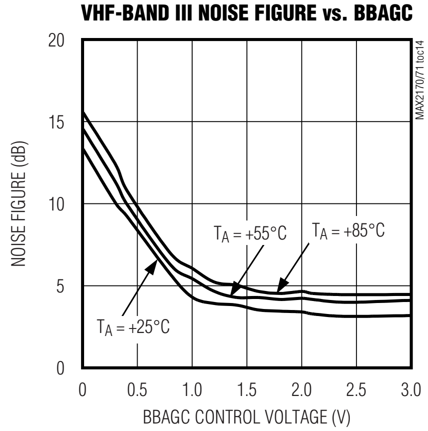
L-BAND NOISE FIGURE vs. FREQUENCY



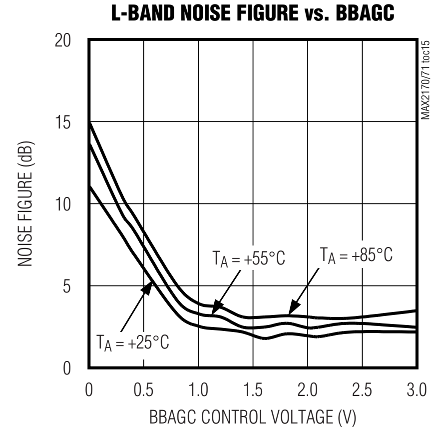
FM-BAND NOISE FIGURE vs. BBAGC



VHF-BAND III NOISE FIGURE vs. BBAGC



L-BAND NOISE FIGURE vs. BBAGC

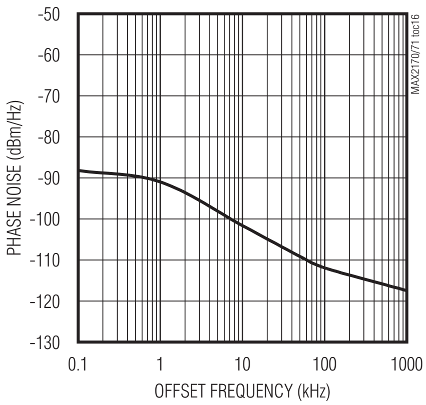


Direct-Conversion to Low-IF Tuners for Digital Audio Broadcast

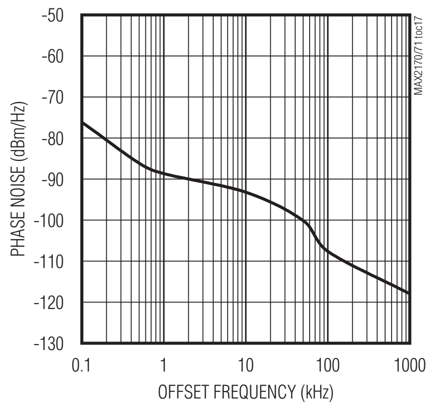
Typical Operating Characteristics (continued)

(MAX2170 EV kit, V_{CC} = +3.0V, FM = 108MHz, VHF band III = 239.2MHz, L-band = 1490.624MHz, IF = 2.148, RFAGC = BBAGC = 2.4V, $\overline{STBY}$ = V_{CC}, VCO running, f_{REF} = 24.576MHz, default register settings, T_A = +25°C, unless otherwise noted.)

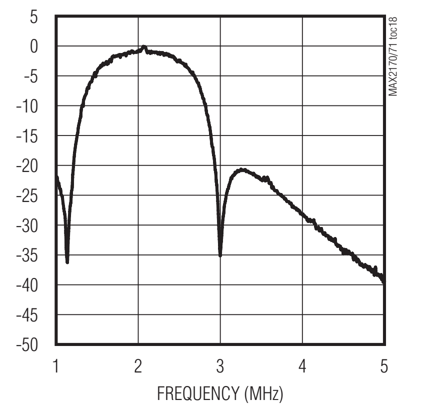
VHF-III BAND PHASE NOISE vs. OFFSET FREQUENCY



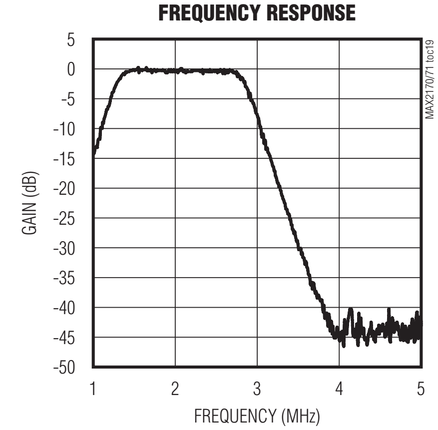
L-BAND PHASE NOISE vs. OFFSET FREQUENCY



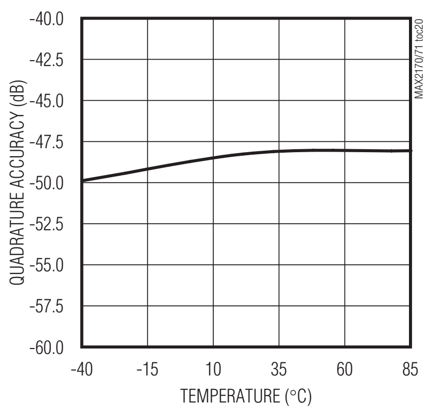
FM MODE NORMALIZED BASEBAND FREQUENCY RESPONSE



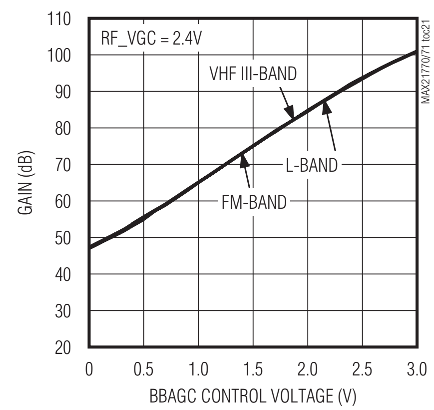
VHF MODE NORMALIZED BASEBAND FREQUENCY RESPONSE



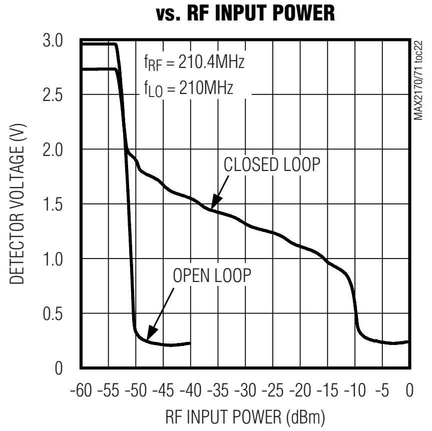
L-BAND QUADRATURE ACCURACY vs. TEMPERATURE



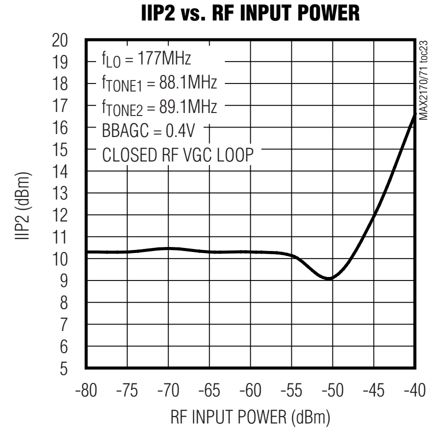
VOLTAGE GAIN vs. BBAGC



DETECTOR VOLTAGE vs. RF INPUT POWER

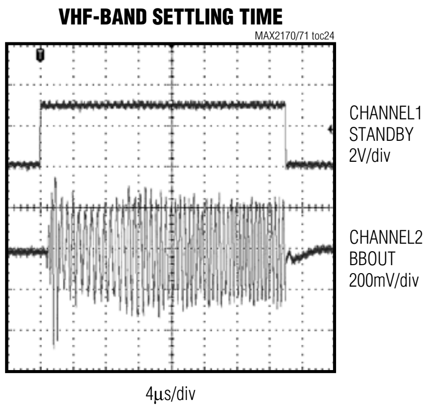


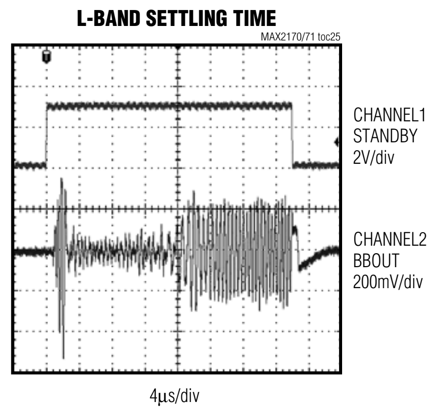
IIP2 vs. RF INPUT POWER

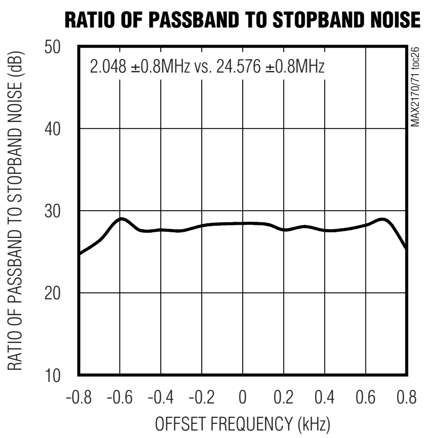


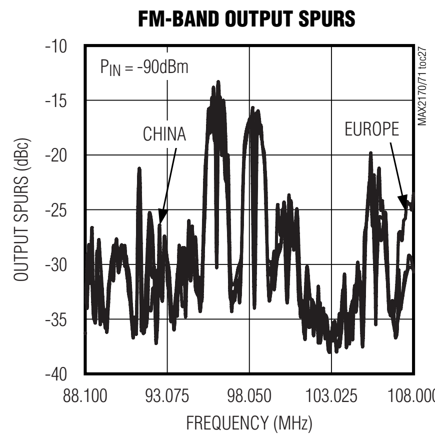
Typical Operating Characteristics (continued)

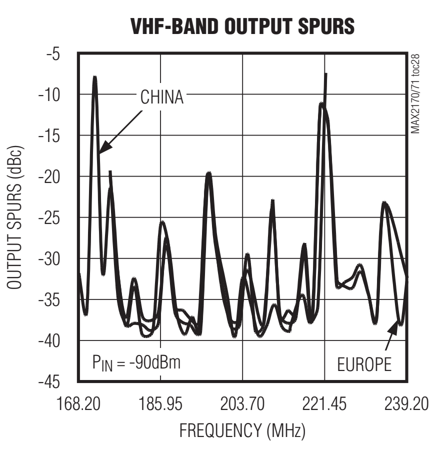
(MAX2170 EV kit, V_{CC} = +3.0V, FM = 108MHz, VHF band III = 239.2MHz, L-band = 1490.624MHz, IF = 2.148, RFAGC = BBAGC = 2.4V, $\overline{STBY}$ = V_{CC}, VCO running, f_{REF} = 24.576MHz, default register settings, T_A = +25°C, unless otherwise noted.)

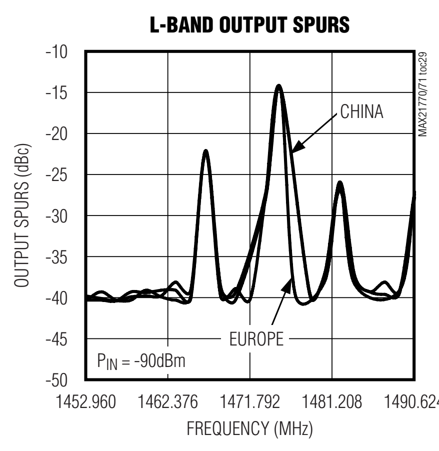








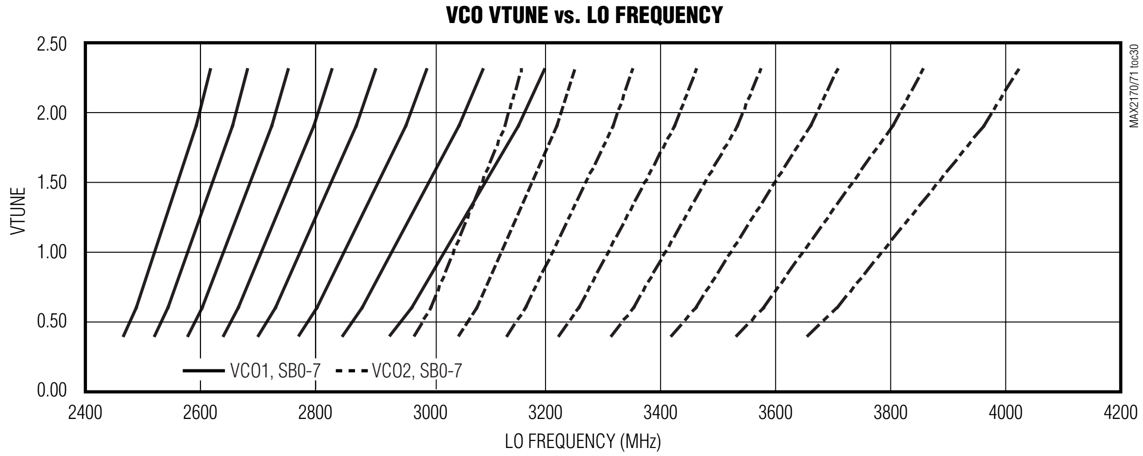




Direct-Conversion to Low-IF Tuners for Digital Audio Broadcast

Typical Operating Characteristics (continued)

(MAX2170 EV kit, V_{CC} = +3.0V, FM = 108MHz, VHF band III = 239.2MHz, L-band = 1490.624MHz, IF = 2.148, RFAGC = BBAGC = 2.4V, $\overline{STBY}$ = V_{CC}, VCO running, f_{REF} = 24.576MHz, default register settings, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	VTUNE	High-Impedance VCO Tune Input. Connect the PLL loop filter output directly to this pin with the shortest connection possible. Use pin 40 as the ground reference for the loop filter.
2	VCC_LDO	Internal LDO Supply. DC supply for the oscillator's internal regulator. Bypass to GND with a 1nF capacitor as close as possible to the pin.
3	LDO_BYPASS	VCO LDO Bypass. Connect 0.1µF capacitor as close as possible from this pin to GND.
4	VCC_LBAND	DC Supply for the L-Band LNA. Connect a 100pF capacitor as close as possible from this pin to GND.
5	N.C.	No Connection. Do not connect to ground.
6	LBAND_IN	RF Input for L-Band. Input to the L-Band LNA. AC-couple from the L-Band bandpass filter.
7, 13, 18, 32, 36, 38, 40	GND	Ground
8	ADDR	Address Line. Sets the device address. Connect to ground to set for device address 0xC0. Connect to V_{CC} to set for device address 0xC2.
9	VHF_IN	RF Input for VHF-III Band and FM Band. Input to the VHF-III and FM band tracking filter. AC-coupled.
10	IND1	Filter Inductor Pin 1
11	IND2	Filter Inductor Pin 2
12, 15	AC_GND	AC Ground. Connect a 1nF capacitor as close as possible to GND.
14	VCC_VHF	DC Supply for the VHF and FM LNA. Connect a 1nF capacitor as close as possible from this pin to GND.
16	VCC_MIX	DC Supply for the VHF and FM LNA. Connect a 1nF capacitor as close as possible from this pin to GND.
17	VCC_BB	DC Supply for Baseband. Connect a 100nF capacitor as close as possible from this pin to GND. Use pin 18 as the ground reference for VCC_BB pin's bypass capacitor.
19	RFAGC	Gain-Control Input for the RFVGA

Pin Description (continued)

PIN	NAME	FUNCTION
20	PDET	Power-Detector Output. Provides a buffered and scaled output of the power detector's output voltage. Connect a 27kΩ pullup resistor to V_{CC} and a RC network to RFAGC.
21	$\overline{STBY}$	Standby Enable. Set to logic "0" for standby mode. Set to logic "1" for normal operation.
22	BBOUT-	Inverted Baseband Output
23	BBOUT+	Noninverted Baseband Output
24	QDC+	Q-Channel DC Offset Bypass. Connect a 0.33µF capacitor as close as possible across pins 24 and 25.
25	QDC-	
26	BBAGC	Gain Control for Baseband VGA
27	IDC+	I-Channel DC Offset Bypass. Connect a 0.33µF capacitor as close as possible across pins 27 and 28.
28	IDC-	
29	MUX	Multiplex Output Line for Testing
30	REF_OUT	Buffered Output of Reference Oscillator
31	VCC_XTAL	DC Supply for the Reference Oscillator. Connect a 100nF capacitor as close as possible from this pin to GND. Use pin 32 as the baseband ground reference for VCC_XTAL pin's bypass capacitor.
33	XTAL	Crystal-Oscillator Input. Connect to parallel resonant mode XTAL through a load-matching capacitor.
34	SCL	Serial-Interface Clock Input Line. Requires a 2.7kΩ pullup resistor to V_{CC}.
35	SDA	Serial-Interface Data Input Line. Requires a 2.7kΩ pullup resistor to V_{CC}.
37	VCC_SYN	DC Supply for the Synthesizer and Serial Interface. Bypass to pins 36 and 38 grounds using 100nF capacitors. Make connections as short as possible. See the *Typical Application Circuit*.
39	CPOUT	Output of Charge Pump. Connect the output to the PLL loop filter input with the shortest connection possible.
EP	EP	Exposed Paddle. Connect to GND with multiple vias for proper operation.

Detailed Description

The MAX2170/MAX2171 are direct-conversion to Zero-IF and an upconversion to Low-IF tuners targeting Digital Audio Broadcast (DAB) applications. These integrated tuners are designed to convert the 1452MHz to 1492MHz L-Band, the 168MHz to 240MHz VHF-III, and also the 87MHz to 108MHz FM frequencies to a centered 2.048MHz baseband frequency. This architecture eliminates the need for the SAW filter used in super-heterodyne architectures.

The MAX2170/MAX2171 integrated tuners include front-end tracking filters for VHF-III and FM band selection, low-noise VGA, direct-conversion mixers, I/Q channel filters, a mixer for upconversion to a low IF, and a VGA output driver. The devices also have a fully integrated fractional-N synthesizer for frequency generation, a power detector for automatic gain control, and DC offset-correction circuitry for the baseband signal.

The MAX2170 provides a buffered reference clock at the crystal frequency, while the MAX2171 outputs a reference at 1/3rd of the crystal frequency.

Register Descriptions

The MAX2170/MAX2171 include 13 user-programmable registers and 3 read-only registers. The register configuration of Table 1 shows each bit name and the bit usage information for all registers. "U" labeled under each bit name indicates that the bit value is user defined to meet specific application requirements. A "0" or "1" indicates that the bit must be set to the defined "0" or "1" value for proper operation. Operation is not tested or guaranteed if these bits are programmed to other values and is only for factory/bench evaluation. Note that all registers must be written after and no earlier than 100µs after device power-up.

Power-up defaults are provided for user convenience only and should not be relied on in the user's application. It is the responsibility of the user to supply all required register values when the device is first powered on.

Table 1. Register Configuration

REGISTER ADDRESS	REGISTER NAME	POR	MSB				LSB			
			DATA BYTE							
			D7	D6	D5	D4	D3	D2	D1	D0
0x00	N-DIVIDER INTEGER	H37	N7 U	N6 U	N5 U	N4 U	N3 U	N2 U	N1 U	N0 U
0x01	CP CONTROL AND FRAC2	H05	— X	— X	— X	CP_LIN 0	F19 U	F18 U	F17 U	F16 U
0x02	FRAC1	H6A	F15 U	F14 U	F13 U	F12 U	F11 U	F10 U	F9 U	F8 U
0x03	FRAC0	HAB	F7 U	F6 U	F5 U	F4 U	F3 U	F2 U	F1 U	F0 U
0x04	TRACKING FILTER	HFF	— 1	— 1	TFC1<2> U	TFC1<1> U	TFC1<0> U	TFC2<2> U	TFC2<1> U	TFC2<0> U
0x05	PLL CONFIG	H1E	RDIV U	ICP 0	— X	— X	— X	— X	— X	— X
0x06	MODE SELECT	HE0	FRAC_EN 1	DUTY_EN 1	— 1	FSTCHG U	LNA_BYP U	SHDN_ALL U	BAND_SEL<1> U	BAND_SEL<0> U
0x07	VCO CONTROL	H1C	— X	VCO_SB<3> U	VCO_SB<2> U	VCO_SB<1> U	VCO_SB<0> U	VAS_EN 1	ADL 0	ADE 0
0x08	BASEBAND CONTROL	H3C	PD_TH<2> R	PD_TH<1> R	PD_TH<0> R	FLBIAS<1> 1	FLBIAS<0> 1	BB_BW<2> R	BB_BW<1> R	BB_BW<0> R
0x09	VCO AND MASTER BIAS	HE0	REFOUT_VPP U	— X	VCO_BIAS 1	BIAS<4> R	BIAS<3> R	BIAS<2> R	BIAS<1> R	BIAS<0> R
0x0A	ROM TABLE ADDRESS	H00	— 0	— 0	— 0	— 0	RTA<3> U	RTA<2> U	RTA<1> U	RTA<0> U
0x0B	ROM TABLE DATA	H00	RTD<7> 0	RTD<6> 0	RTD<5> 0	RTD<4> 0	RTD<3> 0	RTD<2> 0	RTD<1> 0	RTD<0> 0
0x0C	TEST FUNCTIONS	H00	CP_TST<2> 0	CP_TST<1> 0	CP_TST<0> 0	LNA_BIAS<1> 0	LNA_BIAS<0> 0	LD_MUX<2> 0	LD_MUX<1> 0	LD_MUX<0> 0
0x10	ROM TABLE DATA READBACK	NA	TFR<7>	TFR<6>	TFR<5>	TFR<4>	TFR<3>	TFR<2>	TFR<1>	TFR<0>
0x11	STATUS READBACK	NA	POR	VASA	VASE	—	—	—	—	PD_OVLD
0x12	AUTOTUNER READBACK	NA	—	VCO_SBR<3>	VCO_SBR<2>	VCO_SBR<1>	VCO_SBR<0>	ADC<2>	ADC<1>	ADC<0>

Note: *Power-up default is PLL tuned to 170MHz at 24.576MHz reference.*

U: User defined
R: Read from ROM table
0: Set to “0” for factory-tested operation
1: Set to “1” for factory-tested operation
X: Don’t care

Table 2. RegisterAddress 0x00 N-Divider Integer

BIT NAME	BIT LOCATION	FUNCTION
N<7:0>	7, 6, 5, 4, 3, 2, 1, 0	Sets the integer portion of N-divider value. N-divider range can vary from 35 to 251. 00100011 = 35 (Minimum) 00110111 = (Default = 37h = 55d) 11111011 = 251 (Maximum)

Table 3. Register Address 0x01 CP Control and FRAC2

BIT NAME	BIT LOCATION	FUNCTION
F<19:16>	3, 2, 1, 0	Sets MSB of fractional divider value. Fractional divider value is F[19:0] / 1048576. 0000 = Minimum 0101 = Default = 5h 1111 = Maximum
CP_LIN	4	Sets charge-pump linearity 0 = Typically balanced CP source and sink currents, for FM and VHF-III operation (default) 1 = Typically +10% more CP sink current, for L-Band operation
—	7, 6, 5	Unused bits

Table 4. Register Address 0x02 FRAC1

BIT NAME	BIT LOCATION	FUNCTION
F<15:8>	7, 6, 5, 4, 3, 2, 1, 0	Sets middle portion of fractional divider value. Fractional divider value is F[19:0] / 1048576. 00000000 = Minimum 01101010 = Default = 6Ah 11111111 = Maximum

Table 5. Register Address 0x03 FRAC0

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
F<7:0>	7, 6, 5, 4, 3, 2, 1, 0	Sets LSB of fractional divider value. Fractional divider value is F[19:0] / 1048576. 00000000 = Minimum 10101011 = Default = Abh 11111111 = Maximum

Table 6. Register Address 0x04 Tracking Filter

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
TFC2<2:0>	2, 1, 0	Track Filter C2. Minimum weighting set for 000 and maximum weighting set for 111. 111 = Maximum (Default)
TFC1<2:0>	5, 4, 3	Track Filter C1. Minimum weighting set for 000 and maximum weighting set for 111. 111 = Maximum (Default)
—	7, 6	Unused bits

Table 7. Register Address 0x05 PLL Configuration

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
—	0, 1, 2, 3, 4, 5	Unused bits
ICP	6	Charge-Pump Current 0 = 600µA typical (default) 1 = 1200µA typical
RDIV	7	PLL Reference Divider 0 = Divide by 1 (default) 1 = Divide by 2

Table 8. Register Address 0x06 Mode Select

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
BAND_SEL<1:0>	1, 0	Band Selection 00 = VHF band selected (default) 01 = L-Band selected 10 = FM band selected 11 = L-Band selected
SHDN_ALL	2	Shutdown Option when in Standby 0 = All circuitry shuts down except for the crystal oscillator and reference buffer when $\overline{STBY}$ is logic-low (default) 1 = All circuitry shuts down when $\overline{STBY}$ is logic-low
LNA_BYP	3	LNA Bypass Enable (Low LNA Gain) 0 = Disabled. Full LNA gain (default). 1 = Enabled. LNA turned off and bypassed.
FSTCHG	4	DC Correction Loop; Fast-Charge Enable 0 = Disabled. Highpass corner frequency is 100Hz and settling time is typically 10ms (default). 1 = Enabled. Highpass corner frequency is typically 800Hz and settling time is typically 1.25ms.
—	5	Unused
DUTY_EN	6	Reference Buffer Output Duty-Cycle Correction Enable 0 = Disabled 1 = Enabled (default)
FRAC_EN	7	Fractional-N Synthesizer Enable 0 = Disabled. Integer-N mode. 1 = Enabled. Fractional-N mode (default).

Table 9. Register Address 0x07 VCO Control

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
ADE	0	Enable VCO Autoselection (VAS) ADC (Sample VTUNE) 0 = Disabled (default) 1 = Enabled
ADL	1	Latch VCO Autoselection (VAS) ADC (Latch in VTUNE Value) 0 = Disabled (default) 1 = Enabled
VAS_EN	2	VCO Autoselection (VAS) Circuit 0 = Disabled. VCO selection must be programmed through I^2C bus. 1 = Enabled. VCO selection controlled by autoselection circuit (VAS) (default).
VCO_SB<3:0>	6, 5, 4, 3	VCO Sub-Band Selection for 1 to 16 Bands 0000 = 1, lowest band 0001 = 2 0010 = 3 (default) ………… 1110 = 15 1111 = 16, highest band
—	7	Unused

Table 10. Register Address 0x08 Baseband Control

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
BB_BW<2:0>	2, 1, 0	Baseband Lowpass Filter Bandwidth Setting 000 = Typically 0.75 x f_C (f_C is the -3dB corner frequency) 001 = Typically 0.8 x f_C 010 = Typically 0.86 x f_C 011 = Typically 0.92 x f_C 100 = Nominal (f_C) (default) 101 = Typically 1.08 x f_C 110 = Typically 1.19 x f_C 111 = Typically 1.32 x f_C
FL_BIAS<1:0>	4, 3	Baseband Filter Bias Current 00 = Typically 50% of nominal 01 = Typically 66% of nominal 10 = Typically 75% of nominal 11 = Typically 100% (default)
PD_TH<2:0>	7, 6, 5	Power-Detector Threshold 000 = Minimum 001 010 011 100 101 110 111 = Maximum

Table 11. Register Address 0x09 VCO and Master Bias

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
BIAS <2:0>	4, 3, 2, 1, 0	Master Bias Control 00000 = Nominal Current (default) 00001 …….. 11111
VCO_BIAS	5	VCO Bias Current Increase 0 = Typically +25% 1 = Nominal current (default)
—	6	Not used.
REFOUT_VPP	7	Reference Output Buffer (Pin 30) Voltage Swing 0 = 0.7V_{P-P} 1 = 1.5V_{P-P} (default)

Table 12. Register Address 0x0A ROM Table Address

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
RTA<3:0>	3, 2, 1, 0	**ROM Table Register Address** 0000 = Reg 0: Power Detector and Master Bias Trim (Default) 0001 = Reg 1: Tracking Filter Capacitor Weightings, VHF-III High-Frequency Setting 0010 = Reg 2: Tracking Filter Capacitor Weightings, FM Frequency Setting 0011 = Reg 3: Tracking Filter Capacitor Weightings, VHF-III Low-Frequency Setting 0100 = Reg 4: Baseband Lowpass Filter Bandwidth Setting 0101 = Reg 5: Unused 0110 = Reg 6: Unused 0111 = Reg 7: Read Only 1xxx = N/A
—	7, 6, 5, 4	Unused

Table 13. Register Address 0x0C Test Mode

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
LD_MUX<2:0>	2, 1, 0	**MUX Output (N-Divider, R-Divider and Bias-Current Calibration)** 000 = Normal Operation: Mux output logic-high (default) 001 = Monitor N-divider output, post divide by 2 010 = Monitor R-divider output 011 = Monitor test fractional vector output (factory use only) 1xx = Bias current-trim mode (factory use only)
LNA_BIAS<1:0>	4, 3	**LNA Bias Current Setting** 00 = Nominal (Default) 01 = -5% typical 10 = -10% typical 11 = -15% typical
CP_TST<2:0>	7, 6, 5	**Charge-Pump Test Modes** 000 = Normal operation (Default) 0xx = Normal operation 100 = Both source and sink currents enabled 101 = Source current enabled 110 = Sink current enabled 111 = High impedance (both source and sink currents disabled)

Table 14. Register Address 0x10 ROM Table Data Readback

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
TFR<7:0>	7, 6, 5, 4, 3, 2, 1, 0	**ROM Table Readback** 00000000 = Minimum 11111111 = Maximum

Table 15. Register Address 0x11 Status

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
PD_OVLD	0	**Power Detector over Load** 0 = Below power-detector threshold 1 = Overload, above power-detector threshold
—	4, 3, 2, 1	Unused
VASA : VASE	6, 5	**VCO Autoselect (VAS) Status Bits** 00 = Active and searching 01 = Unsuccessful acquisition 10 = Unused/don't care 11 = Successful acquisition
POR	7	**Power-On Reset Status** 0 = Chip-Status register has been read with stop condition since last power-on. 1 = Power-on reset (power cycle) has occurred. Default values have been loaded in registers.

Table 16. VCO Autoselect (VAS) Read Register

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
ADC<2:0>	2, 1, 0	**VAS ADC Output (V_{TUNE})** 000 = V_{TUNE} < 0.416V (unlocked) 001 = 0.416 V_{TUNE} < 0.628V 010 = 0.628 V_{TUNE} < 1.075V 101 = 1.075 V_{TUNE} < 1.830V 110 = 1.830 V_{TUNE} < V_{CC} - 0.40V 111 = V_{TUNE} > V_{CC} - 0.40V (unlocked) *ADC trip points are typical values.
VCO_SBR <3:0>	6, 5, 4, 3	**VCO Sub-Band Readback (1 to 16 Bands)** 0000 = 1, lowest band 0001 = 2 0001 = 3 ….. 1110 = 15 1111 = 16, highest band
—	7	Not used

Table 17. MAX2170/MAX2171 ROM Table

REGISTER	7	6	5	4	3	2	1	0	DESCRIPTION
00	PD_TH<2>	PD_TH<1>	PD_TH<0>	BIAS<4>	BIAS<3>	BIAS<2>	BIAS<1>	BIAS<0>	Power Detector and Master Bias
01	X	X	TFC1H<2>	TFC1H<1>	TFC1H<0>	TFC2H<2>	TFC2H<1>	TFC2H<0>	VHF-III High-Frequency Capacitor Setting
02	X	X	TFC1M<2>	TFC1M<1>	TFC1M<0>	TFC2M<2>	TFC2M<1>	TFC2M<0>	FM Frequency Capacitor Setting
03	X	X	TFC1L<2>	TFC1L<1>	TFC1L<0>	TFC2L<2>	TFC2L<1>	TFC2L<0>	VHF-III Low-Frequency Capacitor Setting
04	X	X	X	X	X	BB_BW<2>	BB_BW<1>	BB_BW<0>	Baseband Filter Bandwidth

2-Wire Serial Interface

The MAX2170/MAX2171 use a two-wire I^2C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the device and the master at clock frequencies up to 400kHz. The master initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX2170/MAX2171 behave as an I^2C slave device that transfers and receives data to and from the master. Pull SDA and SCL high with external pullup resistors (1kΩ or greater) for proper I^2C operation.

One bit is transferred during each SCL clock cycle. A minimum of nine clock cycles are required to transfer a byte in or out of the MAX2170/MAX2171 (8 bits and an ACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

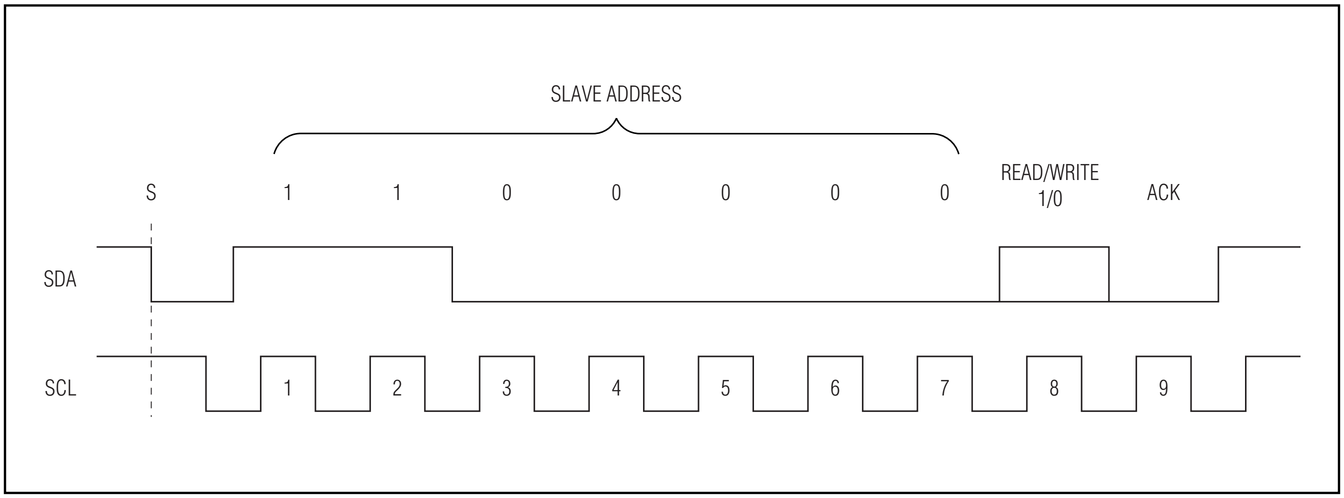


Figure 1. Slave Address Byte with ADDR Pin Set at "0"

Table 18. Programmable Device Address

ADDR	READ/WRITE ADDRESS
0	0xC0
1	0xC2

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK) after a byte is transferred in or out of the MAX2170/MAX2171. Both the master and the MAX2170/MAX2171 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX2170/MAX2171 continuously await a START condition followed by its slave address. The slave address is seven bits that must be sent to the device following a START condition to initiate communication. The slave address can be programmed to one of two possible addresses by the ADDR pin (Table 18). The eighth bit ($R/\overline{W}$) following the 7-bit address determines whether a read or write operation occurs.

Write Cycle

When addressed with a write command, the MAX2170/MAX2171 allow the master to write to a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition followed by the seven slave address bits and a write bit (LSB = "0"). The device issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to write to (see Table 1 for register addresses). The slave acknowledges the address, and the master can then write one byte of data to the register at the specified address. Data is written beginning with the most significant bit. The MAX2170/MAX2171 again issue an ACK if the data is successfully written to the register. The master can continue to write data to the successive internal registers with the device acknowledging each successful transfer, or the master can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

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START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE REGISTER ADDRESS	ACK	WRITE DATA TO REGISTER 0x00	ACK	WRITE DATA TO REGISTER 0x01	ACK	WRITE DATA TO REGISTER 0x02	ACK	STOP
	110000[ADDR]	0		0x00		0x0E		0xD8		0xE1		

Figure 2. Example: Write registers 0 through 2 with 0x0E, 0xD8, and 0xE1, respectively.

START	DEVICE ADDRESS	R/$\overline{W}$	ACK	REGISTER ADDRESS	ACK	START	DEVICE ADDRESS	R/$\overline{W}$	ACK	REG 00 DATA	ACK	REG 01 DATA	ACK	REG 02 DATA	NACK	STOP
	11000[ADDR]	0		00000000			11000[ADDR]	1		xxxxxxxx		xxxxxxxx		xxxxxxxx		

Figure 3. Example: Receive Data from Read Registers

Figure 2 shows an example in which registers 0 through 2 are written with 0x0E, 0xD8, and 0xE1, respectively.

Read Cycle

When addressed with a read command, the MAX2170/MAX2171 allow the master to read back a single register or multiple successive registers.

A read cycle begins with the bus master issuing a START condition followed by the seven slave address bits and a write bit (LSB = "0"). The MAX2170/MAX2171 issue an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to read (see Table 1 for register addresses). The slave acknowledges the address. Then, a START condition is issued by the master, followed by the seven slave address bits and a read bit (LSB = "1"). The MAX2170/MAX2171 issue an ACK if the slave address byte is successfully received. The device starts sending data MSB first with each SCL clock cycle. At the 9th clock cycle, the master can issue an ACK, and continue to read successive registers, or the master can terminate the transmission by issuing a NACK. The read cycle does not terminate until the mastzer issues a STOP condition.

Figure 3 shows an example in which registers 0 through 2 are read back.

Applications Information

Band Selection and RF Input

The MAX2170/MAX2171 are designed to be compatible for operation in the L-Band, VHF-III, and FM band. Band operation selection is selected by the bits BAND_SEL<1:0> of the Mode Selection register. The L-Band option is possible using a LO at the VCO frequency divided by 2. An external bandpass filter is required at the L-Band RF input (LBAND_IN) covering the 1452MHz to 1492MHz range for L-Band selection.

VHF-III and FM band operation use a divide by 16 and 32, respectively. An integrated tracking bandpass filter is provided to cover both the total tuning ranges of 168MHz to 240MHz for VHF-III and 87MHz to 108MHz for FM.

The MAX2170/MAX2171 VHF_IN and LBAND_IN inputs are internally matched to 50Ω and require a DC-blocking capacitor (for L-Band use a 33pF and for VHF-III/FM use a 1nF).

RF Front-End Filters

The MAX2170/MAX2171 integrate a narrowband RF tracking filter for the VHF and FM band. The filter response is determined by two external inductors and internal digitally controlled capacitors.

To set the filter's center frequency, the integrated RF tracking filter uses an external inductor between the IND1 and IND2 pins and another inductor in series with the VHF_IN input. The inductor value must be 91nH±3% to achieve the targeted corner frequency response. The internal variable capacitors are factory calibrated to this particular inductor value. The value of the internal capacitors is set to compensate for process variation of each individual part and to receive the desired RF channel.

Programming the Tracking Filter

The tracking filter is a bandpass filter whose center frequency is user programmable through register 0x04, data bits D5–D0 (see Table 1). Note that bits D5–D3 are labeled TFC1<2,0>. These three bits set the value of tracking filter capacitor, C1. Bits D2–D0 are labeled TFC2<2,0>. These three bits set the value of tracking filter capacitor, C2.

For FM operation, the user should program bits D5–D0 of register 0x04 with bits 5–0 of ROM register 02. These ROM bits have been factory set to give the optimal filter setting for the entire FM band.

For VHF operation, the contents of ROM registers 01 and 03 have been factory set to optimize the tracking filter capacitors for 240MHz (VHF-III high-frequency capacitor setting) and 170MHz (VHF-III low-frequency capacitor setting), respectively. For frequencies between 170MHz and 240MHz, the user should linearly interpolate the ROM table values as described below:

Interpolating tracking filter ROM table values for VHF-III frequencies:

1) Parse and convert ROM table values as follows:
   a. TFC1L = decimal equivalent of ROM register 03, bits 5–3.
   b. TTFC2L = decimal equivalent of ROM register 03, bits 2–0.
   c. TTFC1H = decimal equivalent of ROM register 01, bits 5–3.
   d. TTFC2H = decimal equivalent of ROM register 01, bits 2–0.
2) Interpolate the TFC1 and TFC2 decimal values using the formulas below:
   a. If Freq < 170MHz, then Freq = 170MHz
   TFC1d = TFC1L - round((Freq - 170MHz) / 70MHz x (TFC1L - TFC1H))
   b. TFC2d = TFC2L - round((Freq - 170MHz) / 70MHz x (TFC2L - TFC2H))
3) Convert decimal values TFC1d and TFC2d to 3-bit binary bytes and program into register 0x04:
   a. D5–D3 of register 0x04 = TFC1b
   b. D2–D0 of register 0x04 = TFC2b
4) Example: The desired VHF-III frequency is 205MHz and ROM registers 01 and 03 are factory set to xx010000 and xx111110, respectively.
   a. TFC1H = 2d.
   b. TFC2H = 0d.
   c. TFC1L = 7d.
   d. TFC2L = 6d.

   Now interpolating:
   a. TFC1d = 7 - round(2.5) = 4.
   b. TFC2d = 6 - round(3) = 3.

Thus, register 0x04 should be user programmed to xx100011 for the VHF-III frequency of 205MHz.

Programming the Bias Registers

The LNA and the RF mixer currents are referenced to a stable current calibrated in the factory. This information is stored in bits<4:0> of register 00 in the ROM table. After power-up these five bits of data need to be loaded into bits<4:0> in register 09 to set the proper bias currents for the LNA and RF mixers.

Gain Control

The MAX2170/MAX2171 feature an RFVGA and an IFVGA that can be used to achieve the optimum SNR. The RFVGA and IFVGA provide 40dB and 39dB of total gain range, respectively. The RFVGA can be programmed for either high-gain mode or low-gain mode. In low-gain mode, the RFVGA gain is reduced by 21dB. In typical application, the decision of which mode to use is determined during the initial channel selection and also by the power-detector information. For low-gain mode, set the LNA_BYP bit to a logic “1” in the Mode Select register.

The RFVGA and the IFVGA circuits can be driven independently by the baseband controller. The RF gain control can also be configured for closed-loop automatic gain control when combined with the on-chip baseband power detector. See the *Baseband Power Detector and Programming the Power-Detector Threshold* section.

Baseband Power Detector and Programming the Power-Detector Threshold

The MAX2170/MAX2171 baseband power detector senses the differential baseband output power from the first gain stage of the baseband filter, and compares the sensed signal to the threshold value equivalent to the level produced by a -52dBm RF input signal. The power-detector threshold is factory calibrated to a typical input power of -52dBm. This information is stored in bits<7:5> of register 00 in the ROM table. After power-up, these three bits need to be loaded into bits<7:5> in register 08 to set the proper power-detector response.

Closed-loop RF automatic gain control can be implemented by connecting the current-sink power-detector output (PDET) to V_{CC} with a 27kΩ pullup resistor. For closed-loop control, the resulting voltage at the power-detector output is fed to the RFAGC input by a RC network. See the *Typical Application Circuit* for details.

Programming the Baseband Filters

The baseband filter is factory trimmed to have a typical bandwidth (-3dB corner) at 0.8MHz. The information is stored in bits<2:0> of register 04 in the ROM table. After power-up, these three bits’ data need to be loaded into bits<2:0> in register 08 to set proper baseband filter bandwidth.

VCO Autoselect (VAS)

The MAX2170/MAX2171 VCO consists of 16 sub-bands. The device has a VCO autoselect function that chooses the correct VCO sub-band for the desired operating frequency. Automatic VCO sub-band selection is enabled by setting the VAS_EN bit in the VCO Control register to 1. The autotuner begins selecting the appropriate VCO once the fractional portion of the N-divider has been programmed. Therefore, when changing LO frequencies, all the N-divider registers (integer and fractional) must be programmed to activate the autotuner function.

When a VCO sub-band search is initiated and active, the VASE bit in the Status register is cleared. Upon successful completion, bits VASE and VASA are set and the sub-band selected is reported in the VCO Autoselect Read register. If the search is unsuccessful, the VASA is cleared and the VASE bit is set to 1. This indicates that the search has ended but that no good sub-band has been found, and occurs when trying to tune to a frequency outside the device's specified frequency range.

If VASA = 0 and VASE = 1, then the user must check to ensure that the PLL is locked:

1) Write VAS_EN = 0 and ADE = 1 to register 0x07. This enables the V_{TUNE} ADC.
2) Write ADL = 1 to register 0x07. This latches the ADC value into the hold register. Do not set ADL = 1 with the same command word used to set ADE = 1.
3) Read register 0x12: Bits ADC<2>, ADC<1>, ADC<0>
   a. If 000 or 111, then the PLL is not locked.
   b. All other values indicate that the VCO is locked.
4) Write VAS_EN = 1, ADE = 0, and ADL = 0 to register 7. This enables the VAS for the next tune frequency.

Note: The VASA and VASE bits are only useful for determining PLL lock immediately after sending a tune command. The procedure outlined in section 4 above should be used for determining phase lock during normal operation.

The typical search time within a sub-band is 0.8ms. The total search time across the 16 sub-bands is 12.8ms typically. A frequency vs. sub-band lookup table can be used to speed up the search time. See the *Typical Operating Characteristic* frequency vs. sub-band information. Once a sub-band is determined, it can be programmed into bits <6:3> of register 07 to set the starting point for the VCO autoselection process.

3-Bit ADC

The MAX2170/MAX2171 have an internal 3-bit ADC that samples the VCO tune pin voltage (VTUNE). This ADC is used for checking the lock status of the PLL. Table 16 contains the VCO Autoselect Read register information and summarizes the ADC trip points.

When VCO autoselect is disabled, the ADC must first be enabled by setting the ADE bit in the VCO Control register. The ADC reading is latched by a subsequent programming of the ADC latch bit (ADL = 1). The ADC value is reported in the VCO Autoselect Read register.

Synthesizer Loop Filter

A second-order lowpass loop filter is used to achieve low spurious and low phase noise. The loop bandwidth is chosen for a desirable spurious rejection and a reasonable lock time. Refer to the Evaluation Kit data sheet for the recommended loop-filter component values.

Crystal-Oscillator Interface

The MAX2170/MAX2171 reference oscillator is generated by a crystal oscillator by connecting a parallel resonant-mode crystal through a load-matching capacitor. See the *Typical Application Circuit*. For particular capacitor values, possible changes to accommodate for different crystal frequencies, crystal load-capacitance requirements, and crystal power-dissipation requirements, refer to the Evaluation Kit data sheet for details.

Reference Output

A reference buffer is provided for the reference oscillator. The buffer can provide a typical $0.7V_{P-P}$ or $1.5V_{P-P}$ output into a load of 10kΩ||10pF. Note that the MAX2170 provides a buffered reference clock at the crystal frequency, while the MAX2171 outputs a reference at 1/3rd of the crystal frequency.

DC Offset Correction

The MAX2170/MAX2171 feature an always-active DC offset correction circuitry that requires an external capacitor. The offset-correction circuitry monitors the baseband DC offset voltage and compares this DC signal to a reference voltage. When the magnitude of the baseband DC offset exceeds the reference, the offset-correction circuitry outputs a correction factor at the input of the baseband filter to achieve the desired baseband DC offset.

The settling time or corner frequency of the offset-correction circuit can be programmed by the FSTCHG bit of the Mode Select register.

Shutdown and Standby Mode

To reduce power consumption, put the MAX2170/MAX2171 into standby mode, during which only the serial interface, the crystal oscillator, and the XTAL reference buffer/divider are active. For standby mode, set the $\overline{STBY}$ pin to a logic "0." Set $\overline{STBY}$ to a logic "1" for normal operation.

The MAX2170/MAX2171 can be put into shutdown by programming the SHDN_ALL bit in the Mode Select register when the device is in standby mode. When the SHDN_ALL bit is set, all circuitry including the PLL is shut down.

Power-Supply Bypassing

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at the central V_{CC} node. The V_{CC} traces branch out from this node, with each trace going to separate V_{CC} pins of the MAX2170/MAX2171. Next to each V_{CC} pin is a bypass capacitor with a low-impedance to ground at the frequency of interest. Use at least one via per bypass capacitor for a low-inductance ground connection.

Layout Considerations

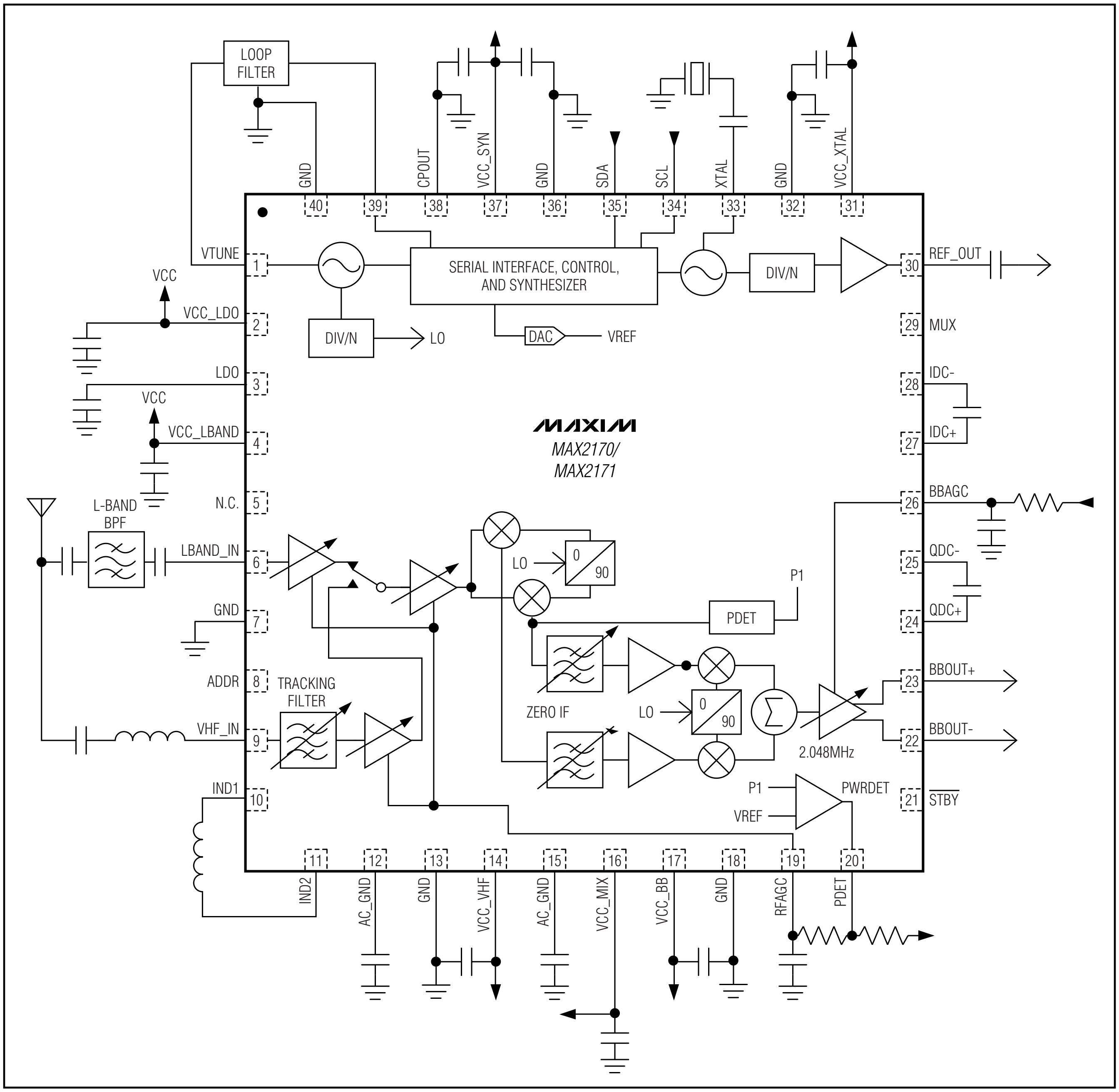
The EV kit serves as a guide for PCB layout. Keep RF signal lines as short as possible to minimize losses and radiation. Use controlled impedance on all high-frequency traces. The exposed paddle must be soldered evenly to the board's ground plane for proper operation. Use abundant vias beneath the exposed paddle for maximum heat dissipation. Use abundant ground vias between RF traces to minimize undesired coupling. Bypass each V_{CC} pin to ground with a capacitor placed as close as possible to the pin . For bypass capacitor values, see the *Pin Description* or refer to the Evaluation Kit schematic.

The ground connection of the bypass capacitors on the power-supply inputs requires careful consideration. In general, use the closest ground pin to the supply input as the ground connection of the supply's bypass capacitor. Use the baseband ground reference for the ground connection of the baseband supply's bypass capacitors. For example, use pins 18, 32, and 36 as the ground connection for the bypass capacitors on VCC_BB, VCC_XTAL, and VCC_SYN, respectively. Likewise, use pin 40 as the ground reference for the PLL loop filter. Finally, note that placing the synthesizer ground reference of VCC_SYN too close to the RF inputs (VHF_IN and LBAND_IN) can cause noise from the VCC_SYN line to couple into the RF inputs. Refer to the Evaluation Kit layout as a general guideline.

Chip Information

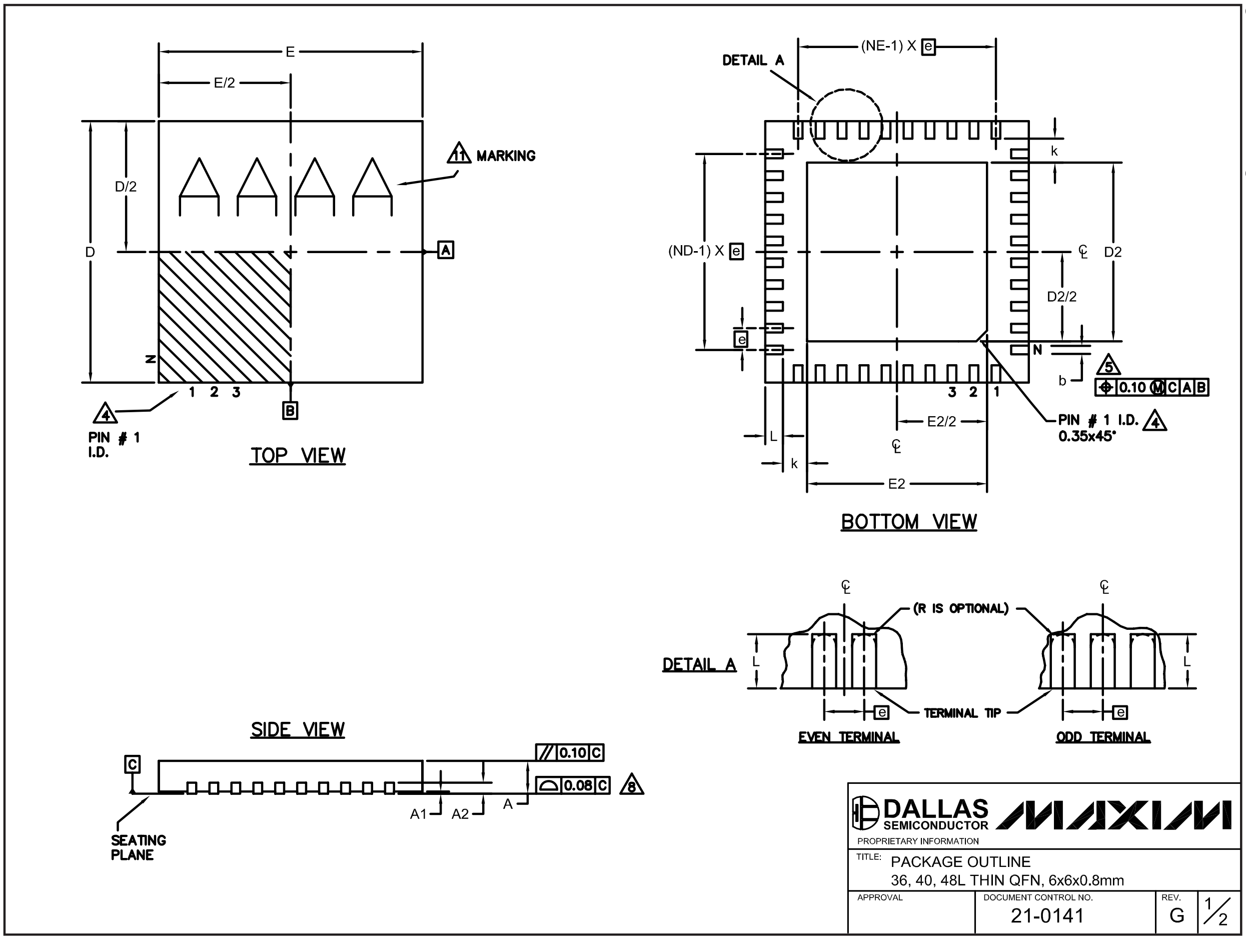
PROCESS: SiGe BiCMOS

Typical Application Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Direct-Conversion to Low-IF Tuners for Digital Audio Broadcast

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0141 | REV. G | 2/2