Click here for production status of specific part numbers.

MAX22517-MAX22519

Self-Powered, 2-Channel, 3.5kV$_{RMS}$ Digital Isolator

General Description

The MAX22517–MAX22519 are dual-channel digital galvanic isolators with integrated field-side supply using Maxim's proprietary process technology. The field-side power is supplied by the logic-side using an integrated isolated DC-DC converter. This approach eliminates the bulky and expensive external isolated power supply when the power demand of the field side is small. All of the devices in the family feature basic isolation with a withstand voltage rating of 3.5kV$_{RMS}$ for 60s or 445V$_{RMS}$ of continuous operation. With a single resistor on each input, the inputs of the MAX22517–MAX22519 can withstand 1.2/50µs surge pulses up to ±2kV between inputs (common mode) or up to ±1kV between input and field ground (differential), as well as continuous shorts to 24VAC. The MAX22517–MAX22519 provide compact, reliable, and cost-efficient solutions for applications such as industrial IoT, industrial networking systems, and building automation.

Both sides of the isolators are powered from a single 3.0V to 5.5V supply on the logic side, which also sets the output logic level. Both channels of the MAX22517–MAX22519 transfer data from the field side to the logic side and are always enabled. Each output is high when the corresponding input is high and low when the corresponding input is low.

Devices are available with either push-pull or open-drain outputs, and output default states are either logic-high (push-pull version) or high impedance (open-drain versions). The default is the state the output assumes when either power domain of the device is undervoltage or the input is open circuit. See the *Ordering Information* for the part numbers associated with each option.

All of the devices in the MAX22517–MAX22519 family are available in a 8-pin wide-body SOIC package with 5.5mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400V, which gives it a group II rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

Applications

- Industrial IoT
- Industrial Networking Systems
- Building Automation
- Medical Equipment

Benefits and Features

- Robust Protection in Small Footprint
  - Integrated Isolated Field-Side Supply
  - Integrated Galvanic Digital Isolation
  - Integrated Surge and Short Protection with External Series Resistor
    - 24VAC Short Protection
    - ±1kV Line-to-Ground and ±2kV Line-to-Line Surge Tolerance (1.2/50µs Waveform)
  - Compact 8-Pin Wide-Body SOIC Package (5.5mm Creepage)
- Robust Galvanic Isolation of Digital Signals
  - 3.5kV$_{RMS}$ Isolation Voltage for 60s (V$_{ISO}$)
  - 445V$_{RMS}$ Continuous Working Voltage (V$_{IOWM}$)
- Design Flexibility
  - 220µA Field-Side Supply External Load Capability
  - 3V to 5.5V Logic-Side Supply
  - -40°C to +125°C Operating Temperature Range

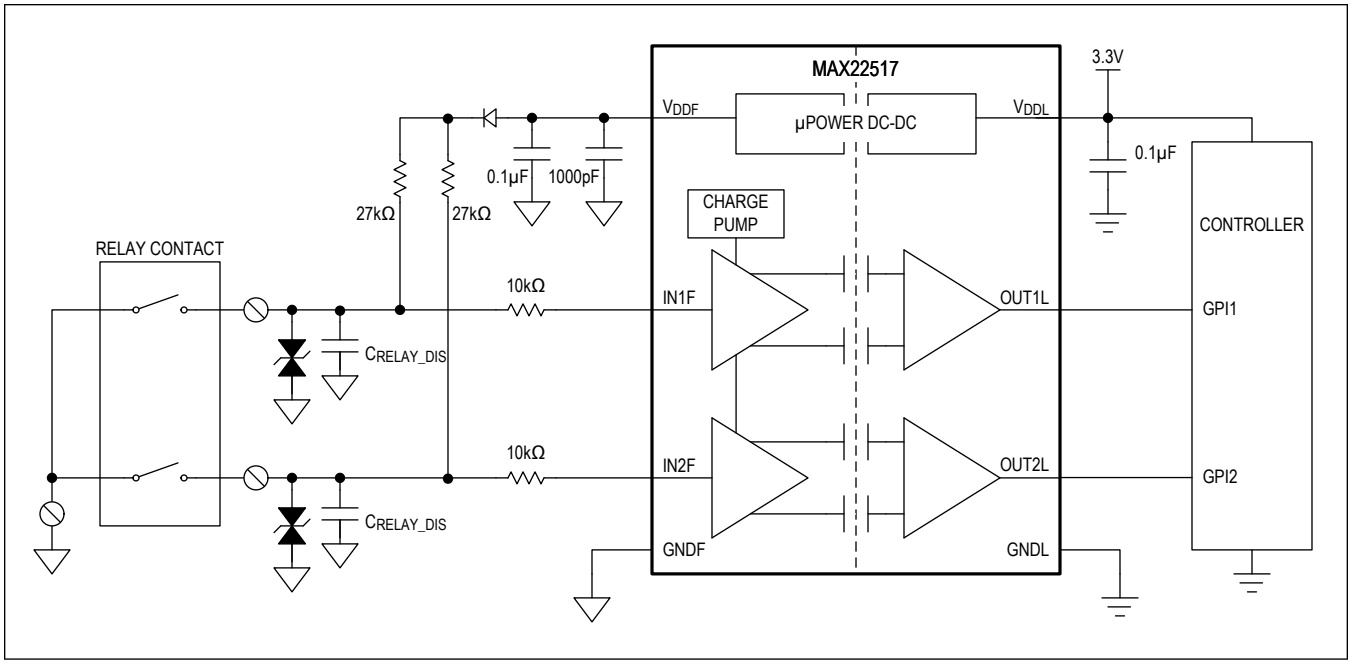
Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A

***Ordering Information* appears at end of data sheet.**

maxim integrated™

Dual Relay Contact Monitoring System



Absolute Maximum Ratings

V_{DDF} to GNDF (internally generated) ..... -0.3V to +6V
IN_F Current
  MAX22517, MAX22518 ..... -6mA to +5.5mA
  MAX22519 ..... -6mA to +6mA
IN_F to GNDF (no series resistor)
  MAX22517, MAX22518 ..... -0.4V to +5.65V
  MAX22519 ..... -0.4V to (V_{DDF} + 0.3V)
IN_F to GNDF (10kΩ series resistor) ..... -60V to +60V
V_{DDL} to GNDL ..... -0.3V to +6V
OUT_L to GNDL
  MAX22517 ..... -0.3V to (V_{DDL} + 0.3V)
  MAX22518, MAX22519 ..... -0.3V to +6V
Short-Circuit Continuous Current
  OUT_L to V_{DDL} or GNDL ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
  Wide SOIC (derate 9.39mW/°C above +70°C) 751.17mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 Wide SOIC

Package Code	W8MS+1
Outline Number	21-0262
Land Pattern Number	90-0258
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	106.5°C/W
Junction to Case (θ_{JC})	46.67°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

DC Electrical Characteristics

(V_{DDL} - V_{GNDL} = 3.0V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDL} - V_{GNDL} = 3.3V, V_{GNDF} = V_{GNDL}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FIELD SIDE						
V_{DDF} Supply Voltage	V_{DDF}	Relative to GNDF, internally regulated	2.7		4	V
V_{DDF} External Load Current	I_{DDF_LD}	Data rate < 100kbps			220	µA
Field-Side Undervoltage-Lockout Threshold	V_{UVLOF}	V_{DDF} rising	1.95	2.1	2.25	V
Field-Side Undervoltage-Lockout Threshold Hysteresis	V_{UVLOF_HYST}			100		mV
FIELD-SIDE INPUTS (IN_F)						
Input Boost Voltage	V_{IN_BST}	MAX22517/MAX22518, I_{IN_BST} = -1µA per input	5		5.5	V
Input Boost Current	I_{IN_BST}	MAX22517/MAX22518		-5		µA

DC Electrical Characteristics (continued)

(V_{DDL} - V_{GNDL} = 3.0V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDL} - V_{GNDL} = 3.3V, V_{GNDF} = V_{GNDL}, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Current	I_{IN_PU}	MAX22519	-10	-5	-1.5	µA
Field Input High Voltage	V_{IH}		0.7 x V_{DDF}			V
Field Input Low Voltage	V_{IL}				0.3 x V_{DDF}	V
Field Input Hysteresis	V_{HYS}			0.4		V
LOGIC SIDE						
V_{DDL} Supply Voltage	V_{DDL}	Relative to GNDL	3		5.5	V
V_{DDL} Supply Current	I_{DDL}	V_{DDL} = 5V, C_L = 0pF		7.5	10	mA
		V_{DDL} = 3.3V, C_L = 0pF		7.5	10	
Logic-Side Undervoltage-Lockout Threshold	V_{UVLOL}	V_{DDL} rising	2.69	2.82	2.95	V
Logic-Side Undervoltage-Lockout Threshold Hysteresis	V_{UVLOL_HYST}			100		mV
LOGIC-SIDE OUTPUTS (OUT_L)						
Output Logic-High Voltage	V_{OH}	MAX22517, OUT_L sourcing 4mA	V_{DDL} - 0.4			V
Output Logic-Low Voltage	V_{OL}	OUT_L sinking 4mA			0.4	V
Output Logic-High Leakage Current	I_{OH_LK}	MAX22518/MAX22519, OUT_L = 0V, 5.5V	-1		+1	µA

Dynamic Characteristics

(V_{DDL} - V_{GNDL} = 3.0V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDL} - V_{GNDL} = 3.3V, V_{GNDF} = V_{GNDL}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_F = GNDF or V_{DDF} (Note 4)		50		kV/µs
Maximum Data Rate	DR_{MAX}	(Note 1)	1			Mbps
Minimum Detectable Field Input Pulse Width	PW_{MIN}	No external capacitor on IN_F (Note 1)			1	µs
Glitch Rejection				55		ns
Power-Up Delay (Figure 2)	t_{DEL}	C_{VDDF} = 0.1µF		280		µs
Propagation Delay (Figure 1)	t_{PLH}	No external input series resistance		80	130	ns
		10kΩ external input series resistance		120		
	t_{PHL}	No external input series resistance		80	130	
		10kΩ external input series resistance		120		

Dynamic Characteristics (continued)

(V_{DDL} - V_{GNDL} = 3.0V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDL} - V_{GNDL} = 3.3V, V_{GNDF} = V_{GNDL}, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	No external input series resistance			20	ns
			10kΩ external input series resistance		10		
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	No external input series resistance				70	ns
	t_{SPHL}	No external input series resistance				70	
Propagation Delay Skew Channel-to-Channel (Same Part) (Figure 1)	t_{SCSLH}	No external input series resistance				10	ns
	t_{SCSHL}	No external input series resistance				10	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	1Mbps			10		ns
Rise Time (Figure 1)	t_R	MAX22517			20	35	ns
Fall Time (Figure 1)	t_F				20	35	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDF or GNDL), unless otherwise noted.

Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDF and GNDL (V_{CM} = 1000V).

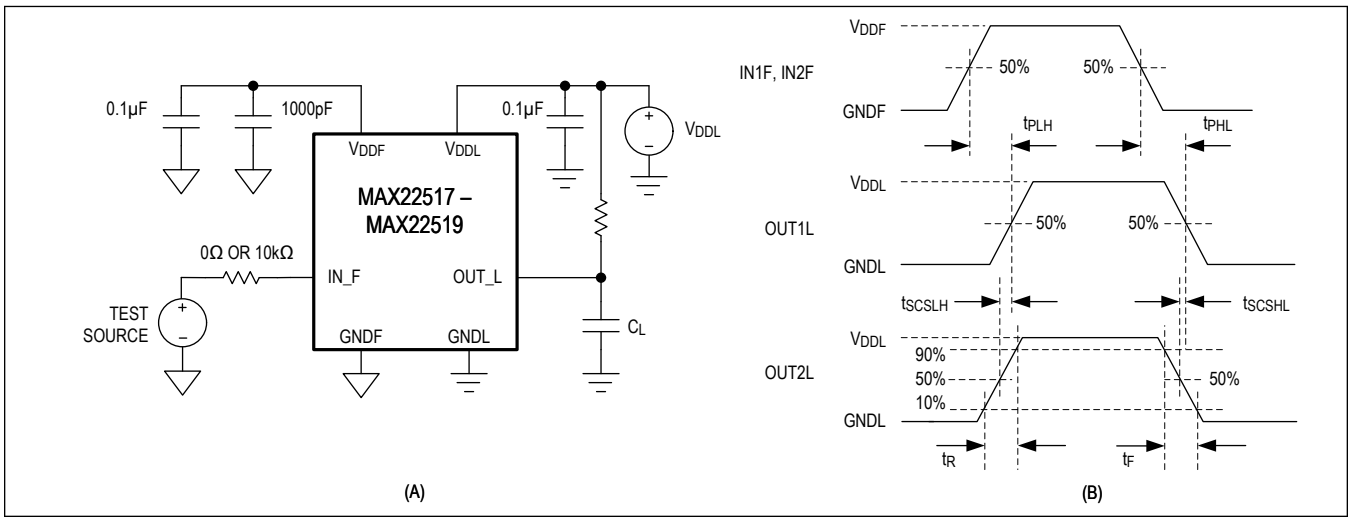


Figure 1. Test Circuit (A) and Timing Diagram (B)

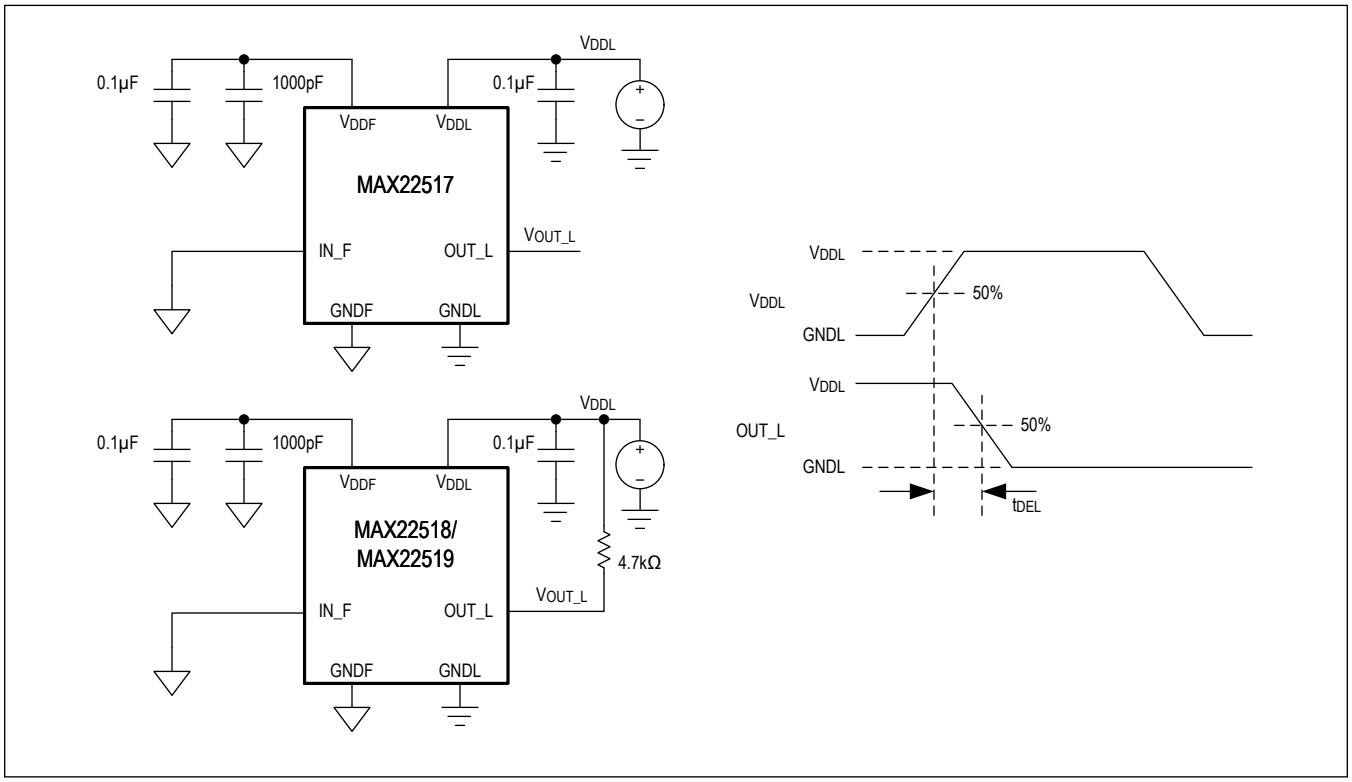


Figure 2. Power-Up Delay Timing Diagram

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 5)		630		V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 5)		445		V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 5)		5000		V_P
Maximum Withstand Isolation Voltage (Table 1)	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 5, 6)		3500		V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 (Note 8)		10		kV
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C		> 10^{12}		Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C		> 10^{11}		
		V_{IO} = 500V at T_S = 150°C		> 10^9		
Barrier Capacitance Field-Side to Logic-Side	C_{IO}	f_{SW} = 1MHz (Note 7)		2		pF
Minimum Creepage Distance	CPG			5.5		mm
Minimum Clearance Distance	CLR			5.5		mm
Internal Clearance		Distance through insulation		0.015		mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)		> 400		
Climate Category				40/125/ 21		
Pollution Degree		DIN VDE 0110, Table 1		2		

Note 5: V_{ISO}, V_{IOTM}, V_{IOSM}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.

Note 6: Product is qualified at V_{ISO} for 60s. Not production tested.

Note 7: Capacitance is measured with all field-side pins tied together and all logic-side pins tied together.

Note 8: Devices are immersed in oil during surge characterization.

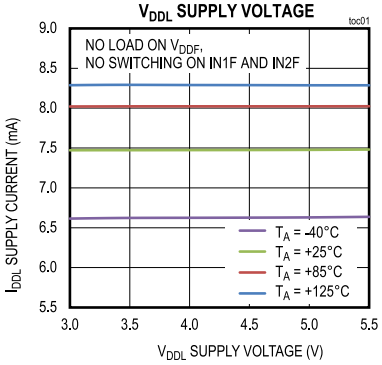
ESD and Transient Immunity Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Surge	IN_F to GNDF	IEC 61000-4-5, 1.2/50µs pulse, minimum 10kΩ resistor in series with IN_F		±1		kV
	IN_F to IN_F	IEC 61000-4-5, 1.2/50µs pulse, minimum 10kΩ resistor in series with IN_F		±2		
	IN_F to Earth	IEC 61000-4-5, 1.2/50µs pulse, minimum 10kΩ resistor in series with IN_F, 220pF Y capacitor between GNDL and Earth or GNDL is shorted to Earth		±10		
EFT	IN_F	IEC 61000-4-4, 5kHz or 100kHz repetition frequency, minimum 10kΩ resistor in series with IN_F		±4		kV
ESD	IN_F to GNDF	IEC 61000-4-2, Contact discharge, minimum 10kΩ resistor in series with IN_F		±8		kV
		IEC 61000-4-2, Air-Gap discharge, minimum 10kΩ resistor in series with IN_F		±15		
	IN_F to Earth	Human Body Model, minimum 10kΩ resistor in series with IN_F, 220pF Y capacitor between GNDF and Earth		±15		
	IN_F to GNDL	Human Body Model, minimum 10kΩ resistor in series with IN_F, 220pF Y capacitor between GNDF and GNDL		±15		
		All other pins, Human Body Model		±4		

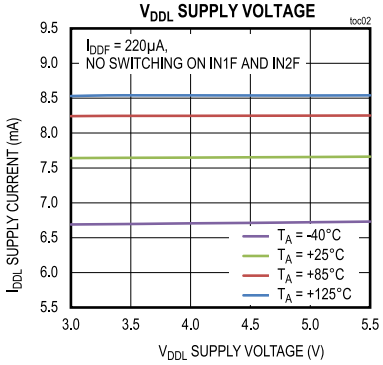
Typical Operating Characteristics

(V_{DDL} - V_{GNDL} = +3.3V, V_{GNDL} = V_{GNDF}, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

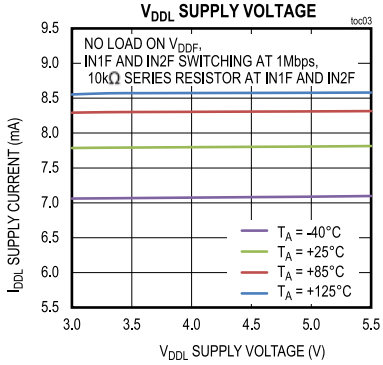
I_{DDL} SUPPLY CURRENT vs. V_{DDL} SUPPLY VOLTAGE



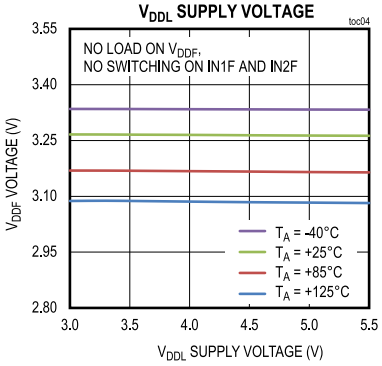
I_{DDL} SUPPLY CURRENT vs. V_{DDL} SUPPLY VOLTAGE



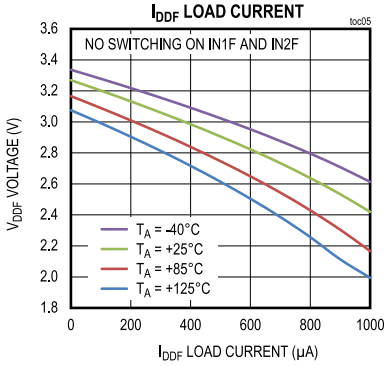
I_{DDL} SUPPLY CURRENT vs. V_{DDL} SUPPLY VOLTAGE



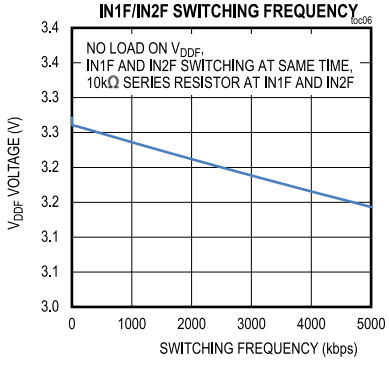
V_{DDF} VOLTAGE vs. V_{DDL} SUPPLY VOLTAGE



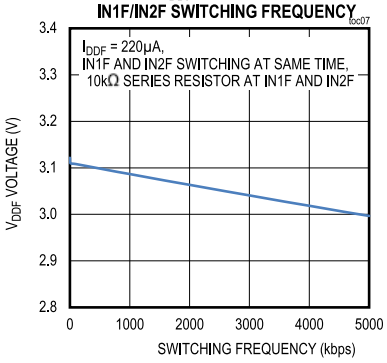
V_{DDF} VOLTAGE vs. I_{DDF} LOAD CURRENT



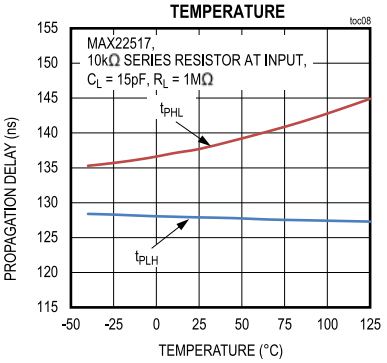
V_{DDF} VOLTAGE vs. IN1F/IN2F SWITCHING FREQUENCY



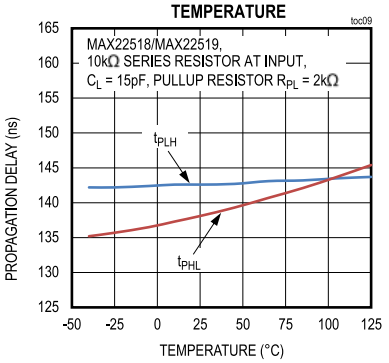
V_{DDF} VOLTAGE vs. IN1F/IN2F SWITCHING FREQUENCY



IN_F TO OUT_L PROPAGATION DELAY vs. TEMPERATURE



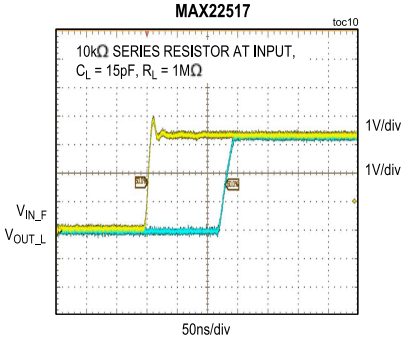
IN_F TO OUT_L PROPAGATION DELAY vs. TEMPERATURE



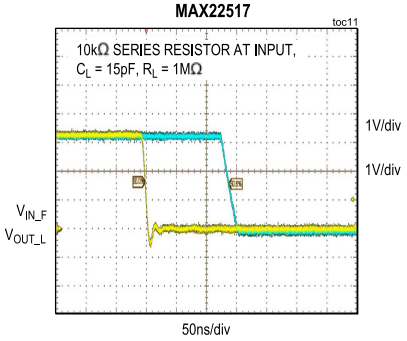
Typical Operating Characteristics (continued)

(V_{DDL} - V_{GNDL} = +3.3V, V_{GNDL} = V_{GNDF}, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

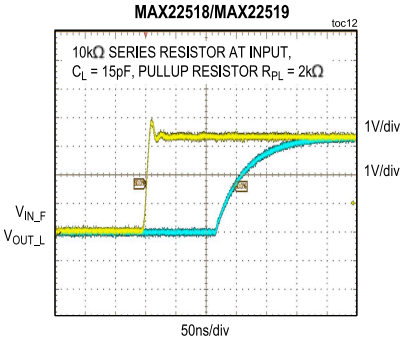
LOW-TO-HIGH PROPAGATION DELAY MAX22517



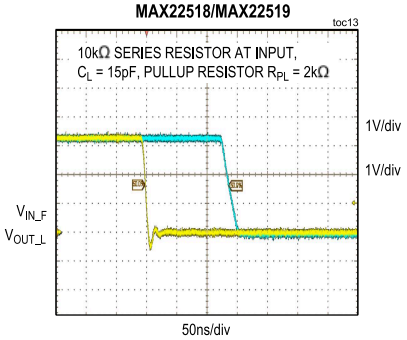
HIGH-TO-LOW PROPAGATION DELAY MAX22517



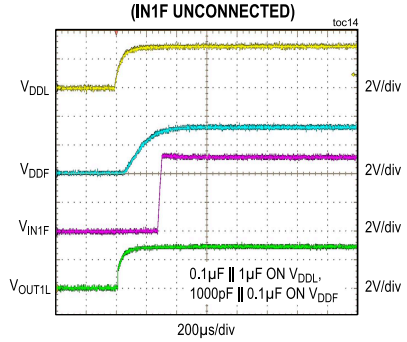
LOW-TO-HIGH PROPAGATION DELAY MAX22518/MAX22519



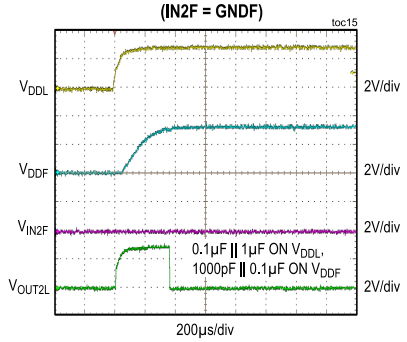
HIGH-TO-LOW PROPAGATION DELAY MAX22518/MAX22519



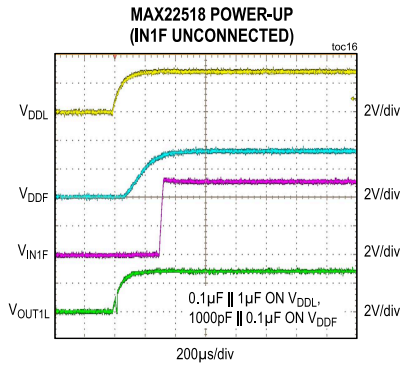
MAX22517 POWER-UP (IN1F UNCONNECTED)



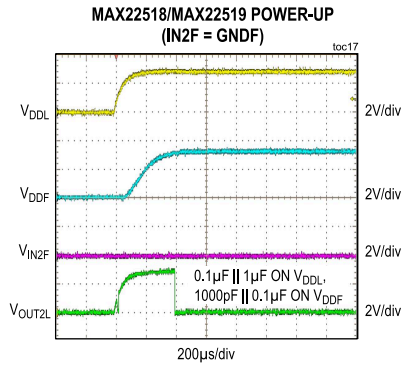
MAX22517 POWER-UP (IN2F = GNDF)



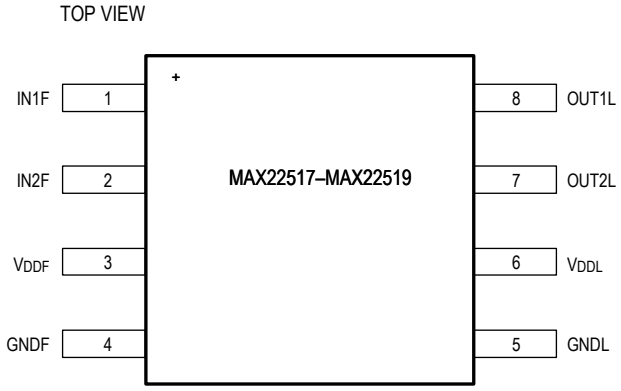
MAX22518 POWER-UP (IN1F UNCONNECTED)



MAX22518/MAX22519 POWER-UP (IN2F = GNDF)



Pin Configuration

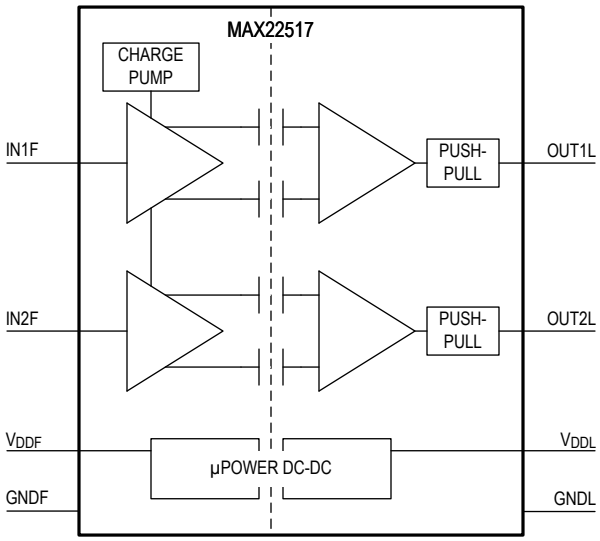


Pin Description

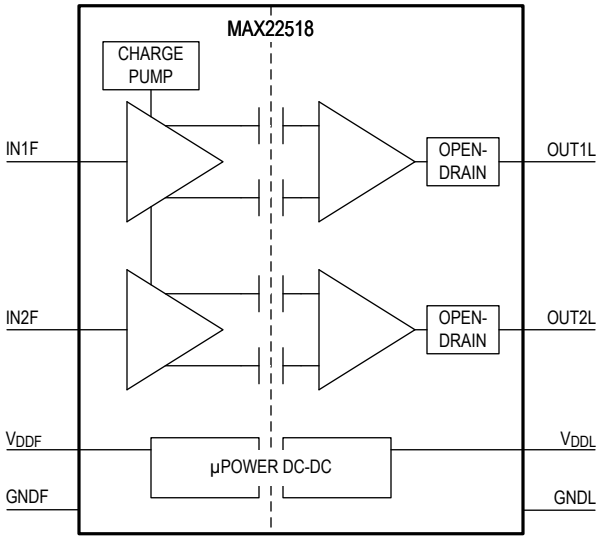
PIN	NAME	FUNCTION	REF SUPPLY
INPUTS			
1	IN1F	Field-Side Input 1. Corresponds to logic-side output 1. Place an optional minimum 10kΩ resistor between IN1F and the field input for protection.	GNDF
2	IN2F	Field-Side Input 2. Corresponds to logic-side output 2. Place an optional minimum 10kΩ resistor between IN2F and the field input for protection.	GNDF
POWER			
3	V_{DDF}	Field-Side Power Supply Output. Bypass V_{DDF} to GNDF with 1000pF || 0.1µF ceramic capacitors as close as possible to the pin.	GNDF
4	GNDF	Field-Side Ground Reference	—
5	GNDL	Logic-Side Ground Reference	—
6	V_{DDL}	Logic-Side Power Supply. Bypass V_{DDL} to GNDL with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDL
OUTPUTS			
7	OUT2L	Logic-Side Output 2. OUT2L is the logic output for the IN2F input on the field side. OUT2L is an open-drain output in the MAX22518 and MAX22519, so connect a pullup resistor between OUT2L and V_{DDL}. OUT2L is a push-pull output in the MAX22517.	GNDL
8	OUT1L	Logic-Side Output 1. OUT1L is the logic output for the IN1F input on the field side. OUT1L is an open-drain output in the MAX22518 and MAX22519, so connect a pullup resistor between OUT1L and V_{DDL}. OUT1L is a push-pull output in the MAX22517.	GNDL

Functional Diagrams

MAX22517

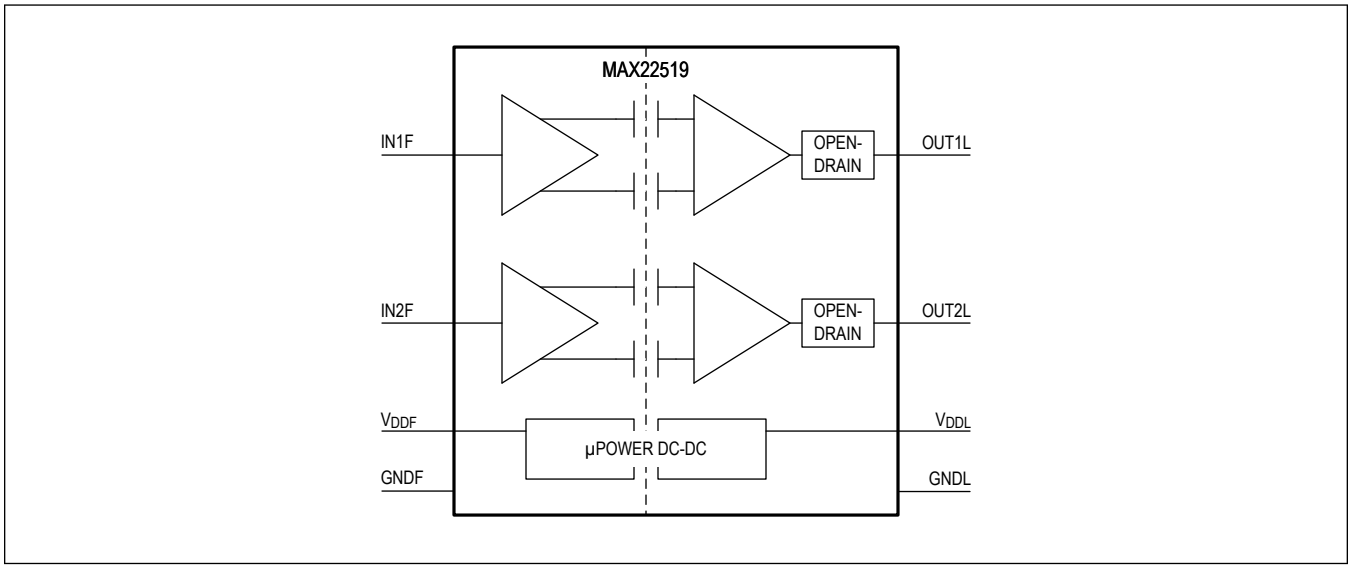


MAX22518



Functional Diagrams (continued)

MAX22519



Detailed Description

The MAX22517–MAX22519 are a family of dual-channel digital galvanic isolators with integrated field-side supply. The field-side power is supplied by the logic side through an integrated isolated DC-DC converter. All of the devices in the family feature basic isolation with an isolation rating of 3.5kV$_{RMS}$ for 60s. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology.

The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. With a single resistor on each input, the inputs of the MAX22517-MAX22519 can withstand 1.2/50µs surge pulses up to ±2kV between inputs (common mode) or up to ±1kV between input and field-ground (differential), as well as continuous short to 24VAC. The MAX22517–MAX22519 provide compact, reliable, and cost-efficient solutions for applications such as industrial IoT, industrial networking systems, and building automation.

Both channels of the MAX22517–MAX22519 transfer data from the field side to the logic side and are always enabled. The device senses the field-side voltage at the IN1F and IN2F pins and compares it against the internal reference levels to determine whether the input is on (logic 1) or off (logic 0). The input state is then transferred to the logic-side output through the capacitive isolation barrier. The inputs of the MAX22517 and MAX22518 feature a boost voltage that provides enough wetting current to clean relay contacts that makes them ideal for use in relay contact detection applications.

Isolated Field-Side Power Supply

As shown in the *Functional Diagrams*, the logic-side supply V_{DDL} powers an integrated DC-DC converter that generates a nominal 3.3V output (V_{DDF}) on the field side. When the input data rate is less than 100kbps, the isolated DC-DC converter provides enough current to power the field side of the MAX22517–MAX22519 as well as up to 220µA to external circuits, such as a window comparator or relay contact detection circuit. This approach eliminates the bulky and expensive external isolated power supply when the power demand of the field side is small.

Digital Isolation

The MAX22517–MAX22519 provide basic galvanic isolation for both power and digital signals that are transmitted from the field side to the logic side. The devices withstand differences in ground potential between the two power domains of up to 3.5kV$_{RMS}$ (V_{ISO}) for up to 60s, and up to 445V$_{RMS}$ (V_{IOWM}) for extended periods of time. See Table 1 for certification information. The devices withstand surge voltages up to 10kV (1.2/50µs pulses).

All of the devices in the MAX22517–MAX22519 family are available in a 8-pin wide-body SOIC package with 5.5mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400V to give it a group II rating in creepage tables.

Table 1. Safety Regulatory Approvals

UL
The MAX22517–MAX22519 are certified under UL1577. For more details, refer to File E351759.
Rated up to 3500V$_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22517–MAX22519 are certified up to 3500V$_{RMS}$ for single protection. For more details, refer to File E351759.

Field Input Charge Pump

The MAX22517 and MAX22518 are equipped with a built-in charge pump at the IN1F and IN2F pins, which makes the devices ideal for use in relay contact detection applications. The charge pump charges the external capacitor with a nominal 5.25V boost voltage providing a typical 5µA boost current. When the input is connected to a relay and the relay contact is switched to the closed position, the charge stored in the capacitor provides enough energy to clean any residual oxidation on the relay contact. The input series resistor should be carefully selected to allow enough current to charge the external capacitor while protecting the field inputs from surge pulses and continuous shorts to 24VAC.

The MAX22519 does not come with input charge pumps. Instead, it features internal pullup current sources to V_{DDF} at the IN1F and IN2F pins.

Field Input Protection

With a single input series resistor of 10kΩ or greater, the input pins (IN1F and IN2F) of the MAX22517–MAX22519 are protected from 1.2/50µs surge pulses up to ±2kV between inputs (common mode) or up to ±1kV between input and field ground (differential), as well as continuous shorts to 24VAC. See the *ESD and Transient Immunity Characteristics* table for details.

When a discharging capacitor is used to clean the oxidation growth on the relay contact, a TVS is recommended to protect it, unless the capacitor is sized properly for the application. See the *Typical Application Circuits* section for details.

Unidirectional Channels and Logic Outputs

Both channels of the MAX22517–MAX22519 are unidirectional; they only pass data from the field side to the logic side, as indicated in the *Functional Diagrams* section.

Both sides of the isolators are powered from a single 3.0V to 5.5V supply on the logic side, which also sets the output logic level. This family of the devices offers two different types of the output drivers. The MAX22517 features push-pull output drivers with an output-high default state. The MAX22518 and MAX22519 have open-drain output drivers with a high-impedance output default state. The default is the state the output assumes when either power domain of the device is undervoltage or the input is open-circuit. The open-drain output requires a pullup resistor between the OUT_L pins and V_{DDL}. See the *Ordering Information* for part numbers associated with different input and output options.

Startup and Undervoltage Lockout

The V_{DDL} and V_{DDF} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage on V_{DDL}, or heavy loads on V_{DDF}. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs (Table 2 and Table 3). Figure 3 through Figure 6 show the behavior of the outputs during power-up and power-down.

The internal DC-DC converter still operates when V_{DDL} is in UVLO (2.82V, typ). The field input charge pumps (MAX22517 and MAX22518 only) stop operating when V_{DDF} is in UVLO (2.1V, typ).

Table 2. MAX22517 Output Behavior During Undervoltage Conditions

V_{IN_F}	V_{DDF}	V_{DDL}	V_{OUT_L}
1	Powered	Powered	High
0	Powered	Powered	Low
X	Undervoltage	Powered	High
X	Don't Care	Undervoltage	High

Note: *The internal DC-DC converter still operates when V_{DDL} is in UVLO (2.82V, typ).*

Table 3. MAX22518/MAX22519 Output Behavior During Undervoltage Conditions

V_{IN_F}	V_{DDF}	V_{DDL}	V_{OUT_L}
1	Powered	Powered	High impedance
0	Powered	Powered	Low
X	Undervoltage	Powered	High impedance
X	Don't care	Undervoltage	High impedance

Note: *The internal DC-DC converter still operates when V_{DDL} is in UVLO (2.82V, typ).*

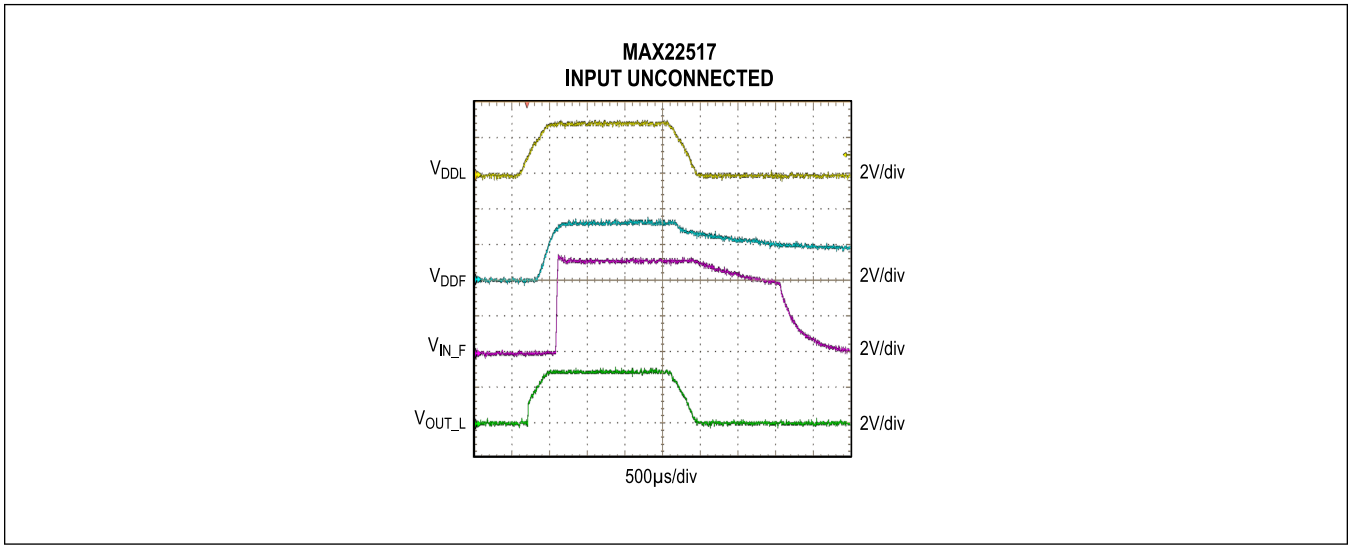


Figure 3. Undervoltage Lockout Behavior (MAX22517, Input Unconnected)

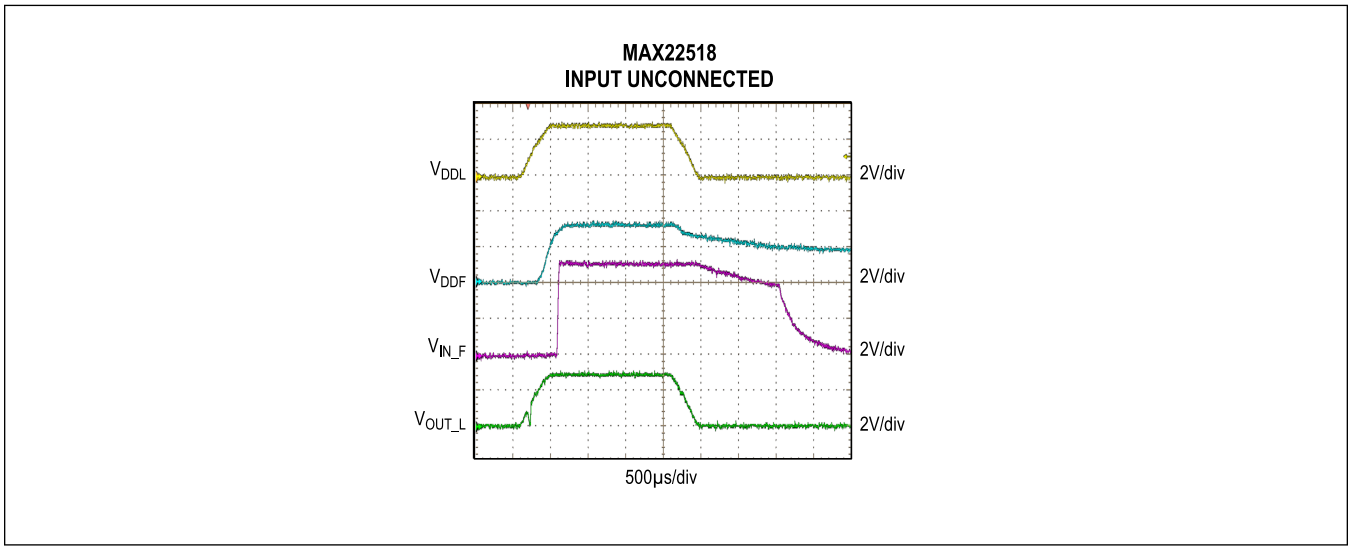


Figure 4. Undervoltage Lockout Behavior (MAX22518, Input Unconnected)

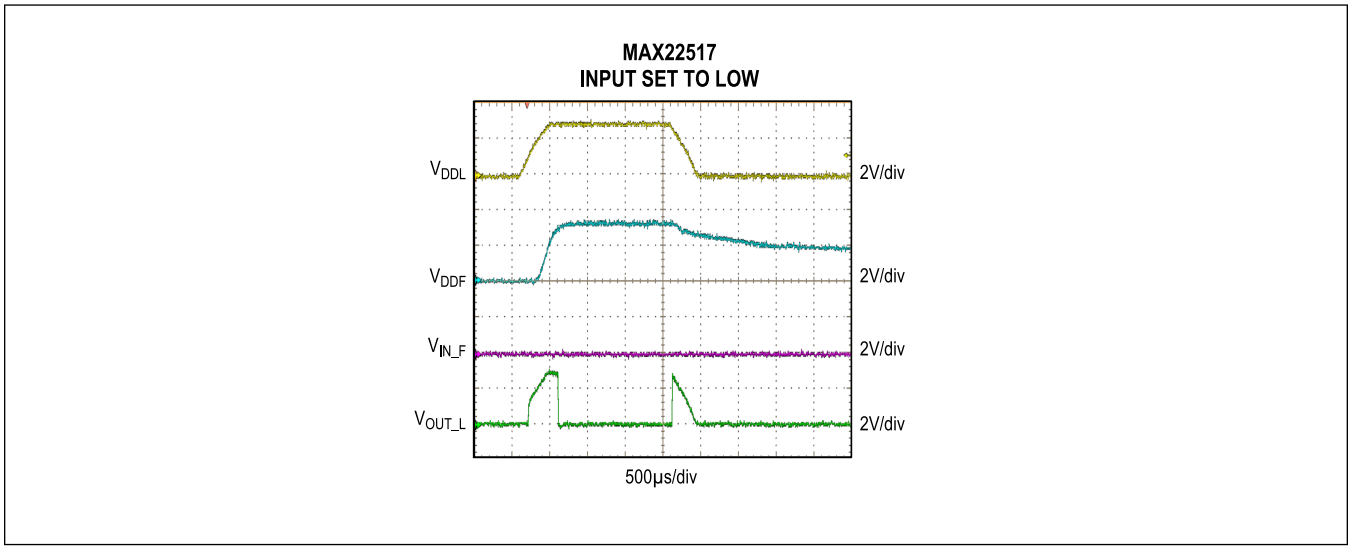


Figure 5. Undervoltage Lockout Behavior (MAX22517, Input Low)

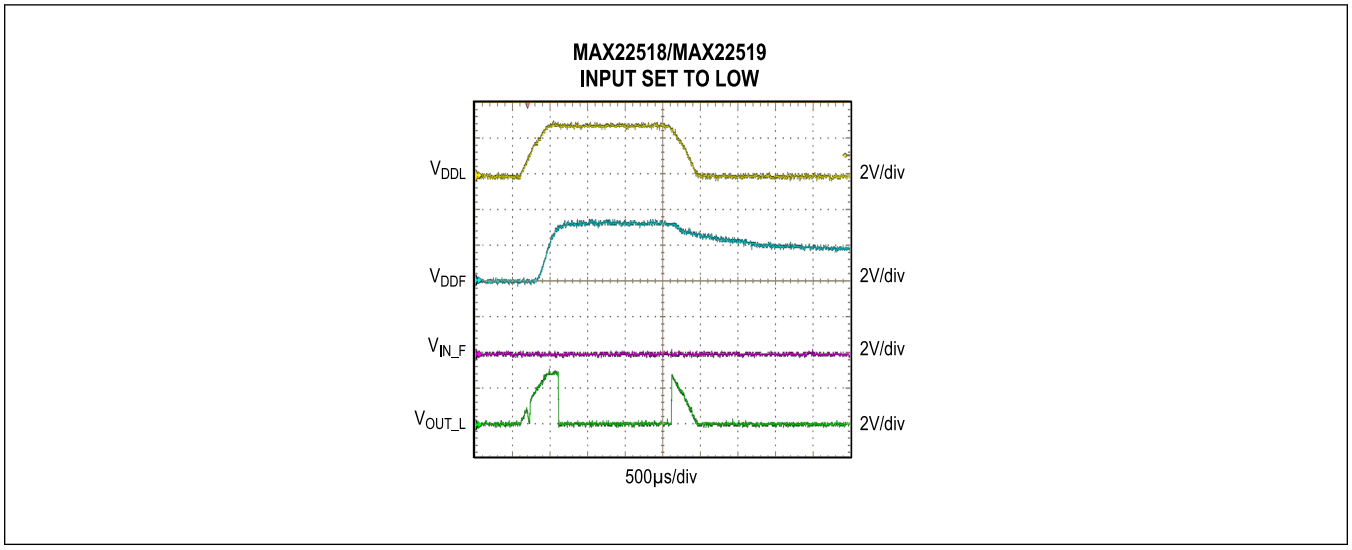


Figure 6. Undervoltage Lockout Behavior (MAX22518/MAX22519, Input Low)

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22517–MAX22519 can dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing long-term reliability issues. Table 4 shows the safety limits for the MAX22517–MAX22519.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings* section. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section of the data sheet. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 7 and Figure 8 show the thermal derating curve for safety limiting the power and the current of the device. Ensure that the junction temperature does not exceed 150°C.

Table 4. Safety Limiting Values for the MAX22517–MAX22519

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = +150°C, T_A = +25°C	200	mA
Total Safety Power Dissipation	P_S	T_J = +150°C, T_A = +25°C	1174	mW
Maximum Safety Temperature	T_S		150	°C

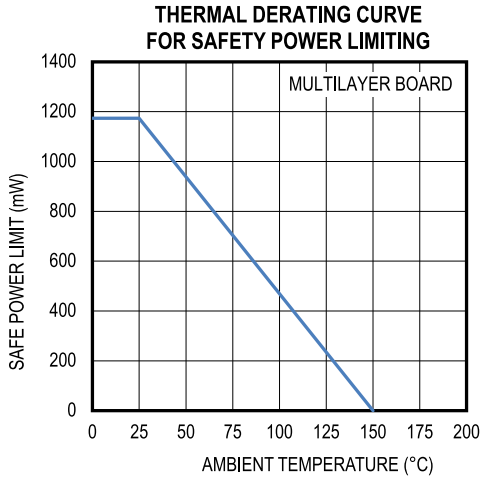


Figure 7. Thermal Derating Curve for Safety Power Limiting

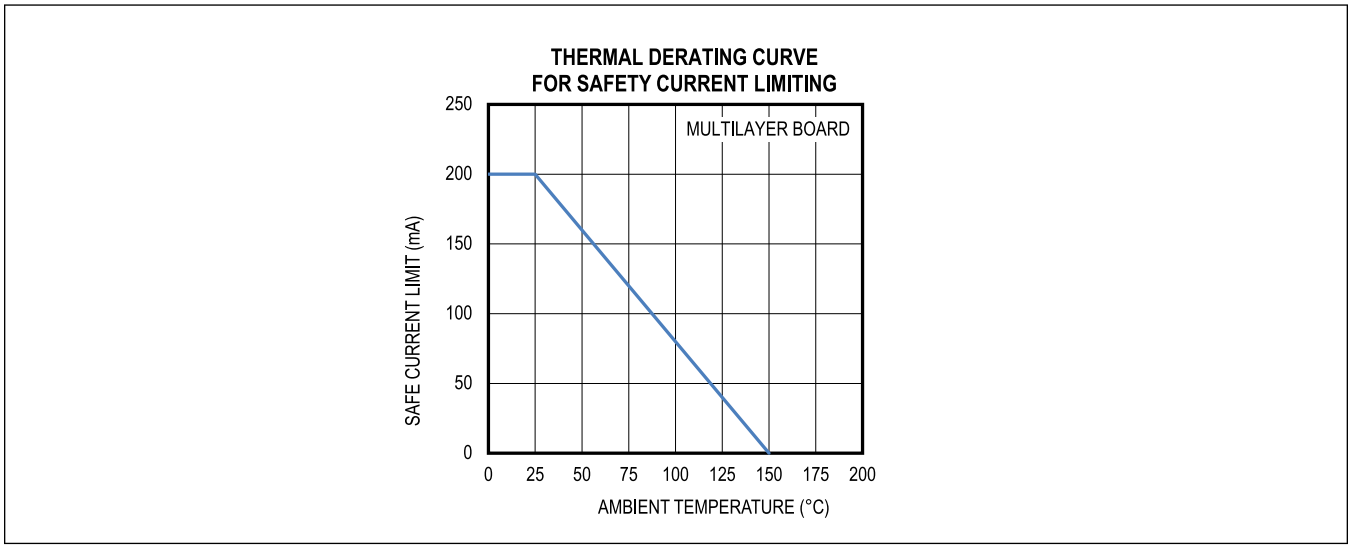


Figure 8. Thermal Derating Curve for Safety Current Limiting

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDL} with a 0.1µF low-ESR ceramic capacitor to GNDL, and place the bypass capacitor as close to the V_{DDL} pin as possible.

The V_{DDF} pin is the integrated DC-DC converter output. It is recommended to decouple it with low-ESR capacitors, 0.1µF in parallel with 1000pF, to GNDF. Place the 1000pF capacitor as close as possible to the V_{DDF} pin.

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Have a solid ground plane underneath the signal layer to minimize the noise.
- Keep the area underneath the MAX22517–MAX22519 free from ground and signal planes. Any galvanic or metallic connection between the field side and logic side defeats the isolation.

Typical Application Circuits

The MAX22517 and MAX22518 are designed for relay contact detection applications. The relay state is continuously monitored by the inputs, and transmitted across the isolation barrier to the logic side. The output pins indicate the real-time relay status. See the *Typical Application Circuits* section for details.

The input charge pump provides a nominal 5.25V voltage and a typical 5µA current to charge an external capacitor. When the relay contact is switched to the closed position, the energy stored in the capacitor cleans the relay of any oxidation residue. The input pins are also protected from hazardous high-voltage transients such as ±1kV input-to-GNDF surge with a single input series resistor per channel.

When the input data rate is less than 100kbps, the isolated field-side supply output V_{DDF} is able to supply up to 220µA to power external field-side circuits such as window comparators or other relay detection circuits.

When the field-side power collapses or is lost, the outputs enter the default state so that the logic-side control unit is not falsely informed a relay is closed.

Radiated Emission

The MAX22517–MAX22519 feature an integrated DC-DC converter to generate a nominal 3.3V supply, powering the field side of the MAX22517–MAX22519 as well as external circuits that consume less than 220µA power. The DC-DC converter uses a switching frequency of 750MHz (typ) to pass power from the logic side across the isolation barrier through an internal transformer. Due to the isolated nature of the device, the split of the ground planes (GNDL and GNDF) prevents the return current from flowing back to the logic side, thus causing high-frequency signals to radiate when crossing the isolation barrier.

The MAX22517–MAX22519 can meet CISPR 22 and FCC radiated emission standards with proper PCB design. A stitching capacitance of 30pF minimum is recommended to be built into the PCB to pass the CISPR 22 and FCC Class B limits. See Figure 11 and Figure 12.

To achieve optimal radiated emission performance, the following layout guidelines are recommended:

- Use at least 4-layer PCB stackup with GNDL and GNDF ground planes on two adjacent internal layers.
- Extend the GNDF and GNDL planes on two adjacent layers so they overlap each other, thus creating a stitching capacitance between GNDL and GNDF. See Figure 9 and Figure 10.
- Calculate the stitching capacitance value by using the following equation, where A is the overlapping area between the GNDL and GNDF planes, ε_0 is the permittivity of free space (8.854 x 10^{-12} F/m), ε_R is the relative permittivity of the PCB insulation material, and d is the dielectric thickness between two adjacent layers.

$$C = \frac{A \times \varepsilon_0 \times \varepsilon_r}{d}$$

- Adjust the overlapping area A or the dielectric thickness d to achieve a minimum 30pF stitching capacitance. Make sure that the creepage and clearance between the GNDF plane and the GNDL plane on the same layer as well as between two different layers are large enough to meet isolation standards for various applications.
- Multiple GNDL and GNDF vias are recommended to be placed next to the GNDF and GNDL pins to provide a good connection between the stitching capacitor and the device ground pins.
- Apply edge guarding vias to stitch the GNDF and GNDL planes on all layers together to limit the emission from escaping from the PCB edges.

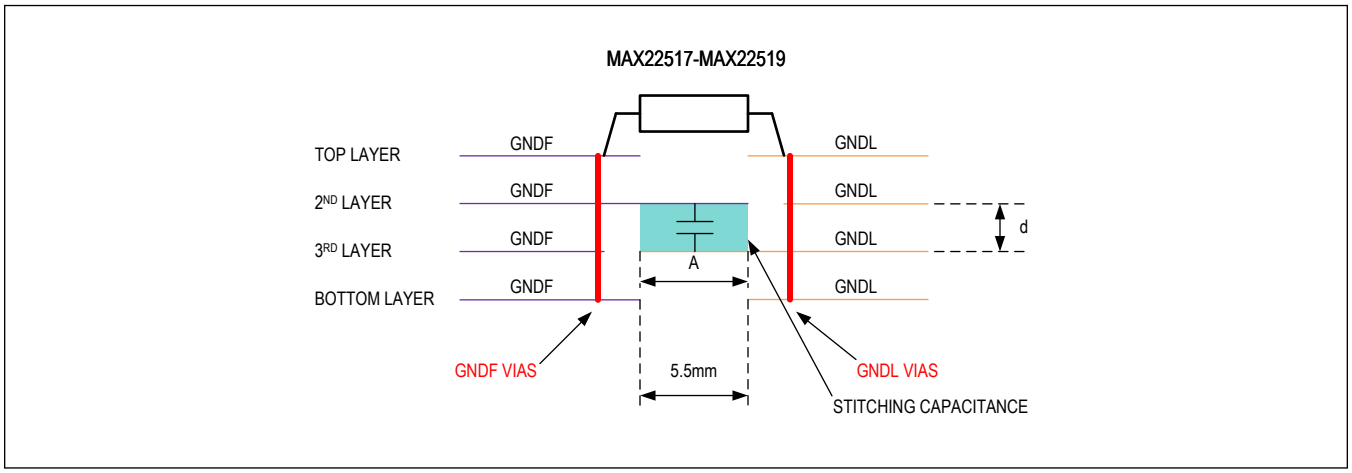


Figure 9. Stitching Capacitance Example on a 4-Layer PCB

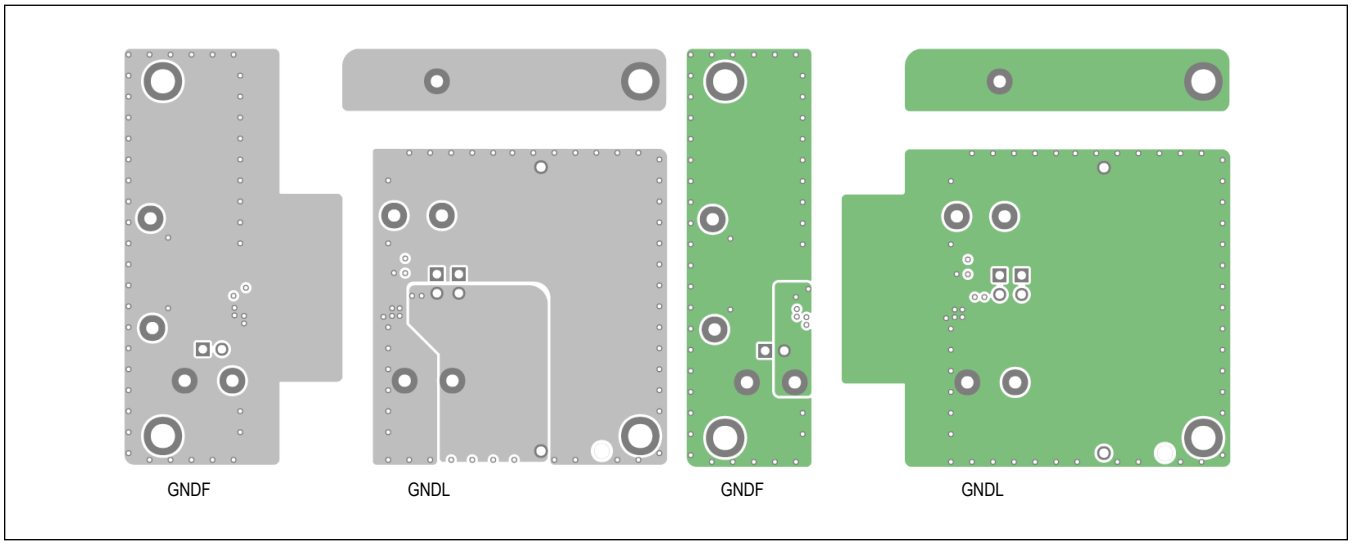


Figure 10. Stitching Capacitance on Internal Layers

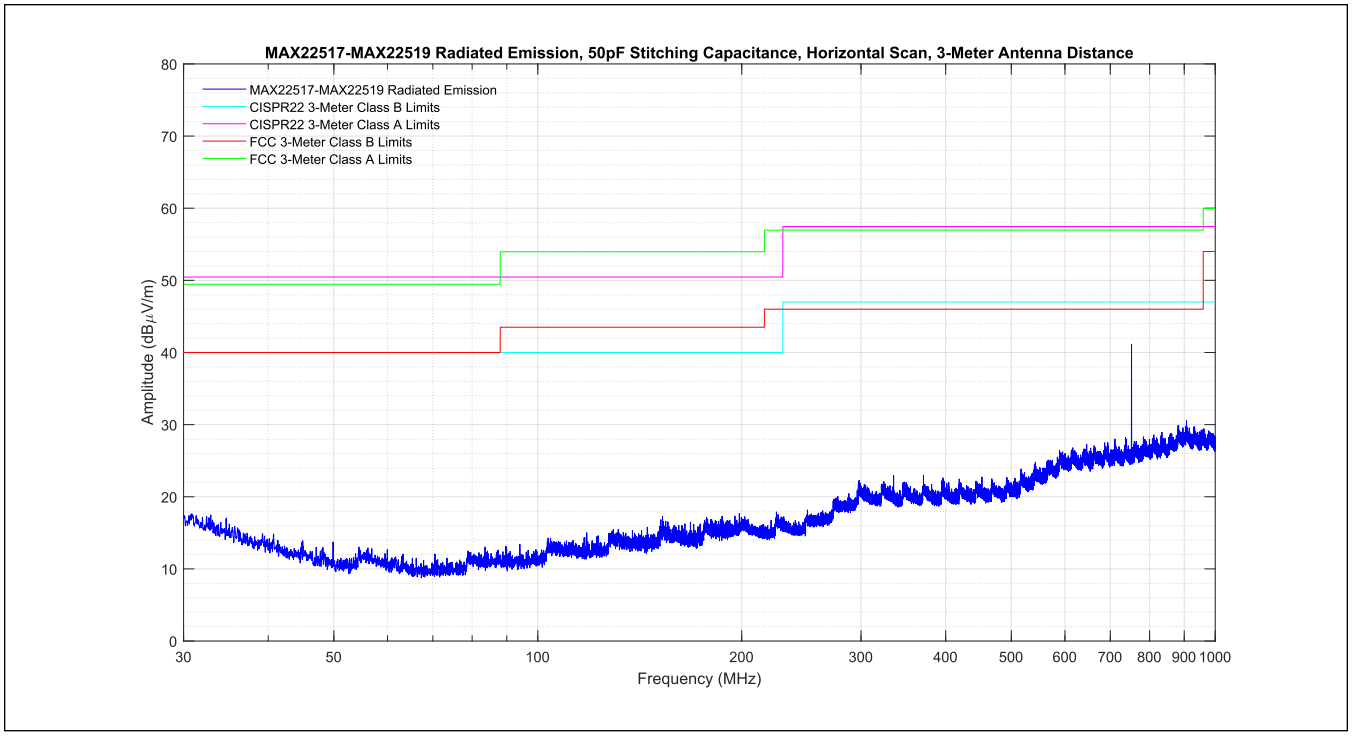


Figure 11. Radiated Emission with 50pF Stitching Capacitance, 3-Meter Antenna Distance, Horizontal Scan

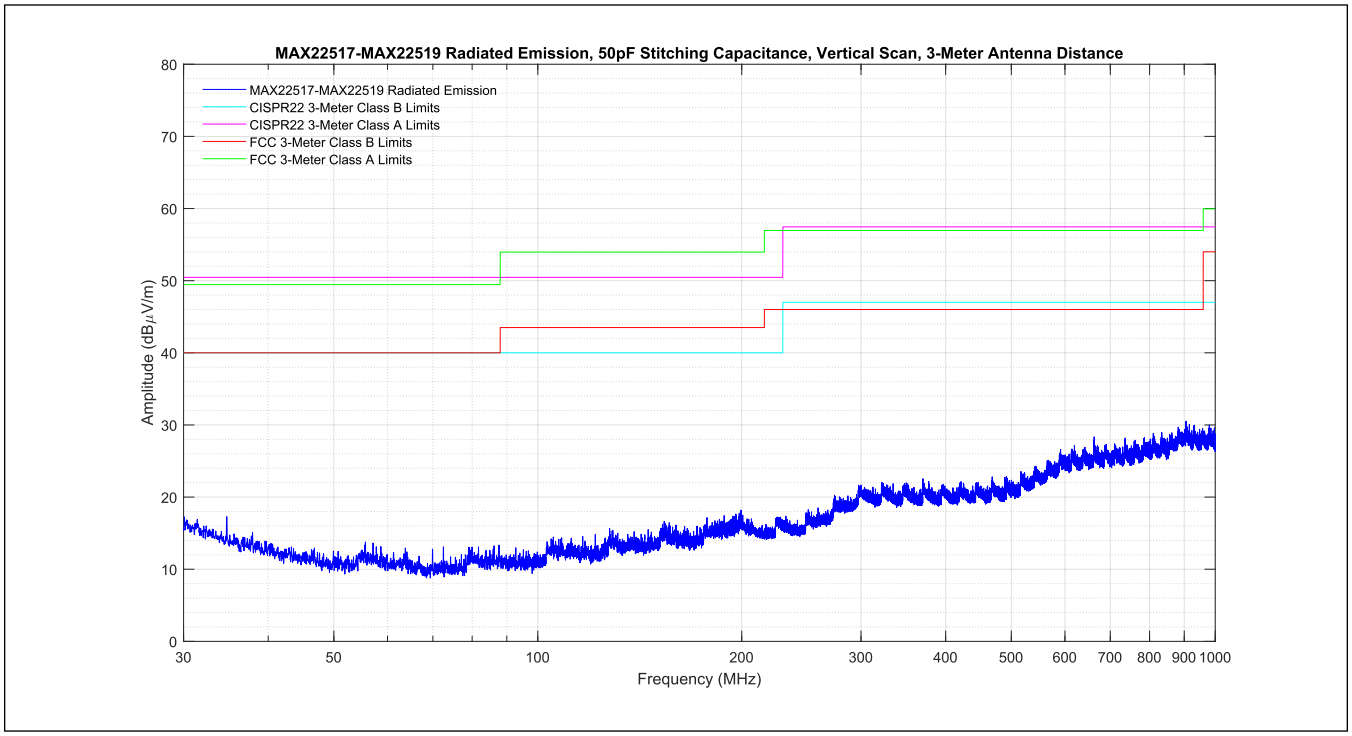
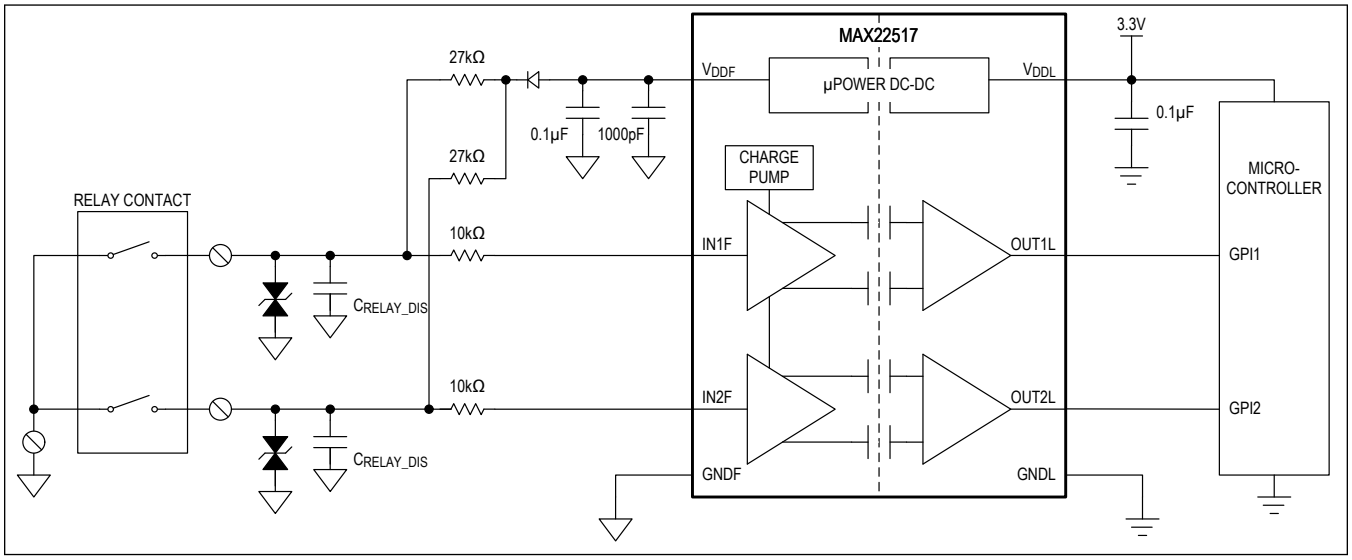


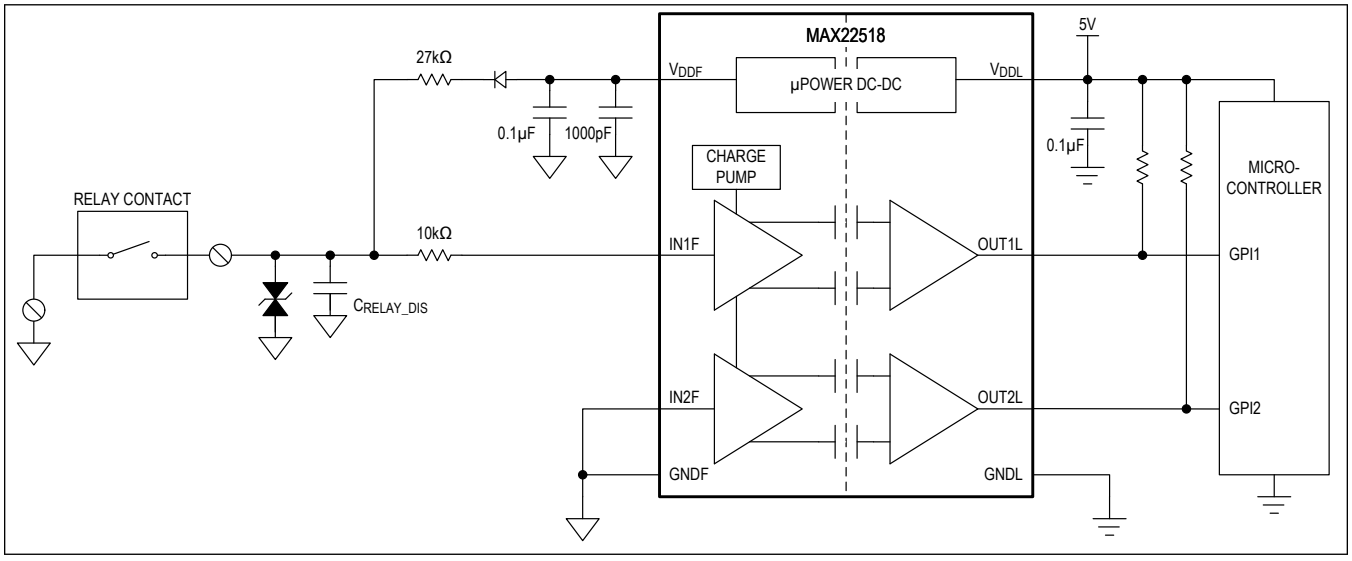
Figure 12. Radiated Emission with 50pF Stitching Capacitance, 3-Meter Antenna Distance, Vertical Scan

Typical Application Circuits

Dual Relay Contact Monitoring System

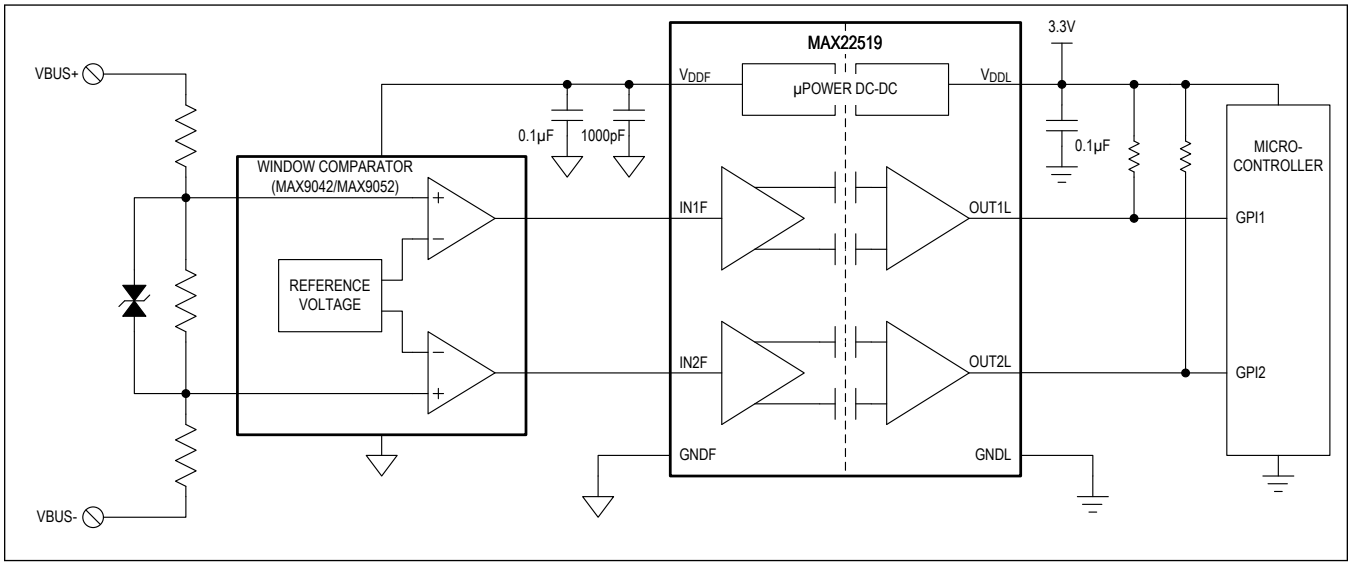


Single-Channel Relay Contact Monitoring With Self-Diagnostics



Typical Application Circuits (continued)

Isolated Power Monitoring System



Ordering Information

PART NUMBER	ISOLATION RATING (V_{RMS})	IN_F CHARGE PUMP	OUT_L DEFAULT	OUT_L TYPE	PIN-PACKAGE
MAX22517AWA+*	3500	Yes	High	Push-pull	8 Wide SOIC
MAX22518AWA+	3500	Yes	High impedance	Open drain	8 Wide SOIC
MAX22519AWA+*	3500	No	High impedance	Open drain	8 Wide SOIC

**Future product—contact Maxim for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/20	Initial release	—

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