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Reinforced, Fast, Low-Power, Six-Channel Digital Isolators

MAX22563-MAX22566

Product Highlights

- **AEC-Q100 Qualification for /V Devices**
- Reinforced Galvanic Isolation for Digital Signals
  - 20-SSOP with 5.5mm Creepage and Clearance
  - Withstands $3.75kV_{RMS}$ for 60s (V_{ISO})
  - Continuously Withstands $784V_{RMS}$ (V_{IOWM})
  - Withstands ±12.8kV Surge Between GNDA and GNDB with 1.2/50μs Waveform
  - High CMTI (50kV/μs, typ)
- Low Power Consumption
  - 0.71mW per Channel at 1Mbps with V_{DD} = 1.8V
  - 1.34mW per Channel at 1Mbps with V_{DD} = 3.3V
  - 3.21mW per Channel at 100Mbps with V_{DD} = 1.8V
- Low Propagation Delay and Low Jitter
  - Maximum Data Rate Up to 200Mbps
  - Low Propagation Delay 7ns (typ) at V_{DD} = 3.3V
  - Clock Jitter RMS 11.1ps (typ)
- Safety Regulatory Approvals (Pending)
  - UL According to UL1577
  - cUL According to CSA Bulletin 5A
  - VDE 0884-11 Reinforced Insulation

Key Applications

- Automotive
  - Hybrid Electric Vehicle
  - Chargers
  - Battery Management System (BMS)
  - Inverters

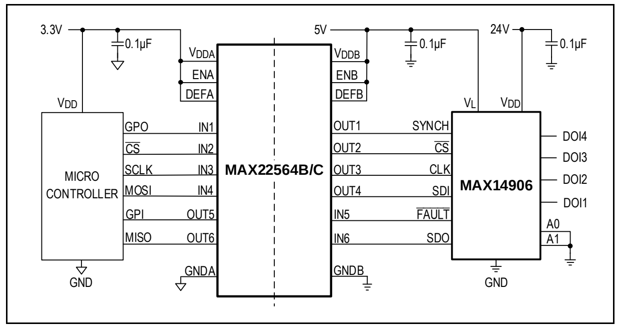
The MAX22563−MAX22566 are a family of 6-channel, reinforced, fast, low-power digital galvanic isolators using Maxim Integrated's proprietary process technology. All devices feature reinforced isolation with a withstand voltage rating of $3.75kV_{RMS}$ for 60 seconds. Both automotive and general-purpose devices are rated for operation at ambient temperatures from -40°C to +125°C.

Devices with /V suffix are AEC-Q100 qualified. See the *Ordering Information* for all automotive grade part numbers.

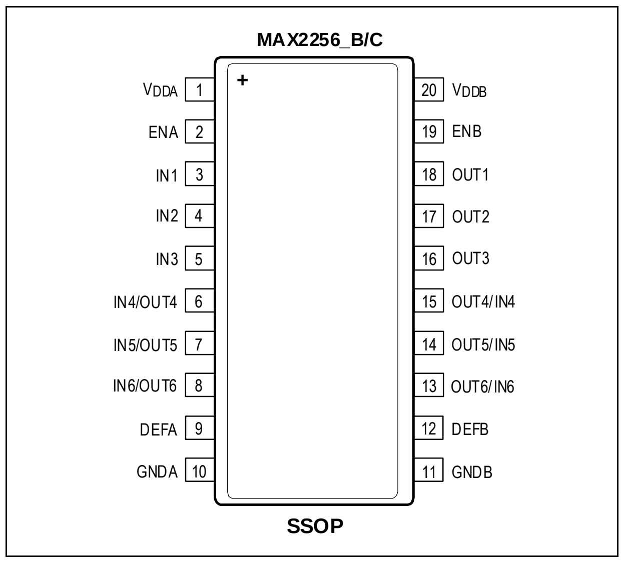
- Industrial
  - Isolated SPI, RS-232/422/485, CAN, Digital I/O
  - Fieldbus Communications
  - Motor Control
  - Medical Systems

These devices transfer digital signals between circuits with different power domains, using as little as 0.71mW per channel at 1Mbps (1.8V supply). The low-power feature reduces system dissipation, increases reliability, and enables compact designs.

Simplified Application Diagram



Pin Description



Devices are available with a maximum data rate of either 25Mbps or 200Mbps and with user-selectable default-high or default-low outputs. The devices feature low propagation delay and low clock jitter, which reduces system latency.

Independent 1.71V to 5.5V supplies on each side also make the devices suitable for use as level translators.

The MAX22563 features three channels transmitting signals in one direction and three in opposite; the MAX22564 offers four channels transmitting signals in one direction and two in opposite; the MAX22565 provides five channels transmitting signals in one direction and one in opposite; the MAX22566 features all six channels transmitting signals in one direction.

***Ordering Information* appears at end of data sheet.**

Absolute Maximum Ratings

V_{DDA} to GNDA..-0.3V to +6V
V_{DDB} to GNDB..-0.3V to +6V
IN_ on Side A, ENA, DEFA to GNDA ....-0.3V to +6V
IN_ on Side B, ENB, DEFB to GNDB ....-0.3V to +6V
OUT_ on Side A to GNDA .... -0.3V to (V_{DDA} + 0.3V)
OUT_ on Side B to GNDB .... -0.3V to (V_{DDB} + 0.3V)
Short-Circuit Continuous Current
OUT_ on Side A to GNDA .... ±30mA
OUT_ on Side B to GNDB..±30mA
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 10.60mW/°C above +70°C)..........848.36mW
Temperature Ratings
Operating Temperature Range .... -40°C to +125°C
Maximum Junction Temperature............................. +150°C
Storage Temperature Range .... -60°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow)............................... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 20 SSOP

Package Code	A20MS+7
Outline Number	*21-0056*
Land Pattern Number	*90-0094*
THERMAL RESISTANCE, FOUR LAYER BOARD:	
Junction-to-Ambient (θ_{JA})	94.30°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	43.70°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE							
Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	$V_{DD\_}$ rising		1.5	1.6	1.66	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				45		mV
MAX22563 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		1.23	2.28	mA
			V_{DDA} = 3.3V		1.22	2.25	
			V_{DDA} = 2.5V		1.21	2.24	
			V_{DDA} = 1.8V		1.18	1.97	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.83	10.26	
			V_{DDA} = 3.3V		6.47	8.71	
			V_{DDA} = 2.5V		5.90	8.03	
			V_{DDA} = 1.8V		5.35	7.10	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.23	2.28	mA
			V_{DDB} = 3.3V		1.22	2.25	
			V_{DDB} = 2.5V		1.21	2.24	
			V_{DDB} = 1.8V		1.18	1.97	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		7.83	10.26	
			V_{DDB} = 3.3V		6.47	8.71	
			V_{DDB} = 2.5V		5.90	8.03	
			V_{DDB} = 1.8V		5.35	7.10	
MAX22564 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		1.09	2.01	mA
			V_{DDA} = 3.3V		1.07	1.99	
			V_{DDA} = 2.5V		1.06	1.98	
			V_{DDA} = 1.8V		1.04	1.66	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.63	10.10	
			V_{DDA} = 3.3V		6.67	9.01	
			V_{DDA} = 2.5V		6.28	8.52	
			V_{DDA} = 1.8V		5.84	7.67	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.38	2.55	mA
			V_{DDB} = 3.3V		1.36	2.52	
			V_{DDB} = 2.5V		1.35	2.51	
			V_{DDB} = 1.8V		1.32	2.28	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		8.04	10.38	
			V_{DDB} = 3.3V		6.27	8.41	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{DDB} = 2.5V		5.54	7.53	
			V_{DDB} = 1.8V		4.87	6.53	
MAX22565 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.94	1.74	mA
			V_{DDA} = 3.3V		0.93	1.72	
			V_{DDA} = 2.5V		0.92	1.71	
			V_{DDA} = 1.8V		0.90	1.34	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.44	9.96	
			V_{DDA} = 3.3V		6.88	9.31	
			V_{DDA} = 2.5V		6.64	9.03	
			V_{DDA} = 1.8V		6.32	8.23	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.53	2.82	mA
			V_{DDB} = 3.3V		1.50	2.79	
			V_{DDB} = 2.5V		1.50	2.78	
			V_{DDB} = 1.8V		1.45	2.59	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		8.36	10.64	
			V_{DDB} = 3.3V		6.16	8.19	
			V_{DDB} = 2.5V		5.24	7.10	
			V_{DDB} = 1.8V		4.45	6.01	
MAX22566 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.79	1.47	mA
			V_{DDA} = 3.3V		0.78	1.45	
			V_{DDA} = 2.5V		0.78	1.44	
			V_{DDA} = 1.8V		0.75	1.02	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		7.25	9.81	
			V_{DDA} = 3.3V		7.08	9.61	
			V_{DDA} = 2.5V		7.00	9.52	
			V_{DDA} = 1.8V		6.78	8.79	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.67	3.09	mA
			V_{DDB} = 3.3V		1.65	3.06	
			V_{DDB} = 2.5V		1.64	3.05	
			V_{DDB} = 1.8V		1.59	2.89	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		8.57	10.81	
			V_{DDB} = 3.3V		5.97	7.91	
			V_{DDB} = 2.5V		4.89	6.62	
			V_{DDB} = 1.8V		3.97	5.44	
LOGIC INTERFACE (IN_, OUT_, EN_, DEF_)							
Input High Voltage	V_{IH}	IN_, EN_, DEF_	2.25V ≤ $V_{DD\_}$ ≤ 5.5V	0.7 x V_{DD}			V

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			1.71V ≤ $V_{DD\_}$ < 2.25V	0.75 x V_{DD}			
Input Low Voltage	V_{IL}	IN_, EN_, DEF_	2.25V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	V
			1.71V ≤ $V_{DD\_}$ < 2.25V			0.7	
Input Hysteresis	V_{HYS}	IN_, EN_, DEF_	MAX2256_B		410		mV
			MAX2256_C		80		
Input Pullup Current	I_{PU}	DEFA = DEFB = high		-10	-5	-1.5	µA
Input Pulldown Current	I_{PD}	DEFA = DEFB = low		1.5	5	10	µA
Input Capacitance	C_{IN}	f_{SW} = 1MHz			2		pF
EN_ Pullup Current	$I_{PU\_EN\_}$			-10	-5	-1.5	µA
DEF_ Pullup Current	$I_{PU\_DEF\_}$			-10	-5	-1.5	µA
Output Voltage High	V_{OH}	I_{OUT} = -4mA source		$V_{DD\_}$ - 0.4			V
Output Voltage Low	V_{OL}	I_{OUT} = 4mA sink				0.4	V

Dynamic Characteristics - MAX2256_C

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 5)			50		kV/µs
Maximum Data Rate	DR_{MAX}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		200			Mbps
		1.71V ≤ $V_{DD\_}$ < 2.25V		150			
Minimum Pulse Width	PW_{MIN}	IN_ to OUT_	2.25V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
			1.71V ≤ $V_{DD\_}$ < 2.25V			6.67	
Propagation Delay (*Figure 1*)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.4	6.2	9.5	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	4.8	7.0	11.2	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.3	8.3	14.7	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.1	12.3	22.1	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.6	6.5	9.9	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	5.0	7.3	11.6	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.4	8.5	14.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.2	12.1	21.8	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		0.4	2.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		0.4	2.0	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		0.3	2.0	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V		0	2.0	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.7	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				6.9	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				12.1	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.9	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				7.0	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				11.8	
Propagation Delay Skew Channel-to-Channel (Same Direction) (*Figure 1*)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2.0	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2.0	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.7	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				6.9	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				12.1	
	t_{SCOHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.9	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				7.0	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				11.8	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	200Mbps			100		ps
Clock Jitter RMS	$t_{JCLK(RMS)}$	500kHz clock input, rising/falling edges			11.1		ps
Rise Time (*Figure 1*)	t_R	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			2.4	
Fall Time (*Figure 1*)	t_F	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			3.0	
Enable to Data Valid (*Figure 2*)	t_{EN}	MAX2256_, EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			3.9	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5.9	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			9.1	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			15.8	
Enable to Tri-state (*Figure 2*)	t_{TRI}	MAX2256_, EN_ to OUT_,	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			6.2	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			8.7	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		C_L = 15pF	2.25V ≤ $V_{DD\_}$ ≤ 2.75V			11.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			17.8	

Dynamic Characteristics - MAX2256_B

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 5)			50		kV/µs
Maximum Data Rate	DR_{MAX}			25			Mbps
Minimum Pulse Width	PW_{MIN}	IN_ to OUT_				40	ns
Glitch Rejection		IN_ to OUT_		10	17	29	ns
Propagation Delay (*Figure 1*)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.7	22.6	30.7	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	17.0	23.4	32.2	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.7	24.8	35.3	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.6	28.8	42.8	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.4	22.7	32.1	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	16.8	23.5	33.8	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.3	24.8	36.7	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.0	28.4	43.7	
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		0.2	4.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		0.2	4.0	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		0.3	4.0	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V		0.6	4.0	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				14.0	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.8	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.2	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.9	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				13.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.5	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.4	
Propagation Delay Skew Channel-to-Channel (Same Direction) (*Figure 1*)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	
	t_{SCOLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				14.0	ns

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposite Direction)		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.8	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.2	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.9	
	t_{SCOHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				13.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.5	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.4	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	25Mbps			250		ps
Rise Time (Figure 1)	t_R	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			2.4	
Fall Time (Figure 1)	t_F	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			3.0	
Enable to Data Valid (Figure 2)	t_{EN}	MAX2256_, EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			3.9	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5.9	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			9.1	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			15.8	
Enable to Tri-state (Figure 2)	t_{TRI}	MAX2256_, EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			6.2	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			8.7	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			11.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			17.8	

Note 1: General purpose devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization. Automotive devices are 100% production tested at T_A = +25°C and T_A = +125°C.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective grounds (GNDA or GNDB), unless otherwise noted.

Note 4: All measurements are taken with V_{DDA} = V_{DDB}, unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
ESD		Human Body Model, All Pins	±4	kV
ESD		IEC 61000-4-2 Contact, GNDB to GNDA	±8	kV

Test Circuit and Timing Diagrams

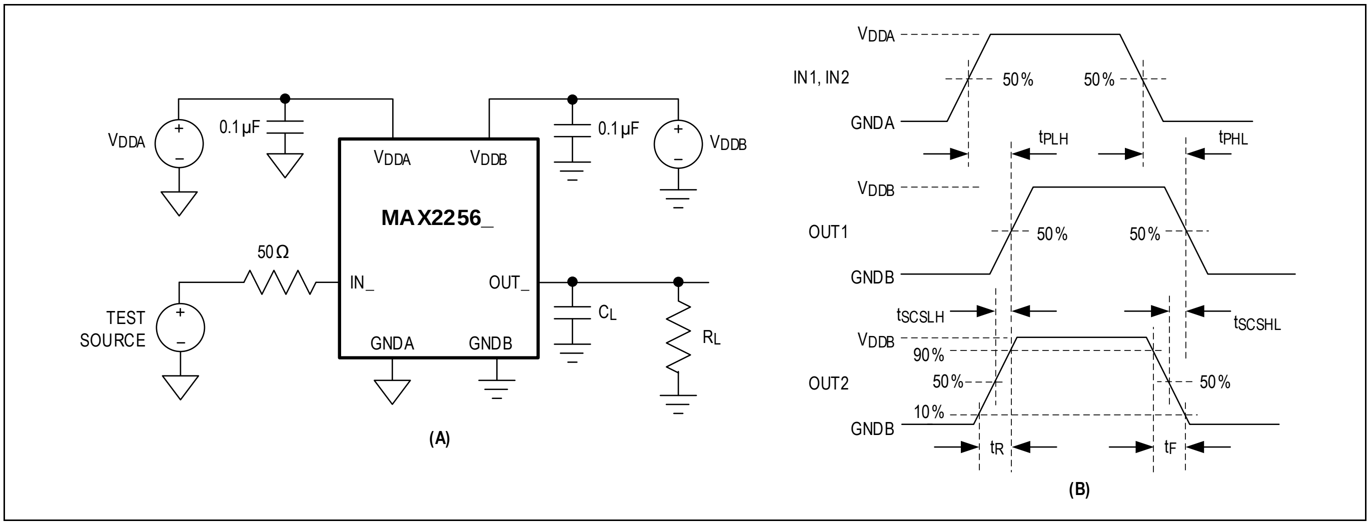


Figure 1. Test Circuit (A) and Timing Diagram (B)

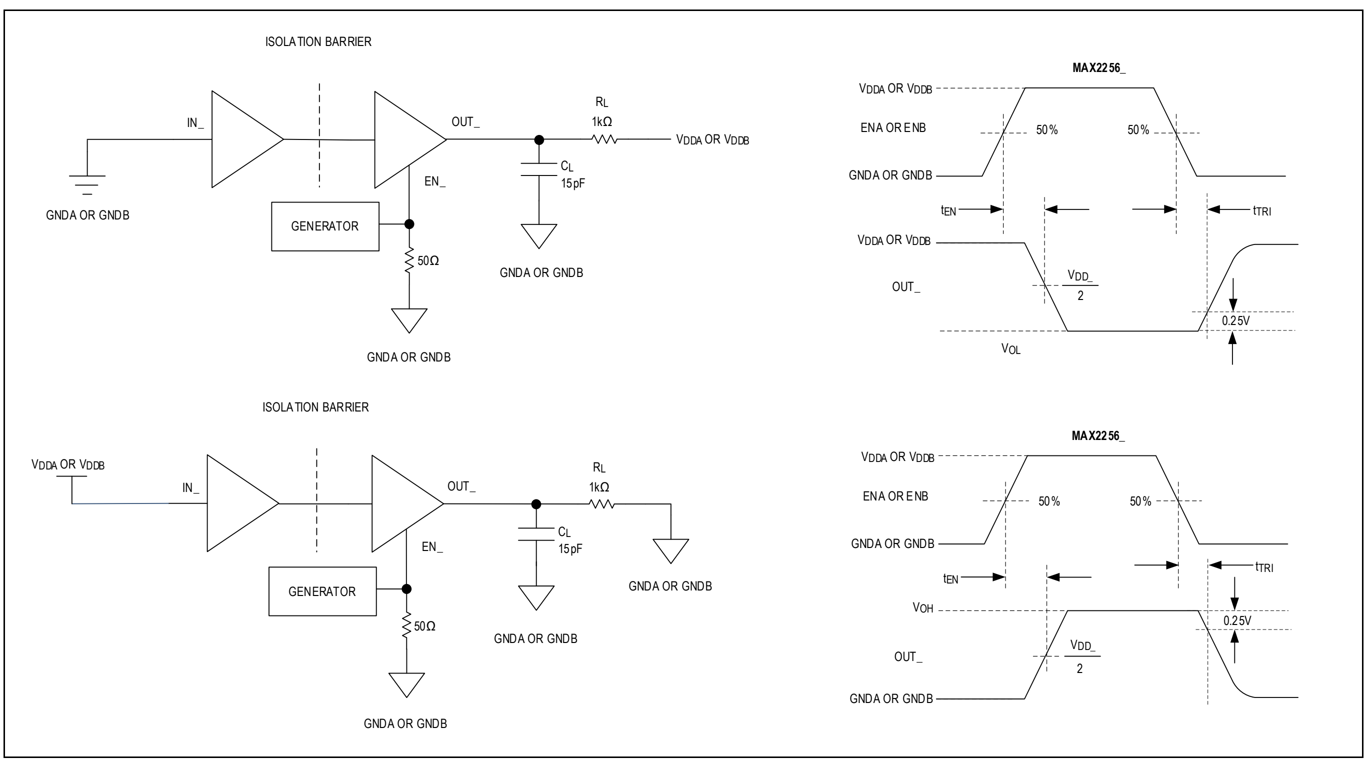


Figure 2. Enable to Output Timing (t_{EN}, t_{TRI})

Table 1. Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2,078	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 6)	1,108	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 6)	784	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 6)	5,300	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Notes 6, 7)	3,750	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 12,800V_{PEAK} (Notes 6, 9)	8,000	V_P
Isolation Resistance	R_{IO}	V_{IO} = 500V, T_A = +25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V, T_S = 150°C	$>10^{9}$	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 8)	1.5	pF
Minimum Creepage Distance	CPG		5.5	mm
Minimum Clearance Distance	CLR		5.5	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	>400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOWM}, V_{IOTM}, V_{IORM}, and V_{IOSM} are defined by the IEC 60747-5-5 standard.
Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 8: Capacitance is measured with all pins on the A side and B side tied together.
Note 9: Devices are immersed in oil during surge characterization.

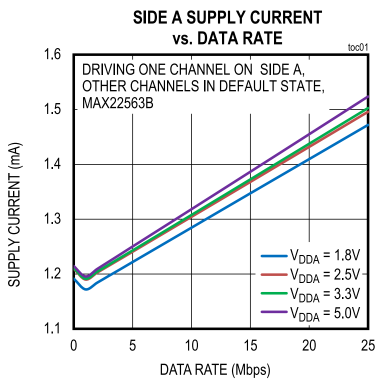
Safety Regulatory Approvals (Pending)

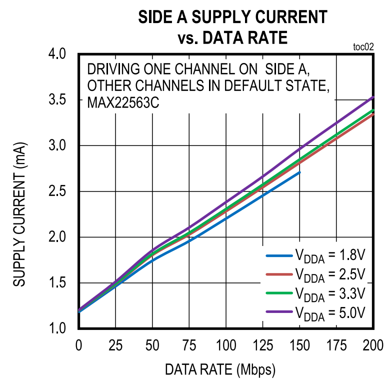
UL
The MAX22563-MAX22566 are certified under UL1577. For more details, refer to File E351759.
Rated up to 3750V_{RMS} isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22563−MAX22566 are certified up to 3750V_{RMS} for single protection. For more details, refer to File E351759.
VDE
The MAX22563−MAX22566 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Transient Isolation Voltage 5300V_{PK}, Maximum Repetitive Peak Isolation Voltage 1108V_{PK}.

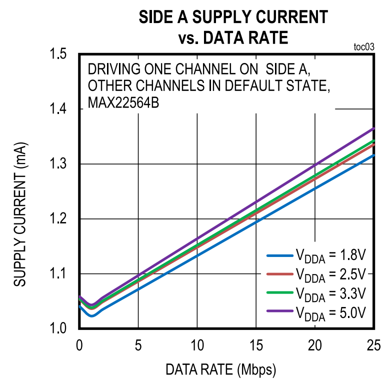
These couplers are suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

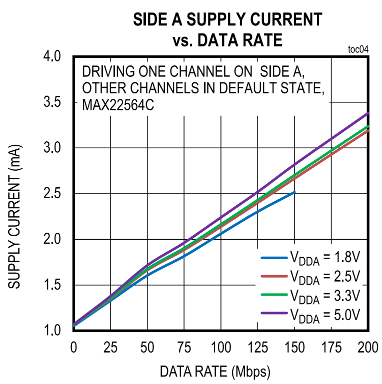
Typical Operating Characteristics

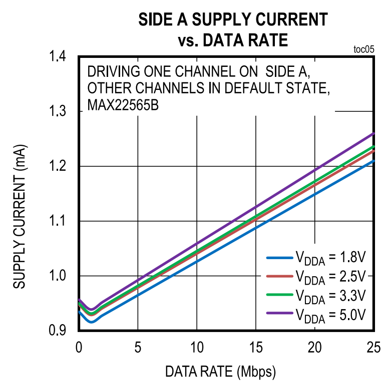
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

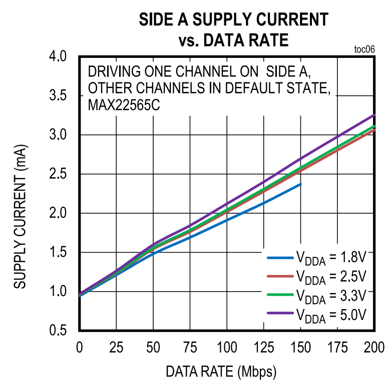


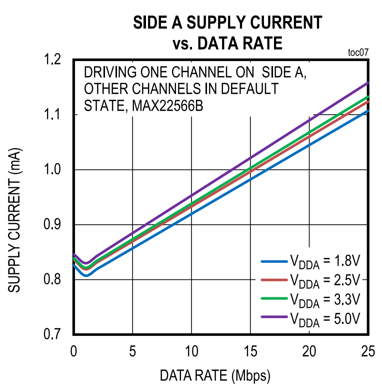


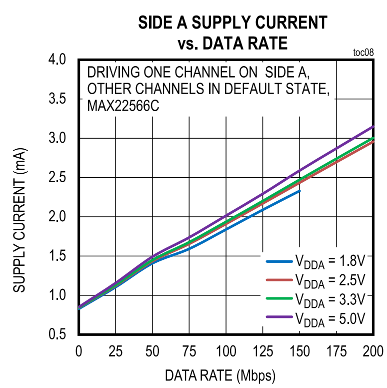


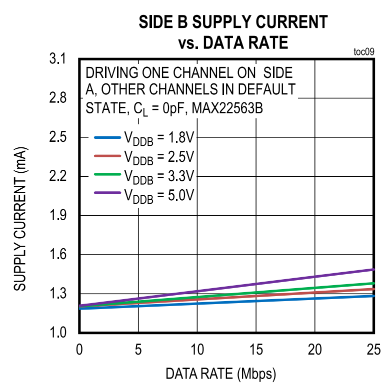


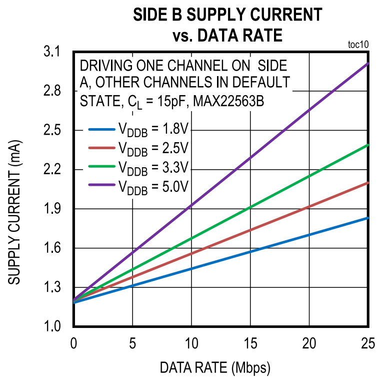


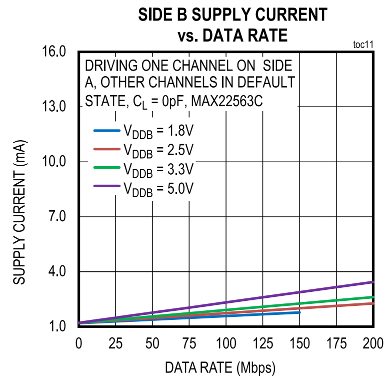


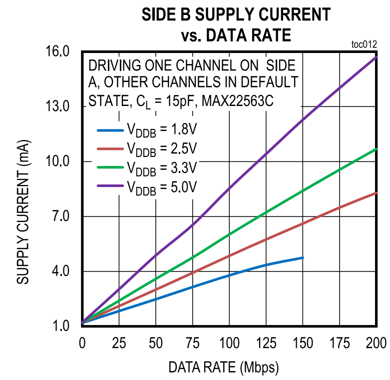


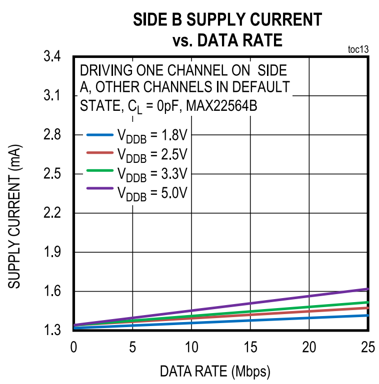


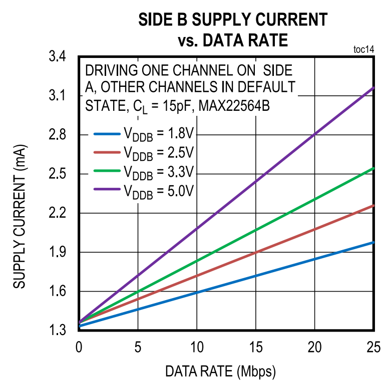


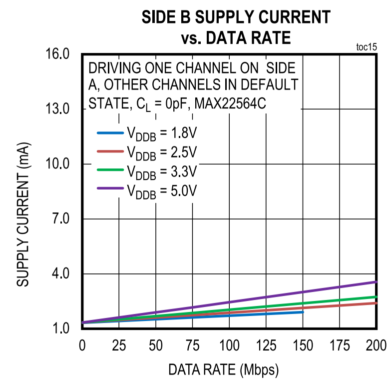

SIDE B SUPPLY CURRENT vs. DATA RATE
toc10
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22563B
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

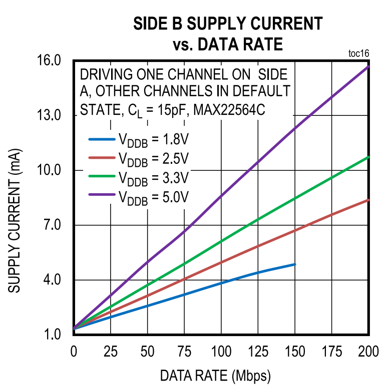

SIDE B SUPPLY CURRENT vs. DATA RATE
toc11
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 0pF, MAX22563C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

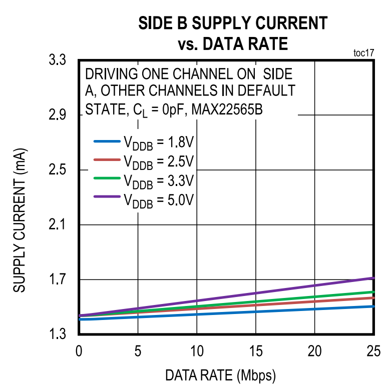

SIDE B SUPPLY CURRENT vs. DATA RATE
toc012
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22563C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

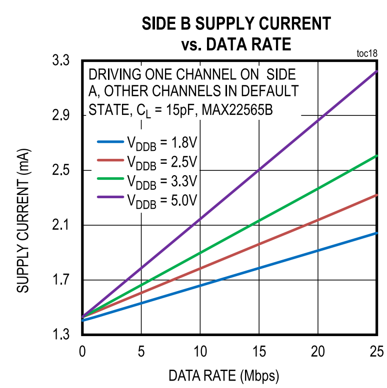

SIDE B SUPPLY CURRENT vs. DATA RATE
toc13
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 0pF, MAX22564B
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

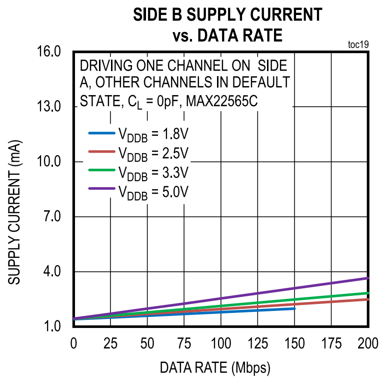

SIDE B SUPPLY CURRENT vs. DATA RATE
toc14
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22564B
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

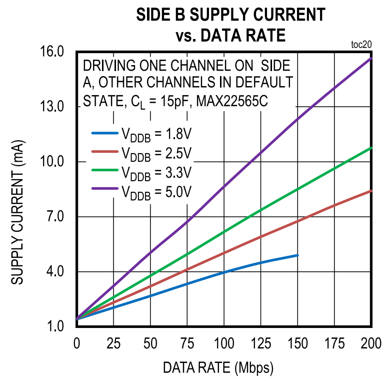

SIDE B SUPPLY CURRENT vs. DATA RATE
toc15
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 0pF, MAX22564C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

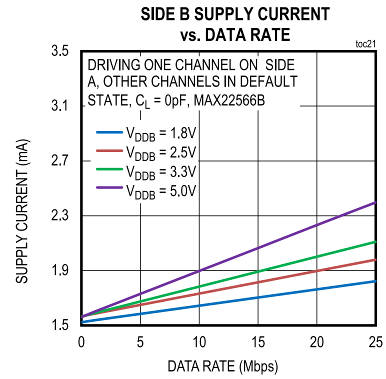

SIDE B SUPPLY CURRENT vs. DATA RATE
toc16
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22564C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

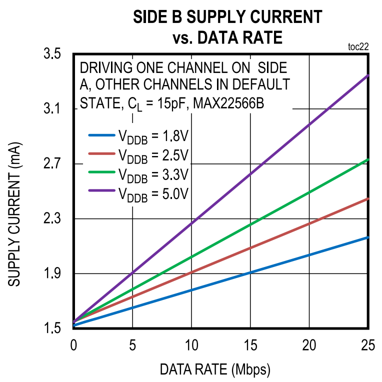

SIDE B SUPPLY CURRENT vs. DATA RATE
toc17
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 0pF, MAX22565B
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

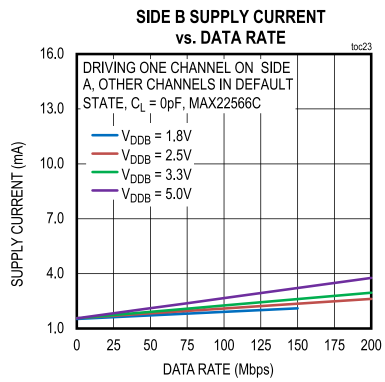

SIDE B SUPPLY CURRENT vs. DATA RATE
toc18
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22565B
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
DATA RATE (Mbps)

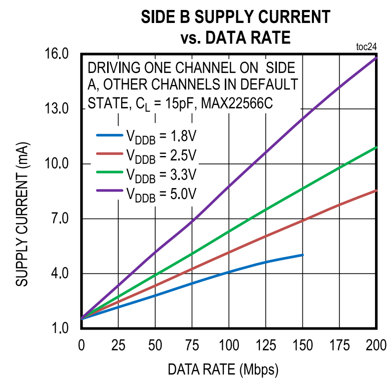

SIDE B SUPPLY CURRENT
vs. DATA RATE
toc19
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 0pF, MAX22565C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
16.0
13.0
10.0
7.0
4.0
1.0
0
25
50
75
100
125
150
175
200
DATA RATE (Mbps)

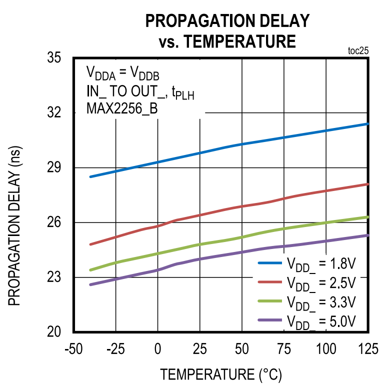

SIDE B SUPPLY CURRENT
vs. DATA RATE
toc20
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22565C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
16.0
13.0
10.0
7.0
4.0
1.0
0
25
50
75
100
125
150
175
200
DATA RATE (Mbps)

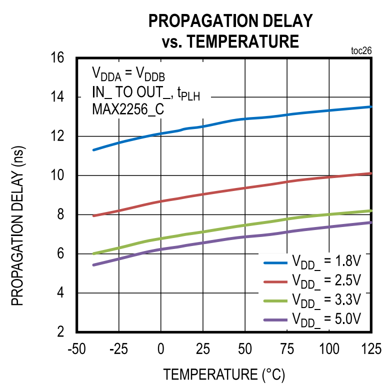

SIDE B SUPPLY CURRENT
vs. DATA RATE
toc21
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 0pF, MAX22566B
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
3.5
3.1
2.7
2.3
1.9
1.5
0
5
10
15
20
25
DATA RATE (Mbps)

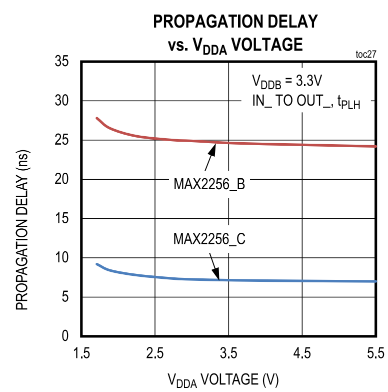

SIDE B SUPPLY CURRENT
vs. DATA RATE
toc22
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22566B
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
3.5
3.1
2.7
2.3
1.9
1.5
0
5
10
15
20
25
DATA RATE (Mbps)

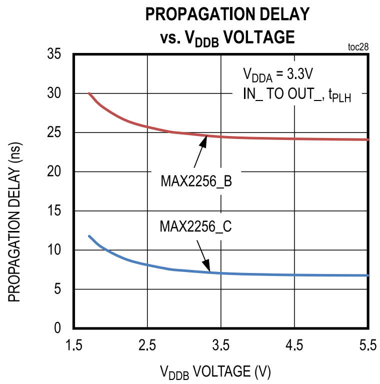

SIDE B SUPPLY CURRENT
vs. DATA RATE
toc23
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 0pF, MAX22566C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
16.0
13.0
10.0
7.0
4.0
1.0
0
25
50
75
100
125
150
175
200
DATA RATE (Mbps)

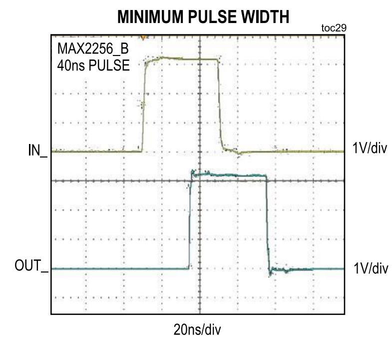

SIDE B SUPPLY CURRENT
vs. DATA RATE
toc24
DRIVING ONE CHANNEL ON SIDE A, OTHER CHANNELS IN DEFAULT STATE, C_L = 15pF, MAX22566C
V_{DDB} = 1.8V
V_{DDB} = 2.5V
V_{DDB} = 3.3V
V_{DDB} = 5.0V
SUPPLY CURRENT (mA)
16.0
13.0
10.0
7.0
4.0
1.0
0
25
50
75
100
125
150
175
200
DATA RATE (Mbps)

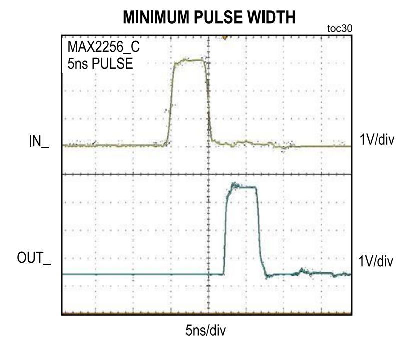

PROPAGATION DELAY
vs. TEMPERATURE
toc25
V_{DDA} = V_{DDB}
IN_ TO OUT_, t_{PLH}
MAX2256_B
$V_{DD\_}$ = 1.8V
$V_{DD\_}$ = 2.5V
$V_{DD\_}$ = 3.3V
$V_{DD\_}$ = 5.0V
PROPAGATION DELAY (ns)
35
32
29
26
23
20
-50
-25
0
25
50
75
100
125
TEMPERATURE (°C)

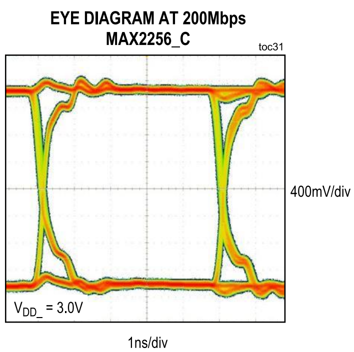

PROPAGATION DELAY
vs. TEMPERATURE
toc26
V_{DDA} = V_{DDB}
IN_ TO OUT_, t_{PLH}
MAX2256_C
$V_{DD\_}$ = 1.8V
$V_{DD\_}$ = 2.5V
$V_{DD\_}$ = 3.3V
$V_{DD\_}$ = 5.0V
PROPAGATION DELAY (ns)
16
14
12
10
8
6
4
2
-50
-25
0
25
50
75
100
125
TEMPERATURE (°C)

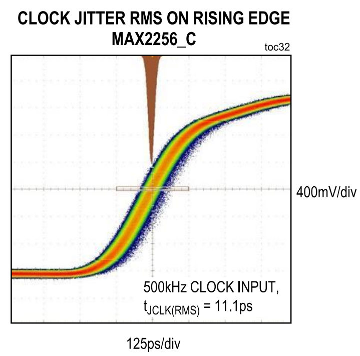

PROPAGATION DELAY
vs. V_{DDA} VOLTAGE
toc27
V_{DDB} = 3.3V
IN_ TO OUT_, t_{PLH}
MAX2256_B
MAX2256_C
PROPAGATION DELAY (ns)
35
30
25
20
15
10
5
0
1.5
2.5
3.5
4.5
5.5
V_{DDA} VOLTAGE (V)

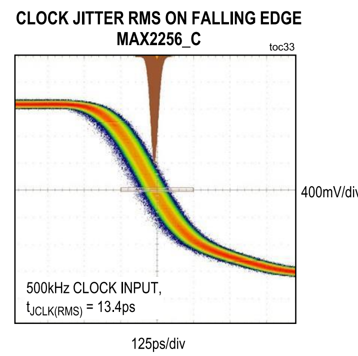

PROPAGATION DELAY
vs. VDDB VOLTAGE
toc28
VDDA = 3.3V
IN_ TO OUT_, tPLH
MAX2256_B
MAX2256_C
PROPAGATION DELAY (ns)
35
30
25
20
15
10
5
0
1.5
2.5
3.5
4.5
5.5
VDDB VOLTAGE (V)

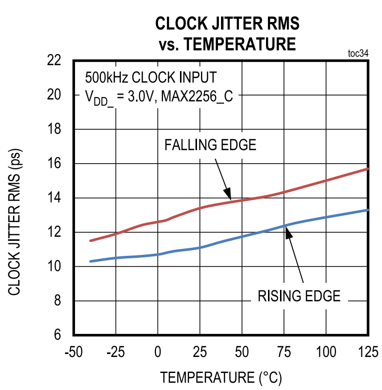

MINIMUM PULSE WIDTH
toc29
MAX2256_B
40ns PULSE
IN_
1V/div
OUT_
1V/div
20ns/div


MINIMUM PULSE WIDTH
toc30
MAX2256_C
5ns PULSE
IN_
1V/div
OUT_
1V/div
5ns/div

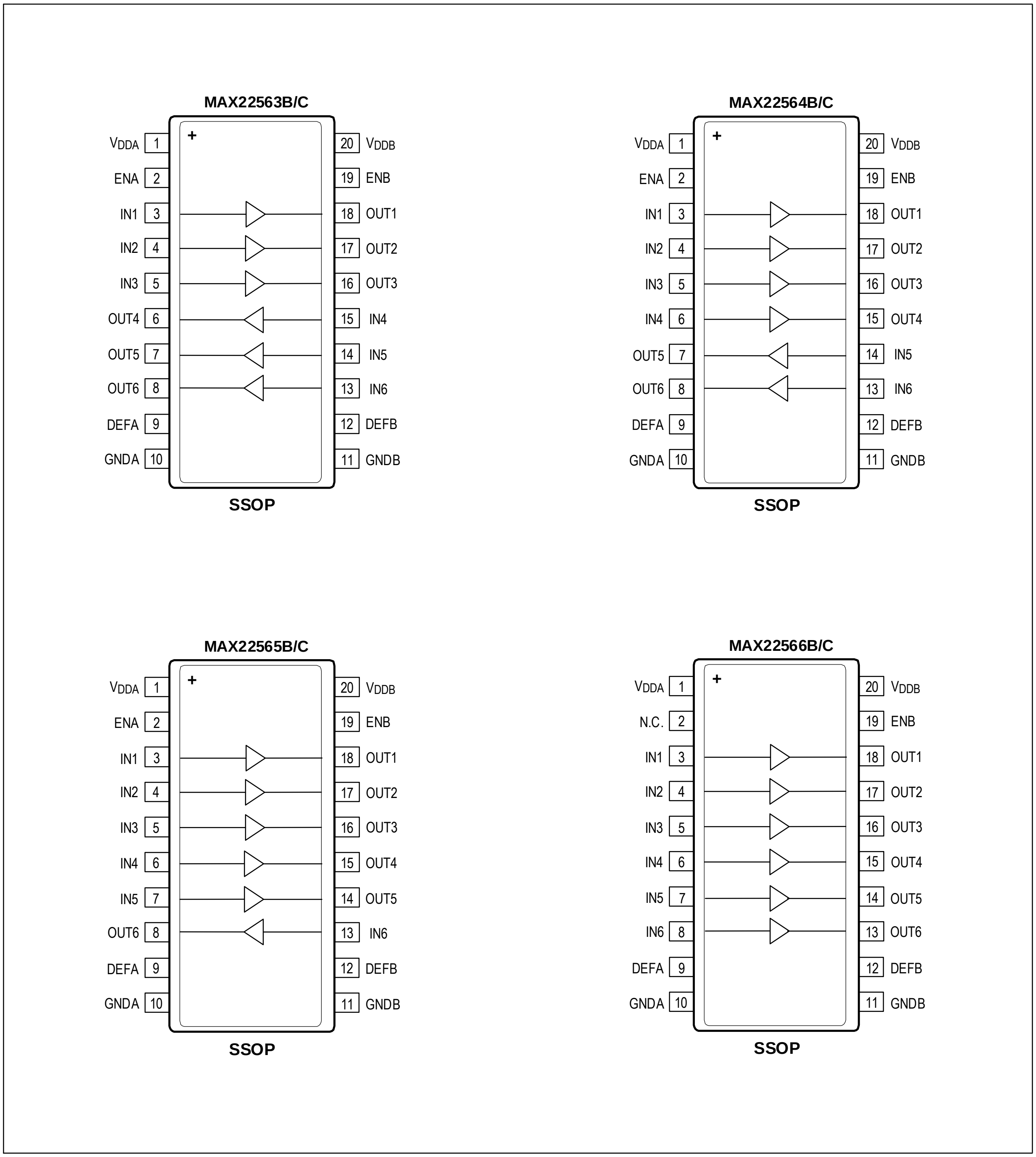

EYE DIAGRAM AT 200Mbps
MAX2256_C
toc31
400mV/div
VDD_ = 3.0V
1ns/div


CLOCK JITTER RMS ON RISING EDGE
MAX2256_C
toc32
400mV/div
500kHz CLOCK INPUT,
tJCLK(RMS) = 11.1ps
125ps/div


CLOCK JITTER RMS ON FALLING EDGE
MAX2256_C
toc33
400mV/div
500kHz CLOCK INPUT,
tJCLK(RMS) = 13.4ps
125ps/div


CLOCK JITTER RMS
vs. TEMPERATURE
toc34
500kHz CLOCK INPUT
VDD_ = 3.0V, MAX2256_C
FALLING EDGE
RISING EDGE
CLOCK JITTER RMS (ps)
22
20
18
16
14
12
10
8
6
-50
-25
0
25
50
75
100
125
TEMPERATURE (°C)

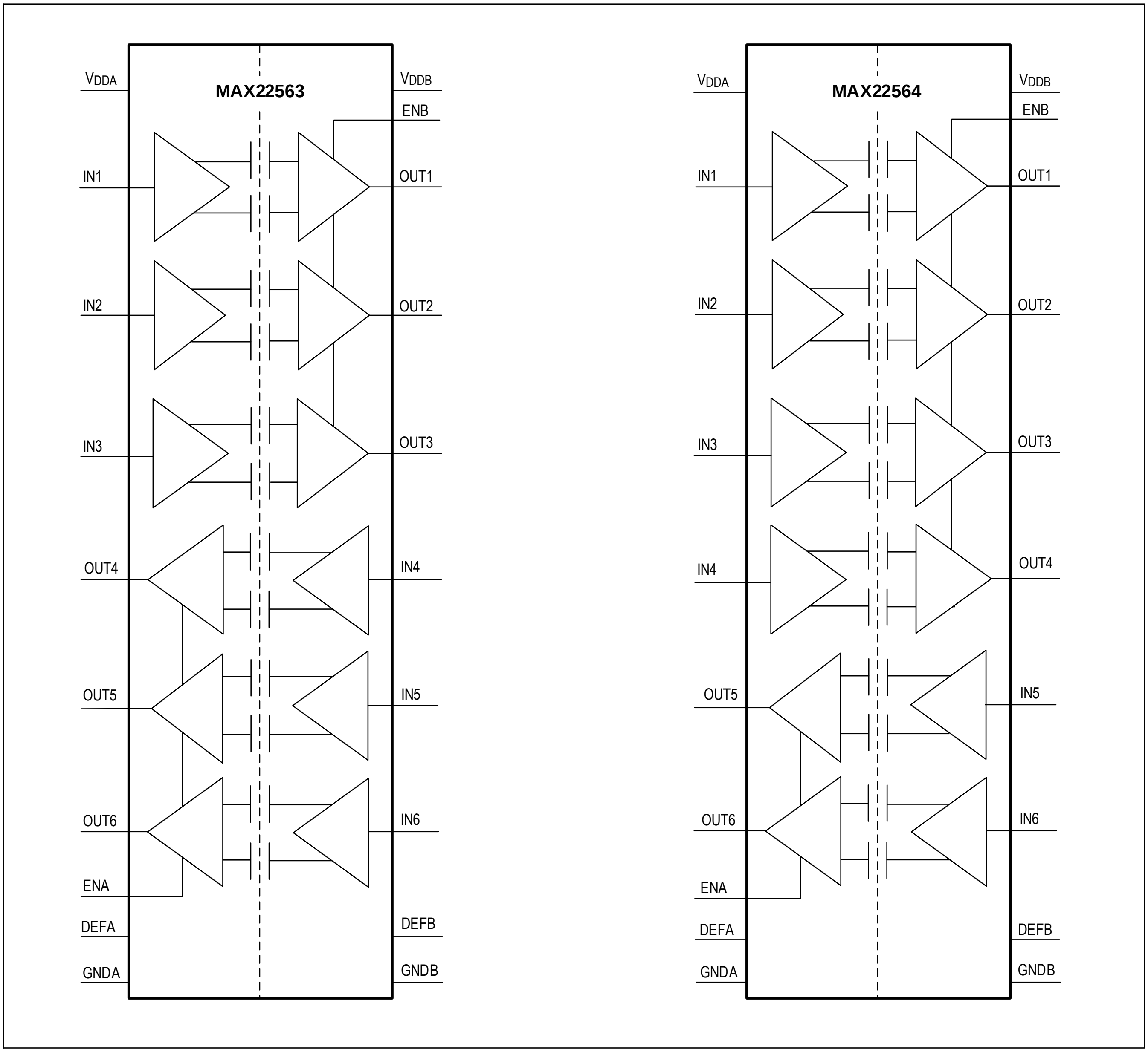
Pin Configurations

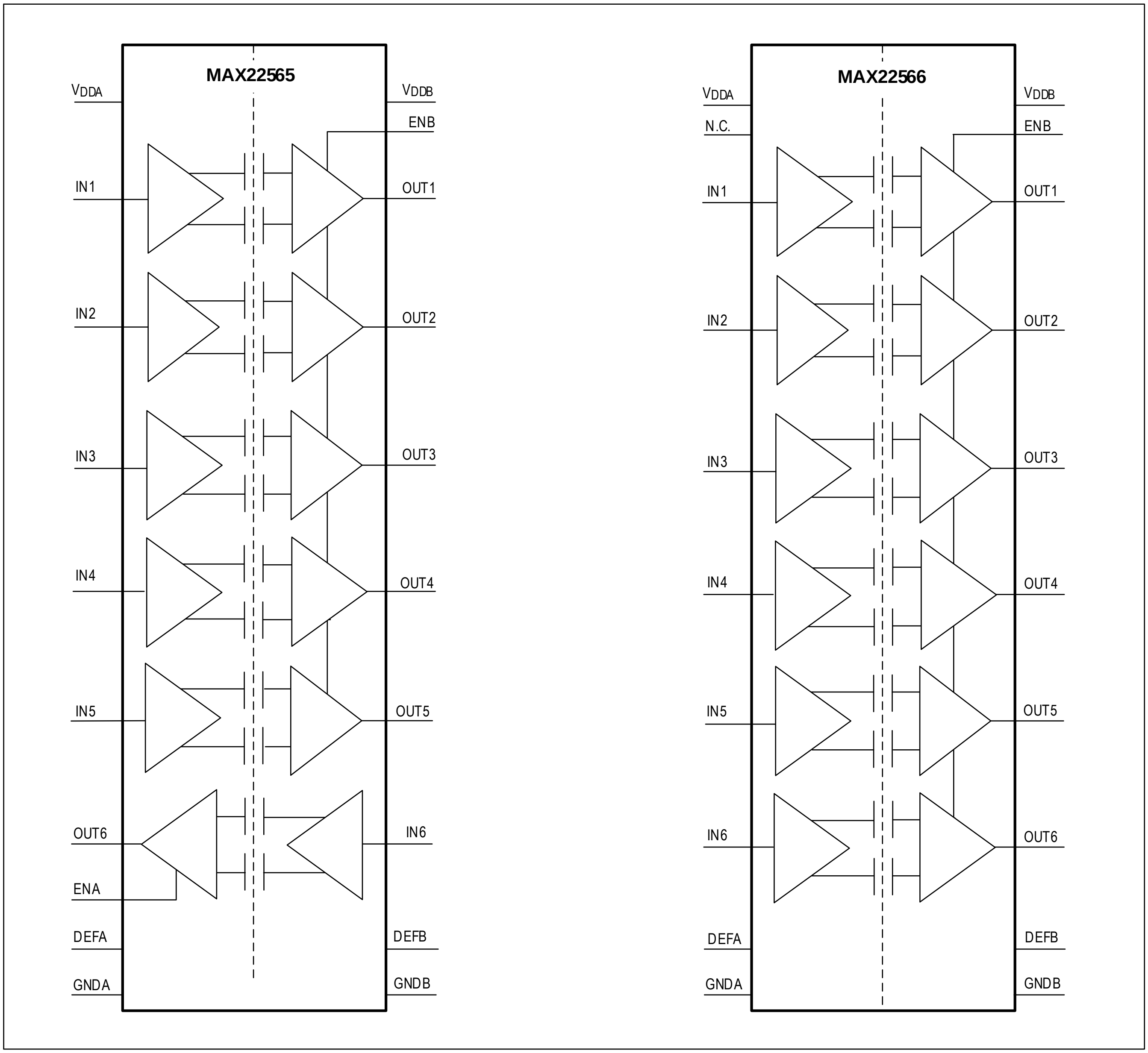


Pin Descriptions

PIN				NAME	FUNCTION
MAX22563	MAX22564	MAX22565	MAX22566		
1	1	1	1	V_{DDA}	Power Supply Input for Side A. Bypass V_{DDA} to GNDA with a 0.1µF ceramic capacitor as close as possible to the pin.
–	–	–	2	N.C.	Not Connected. Not internally connected.
2	2	2	–	ENA	Active-High Enable for Side A. ENA has an internal 5µA pullup to V_{DDA}.
3	3	3	3	IN1	Logic Input 1 on Side A. Corresponds to Logic Output 1 on Side B.
4	4	4	4	IN2	Logic Input 2 on Side A. Corresponds to Logic Output 2 on Side B.
5	5	5	5	IN3	Logic Input 3 on Side A. Corresponds to Logic Output 3 on Side B.
15	6	6	6	IN4	Logic Input 4 on Side A/B. Corresponds to Logic Output 4 on Side B/A.
14	14	7	7	IN5	Logic Input 5 on Side A/B. Corresponds to Logic Output 5 on Side B/A.
13	13	13	8	IN6	Logic Input 6 on Side A/B. Corresponds to Logic Output 6 on Side B/A.
9	9	9	9	DEFA	Default Control Input for Side A. Connect DEFA to V_{DDA} to set side A outputs to default-high state and to enable the pullup current on side A inputs. Connect DEFA to GNDA to set side A outputs to a default-low state and enable the pulldown current on side A inputs. DEFA must be tied to the same state (high or low) as DEFB.
10	10	10	10	GNDA	Ground Reference for Side A.
11	11	11	11	GNDB	Ground Reference for Side B.
12	12	12	12	DEFB	Default Control Input for Side B. Connect DEFB to V_{DDB} to set side B outputs to a default-high state and to enable the pullup current on side B inputs. Connect DEFB to GNDB to set side B outputs to default-low state and enable the pulldown current on side B inputs. DEFB must be tied to the same state (high or low) as DEFA.
8	8	8	13	OUT6	Logic Output 6 on Side B/A. OUT6 is the logic output for the IN6 input on Side A/B.
7	7	14	14	OUT5	Logic Output 5 on Side B/A. OUT5 is the logic output for the IN5 input on Side A/B.
6	15	15	15	OUT4	Logic Output 4 on Side B/A. OUT4 is the logic output for the IN4 input on Side A/B.
16	16	16	16	OUT3	Logic Output 3 on Side B. OUT3 is the logic output for the IN3 input on Side A.
17	17	17	17	OUT2	Logic Output 2 on Side B. OUT2 is the logic output for the IN2 input on Side A.
18	18	18	18	OUT1	Logic Output 1 on Side B. OUT1 is the logic output for the IN1 input on Side A.
19	19	19	19	ENB	Active-High Enable for Side B. ENB has an internal 5µA pullup to V_{DDB}.
20	20	20	20	V_{DDB}	Power Supply Input for Side B. Bypass V_{DDB} to GNDB with a 0.1µF ceramic capacitor as close as possible to the pin.

Functional Diagrams




MAX22565
VDDA
VDDB
ENB
IN1
OUT1
IN2
OUT2
IN3
OUT3
IN4
OUT4
IN5
OUT5
OUT6
IN6
ENA
DEFA
DEFB
GNDA
GNDB
MAX22566
VDDA
VDDB
N.C.
ENB
IN1
OUT1
IN2
OUT2
IN3
OUT3
IN4
OUT4
IN5
OUT5
IN6
OUT6
DEFA
DEFB
GNDA
GNDB

Detailed Description

The MAX22563−MAX22566 are a family of 6-channel reinforced digital isolators in a compact 20-SSOP package, with an isolation rating of $3.75kV_{RMS}$. This family of devices offers all possible unidirectional channel configurations to accommodate any 6-channel design.

The MAX22563 features three channels transmitting digital signals in one direction and three channels transmitting in the opposite direction for applications such as an isolated micro-controller interface. The MAX22564 offers four channels transmitting digital signals in one direction and two channels transmitting in the opposite direction, making it an ideal candidate for applications such as isolated SPI. The MAX22565 provides five channels transmitting digital signals in one direction and one channel transmitting in the opposite direction. The MAX22566 features all six channels transmitting digital signals in one direction, which is suitable in applications such as isolated digital I/O.

The MAX22563-MAX22566 are available in a 20-pin SSOP package with 5.5mm creepage and clearance, with an isolation rating of $3.75kV_{RMS}$. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim Integrated's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

The devices are available with a maximum data rate of either 25Mbps (B version) or 200Mbps (C version). All devices feature user-selectable default-high or default-low outputs. The default is the state the output assumes when the input is not powered or if the input is open-circuit. The MAX22563-MAX22566 have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX22563-MAX22566 also feature a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The family of devices provides reinforced galvanic isolation for digital signals that are transmitted between two ground domains. The MAX22563-MAX22566 can withstand differences of up to $3.75kV_{RMS}$ for up to 60 seconds, and up to $1108V_{PEAK}$ of continuous isolation.

AEC-Q100 Qualification

Devices with /V suffix are AEC-Q100 qualified. See the *Ordering Information* for all automotive grade part numbers.

Level Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX22563-MAX22566 to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the device is unidirectional; it only passes data in one direction, as indicated in the *Functional Diagram*. All devices feature six unidirectional channels that operate independently with guaranteed data rates from DC to 25Mbps (B version), or from DC to 200Mbps (C version). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage-Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs as seen in *Table 2*. *Figure 3* through *Figure 6* show the behavior of the outputs during power-up and power-down.

Table 2. Output Behavior During Undervoltage Conditions

$V_{IN\_}$	V_{DDA}	V_{DDB}	ENA, ENB	V_{OUTA}	V_{OUTB}
1	Powered	Powered	1	High	High
			0	Hi-Z	Hi-Z
0	Powered	Powered	1	Low	Low
			0	Hi-Z	Hi-Z
X	Undervoltage	Powered	1	Default	Default
			0	Hi-Z	Hi-Z
X	Powered	Undervoltage	1	Default	Default
			0	Hi-Z	Hi-Z

Note: "X" is don't care.

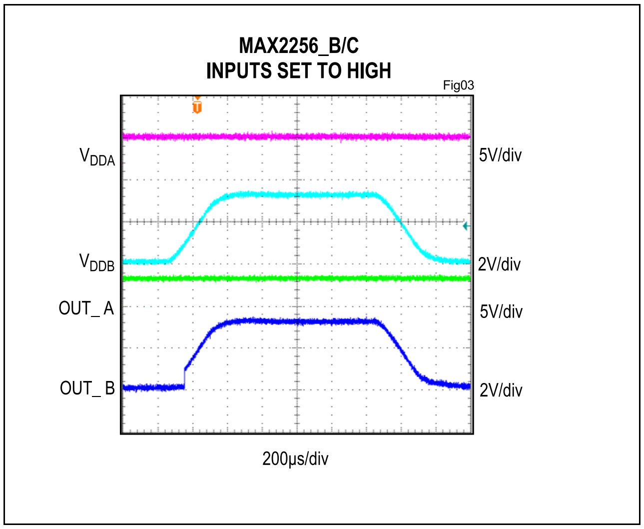


Figure 3. Undervoltage Lockout Behavior, Default sets to High, Inputs set to High

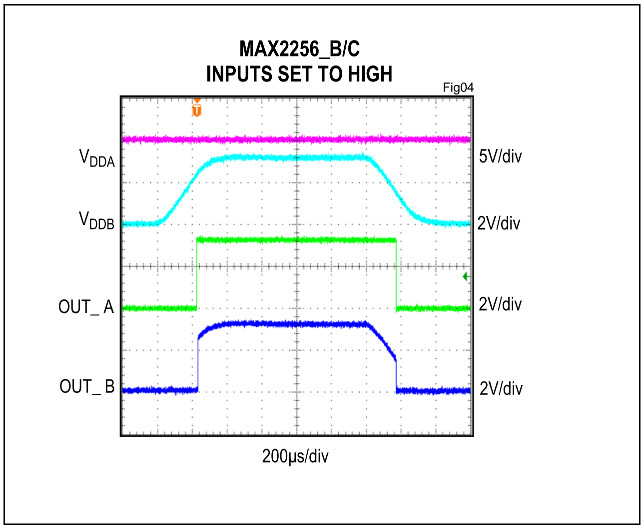


Figure 4. Undervoltage Lockout Behavior, Default sets to Low, Inputs set to High

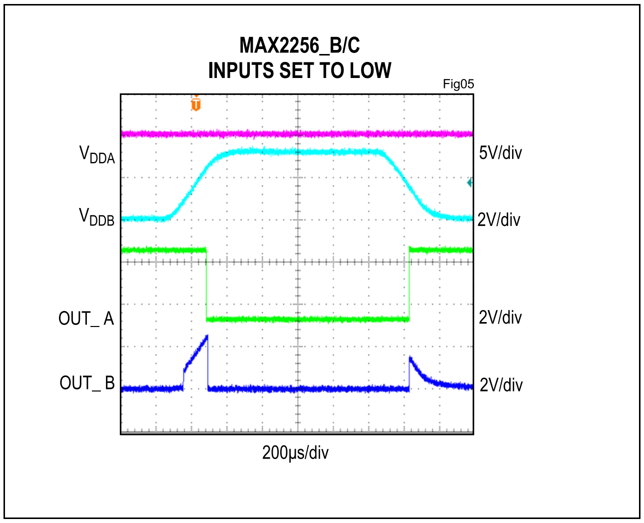


Figure 5. Undervoltage Lockout Behavior, Default sets to High, Inputs set to Low

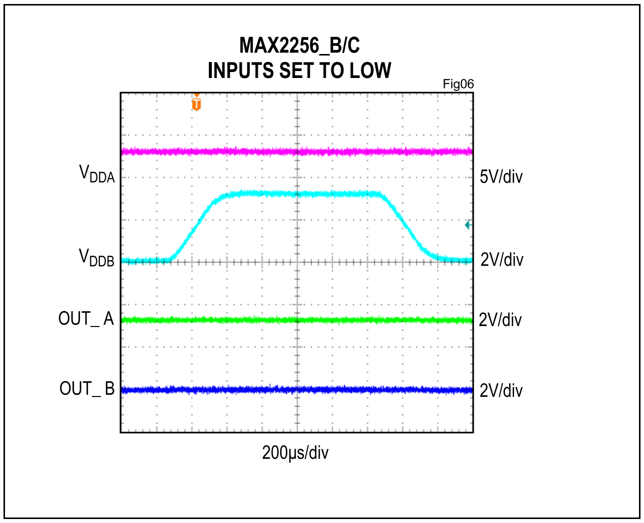


Figure 6. Undervoltage Lockout Behavior, Default sets to Low, Inputs set to Low

Selectable Output Default (DEFA, DEFB)

The default is the state the output assumes when the input is not powered or if the input is open-circuit. The MAX22563-MAX22566 feature user-selectable default-high or default-low outputs. Tie both DEFA and DEFB high to set all channels to default-high, or tie both DEFA and DEFB low to set all channels to default-low.

Ensure the logic state (high or low) of DEFA is the same as that of DEFB. Do not toggle DEFA or DEFB during normal operation.

Safety Limit

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22563-MAX22566 can dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. *Table 3* shows the safety limits for the MAX22563-MAX22566.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section and power dissipation calculations are discussed in the *Calculating Power Dissipation* section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 7 shows the thermal derating curve for safety limiting the power of the devices, and *Figure 8* shows the thermal derating curve for safety limiting the current of the devices. Ensure that the junction temperature does not exceed 150°C.

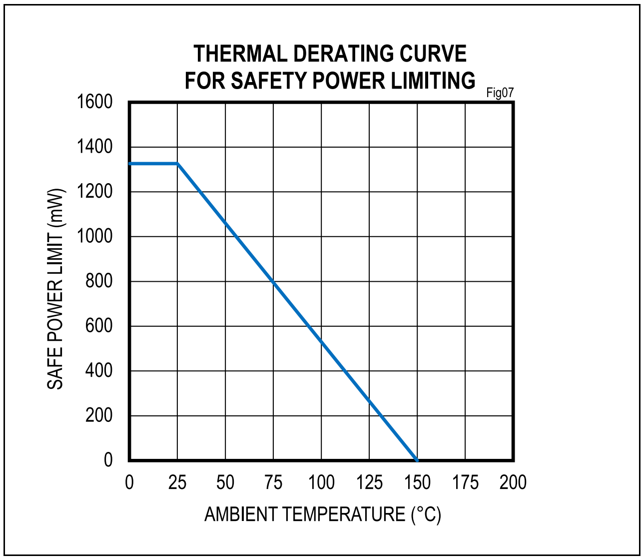


Figure 7. Thermal Derating Curve for Safety Power Limiting

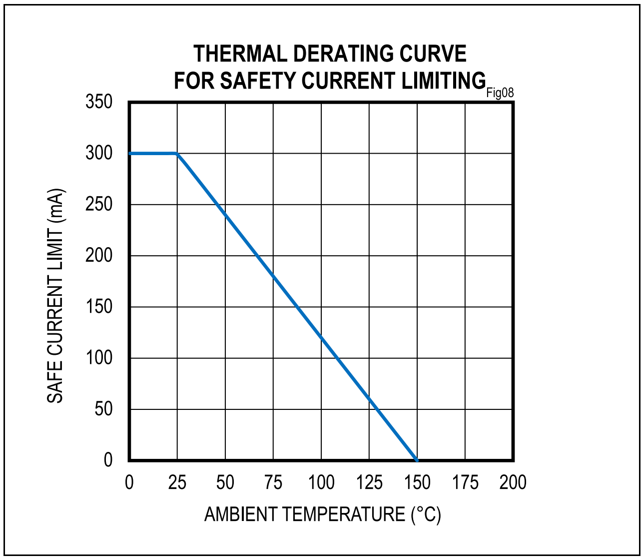


Figure 8. Thermal Derating Curve for Safety Current Limiting

Table 3. Safety Limiting Values

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C	300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	1326	mW
Maximum Safety Temperature	T_S		150	°C

Applications Information

Power-Supply Sequencing

The MAX22563-MAX22566 do not require any special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1μF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the devices free from ground and signal planes. Any galvanic or metallic connection between Side A and Side B defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in *Figure 9* and *Figure 10*. Note that the data in *Figure 9* and *Figure 10* are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the no load current (shown in *Figure 9* and *Figure 10*) which is a function of voltage and data rate, and the load current, which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where:

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second/2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD}/R_L$$

where:

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

Example (shown in *Figure 11*): A MAX22564C is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 20Mbps with a 15kΩ resistive load; channel 2 operating at 100Mbps with a 10pF capacitive load; channel 3 is not in use and the resistive load is negligible since the isolator is driving a CMOS input; channel 4 held high with a 10kΩ resistive load; channel 5 operating at 50Mbps with a 20kΩ resistive load; and channel 6 operating at 200Mbps with a 15pF capacitive load. See *Table 4* and *Table 5* for V_{DDA} and V_{DDB} supply current calculation worksheets.

V_{DDA} must supply (with V_{DDA} = 2.5V):

- Channel 1 is an input channel operating at 2.5V and 20Mbps, consuming 0.35mA, estimated from *Figure 9*.
- Channel 2 is an input channel operating at 2.5V and 100Mbps, consuming 1.19mA, estimated from *Figure 9*.
- Channels 3 and 4 are input channels operating at 2.5V with DC signal, consuming 0.14mA, estimated from *Figure 9*.
- Channel 5 is an output channel operating at 2.5V and 50Mbps, consuming 0.52mA, estimated from *Figure 10*.
- I_{RL} on channel 5 for 20kΩ resistive load at 2.5V and switching at 50Mbps with 50% duty cycle is 0.0625mA.
- Channel 6 is an output channel operating at 2.5V and 200Mbps, consuming 1.31mA, estimated from *Figure 10*.
- I_{CL} on channel 6 for 15pF capacitive load at 2.5V and 200Mbps is 3.75mA.

Total current for Side A = 7.46mA (typ).

V_{DDB} must supply (with V_{DDB} = 3.3V):

- Channel 1 is an output channel operating at 3.3V and 20Mbps, consuming 0.40mA, estimated from *Figure 10*.
- I_{RL} on channel 1 for 15kΩ resistive load at 3.3V and switching at 20Mbps with 50% duty cycle is 0.11mA.
- Channel 2 is an output channel operating at 3.3V and 100Mbps, consuming 0.96mA, estimated from *Figure 10*.
- I_{CL} on channel 2 for 10pF capacitive load at 3.3V and 100Mbps is 1.65mA.
- Channels 3 and 4 are output channels operating at 3.3V with DC signal, consuming 0.26mA, estimated from *Figure 10*.
- I_{RL} on channel 4 for 10kΩ resistive load held at 3.3V is 0.33mA.
- Channel 5 is an input channel operating at 3.3V and 50Mbps, consuming 0.68mA, estimated from *Figure 9*.
- Channel 6 is an input channel operating at 3.3V and 200Mbps, consuming 2.29mA, estimated from *Figure 9*.

Total current for Side B = 6.94mA (typ).

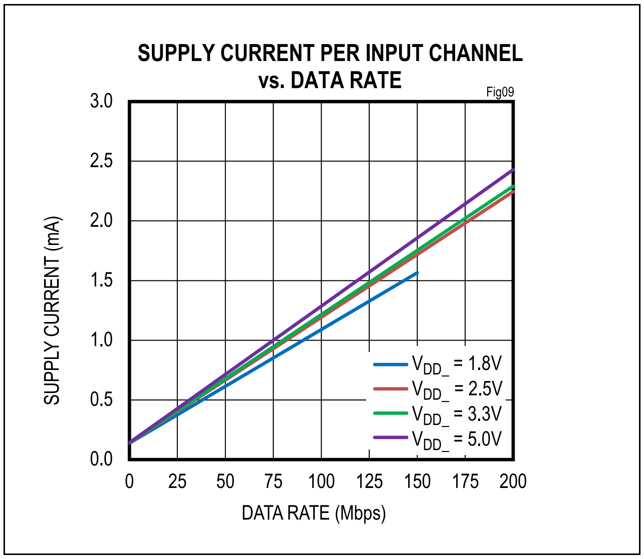


Figure 9. Supply Current Per Input Channel (Calculated)

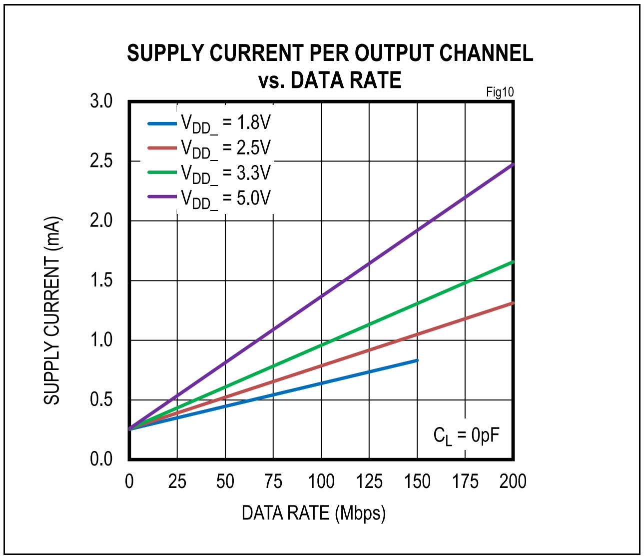


Figure 10. Supply Current Per Output Channel (Calculated)

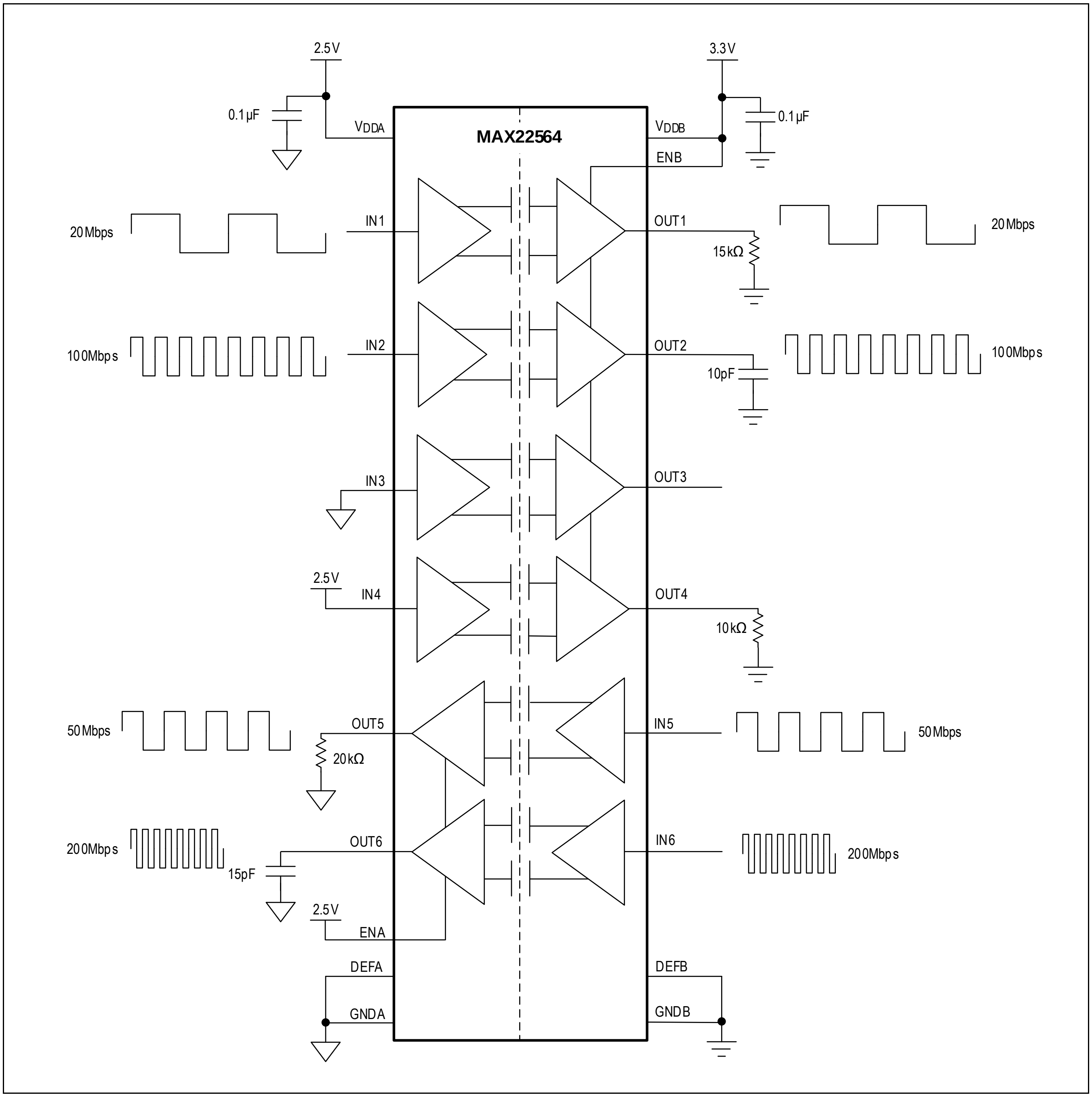


Figure 11. Example Circuit for Supply Current Calculation

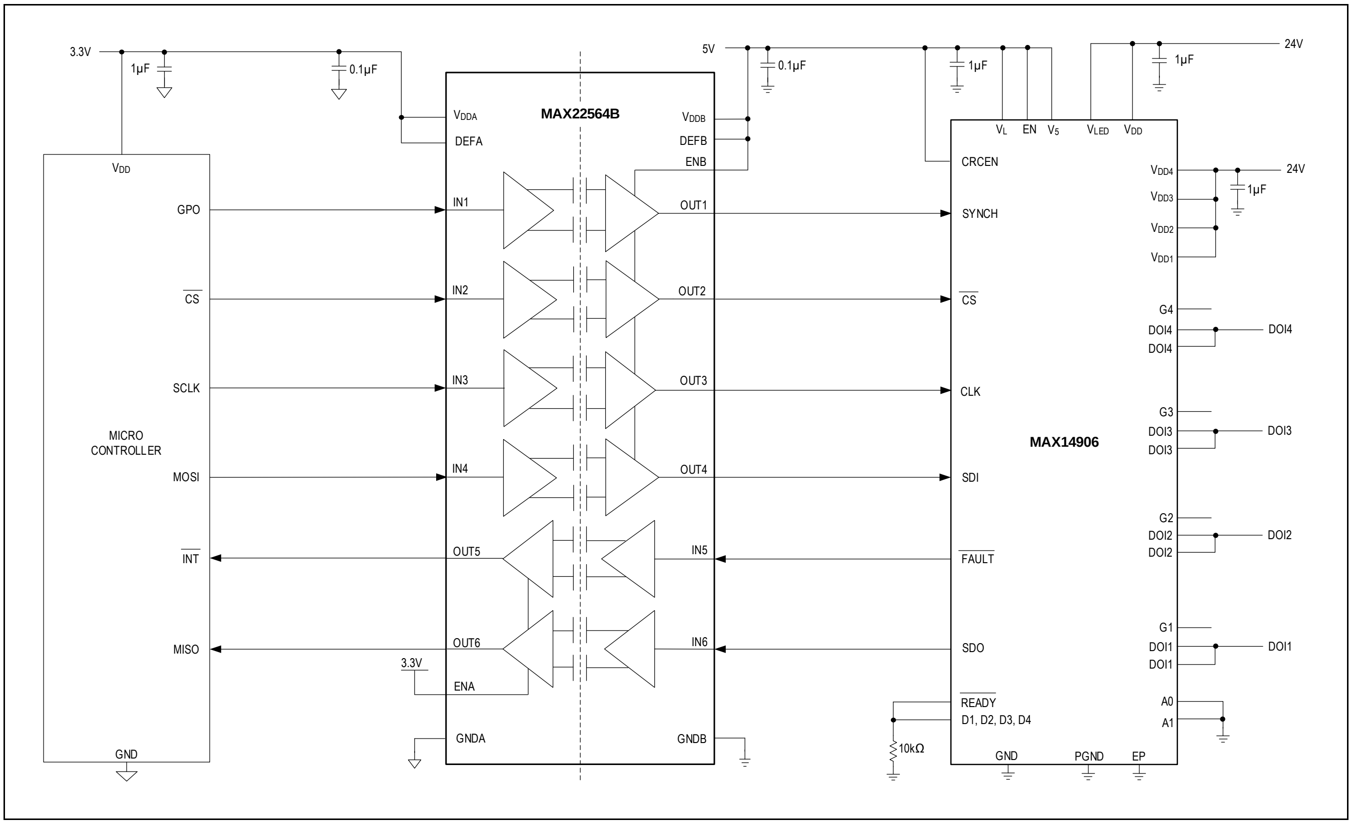
Table 4. Side A Supply Current Calculation Worksheet

SIDE A	V_{DDA} = 2.5V					
CHANNEL	**IN/OUT**	**DATA RATE (Mbps)**	**LOAD TYPE**	**LOAD**	**"NO LOAD" CURRENT (mA)**	**LOAD CURRENT (mA)**
1	IN	20			0.35	
2	IN	100			1.19	
3	IN	0			0.14	
4	IN	0			0.14	
5	OUT	50	Resistive	20kΩ	0.52	2.5V/20kΩ x 0.5 = 0.0625mA
6	OUT	200	Capacitive	15pF	1.31	2.5V x 100MHz x 15pF = 3.75mA
Total: 7.46mA						

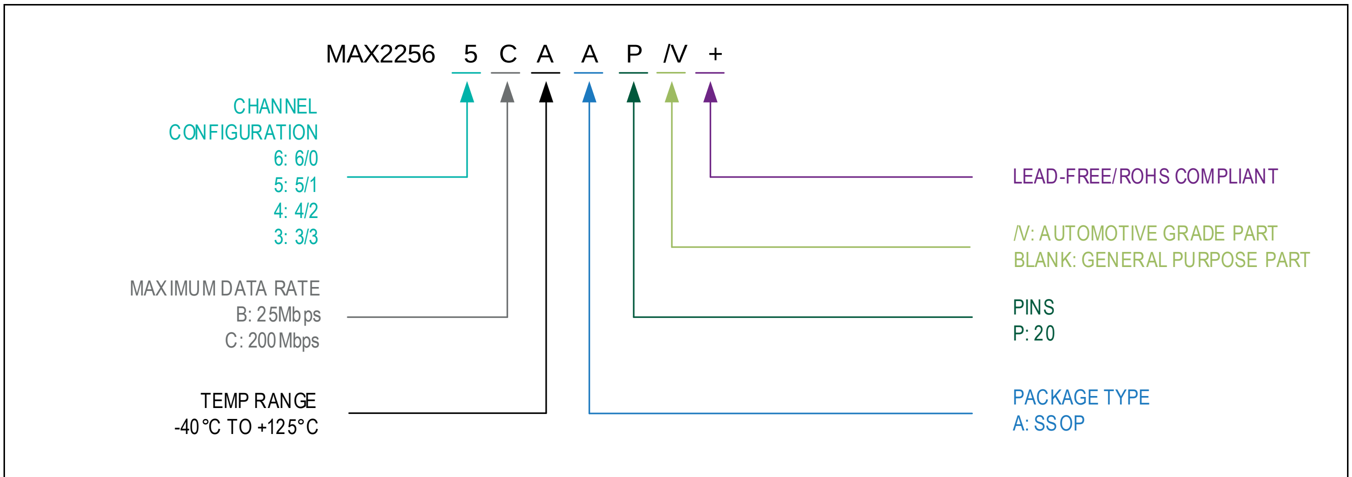
Table 5. Side B Supply Current Calculation Worksheet

SIDE B	V_{DDB} = 3.3V					
CHANNEL	**IN/OUT**	**DATA RATE (Mbps)**	**LOAD TYPE**	**LOAD**	**"NO LOAD" CURRENT (mA)**	**LOAD CURRENT (mA)**
1	OUT	20	Resistive	15kΩ	0.40	3.3V/15kΩ x 0.5 = 0.11mA
2	OUT	100	Capacitive	10pF	0.96	3.3V x 50MHz x 10pF = 1.65mA
3	OUT	0			0.26	
4	OUT	0	Resistive	10kΩ	0.26	3.3V/10kΩ = 0.33mA
5	IN	50			0.68	
6	IN	200			2.29	
Total: 6.94mA						

Typical Application Circuit



Product Selector Guide



Ordering Information

PART NUMBER	CHANNEL CONFIGURATION	DATA RATE (Mbps)	DEFAULT OUTPUT	ISOLATION VOLTAGE (kV_{RMS})	TEMPERATURE RANGE (°C)	PIN-PACKAGE
GENERAL PURPOSE DEVICES						
MAX22563BAAP+*	3/3	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22563CAAP+*	3/3	200	Selectable	3.75	-40 to +125	20-SSOP
MAX22564BAAP+*	4/2	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22564CAAP+*	4/2	200	Selectable	3.75	-40 to +125	20-SSOP
MAX22565BAAP+*	5/1	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22565CAAP+	5/1	200	Selectable	3.75	-40 to +125	20-SSOP
MAX22566BAAP+*	6/0	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22566CAAP+*	6/0	200	Selectable	3.75	-40 to +125	20-SSOP
AUTOMOTIVE DEVICES						
MAX22563BAAP/V+*	3/3	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22563CAAP/V+*	3/3	200	Selectable	3.75	-40 to +125	20-SSOP
MAX22564BAAP/V+*	4/2	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22564CAAP/V+*	4/2	200	Selectable	3.75	-40 to +125	20-SSOP
MAX22565BAAP/V+*	5/1	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22565CAAP/V+*	5/1	200	Selectable	3.75	-40 to +125	20-SSOP
MAX22566BAAP/V+*	6/0	25	Selectable	3.75	-40 to +125	20-SSOP
MAX22566CAAP/V+*	6/0	200	Selectable	3.75	-40 to +125	20-SSOP

**Future product—contact factory for availability.*

+Denotes a lead (Pb)–free/RoHS-compliant package.

/V Denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/21	Release for Market Intro	—