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## MAX22700D–MAX22702D MAX22700E–MAX22702E

### General Description

The MAX22700–MAX22702 are a family of single-channel isolated gate drivers with ultra-high common-mode transient immunity (CMTI) of 300kV/μs (typ). The devices are designed to drive silicon-carbide (SiC) or gallium-nitride (GaN) transistors in various inverter or motor control applications with different output gate-drive circuitry and B-side supply voltages. The devices feature variants with output options for gate driver common pin GNDB (MAX22700), Miller Clamp (MAX22701), and adjustable undervoltage-lockout UVLO (MAX22702). In addition, variants are offered as differential (D versions) or single-ended (E versions) inputs. All devices have integrated digital galvanic isolation using Maxim's proprietary process technology. The MAX22700–MAX22702 feature isolation for a withstand voltage rating of 3kV<sub>RMS</sub> (narrow SOIC package) or 5kV<sub>RMS</sub> (wide SOIC package) for 60 seconds.

All devices support a minimum pulse width of 20ns with a maximum pulse width distortion of 2ns. The part-to-part propagation delay is matched within 2ns (max) at +25°C ambient temperature, and 5ns (max) over the -40°C to +125°C operating temperature range. This feature reduces the power transistor's dead time, thus improving overall efficiency.

The MAX22700 and the MAX22702 have a maximum R<sub>DS(on)</sub> of 1.25Ω for the low-side driver, and the MAX22701 has an R<sub>DS(on)</sub> of 2.5Ω for the low-side driver. All devices have a maximum R<sub>DS(on)</sub> of 4.5Ω for the high-side driver. See the [Ordering Information](#) for suffixes associated with each option.

The MAX22700–MAX22702 are available either in an 8-pin wide-body SOIC package with 8mm creepage and clearance, or in a smaller 8-pin narrow-body SOIC package with 4mm of creepage and clearance. The narrow SOIC package material has a minimum comparative tracking index (CTI) of 600, which gives it a group I rating in creepage tables, while the wide SOIC package material has a minimum CTI of 400, which gives it a group II rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

### Applications

- Isolated Gate Driver for Inverters
- Motor Drives
- UPS and PV Inverters

## Ultra-High CMTI Isolated Gate Drivers

### Benefits and Features

- Matching Propagation Delay
  - 20ns Minimum Pulse Width
  - 35ns Propagation Delay at Room Temperature
  - 2ns Part-to-Part Propagation Delay Matching at Room Temperature
  - 5ns Part-to-Part Propagation Delay Matching over -40°C to +125°C Temperature Range
- High CMTI (300kV/μs, typ)
- Robust Galvanic Isolation
  - Withstands 3kV<sub>RMS</sub> (Narrow SOIC) or 5kV<sub>RMS</sub> (Wide SOIC) for 60s (V<sub>ISO</sub>)
  - Continuously Withstands 600V<sub>RMS</sub> (Narrow SOIC) or 848V<sub>RMS</sub> (Wide SOIC) (V<sub>IOWM</sub>)
  - Withstands ±5kV Surge Between GNDA and V<sub>SSB</sub> with 1.2/50μs Waveform
- Precision UVLO
- Options to Support a Broad Range of Applications
  - 3 Output Options: GNDB, Miller Clamp, or Adjustable UVLO
  - 2 Input Configurations: Single-Ended with Enable (E versions) or Differential (D versions)

### Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-11 Basic Insulation (Wide SOIC) (Pending)

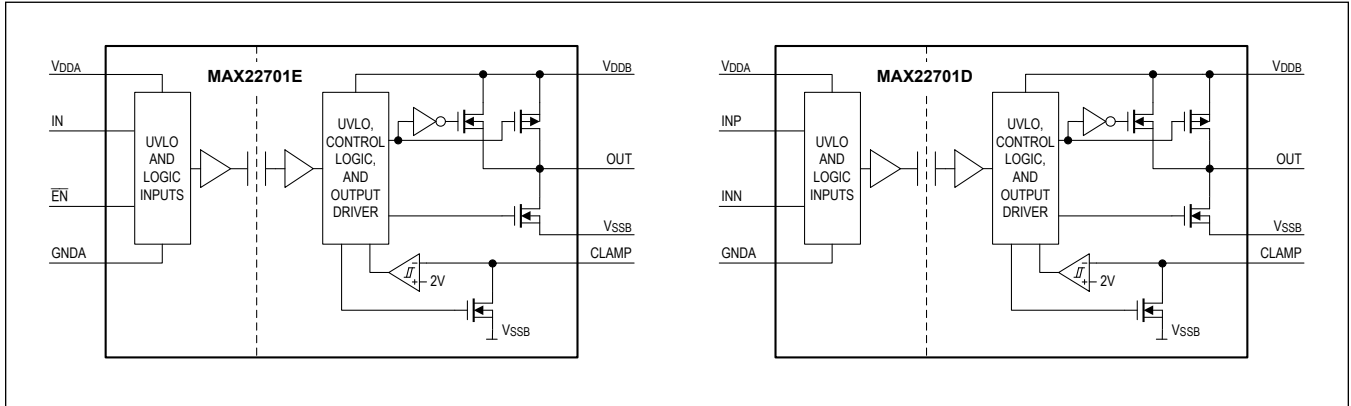
[Ordering Information](#) appears at end of data sheet.

MAX22700D–MAX22702D  
 MAX22700E–MAX22702E

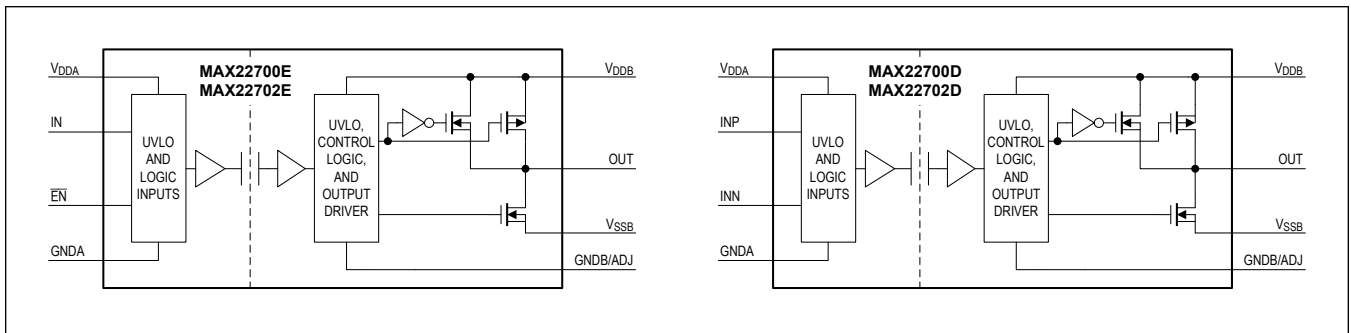
Ultra-High CMTI Isolated Gate Drivers

Functional Diagrams

MAX22701



MAX22700 and MAX22702



## Absolute Maximum Ratings

V <sub>DDA</sub> to GNDA .....	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C) Narrow SOIC (derate 9.39mW/°C above +70°C) ..... 750.89mW Wide SOIC (derate 8.51mW/°C above +70°C) ..... 681.14mW Operating Temperature Range ..... -40°C to +125°C Maximum Junction Temperature ..... +150°C Storage Temperature Range ..... -60°C to +150°C Soldering Temperature (reflow) ..... +260°C
V <sub>DDB</sub> to GNDB .....	-0.3V to +40V	
GNDB to V <sub>SSB</sub> .....	-0.3V to +40V	
V <sub>DDB</sub> to V <sub>SSB</sub> .....	-0.3V to +40V	
INP, INN, IN, EN to GNDA .....	-0.3V to +6V	
V <sub>DDB</sub> to ADJ.....	-0.3V to +6V	
CLAMP to V <sub>SSB</sub> .....	-0.3V to (V <sub>DDB</sub> + 0.3V)	
OUT to V <sub>SSB</sub> .....	-0.3V to (V <sub>DDB</sub> + 0.3V)	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 8 Narrow SOIC

Package Code	S8MS+23
Outline Number	<a href="#">21-0041</a>
Land Pattern Number	<a href="#">90-0096</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	106.54°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	44.91°C/W

### 8 Wide SOIC

Package Code	W8MS+6
Outline Number	<a href="#">21-100415</a>
Land Pattern Number	<a href="#">90-100146</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	117.45°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	58.48°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### DC Electrical Characteristics

( $V_{DDA} - V_{GNDA} = 5V$ ,  $V_{DDB} - V_{SSB} = 20V$ ,  $V_{GNDA} = V_{SSB} = 0V$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Supply Voltage	$V_{DDA}$	Relative to GNDA	3		5.5	V
	$V_{DDB}$	Relative to GNDB, MAX22700	13		28	
		Relative to $V_{SSB}$ , MAX22701	13		28	
		Relative to $V_{SSB}$ , MAX22702	6		28	
$V_{SSB}$	Relative to GNDB, MAX22700	-16		0		
Differential Supply	$V_{DIFF}$	$V_{DDB} - V_{SSB}$ , MAX22700	13		28	V
Undervoltage-Lockout Threshold	$V_{UVLOAP}$	$V_{DDA}$ rising	2.69	2.82	2.95	V
	$V_{UVLOAN}$	$V_{DDA}$ falling	2.59	2.72	2.85	
Undervoltage-Lockout Threshold Hysteresis	$V_{UVLOA\_HYST}$			100		mV
Undervoltage-Lockout Threshold	$V_{UVLOBP}$	$V_{DDB}$ rising, relative to GNDB, MAX22700		13	13.3	V
	$V_{UVLOBN}$	$V_{DDB}$ falling, relative to GNDB, MAX22700	11.6	12		
	$V_{UVLOBP}$	$V_{DDB}$ rising, relative to $V_{SSB}$ , MAX22701		13	13.3	
	$V_{UVLOBN}$	$V_{DDB}$ falling, relative to $V_{SSB}$ , MAX22701	11.6	12		
	$V_{UVLOBP}$	$V_{DDB}$ rising, relative to ADJ, MAX22702		2	2.05	
	$V_{UVLOBN}$	$V_{DDB}$ falling, relative to ADJ, MAX22702	1.79	1.84		
Undervoltage-Lockout Threshold Hysteresis	$V_{UVLOB\_HYST}$	MAX22700, MAX22701		1		V
		MAX22702		0.16		
<b>SUPPLY CURRENT</b>						
A-Side Quiescent Supply Current	$I_{DDA}$	$V_{DDA} = 5V$ , $\overline{INN}/\overline{EN} = V_{DDA}$		5	6.5	mA
		$V_{DDA} = 3.3V$ , $\overline{INN}/\overline{EN} = V_{DDA}$		3	4	
A-Side Active Supply Current	$I_{DDA}$	$V_{DDA} = 5V$ , $f_{PWM} = 1MHz$		5	6.5	mA
		$V_{DDA} = 3.3V$ , $f_{PWM} = 1MHz$		3	4	
B-Side Quiescent Positive Supply Current	$I_{DDB}$	$\overline{INN}/\overline{EN} = V_{DDA}$		3.5	6	mA
B-Side Active Positive Supply Current	$I_{DDB}$	$f_{PWM} = 1MHz$ ( <i>Note 2</i> )		6	10	mA
B-Side Ground Current	$I_{GNDB}$	MAX22700	-25			$\mu A$
<b>LOGIC INTERFACE (INP, INN, IN, <math>\overline{EN}</math>)</b>						
Input High Voltage	$V_{IH}$			$0.7 \times V_{DDA}$		V
Input Low Voltage	$V_{IL}$				$0.3 \times V_{DDA}$	V
Input Hysteresis	$V_{HYS}$			$0.1 \times V_{DDA}$		mV
Input Pullup Current	$I_{PU}$	$\overline{INN}$ , $\overline{EN}$ ( <i>Note 3</i> )	-10	-5	-1.5	$\mu A$
Input Pulldown Current	$I_{PD}$	INP, IN ( <i>Note 3</i> )	1.5	5	10	$\mu A$
Input Capacitance	$C_{IN}$	$f_{PWM} = 1MHz$		2		pF

**DC Electrical Characteristics (continued)**

( $V_{DDA} - V_{GNDA} = 5V$ ,  $V_{DDB} - V_{SSB} = 20V$ ,  $V_{GNDA} = V_{SSB} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ADJ (MAX22702 ONLY)</b>						
Input Leakage Current	$I_{ADJ}$	$V_{DDB} - V_{ADJ} = 3V$	-100		100	nA
<b>GATE DRIVER</b>						
High-Side Transistor On-Resistance	$R_{DSON\_H}$	$I_{OUT} = -100mA$ ( <i>Note 3</i> )			4.7	$\Omega$
Low-Side Transistor On-Resistance	$R_{DSON\_L}$	$I_{OUT} = 100mA$ ( <i>Note 3</i> )	MAX22700/ MAX22702		1.25	$\Omega$
			MAX22701		2.5	
Output-Voltage High	$V_{OH}$	$I_{OUT} = -10mA$ ( <i>Note 3</i> )		19.95		V
Output-Voltage Low	$V_{OL}$	$I_{OUT} = 10mA$ ( <i>Note 3</i> )	MAX22700/ MAX22702		0.01	V
			MAX22701		0.02	
High-Side Transistor Peak Output Current	$I_{OH}$	$C_L = 10nF$ , $f_{PWM} = 1kHz$ ( <i>Note 2</i> )	2.35	4		A
Low-Side Transistor Peak Output Current	$I_{OL}$	$C_L = 10nF$ , $f_{PWM} = 1kHz$ ( <i>Note 2</i> )	MAX22700/ MAX22702		3.7	A
			MAX22701		1.9	
Active Pulldown Voltage	$V_{OUTSD}$	$I_{OUT} = 150mA$ ( <i>Note 3</i> )			2.2	V
<b>MILLER CLAMP (MAX22701 ONLY)</b>						
Miller Clamp Transistor On-Resistance	$R_{DSON\_CLMP}$	$I_{CLAMP} = 100mA$ ( <i>Note 3</i> )			2.5	$\Omega$
Miller Clamp Threshold	$V_{TH\_CLMP}$		1.7	2	2.3	V
Miller Clamp Turn-On Time	$t_{ON}$	See <a href="#">Figure 2</a>		20		ns
<b>THERMAL SHUTDOWN</b>						
Thermal-Shutdown Threshold	$T_{SHDN}$			160		$^{\circ}C$
Thermal-Shutdown Hysteresis	$T_{SHDN\_HYS}$			25		$^{\circ}C$

## Dynamic Characteristics

( $V_{DDA} - V_{GNDA} = 5V$ ,  $V_{DDB} - V_{SSB} = 20V$ ,  $V_{GNDA} = V_{SSB} = 0V$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Common-Mode Transient Immunity	CMTI	( <a href="#">Note 4</a> )		300		kV/ $\mu\text{s}$	
Minimum Pulse Width	PW <sub>MIN</sub>	$C_L = 200\text{pF}$			20	ns	
Maximum PWM Frequency	f <sub>PWM</sub>		1			MHz	
Propagation Delay ( <a href="#">Figure 1</a> )	t <sub>PLH</sub>	$C_L = 200\text{pF}$ , output is not connected to CLAMP pin (MAX22701) ( <a href="#">Note 5</a> )	$T_A = +25^\circ\text{C}$ to $+125^\circ\text{C}$	34		39	ns
			$T_A = +25^\circ\text{C}$	34	35	36	
			$T_A = -40^\circ\text{C}$ to $+25^\circ\text{C}$	31		36	
	t <sub>PHL</sub>		$T_A = +25^\circ\text{C}$ to $+125^\circ\text{C}$	34		39	
			$T_A = +25^\circ\text{C}$	34	35	36	
			$T_A = -40^\circ\text{C}$ to $+25^\circ\text{C}$	31		36	
Part-to-Part Propagation Delay Matching ( <a href="#">Figure 1</a> )	t <sub>PM</sub>	$C_L = 200\text{pF}$ ( <a href="#">Note 5</a> )	$T_A = +25^\circ\text{C}$			2	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , parts at the same temperature			5	
Pulse Width Distortion	PWD	$C_L = 200\text{pF}$ , $ t_{PLH} - t_{PHL} $			2	ns	
Peak Eye Diagram Jitter	T <sub>JIT(PK)</sub>	1MHz square wave, $C_L = 200\text{pF}$		60		ps	
Rise Time ( <a href="#">Figure 1</a> )	t <sub>R</sub>	$C_L = 200\text{pF}$ , 20% to 80% ( <a href="#">Note 2</a> )			3.6	ns	
Fall Time ( <a href="#">Figure 1</a> )	t <sub>F</sub>	$C_L = 200\text{pF}$ , 80% to 20% ( <a href="#">Note 2</a> )	MAX22700/ MAX22702			1.8	ns
			MAX22701			2.5	

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ\text{C}$ . Specifications over temperature are guaranteed by design and characterization.

**Note 2:** Not production tested. Guaranteed by design and characterization.

**Note 3:** All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or V<sub>SSB</sub>), unless otherwise noted.

**Note 4:** CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. CMTI is tested with the transient generator connected between GNDA and V<sub>SSB</sub> ( $V_{CM} = 1000V$ ).

**Note 5:** Propagation delay is measured from 50% of the input to 2V at the output.

## ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, All Pins		±4		kV

Insulation Characteristics - 8 Narrow SOIC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Partial Discharge Test Voltage	V <sub>PR</sub>	Method B1 = V <sub>IORM</sub> x 1.5 (t = 1s, partial discharge < 5pC)		1272		V <sub>P</sub>
Maximum Repetitive-Peak Isolation Voltage	V <sub>IORM</sub>	( <a href="#">Note 6</a> )		848		V <sub>P</sub>
Maximum Working Isolation Voltage	V <sub>IOWM</sub>	Continuous RMS voltage ( <a href="#">Note 6</a> )		600		V <sub>RMS</sub>
Maximum Transient Isolation Voltage	V <sub>IOTM</sub>	t = 1s ( <a href="#">Note 6</a> )		4242		V <sub>P</sub>
Maximum Withstand Isolation Voltage	V <sub>ISO</sub>	f <sub>SW</sub> = 60Hz, duration = 60s ( <a href="#">Note 6</a> , <a href="#">Note 7</a> )		3000		V <sub>RMS</sub>
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 ( <a href="#">Note 6</a> , <a href="#">Note 9</a> )		5		kV
Insulation Resistance	RIO	V <sub>IO</sub> = 500V, T <sub>A</sub> = 25°C		> 10 <sup>12</sup>		Ω
		V <sub>IO</sub> = 500V, 100°C ≤ T <sub>A</sub> ≤ 125°C		> 10 <sup>11</sup>		
		V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C		> 10 <sup>9</sup>		
Barrier Capacitance Side A-to-Side B	CIO	f <sub>SW</sub> = 1MHz ( <a href="#">Note 8</a> )		1		pF
Minimum Creepage Distance	CPG	Narrow SOIC		4		mm
Minimum Clearance Distance	CLR	Narrow SOIC		4		mm
Internal Clearance		Distance through insulation		0.015		mm
Comparative Tracking Index	CTI	Material Group I (IEC 60112)		> 600		
Climate Category				40/125/ 21		
Pollution Degree (DIN VDE 0110, Table 1)				2		

Insulation Characteristics - 8 Wide SOIC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Partial Discharge Test Voltage	V <sub>PR</sub>	Method B1 = V <sub>IORM</sub> x 1.5 (t = 1s, partial discharge < 5pC)		1800		V <sub>P</sub>
Maximum Repetitive Peak Isolation Voltage	V <sub>IORM</sub>	( <i>Note 6</i> )		1200		V <sub>P</sub>
Maximum Working Isolation Voltage	V <sub>IOWM</sub>	Continuous RMS voltage ( <i>Note 6</i> )		848		V <sub>RMS</sub>
Maximum Transient Isolation Voltage	V <sub>IOTM</sub>	t = 1s ( <i>Note 6</i> )		7000		V <sub>P</sub>
Maximum Withstand Isolation Voltage	V <sub>ISO</sub>	f <sub>SW</sub> = 60Hz, duration = 60s ( <i>Note 6, Note 7</i> )		5000		V <sub>RMS</sub>
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 ( <i>Note 6, Note 9</i> )		5		kV
Insulation Resistance	RIO	V <sub>IO</sub> = 500V, T <sub>A</sub> = 25°C		> 10 <sup>12</sup>		Ω
		V <sub>IO</sub> = 500V, 100°C ≤ T <sub>A</sub> ≤ 125°C		> 10 <sup>11</sup>		
		V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C		> 10 <sup>9</sup>		
Barrier Capacitance Side A-to-Side B	CIO	f <sub>SW</sub> = 1MHz ( <i>Note 8</i> )		1		pF
Minimum Creepage Distance	CPG	Wide SOIC		8		mm
Minimum Clearance Distance	CLR	Wide SOIC		8		mm
Internal Clearance		Distance through insulation		0.015		mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)		> 400		
Climate Category				40/125/21		
Pollution Degree (DIN VDE 0110, Table 1)				2		

**Note 6:** V<sub>ISO</sub>, V<sub>IOTM</sub>, V<sub>IOSM</sub>, V<sub>IOWM</sub>, and V<sub>IORM</sub> are defined by the IEC 60747-5-5 standard.

**Note 7:** Product is qualified at V<sub>ISO</sub> for 60s and 100% production tested at 120% of V<sub>ISO</sub> for 1s.

**Note 8:** Capacitance is measured with all pins on side A and side B tied together.

**Note 9:** Devices are immersed in oil during surge characterization.



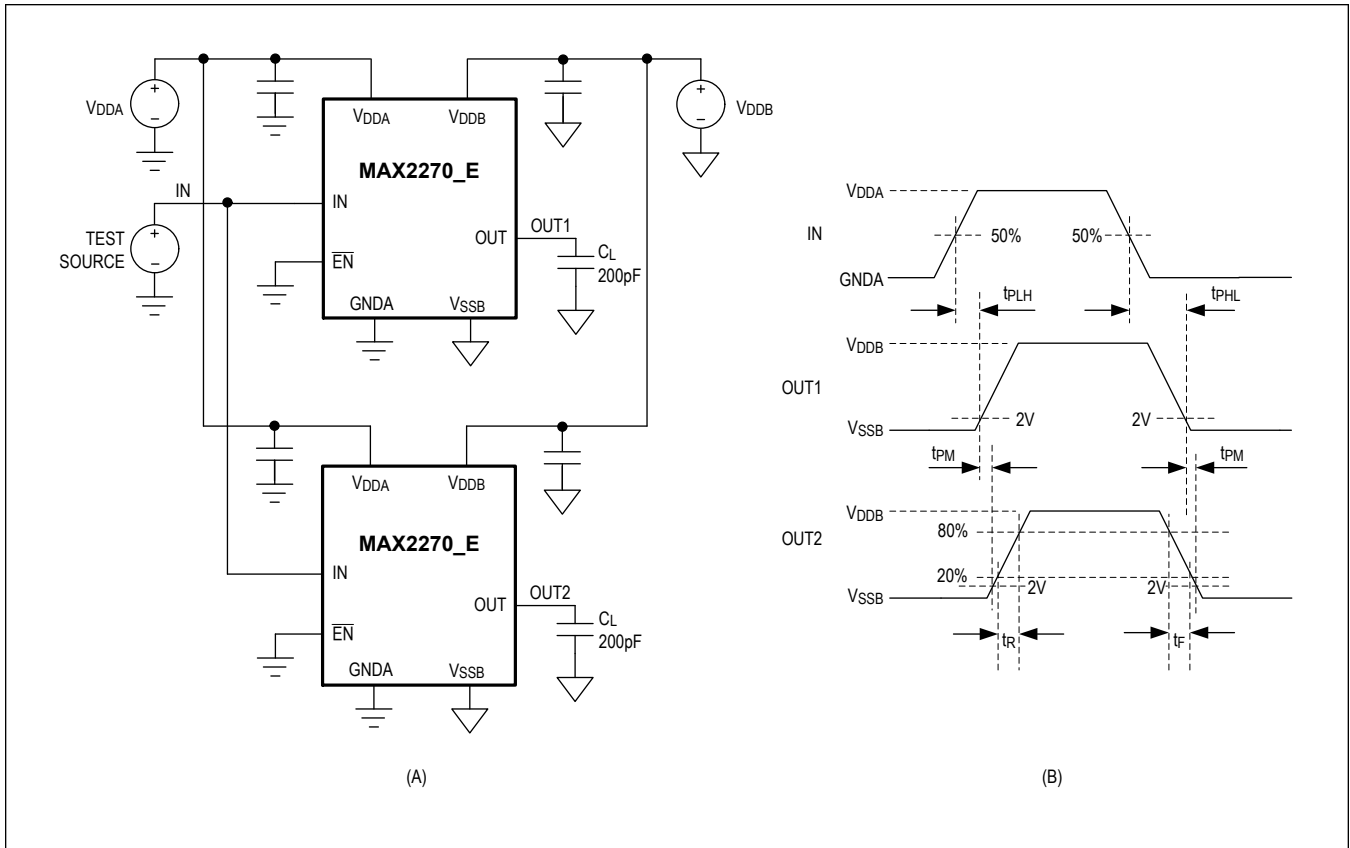


Figure 1. Test Circuit (A) and Timing Diagram (B)

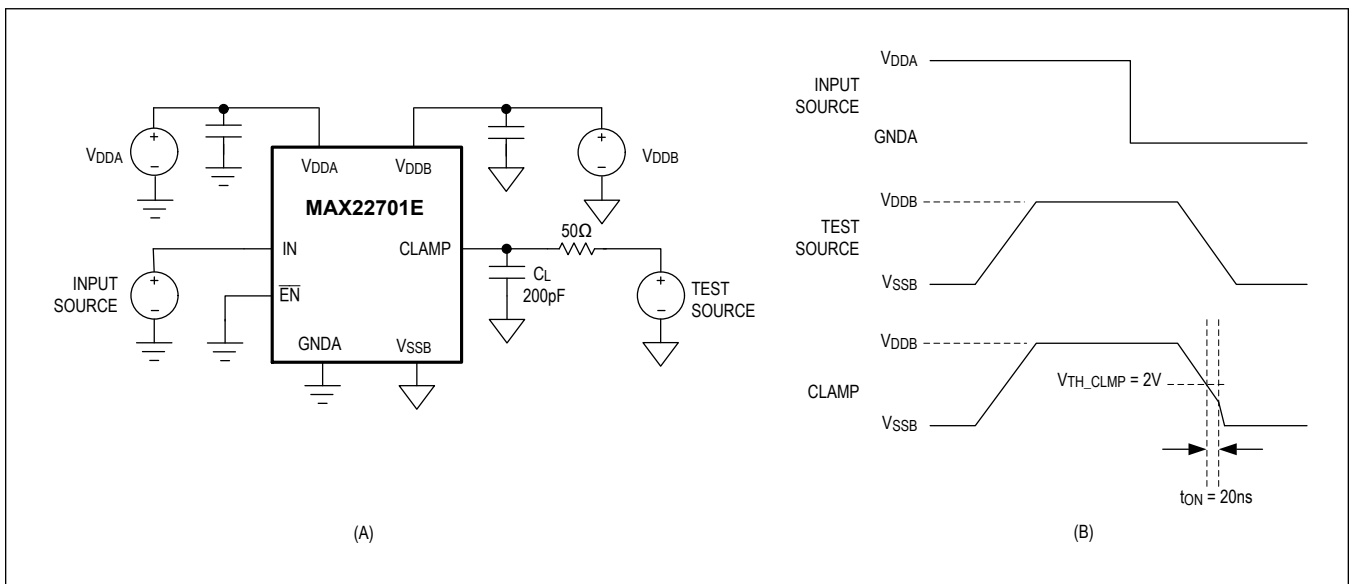
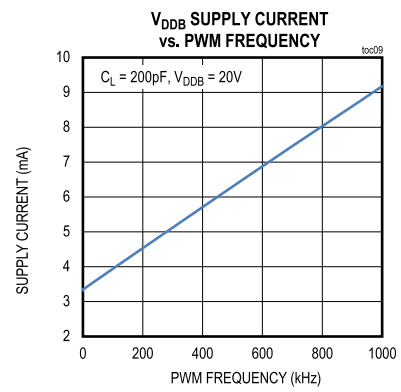
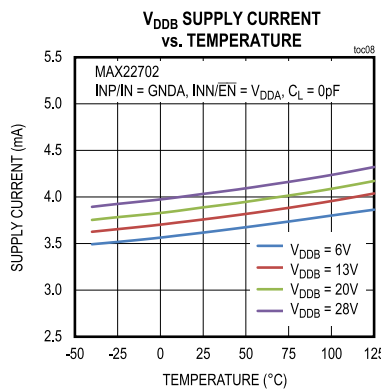
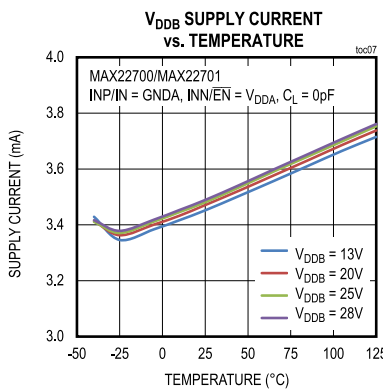
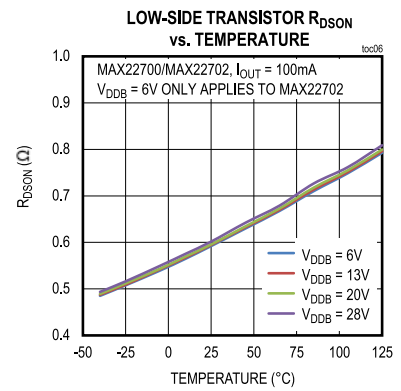
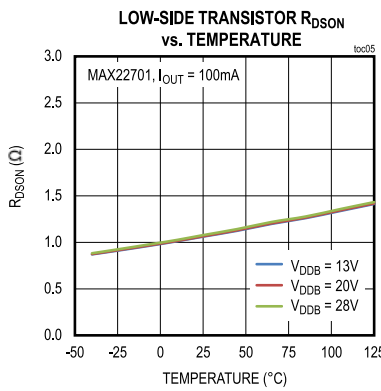
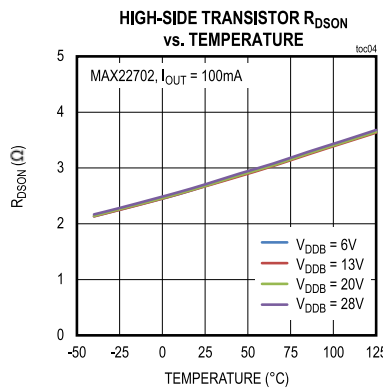
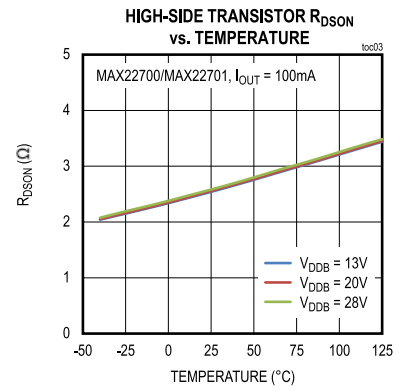
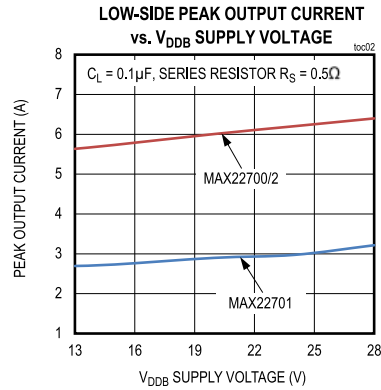
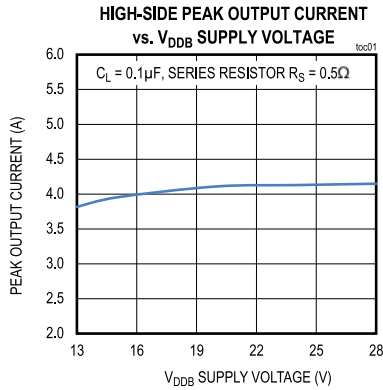


Figure 2. MAX22701 Miller Clamp Test Circuit (A) and Timing Diagram (B)

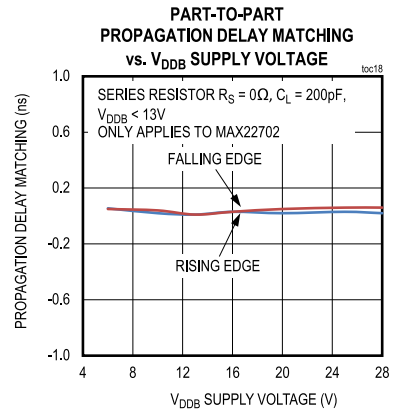
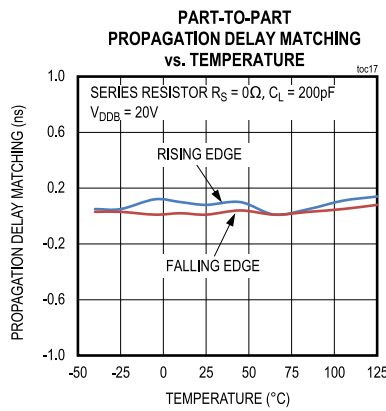
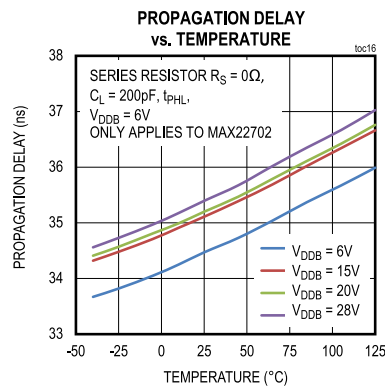
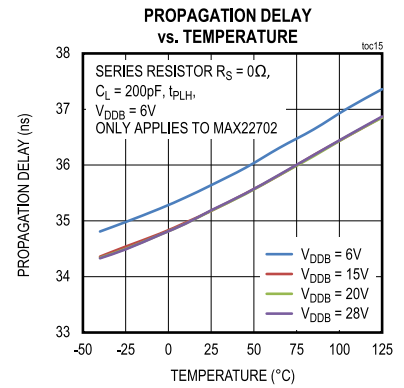
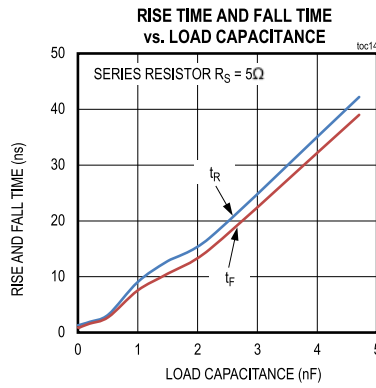
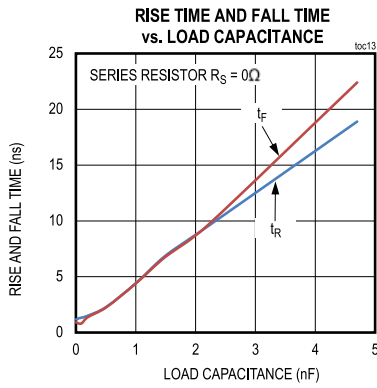
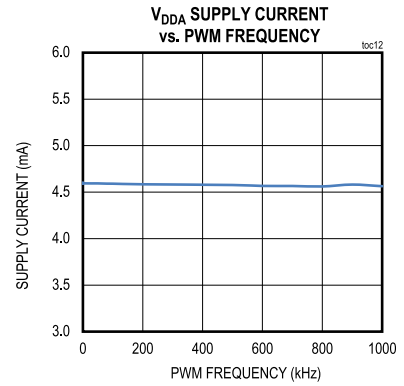
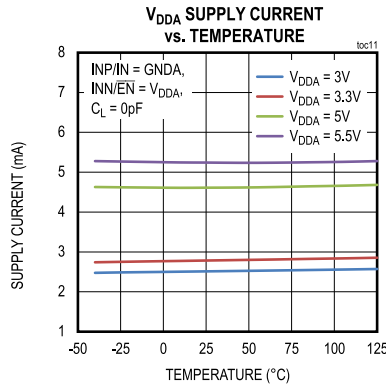
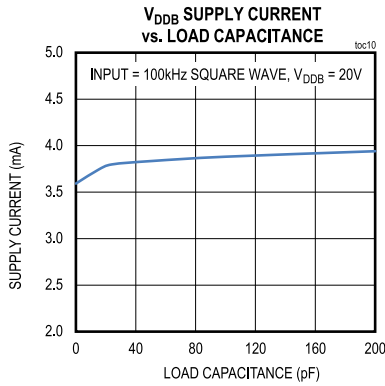
Typical Operating Characteristics

( $V_{DDA} - V_{GNDA} = 5V$ ,  $V_{DDB} - V_{SSB} = 20V$ ,  $V_{GNDA} = V_{SSB}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



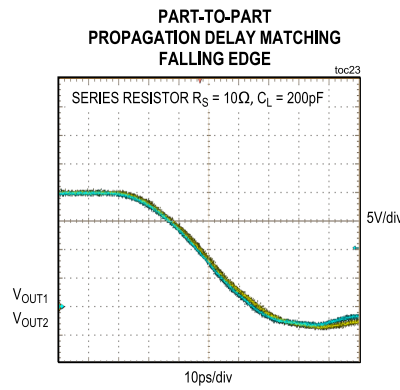
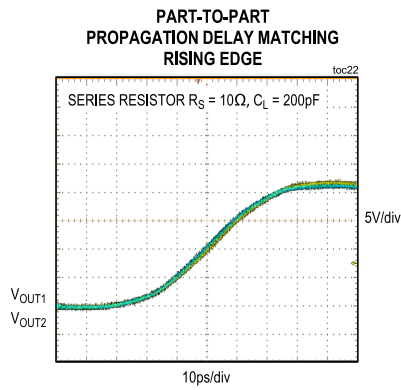
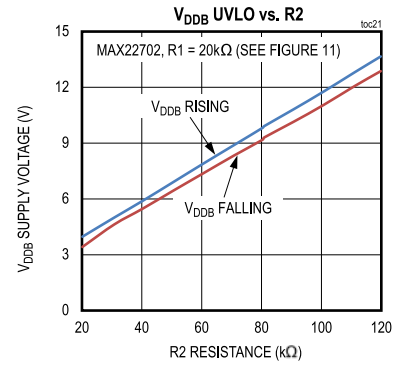
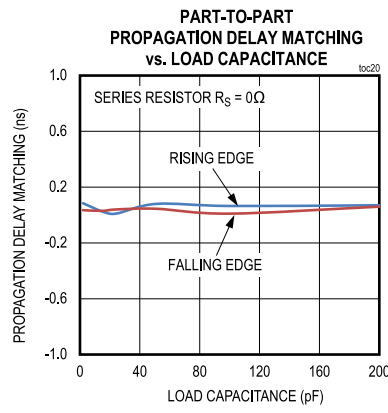
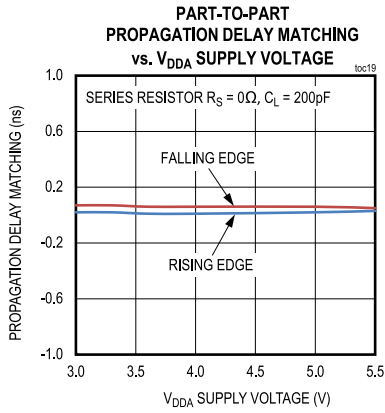
Typical Operating Characteristics (continued)

( $V_{DDA} - V_{GNDA} = 5V$ ,  $V_{DDB} - V_{SSB} = 20V$ ,  $V_{GNDA} = V_{SSB}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

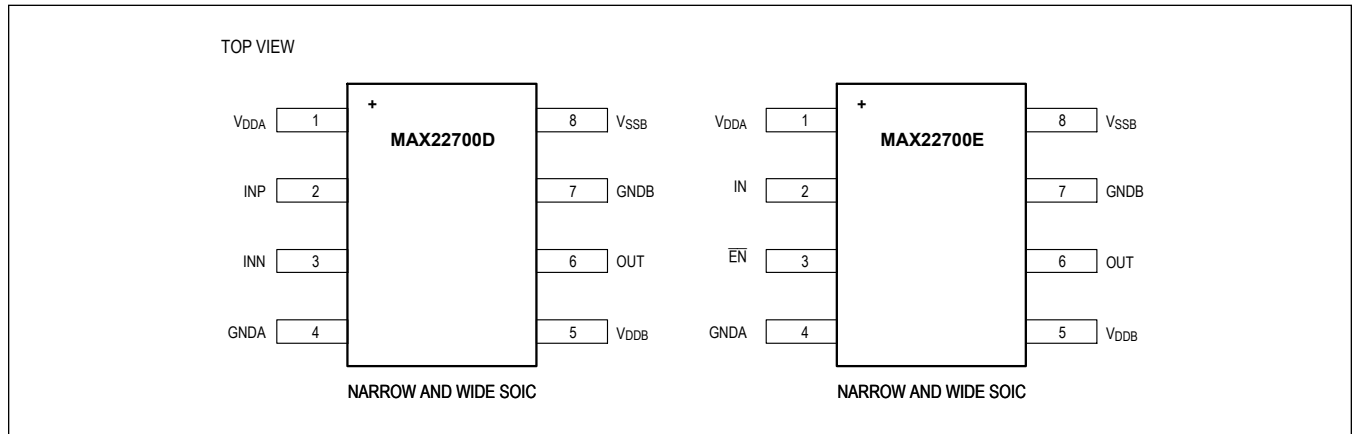


Typical Operating Characteristics (continued)

( $V_{DDA} - V_{GNDA} = 5V$ ,  $V_{DDB} - V_{SSB} = 20V$ ,  $V_{GNDA} = V_{SSB}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



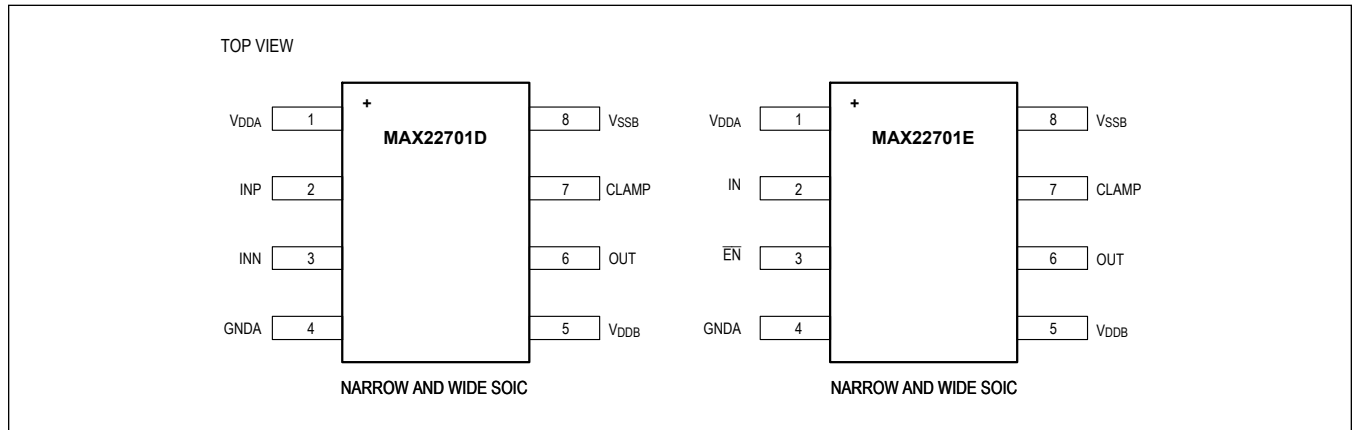
Pin Configurations - MAX22700



Pin Description - MAX22700

PIN		NAME	FUNCTION	REF SUPPLY
MAX22700D	MAX22700E			
<b>POWER</b>				
1	1	V <sub>DDA</sub>	Power Supply Input for Side A (Transmitter Side). Bypass V <sub>DDA</sub> to GNDA with 1nF    0.1µF    1µF ceramic capacitors as close as possible to the pin.	GNDA
4	4	GNDA	Ground Reference for Side A (Transmitter Side).	GNDA
5	5	V <sub>DDB</sub>	Positive Power Supply Input for Side B (Driver Side). Bypass V <sub>DDB</sub> to V <sub>SSB</sub> with 1nF    0.1µF    1µF ceramic capacitors as close as possible to the pin. Place an additional 22µF capacitor between V <sub>DDB</sub> and V <sub>SSB</sub> .	GNDB
8	8	V <sub>SSB</sub>	Negative Power Supply Input for Side B (Driver Side).	GNDB
7	7	GNDB	Gate Driver Common Pin. Connect to the power transistor's source pin. The B-side UVLO is referenced to GNDB in the MAX22700 versions.	GNDB
<b>INPUTS</b>				
2	-	INP	Non-Inverting PWM Input on Side A (D Version). Has a weak internal pulldown. Connect the differential PWM control inputs to INP and INN. Refer to <a href="#">Table 2</a> for Inputs vs. Output Truth table.	GNDA
3	-	INN	Inverting PWM Input on Side A (D Version). Has a weak internal pullup to V <sub>DDA</sub> . Connect the differential PWM control inputs to INP and INN. Refer to <a href="#">Table 2</a> for Inputs vs. Output Truth table.	GNDA
-	2	IN	Single-Ended PWM Input on Side A (E Version). Has a weak internal pulldown. Refer to <a href="#">Table 3</a> for Inputs vs. Output Truth table.	GNDA
-	3	$\overline{EN}$	Active-Low Enable on Side A (E Version). Has a weak internal pullup to V <sub>DDA</sub> .	GNDA
<b>OUTPUT</b>				
6	6	OUT	Gate Driver Output on Side B.	GNDB

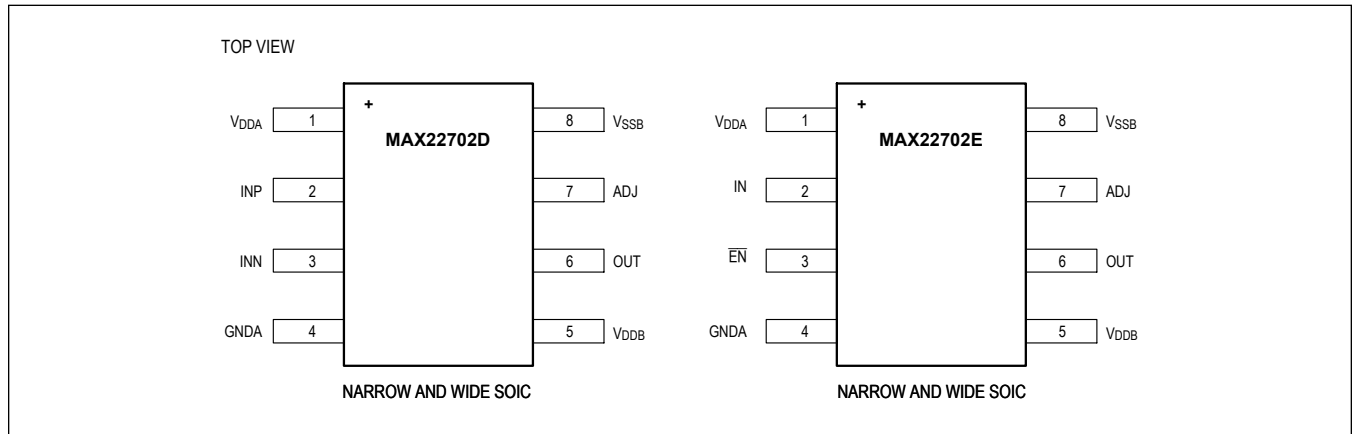
Pin Configurations - MAX22701



Pin Description - MAX22701

PIN		NAME	FUNCTION	REF SUPPLY
MAX22701D	MAX22701E			
<b>POWER</b>				
1	1	V <sub>DDA</sub>	Power Supply Input for Side A (Transmitter Side). Bypass V <sub>DDA</sub> to GNDA with 1nF    0.1µF    1µF ceramic capacitors as close as possible to the pin.	GNDA
4	4	GNDA	Ground Reference for Side A (Transmitter Side).	GNDA
5	5	V <sub>DDB</sub>	Positive Power Supply Input for Side B (Driver Side). Bypass V <sub>DDB</sub> to V <sub>SSB</sub> with 1nF    0.1µF    1µF ceramic capacitors as close as possible to the pin. Place an additional 22µF capacitor between V <sub>DDB</sub> and V <sub>SSB</sub> .	V <sub>SSB</sub>
8	8	V <sub>SSB</sub>	Negative Power Supply Input for Side B (Driver Side).	V <sub>SSB</sub>
<b>INPUTS</b>				
2	-	INP	Non-Inverting PWM Input on Side A (D Version). Has a weak internal pulldown. Connect the differential PWM control inputs to INP and INN. Refer to <a href="#">Table 2</a> for Inputs vs. Output Truth table.	GNDA
3	-	INN	Inverting PWM Input on Side A (D Version). Has a weak internal pullup to V <sub>DDA</sub> . Connect the differential PWM control inputs to INP and INN. Refer to <a href="#">Table 2</a> for Inputs vs. Output Truth table.	GNDA
-	2	IN	Single-Ended PWM Input on Side A (E Version). Has a weak internal pulldown. Refer to <a href="#">Table 3</a> for Inputs vs. Output Truth table.	GNDA
-	3	$\overline{\text{EN}}$	Active-Low Enable on Side A (E Version). Has a weak internal pullup to V <sub>DDA</sub> .	GNDA
<b>INPUT/OUTPUT</b>				
7	7	CLAMP	Active Miller Clamp Input/Output on Side B. Prevents false turn-on of the power transistor.	V <sub>SSB</sub>
<b>OUTPUT</b>				
6	6	OUT	Gate Driver Output on Side B.	V <sub>SSB</sub>

Pin Configurations - MAX22702



Pin Description - MAX22702

PIN		NAME	FUNCTION	REF SUPPLY
MAX22702D	MAX22702E			
<b>POWER</b>				
1	1	V <sub>DDA</sub>	Power Supply Input for Side A (Transmitter Side). Bypass V <sub>DDA</sub> to GNDA with 1nF    0.1µF    1µF ceramic capacitors as close as possible to the pin.	GNDA
4	4	GNDA	Ground Reference for Side A (Transmitter Side).	GNDA
5	5	V <sub>DDB</sub>	Positive Power Supply Input for Side B (Driver Side). Bypass V <sub>DDB</sub> to V <sub>SSB</sub> with 1nF    0.1µF    1µF ceramic capacitors as close as possible to the pin. Place an additional 22µF capacitor between V <sub>DDB</sub> and V <sub>SSB</sub> .	V <sub>SSB</sub>
8	8	V <sub>SSB</sub>	Negative Power Supply Input for Side B (Driver Side).	V <sub>SSB</sub>
<b>INPUTS</b>				
2	-	INP	Non-Inverting PWM Input on Side A (D Version). Has a weak internal pulldown. Connect the differential PWM control inputs to INP and INN. Refer to <a href="#">Table 2</a> for Inputs vs. Output Truth table.	GNDA
3	-	INN	Inverting PWM Input on Side A (D Version). Has a weak internal pullup to V <sub>DDA</sub> . Connect the differential PWM control inputs to INP and INN. Refer to <a href="#">Table 2</a> for Inputs vs. Output Truth table.	GNDA
-	2	IN	Single-Ended PWM Input on Side A (E Version). Has a weak internal pulldown. Refer to <a href="#">Table 3</a> for Inputs vs. Output Truth table.	GNDA
-	3	EN	Active-Low Enable on Side A (E Version). Has a weak internal pullup to V <sub>DDA</sub> .	GNDA
7	7	ADJ	Adjustable UVLO Input on Side B. Connect external resistors between V <sub>DDB</sub> and ADJ and between ADJ and the power transistor's source pin to adjust the B-side UVLO.	V <sub>SSB</sub>
<b>OUTPUT</b>				
6	6	OUT	Gate Driver Output on Side B.	V <sub>SSB</sub>

## Detailed Description

The MAX22700–MAX22702 are a family of single-channel isolated gate drivers with an ultra-high CMTI of 300kV/μs (typ). All devices have integrated digital galvanic isolation with an isolation rating of 3kV<sub>RMS</sub> in an 8-pin narrow-body SOIC package, or 5kV<sub>RMS</sub> in an 8-pin wide-body SOIC package. This family of devices offers high common-mode transient immunity, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices feature variants with output options for gate driver common pin GNDB (MAX22700), Miller clamp (MAX22701), and adjustable UVLO (MAX22702). In addition, variants are offered as differential inputs INP and INN (D versions) or single-ended input IN with enable EN (E versions). Refer to the [Ordering Information](#) for details.

The MAX22700 has a gate driver common pin (GNDB) that is a reference ground for V<sub>DDB</sub> and V<sub>SSB</sub>. V<sub>SSB</sub> has a voltage range between -16V and 0V with reference to GNDB. The MAX22701 has an active Miller clamp pin, CLAMP, which prevents false turn-on of the external power transistor caused by the Miller current. The MAX22702 provides an adjustable B-side UVLO, offering design flexibility with different types of external power transistors.

All devices support a minimum pulse width of 20ns with maximum pulse-width distortion of 2ns. The part-to-part propagation delay is matched within 2ns maximum at +25°C ambient temperature, and is guaranteed to be within 5ns maximum over the temperature range of -40°C to +125°C.

All MAX22700–MAX22702 have a default-low output. The default is the state the output assumes when the input is either not powered or is open-circuit. The output is set to logic-low when side A or side B supply is in UVLO, the device is in thermal shutdown, or EN is high (E versions).

## Output Driver Stage

The output driver stage of the MAX22700–MAX22702 features a pullup structure and a pulldown structure. The pullup structure consists of a pMOS transistor and a nMOS transistor in parallel (see the [Functional Diagrams](#)). The pMOS transistor has a maximum R<sub>DS(on)</sub> of 4.5Ω. The nMOS transistor only turns on for a short period of time during the output low-to-high transition and provides a boost current to enable the fast turn-on of the device. The nMOS transistor has a much lower on-resistance than the pMOS transistor; thus the parallel combination of the nMOS and the pMOS enables a faster turn-on during the output low-to-high transition.

The pulldown structure of the MAX22700–MAX22702 consists of a nMOS transistor. The nMOS transistor in the MAX22700 and the MAX22702 has a maximum R<sub>DS(on)</sub> of 1.25Ω, while the nMOS in the MAX22701 has an R<sub>DS(on)</sub> of 2.5Ω. For the MAX22701, when both OUT and CLAMP pins are connected to the gate of the external power transistor, an additional nMOS is connected in parallel to the pulldown nMOS transistor to prevent false turn-on of the external power transistor by providing an additional low-impedance path to V<sub>SSB</sub>. Refer to [Active Miller Clamp \(MAX22701 Only\)](#) section and the [Functional Diagrams](#) for details.

## Digital Isolation

The MAX22700–MAX22702 provide basic galvanic isolation for digital signals transmitted between two ground domains, and block high-voltage/high-current transients. The devices in the narrow-body SOIC package withstand differences of up to 3kV<sub>RMS</sub> for up to 60 seconds, and up to 848V<sub>PEAK</sub> of continuous isolation. The devices in the wide-body SOIC package withstand differences of up to 5kV<sub>RMS</sub> for up to 60 seconds and up to 1200V<sub>PEAK</sub> of continuous isolation. Refer to [Table 1](#) for certification information.

The devices have two supply inputs (V<sub>DDA</sub> and V<sub>DDB</sub>) that independently set the logic levels on either side of the device. V<sub>DDA</sub> and V<sub>DDB</sub> are referenced to GNDA and V<sub>SSB</sub>, respectively. Logic input and output levels match the supply voltages used in the associated power domain. The difference in ground potential between the two power domains can be as large as V<sub>IOWM</sub> for extended periods of time and withstand surge voltages up to 5kV. Data transfer integrity is maintained for a differential ground potential change up to 300kV/μs (typ).



**Table 1. Safety Regulatory Approvals**

<b>UL</b>
The MAX22700–MAX22702 are certified under UL1577. For more details, refer to file E351759.
Devices in narrow SOIC package are rated up to 3000V <sub>RMS</sub> isolation voltage for single protection.
Devices in wide SOIC package are rated up to 5000V <sub>RMS</sub> isolation voltage for single protection.
<b>cUL (Equivalent to CSA notice 5A)</b>
The MAX22700–MAX22702 are certified up to 3000V <sub>RMS</sub> (narrow SOIC package) or 5000V <sub>RMS</sub> (wide SOIC package) for single protection. For more details, refer to file E351759.
<b>VDE (Pending)</b>
The MAX22700–MAX22702 in wide SOIC are certified to DIN VDE V 0884-11: 2017-1. Basic Insulation, Maximum Transient Isolation Voltage 7000V <sub>PK</sub> , Maximum Repetitive Peak Isolation Voltage 1200V <sub>PK</sub>

**Note:** These couplers are suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

**Unidirectional Channel and Active Pulldown**

The MAX22700–MAX22702 have an unidirectional channel that passes data in one direction, as indicated in the [Functional Diagrams](#). The two internal transistors in the output driver are configured for push-pull operation and feature an active pulldown function to turn off the external power transistor when either side of the power supply is in UVLO. This prevents the external power transistor from falsely turning on during startup or UVLO.

**INN vs.  $\overline{EN}$  Function**

The MAX2270\_D features differential PWM inputs (INP and INN). The differential inputs reject input glitches and prevent false turn-on of the output. The output holds the previous value when a glitch is detected on either input ([Figure 3](#)). The MAX2270\_E features a single-ended input (IN) and an active-low input enable ( $\overline{EN}$ ). The  $\overline{EN}$  pin allows the output (OUT) to be quickly set to logic-low, turning off the external power transistor. The output remains at logic-low until the PWM input (IN) receives a logic-high signal ([Figure 4](#)).

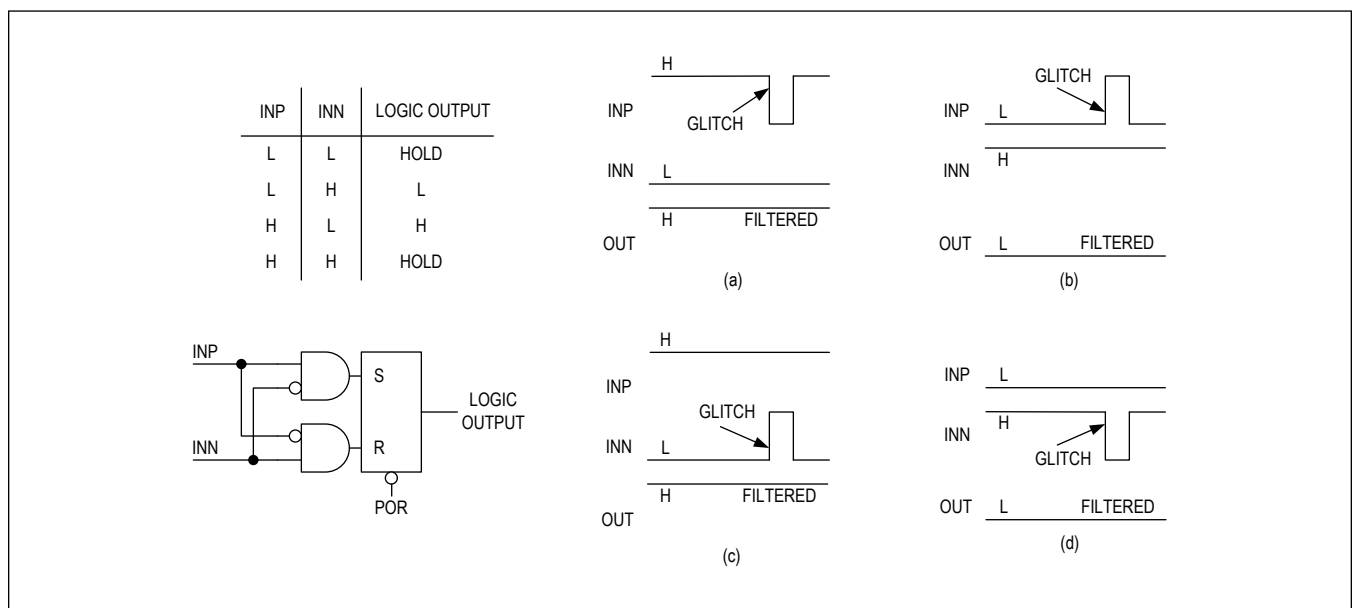


Figure 3. MAX2270\_D Differential Inputs

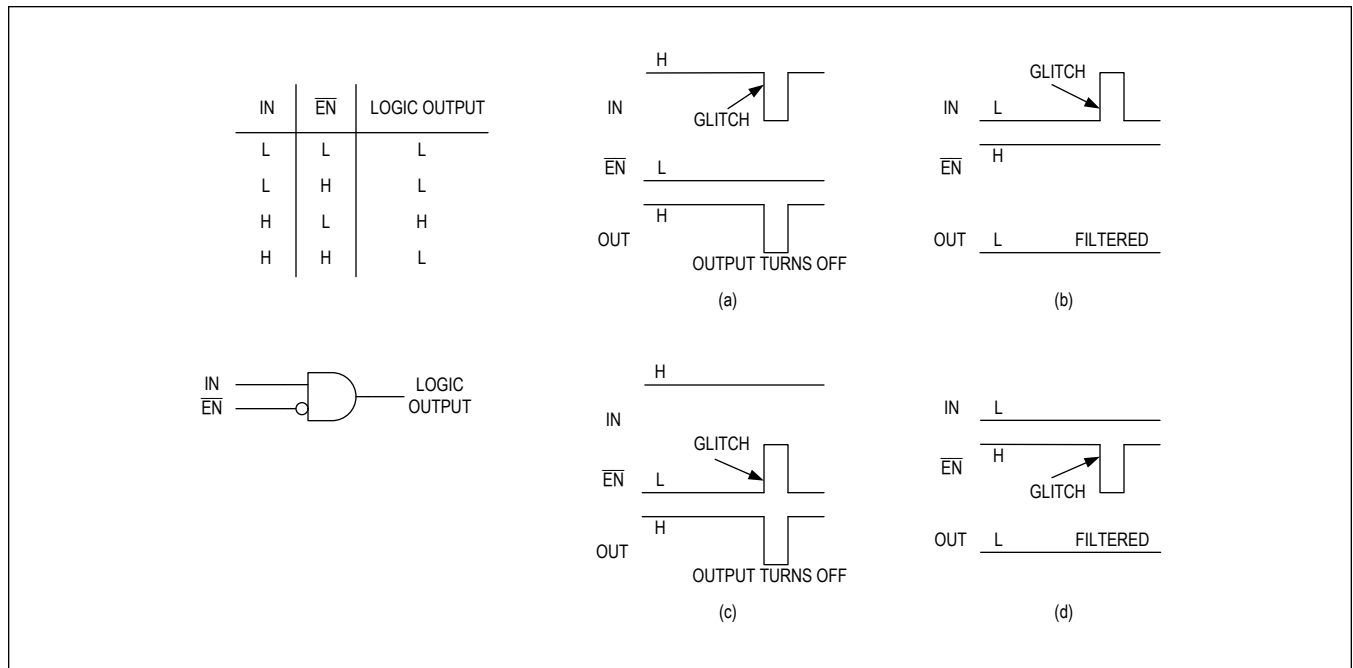


Figure 4. MAX2270\_E Single-Ended Input with Enable

Current sources are used at both A-side inputs to prevent the output from falsely turning on by input glitches or noise. The INN pin has a weak pullup and the INP has a weak pulldown in the MAX2270\_D devices. The EN pin has a weak pullup and the IN pin has a weak pulldown in the MAX2270\_E devices. Refer to [Table 2](#) and [Table 3](#) for the Inputs vs. Output Truth Tables.

**Table 2. MAX2270\_D Inputs vs. Output Truth Table**

INP	INN	OUT
Low	Low	Hold
Low	High	Low
High	Low	High
High	High	Hold

**Table 3. MAX2270\_E Inputs vs. Output Truth Table**

IN	$\overline{\text{EN}}$	OUT
Low	Low	Low
Low	High	Low (Default)
High	Low	High
High	High	Low (Default)

### Undervoltage Lockout (UVLO)

The  $V_{\text{DDA}}$  and  $V_{\text{DDB}}$  supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, the output is set to logic-low (default state) to turn off the external power transistor, regardless of the state of the MAX22700–MAX22702 inputs. The B-side UVLO has an internal filter to reject any  $V_{\text{DDB}}$  glitches less than 32 $\mu\text{s}$  (typ) (see [Figure 9](#) and [Figure 10](#)). [Figure 5](#) through [Figure 8](#) show the behavior of the outputs during power-up and power-down.

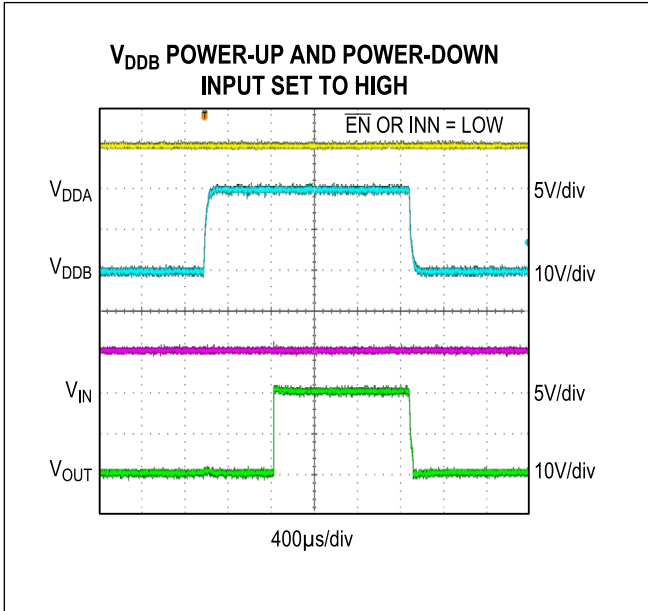


Figure 5.  $V_{DDB}$  Undervoltage Lockout Behavior (Input High)

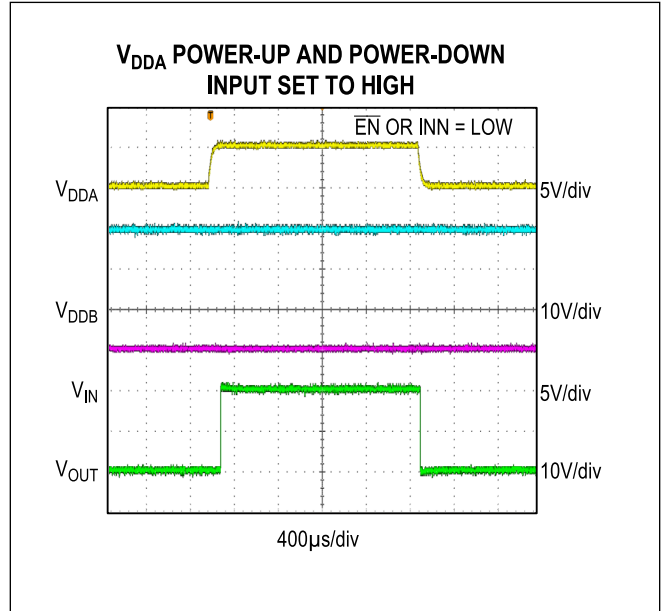


Figure 6.  $V_{DDA}$  Undervoltage Lockout Behavior (Input High)

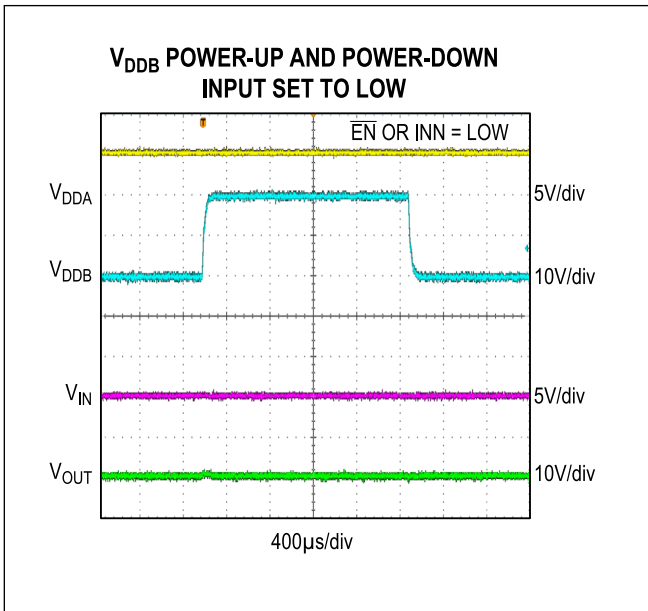


Figure 7.  $V_{DDB}$  Undervoltage Lockout Behavior (Input Low)

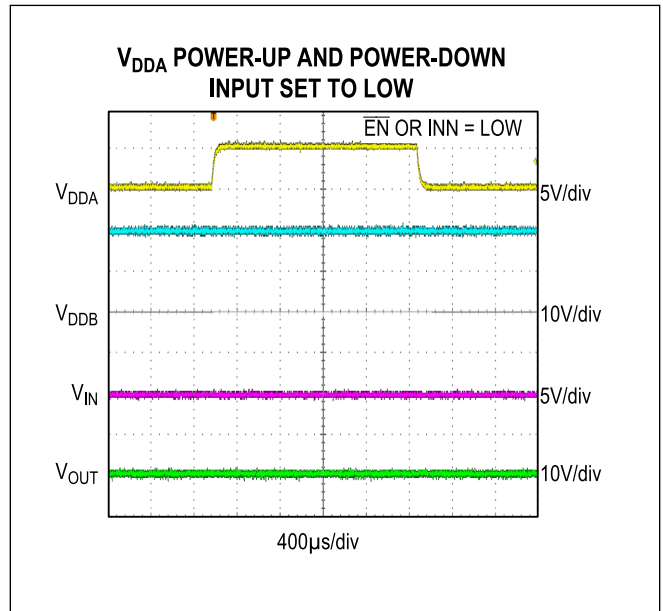


Figure 8.  $V_{DDA}$  Undervoltage Lockout Behavior (Input Low)

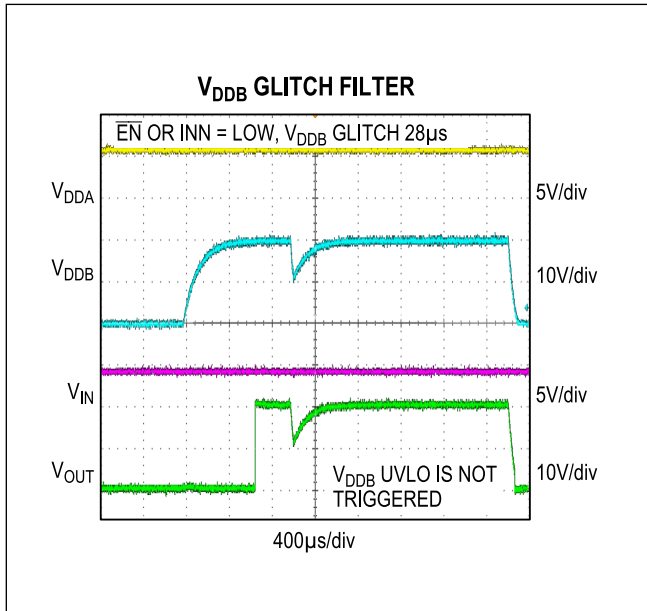


Figure 9.  $V_{DDB}$  Undervoltage Lockout Glitch Filter, UVLO Not Triggered

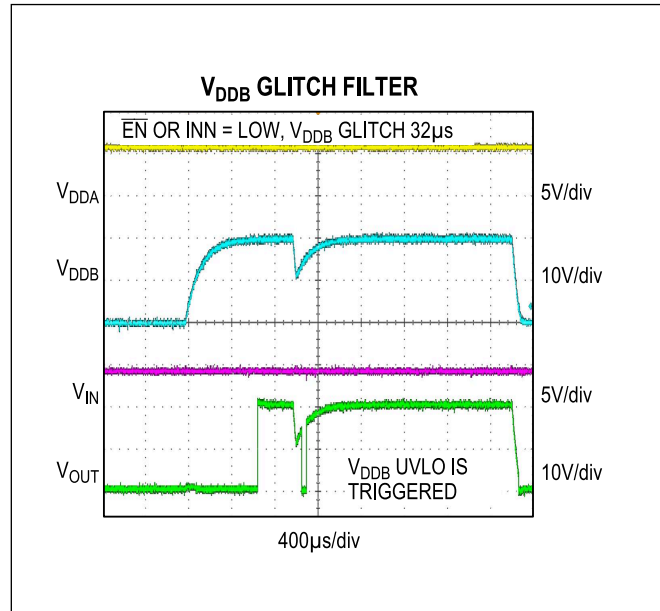


Figure 10.  $V_{DDB}$  Undervoltage Lockout Glitch Filter, UVLO Triggered

### Thermal Shutdown

The MAX22700–MAX22702 operate at an ambient temperature up to +125°C on a properly designed multilayer PCB. Operating at higher voltages or with heavy output loads increases the junction temperature and power dissipation, and also reduce the maximum allowable operating temperature. See the [Package Information](#), [Absolute Maximum Ratings](#) and [Safety Limits](#) sections for details.

The MAX22700–MAX22702 is in thermal shutdown when the junction temperature of the device exceeds +160°C (typ). During thermal shutdown, the output is set to logic-low to turn off the external power transistor regardless of the state of the MAX22700–MAX22702 inputs.

### Active Miller Clamp (MAX22701 Only)

The MAX22701 features an active Miller clamp to prevent false turn-on of the external power transistor caused by the Miller current. When the external high-side transistor is turned on after the external low-side transistor is turned off, the internal Miller clamp transistor starts to engage when the Miller clamp pin voltage drops below the 2V threshold, and it provides a low-impedance path to direct the Miller current to  $V_{SSB}$ . Refer to [Figure 2](#) for a Miller clamp timing diagram.

### Adjustable UVLO (MAX22702 Only)

The MAX22702 features an adjustable B-side UVLO to accommodate UVLO requirements of different types of external power transistors. To set a user-defined B-side UVLO, connect external resistors between  $V_{DDB}$  and ADJ, and between ADJ and the external power transistor ground so that:

$$V_{ADJ\_UVLO} = 2 \times (1 + R2 \div R1)$$

where R1 is placed between  $V_{DDB}$  and ADJ, and R2 is placed between ADJ and the external power transistor ground (see [Figure 11](#)).

For example, to set the B-side UVLO to 13V, connect 20kΩ (R1) between  $V_{DDB}$  and ADJ. R2 is:

$$(13 \div 2 - 1) \times 20 = 110k\Omega$$

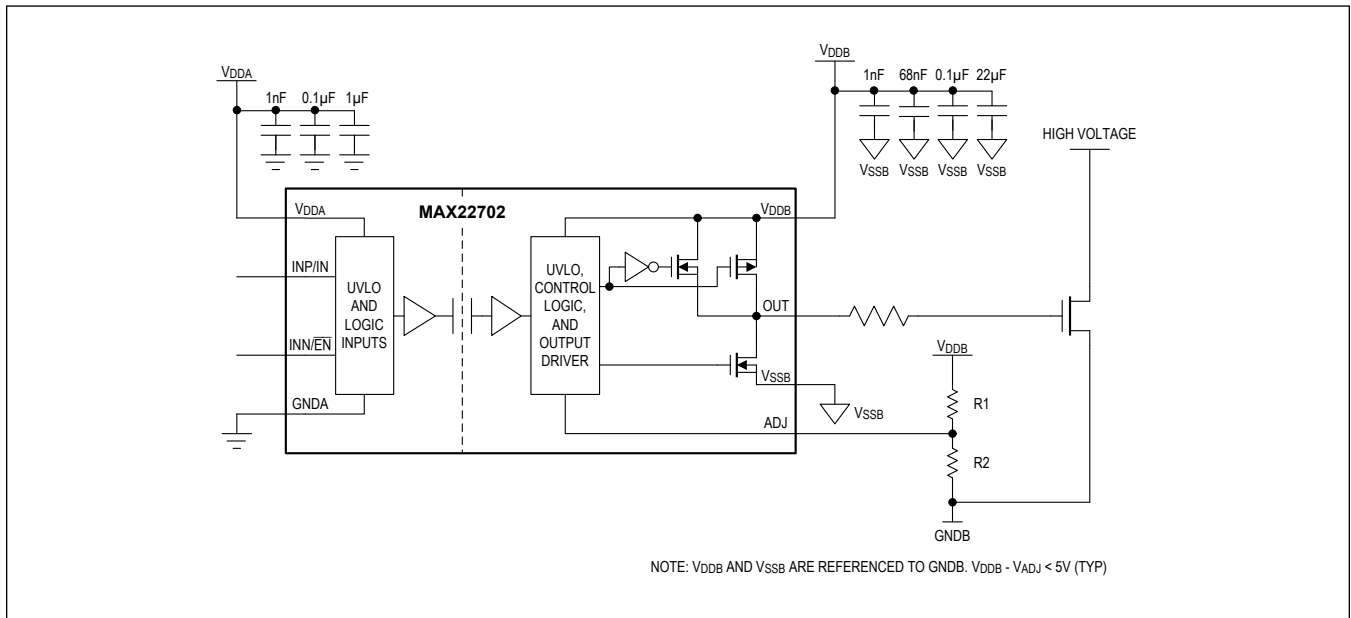


Figure 11. Example Circuit for MAX22702 Adjustable UVLO

### Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22700–MAX22702 could dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing long-term reliability issues. [Table 4](#) shows the safety limits for the MAX22700–MAX22702.

The maximum safety temperature ( $T_S$ ) for the device is the +150°C maximum junction temperature specified in the [Absolute Maximum Ratings](#). The power dissipation ( $P_D$ ) and junction-to-ambient thermal impedance ( $\theta_{JA}$ ) determine the junction temperature. Thermal impedance values ( $\theta_{JA}$  and  $\theta_{JC}$ ) are available in the [Package Information](#) section of the data sheet and power dissipation calculations are discussed in the [Calculating Power Dissipation](#) section. Calculate the junction temperature ( $T_J$ ) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

[Figure 12](#) to [Figure 14](#) show the thermal derating curves for safety limiting the power and the current of the devices. Ensure that the junction temperature does not exceed +150°C.

**Table 4. Safety Limiting Values for the MAX22700–MAX22702**

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT	
Safety Operating Current on B-Side Pins	$I_{OUT}$	$T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ , IN = Low, OUT = $V_{DDB}$ , OUT = Low during thermal shutdown	$V_{DDB} = 28\text{V}$	38	mA
			$V_{DDB} = 20\text{V}$	53	mA
Safety Current on Any Pins (No Damage to Isolation Barrier)	$I_S$	$T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$	300	mA	
Total Safety Power Dissipation	$P_S$	$T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$	8 Narrow SOIC	1173	mW
			8 Wide SOIC	1064	
Maximum Safety Temperature	$T_S$		150	°C	

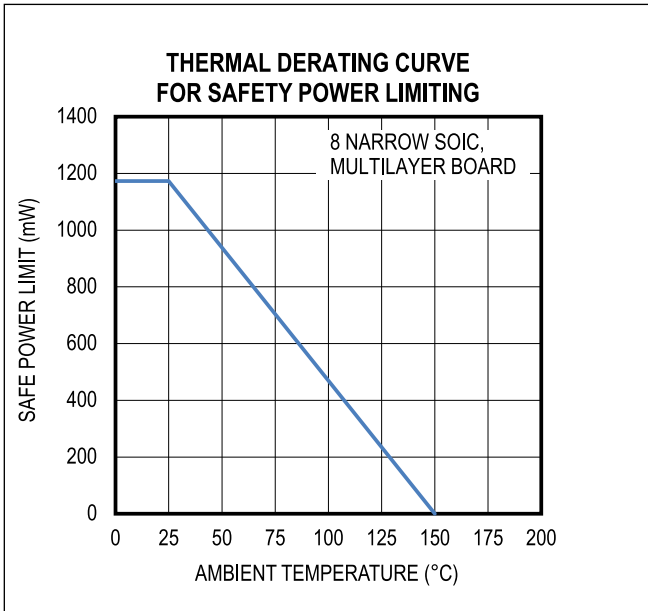


Figure 12. Thermal Derating Curve for Safety Power Limiting (8 Narrow SOIC)

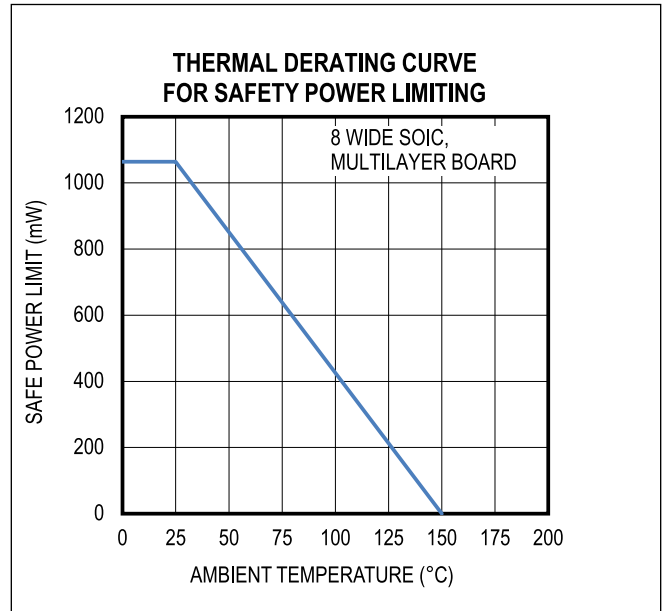


Figure 13. Thermal Derating Curve for Safety Power Limiting (8 Wide SOIC)

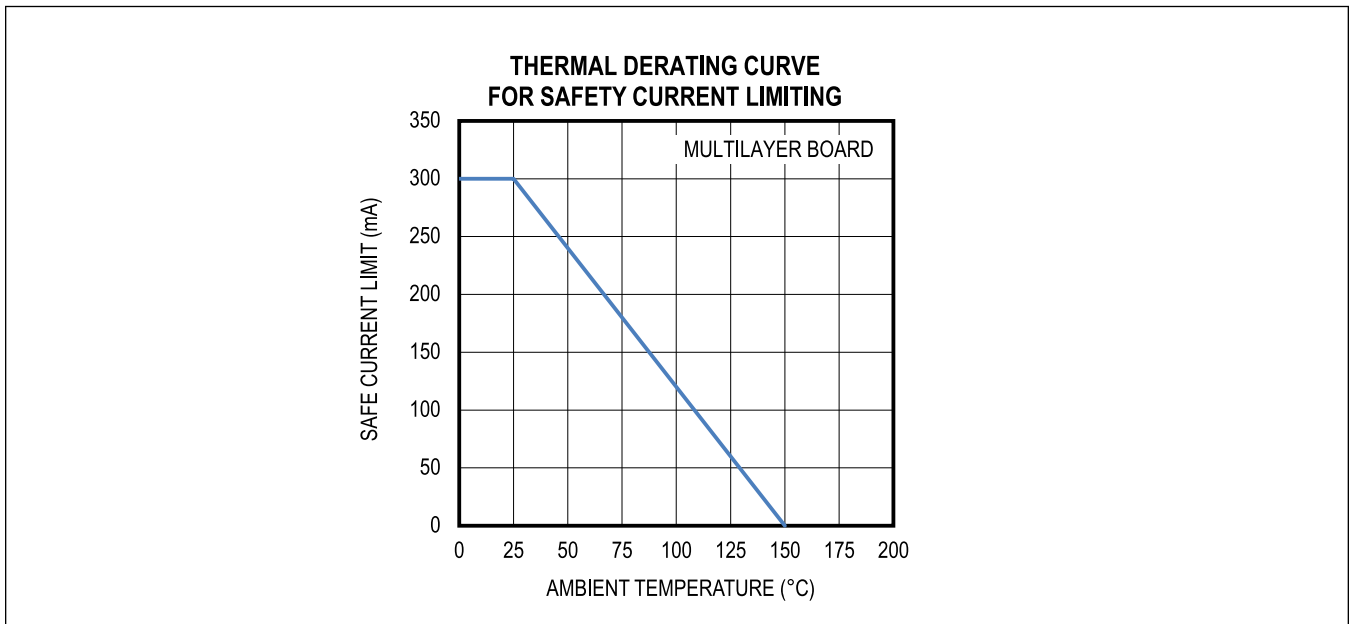


Figure 14. Thermal Derating Curve for Safety Current Limiting

## Applications Information

### Power-Supply Sequencing

The MAX22700–MAX22702 do not require special power-supply sequencing. The logic levels are set independently on either side by  $V_{DDA}$  and  $V_{DDB}$ . Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

### Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass  $V_{DDA}$  and  $V_{DDB}$  with 1nF, 0.1 $\mu$ F, and 1 $\mu$ F low-ESR and low-ESL ceramic capacitors with sufficient voltage rating in parallel to GND and  $V_{SSB}$ , respectively. To ensure the best performance, place the decoupling capacitors as close to the power-supply pins as possible.

On the B side, it is recommended to place the 1nF and 1 $\mu$ F capacitors close to the  $V_{SSB}$  pin, and place the 0.1 $\mu$ F capacitor close to the  $V_{DDB}$  pin. To further reduce supply ripple while operating at higher supply voltage and data rates, place a 68nF 1206 C0G/NP0 capacitor across the  $V_{DDB}$  pin and  $V_{SSB}$  pin as close to the pins as possible. It is also recommended to include a 22 $\mu$ F reservoir capacitor (tantalum or electrolytic type) between  $V_{DDB}$  and  $V_{SSB}$  in case the  $V_{DDB}$  power supply is located far away from the  $V_{DDB}$  pin. All bypass capacitors on  $V_{DDB}$  are required to have at least a 50V voltage rating.

### Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To maintain low signal-path inductance, avoid using vias.
- Place the gate driver as close to the external power transistor as possible to decrease the trace inductance and avoid output ringing.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX22700–MAX22702 free from ground and signal planes. Any galvanic or metallic connection between side A and side B defeats the isolation.
- Have a solid ground plane next to  $V_{SSB}$  pin with multiple  $V_{SSB}$  vias to reduce the parasitic inductance and minimize the ringing on the output signal.
- Place a 68nF 1206 C0G/NP0 bypass capacitor across pin 5 and pin 8 as close as possible to the pins to mitigate B-side supply ripple.

### Calculating Power Dissipation

The required current for the A side of the MAX22700–MAX22702 depends on the  $V_{DDA}$  supply voltage and the data rate. The required current for the B side of the MAX22700–MAX22702 depends on the  $V_{DDB}$  supply voltage, the data rate, and the load condition. The typical current for different  $V_{DDA}$  and  $V_{DDB}$  supply voltages at any data rate without external load can be estimated from the graphs in [Figure 15](#) and [Figure 16](#). Please note that the data in [Figure 15](#) and [Figure 16](#) are extrapolated from supply current measurements in a typical operating condition.

The total current for the B side is the sum of the “no load” current (shown in [Figure 16](#)) which is a function of the voltage and the data rate, and the “load current”, which depends on the load impedance. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DDB}$$

where:

$I_{CL}$  = Current required to drive the capacitive load.

$C_L$  = Load capacitance on the output pin.

$f_{SW}$  = Switching frequency in Hz.

$V_{DDB}$  = B-side supply voltage.

The total power dissipation ( $P_D$ ) can be calculated as:

$$P_D = V_{DDA} \times I_{DDA} + V_{DDB} \times I_{DDB}$$

where  $I_{DDA}$  is the A-side supply current and  $I_{DDB}$  is the B-side supply current.

**Example:** A MAX22701 is operating with  $V_{DDA} = 5V$ ,  $V_{DDB} = 20V$ . The output is operating at 10kHz with 1nF capacitive load.  $V_{DDA}$  must supply about 4.56mA with a 10kHz data rate and a 5V supply voltage according to Figure 15.  $V_{DDB}$  must supply the sum of the no load current and the load current. The no load current is about 3.77mA with a 10kHz data rate and a 20V supply voltage according to Figure 16. The load current is equal to  $1nF \times 10kHz \times 20V = 0.2mA$ .  $V_{DDB}$  must therefore supply about 3.97mA. The total power dissipation is  $5V \times 4.56mA + 20V \times 3.97mA = 102.2mW$ .

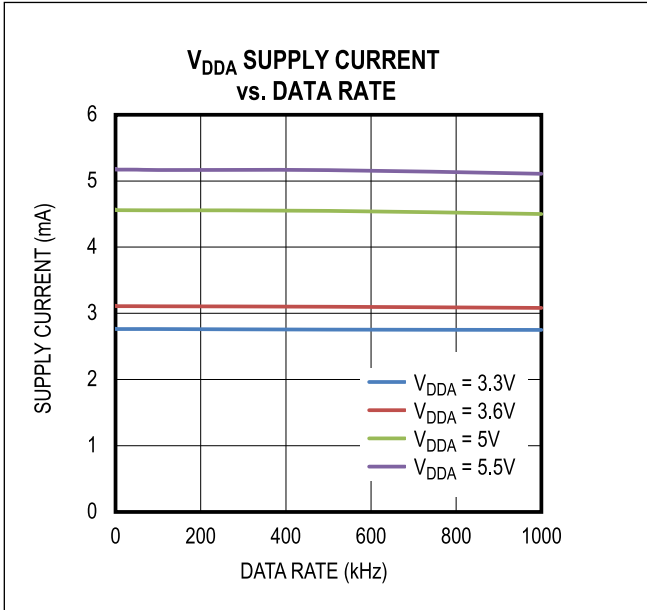


Figure 15.  $V_{DDA}$  Supply Current vs. Data Rate (typ)

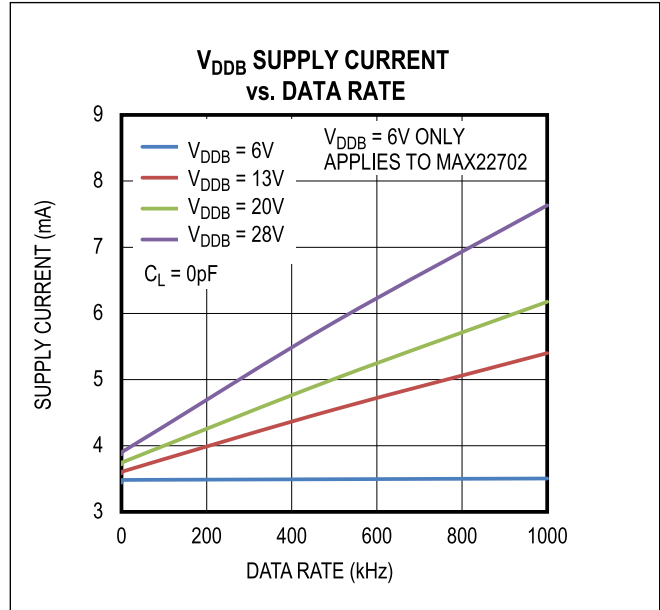


Figure 16.  $V_{DDB}$  Supply Current vs. Data Rate (typ)

### Gate Driver Output Resistors

External series resistors ( $R_{ON}$  and  $R_{OFF}$ ) between the MAX22700–MAX22702 output and the gate of the power transistor are required in gate driver applications. These resistors control the turn-on and turn-off time of the power transistor to optimize switching efficiency and EMI performance.

The  $R_{ON}$  resistance and external FET's gate capacitance determine the turn-on time. The parallel combination of both  $R_{ON}$  and  $R_{OFF}$  resistance and the external FET's gate capacitance determine the turn-off time. Turn-off time is usually much faster than turn-on time to avoid shoot-through. Figure 17 shows a typical  $R_{ON}$  and  $R_{OFF}$  network for the MAX22700–MAX22702.  $R_{ON}$  and  $R_{OFF}$  values should be adjusted based on the required slew rate and the external FET's gate capacitance.

The gate driver output resistors also help limit ringing caused by parasitic inductances and capacitances due to PCB layout and device package leads. Output ringing can happen during high voltage  $dV/dt$  and high current  $di/dt$  switching. Increasing  $R_{ON}$  and  $R_{OFF}$  can help reduce the ringing.



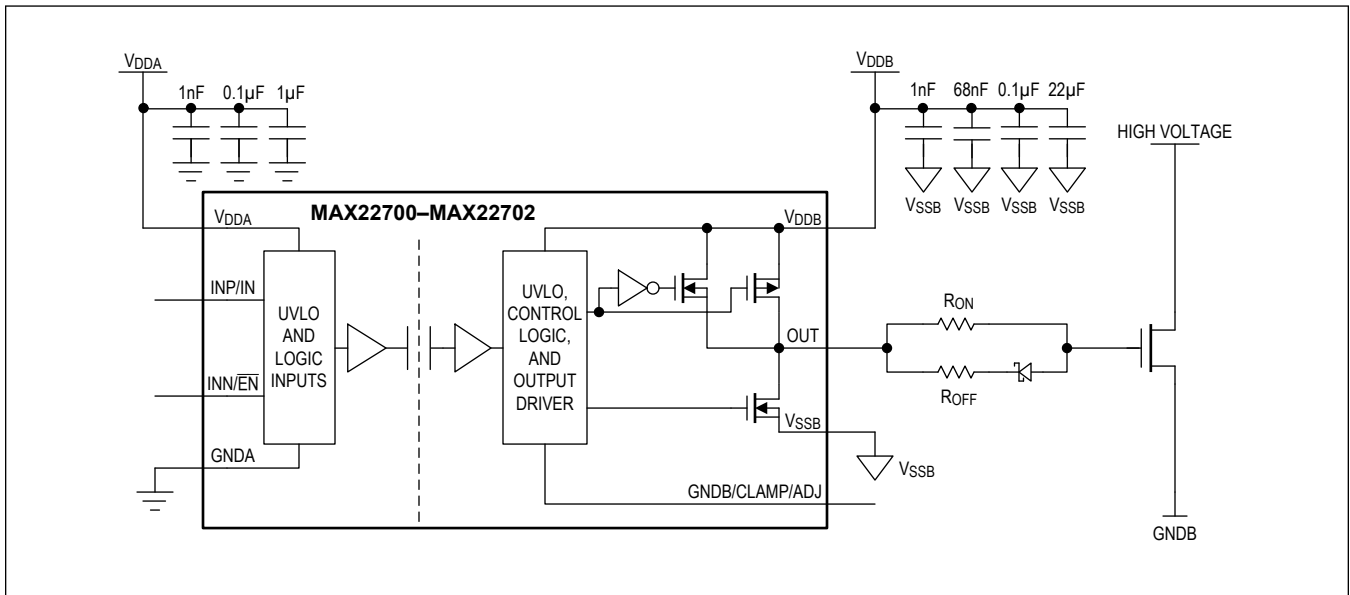


Figure 17. Typical Gate Driver Output Network with  $R_{ON}$  and  $R_{OFF}$

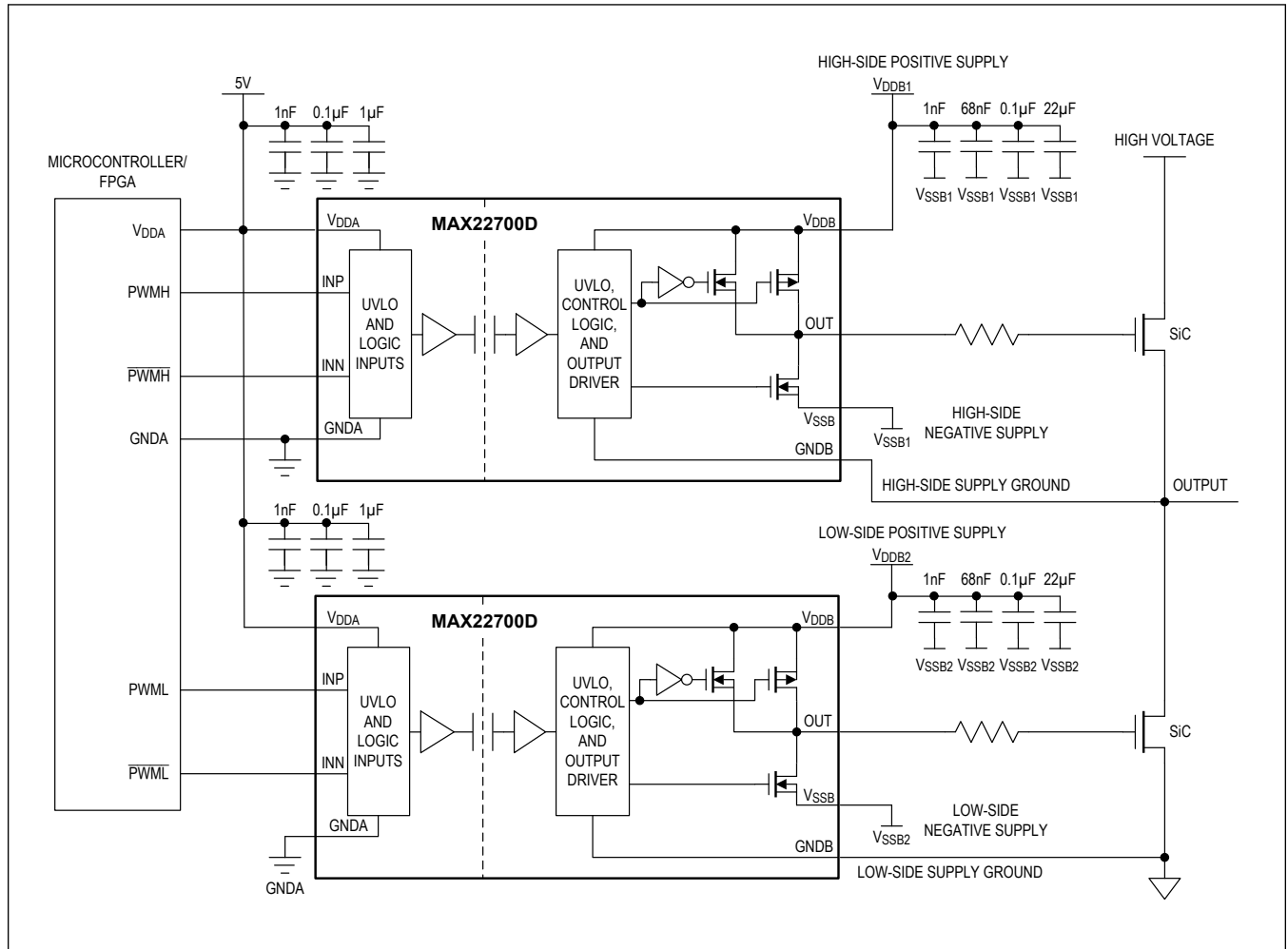
### Driving GaN Transistors

The high CMTI rating of  $300\text{kV}/\mu\text{s}$  (typ) and the propagation delay matching of  $5\text{ns}$  (max) between the high-side and low-side drivers make the MAX22701 and MAX22702 ideal to drive GaN devices. The MAX22702 also features an adjustable B-side UVLO to accommodate the low gate drive voltage of GaN devices.

As shown in the [Typical Application Circuits](#), a positive supply ( $V_{DDB}$ ) and a negative supply ( $V_{SSB}$ ) with reference to  $\text{GNDB}$  are required to meet the gate voltage requirement of GaN devices when using the MAX22701 and MAX22702 as GaN gate drivers. A boost current is required during the GaN device's turn-on period; hence a capacitor is placed in series with one of the resistors at the output. This capacitor needs to be discharged during the turn-off period. Therefore, a diode is placed in parallel to the resistor to provide a discharge path. On the layout, it is recommended to place the gate driver very close to the GaN device to minimize series inductance and reduce gate drive loop area. To prevent ringing and support high peak currents when turning on GaN devices, good decoupling is required on the  $V_{DDB}$  and  $V_{SSB}$  pins.

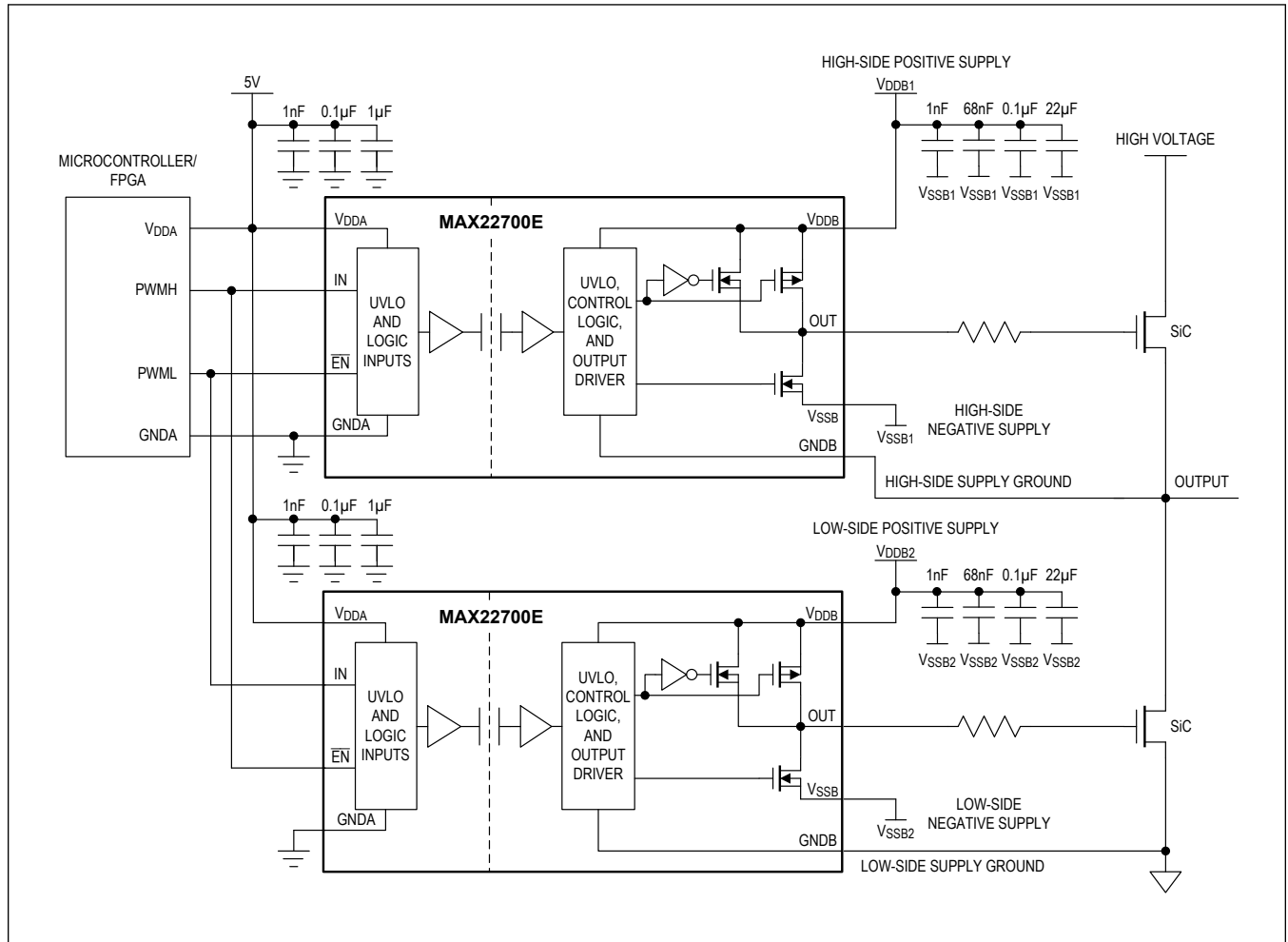
Typical Application Circuits

MAX22700D



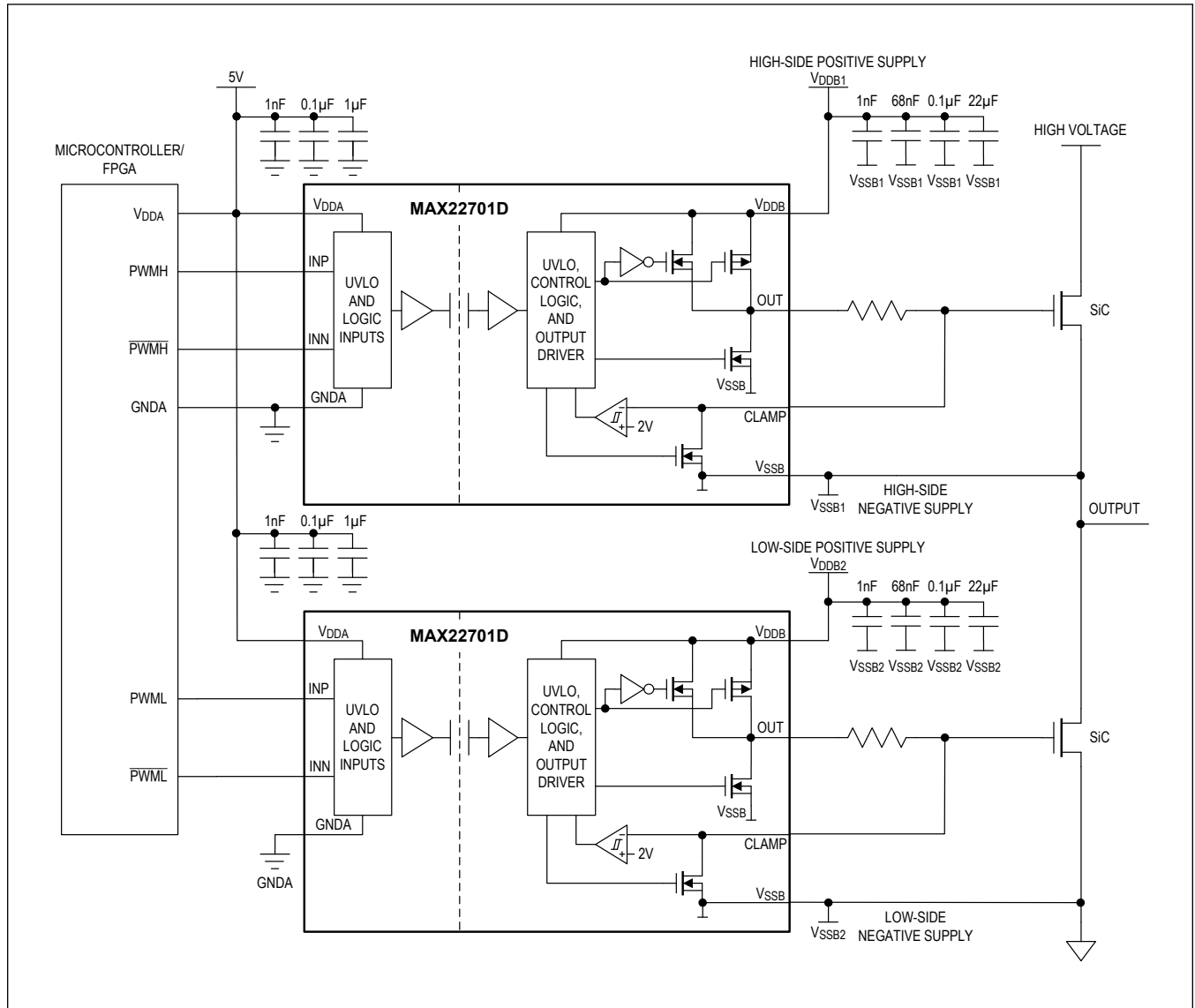
Typical Application Circuits (continued)

MAX22700E



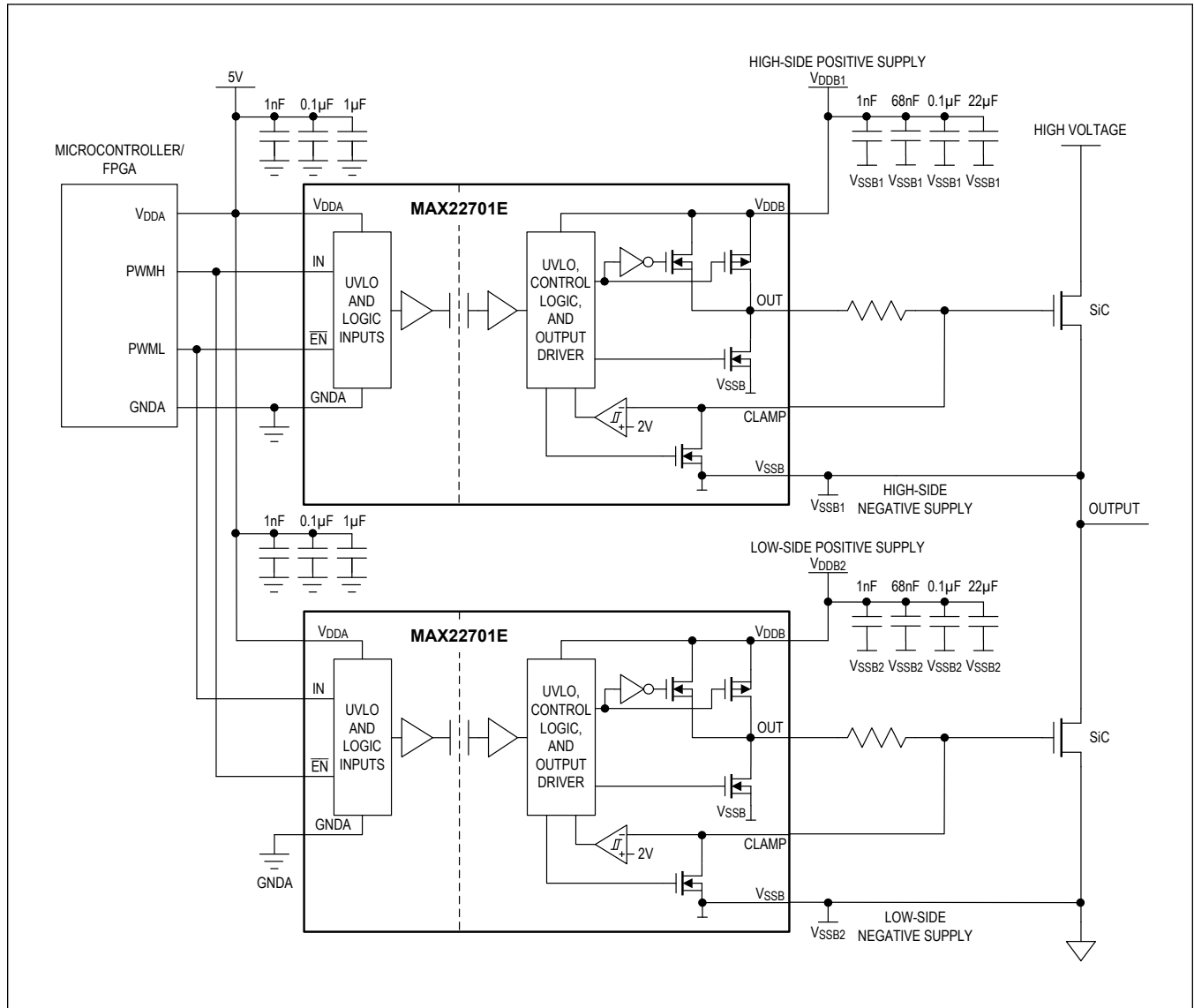
Typical Application Circuits (continued)

MAX22701D



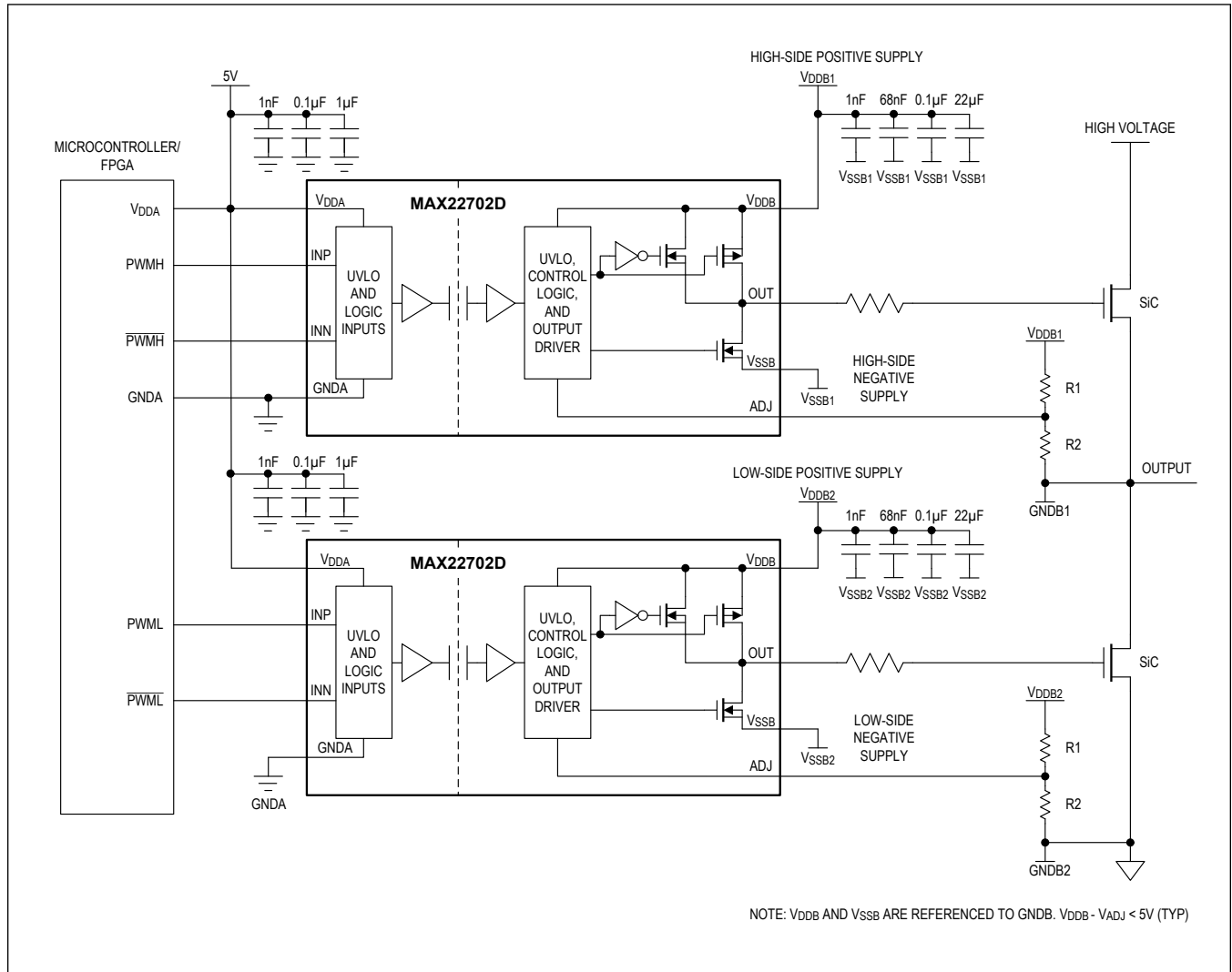
Typical Application Circuits (continued)

MAX22701E



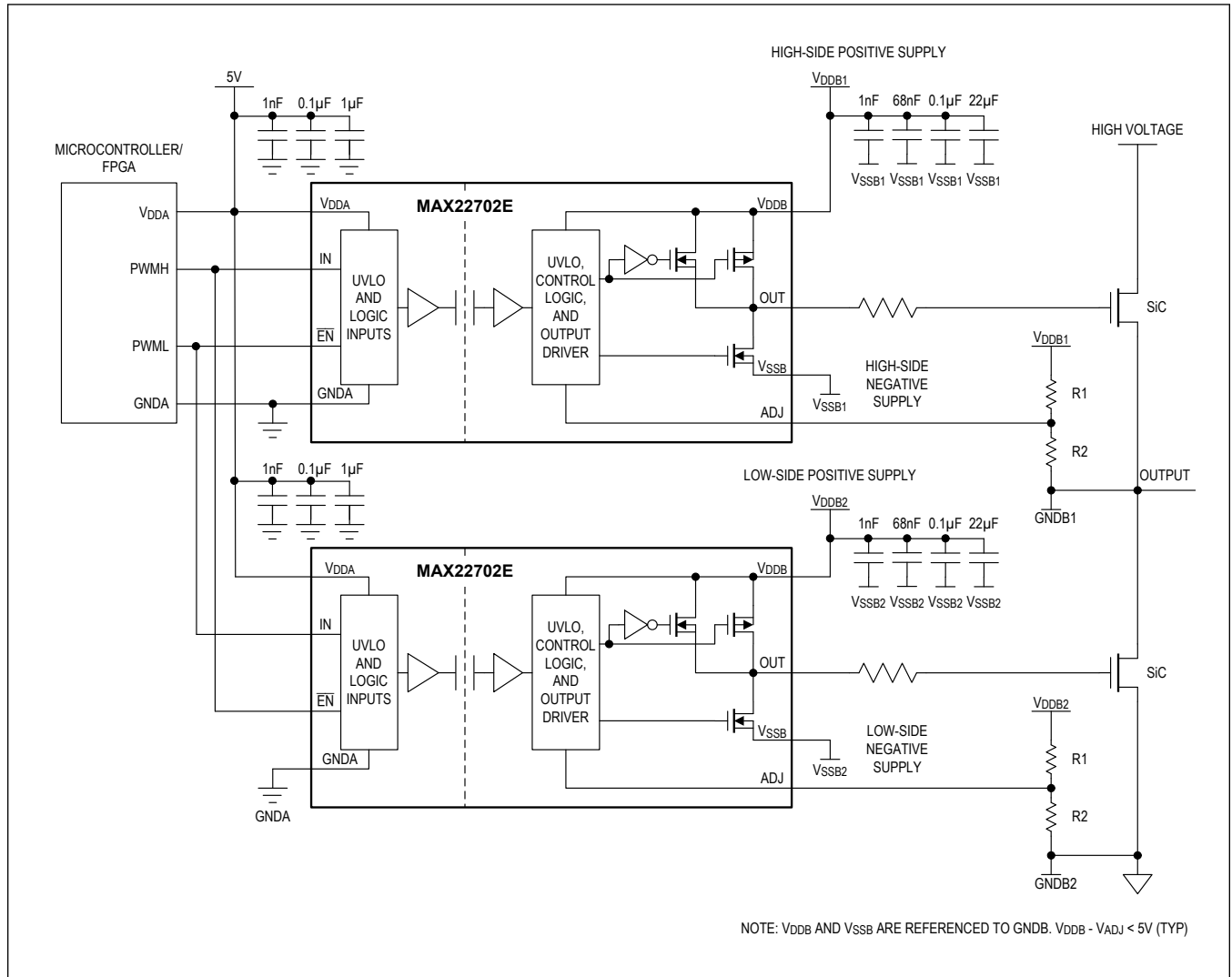
Typical Application Circuits (continued)

MAX22702D



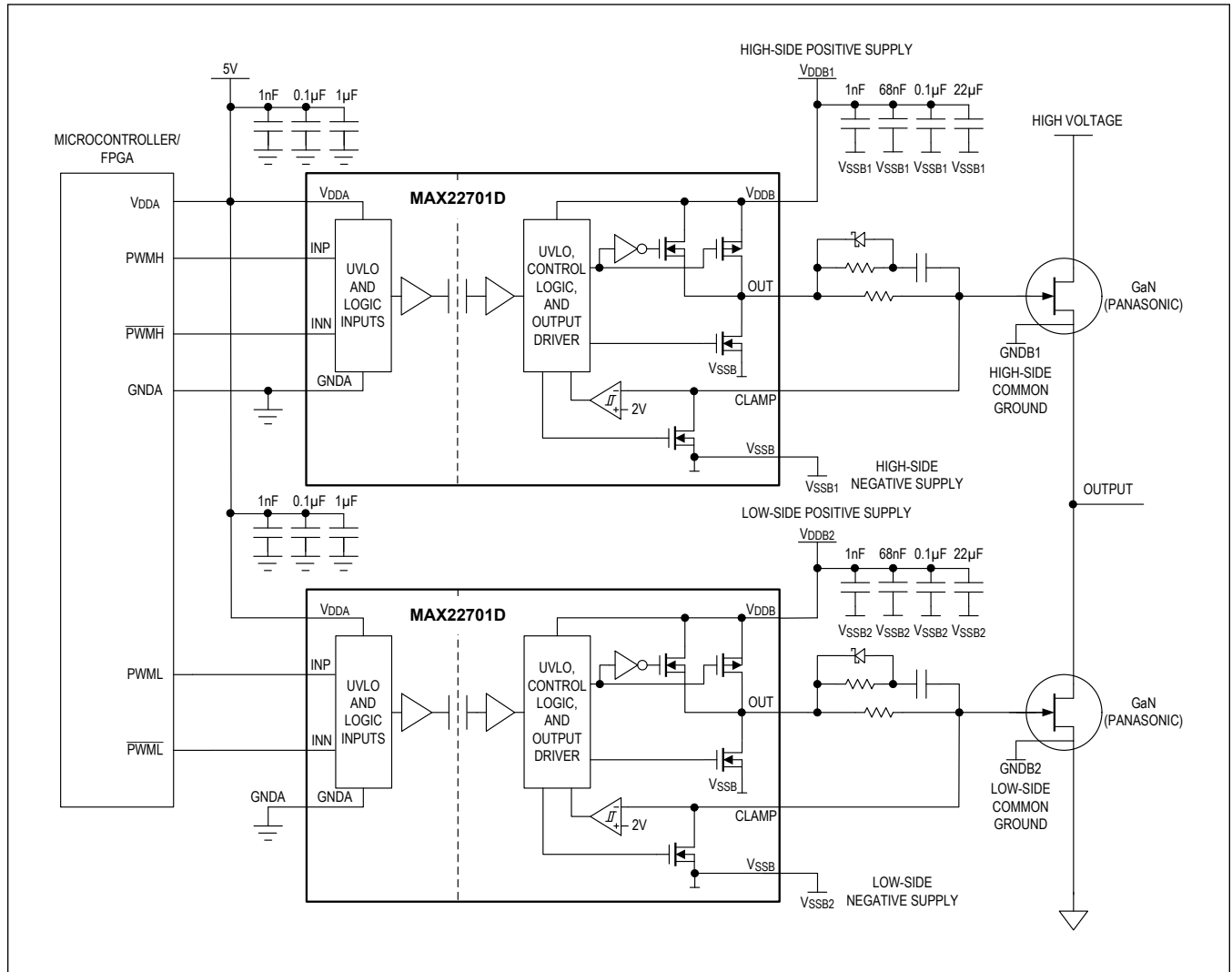
Typical Application Circuits (continued)

MAX22702E



Typical Application Circuits (continued)

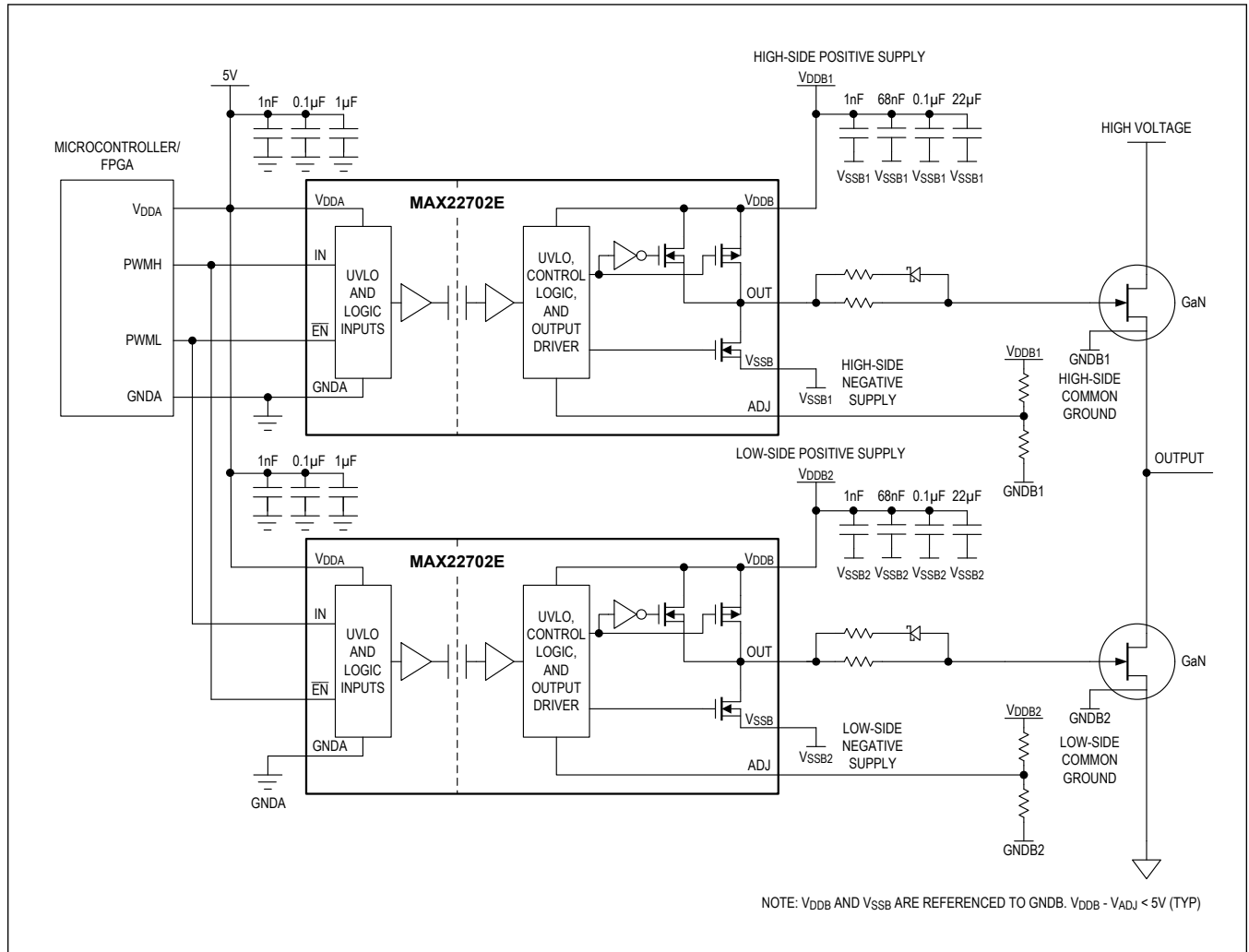
MAX22701D as GaN Gate Driver





Typical Application Circuits (continued)

MAX22702E as GaN Gate Driver



## Ordering Information

PART NUMBER	INPUTS	PIN 7	UVLO	LOW-SIDE R <sub>DS(ON)</sub> (Ω)	ISOLATION VOLTAGE (kV <sub>RMS</sub> )	TEMP RANGE (°C)	PIN-PACKAGE
MAX22700DASA+	Differential, INP and INN	GNDB	13V to GNDB	1.25	3	-40 to +125	8 Narrow SOIC
MAX22700DAWA+*	Differential, INP and INN	GNDB	13V to GNDB	1.25	5	-40 to +125	8 Wide SOIC
MAX22700EASA+	Single-Ended, IN and EN	GNDB	13V to GNDB	1.25	3	-40 to +125	8 Narrow SOIC
MAX22700EAWA+*	Single-Ended, IN and EN	GNDB	13V to GNDB	1.25	5	-40 to +125	8 Wide SOIC
MAX22701DASA+	Differential, INP and INN	CLAMP	13V to V <sub>SSB</sub>	2.5	3	-40 to +125	8 Narrow SOIC
MAX22701DAWA+*	Differential, INP and INN	CLAMP	13V to V <sub>SSB</sub>	2.5	5	-40 to +125	8 Wide SOIC
MAX22701EASA+	Single-Ended, IN and EN	CLAMP	13V to V <sub>SSB</sub>	2.5	3	-40 to +125	8 Narrow SOIC
MAX22701EAWA+	Single-Ended, IN and EN	CLAMP	13V to V <sub>SSB</sub>	2.5	5	-40 to +125	8 Wide SOIC
MAX22702DASA+	Differential, INP and INN	ADJ	Adjustable	1.25	3	-40 to +125	8 Narrow SOIC
MAX22702DAWA+*	Differential, INP and INN	ADJ	Adjustable	1.25	5	-40 to +125	8 Wide SOIC
MAX22702EASA+	Single-Ended, IN and EN	ADJ	Adjustable	1.25	3	-40 to +125	8 Narrow SOIC
MAX22702EAWA+*	Single-Ended, IN and EN	ADJ	Adjustable	1.25	5	-40 to +125	8 Wide SOIC

+Denotes a lead (Pb)-free/RoHS-compliant package.

\*Future product—contact factory for availability.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—
1	8/19	Updated the <i>Absolute Maximum Ratings</i> and <i>Package Information</i> sections, Table 2, and Figure 1	2, 7
2	9/19	Updated the <i>General Description</i> , <i>Benefits and Features</i> , <i>DC Electrical Characteristics</i> , and <i>Dynamic Characteristics</i> sections	1, 4
3	1/20	Removed future product designation from MAX22702EASA+ in the <i>Ordering Information</i> section	29
4	5/20	Removed future product designation from MAX22700DASA+ and MAX22701DASA+ in the <i>Ordering Information</i> section	29
5	7/20	Updated the <i>Benefits and Features</i> and <i>Digital Isolation</i> sections; updated Table 1	1, 6, 15
6	10/20	Removed future product designation from MAX22700EASA+ and MAX22702DASA+ in the <i>Ordering Information</i> section	29
7	10/20	Updated the <i>General Description</i> , <i>Benefit and Features</i> , <i>Safety Regulatory Approvals (Pending)</i> , <i>Absolute Maximum Ratings</i> , <i>Package Information</i> , <i>Electrical Characteristics</i> , <i>Pin Configurations</i> , <i>Pin Description</i> , <i>Detailed Description</i> , <i>Digital Isolation</i> , and <i>Safety Limits</i> sections; added the <i>Insulation Characteristics—8 Wide SOIC</i> table and new Figure 1–2 and renumbered remaining figures; moved the <i>Functional Diagrams</i> to the second page; updated Figures 12–13, Table 1, and Table 4; added MAX22700DAWA+, MAX22700EAWA+, MAX22701DAWA+, MAX22701EAWA+, MAX22702DAWA+, and MAX22702EAWA+ as future products to the <i>Ordering Information</i> table	1–3, 8–9, 13–16, 17–24, 36
8	4/21	Updated the <i>General Description</i> , <i>Safety Regulatory Approvals</i> , <i>Electrical Characteristics</i> , <i>Insulation Characteristics—8 Narrow SOIC</i> , <i>Insulation Characteristics—8 Wide SOIC</i> , <i>Typical Operating Characteristics</i> , <i>Power-Supply Decoupling</i> , <i>Layout Considerations</i> , and <i>Typical Application Circuit</i> sections; updated Table 1, Table 4, Figures 5–6, 8, 11, 16–17, and TOC01–TOC08, TOC15–TOC16, and TOC 18	1, 4, 7–8, 10–12, 17, 19, 21, 24–34
9	6/21	Removed future product designation from MAX22701EAWA+ in the <i>Ordering Information</i> section	34

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