

## MAX25014

# Automotive Low Input Voltage I<sup>2</sup>C 4-Channel 150mA Backlight Driver

### General Description

The MAX25014 is a 4-channel backlight driver IC with boost controller for automotive displays. The integrated current outputs can sink up to 150mA LED current each. The device accepts a wide 2.5V to 36V input voltage range and withstands automotive load-dump events.

The internal current-mode switching DC-DC controller supports boost or SEPIC topologies and operates in the 400kHz to 2.2MHz frequency range. Integrated spread spectrum helps reduce EMI. An adaptive output-voltage-control scheme minimizes power dissipation in the LED current-sink paths.

Control is included for an external nMOSFET series switch to reduce quiescent current when the backlight is off and to disconnect the boost converter in the case of a fault.

The device features I<sup>2</sup>C-controlled pulse-width-modulation (PWM) dimming and hybrid dimming. In either case, the minimum pulse width is 500ns. Phase-shifted dimming of the strings is incorporated for lower EMI.

The MAX25014 is available in a 24-pin TQFN or 24-pin side-wettable TQFN (SWTQFN) package and operates over the -40°C to +125°C temperature range.

### Applications

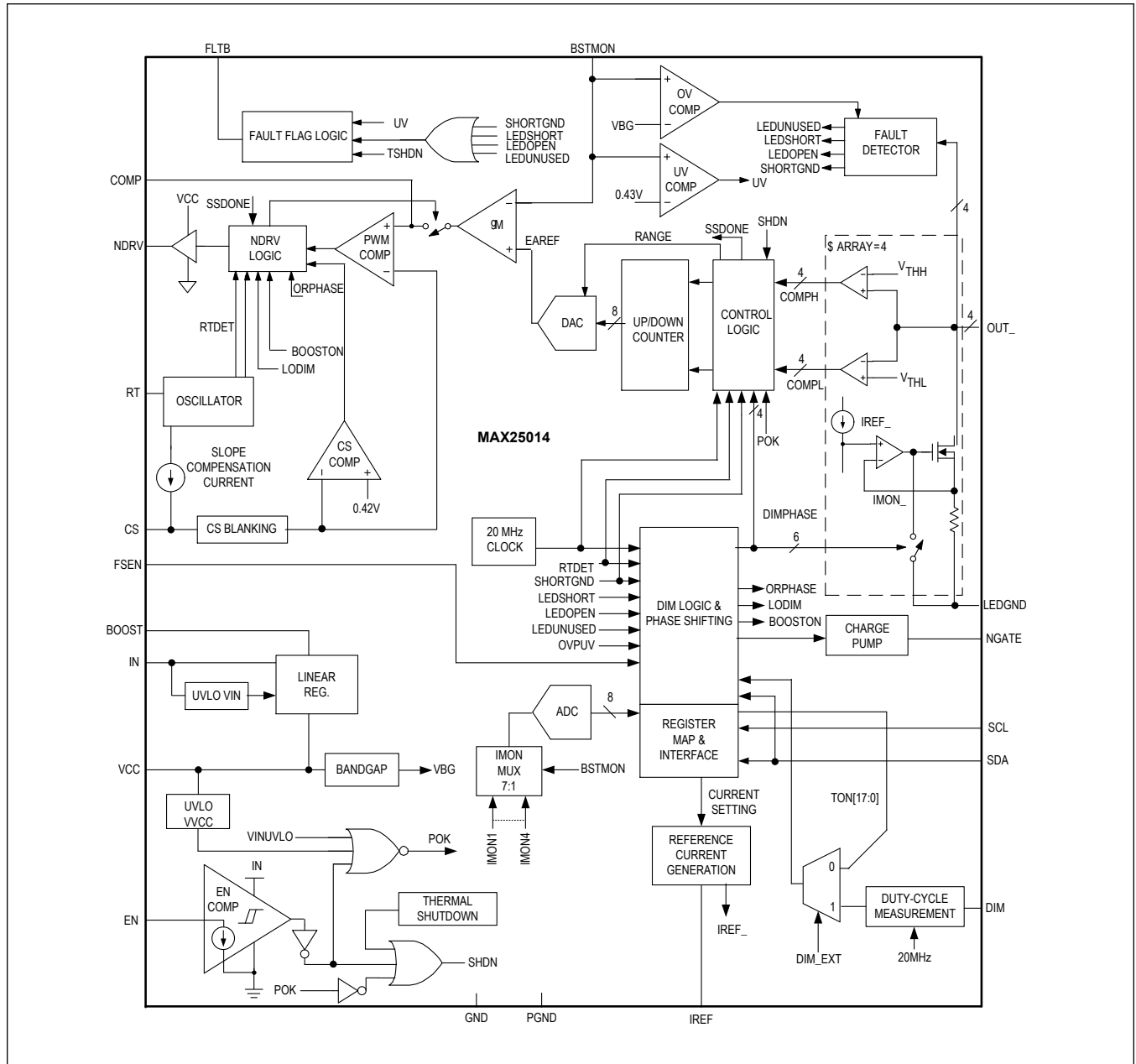
- Instrument Clusters
- Central Information Displays
- Infotainment Displays

### Benefits and Features

- Wide Voltage-Range Operation
  - Operates Down to 2.5V Supply After Startup
  - Survives Load Dumps Up to 40V
- High Integration
  - Complete 4-Channel Solution Including Boost Controller
  - I<sup>2</sup>C Control for Minimum Parts Count
- Robust and Low EMI
  - Spread-Spectrum Oscillator
  - Phase Shifting
  - 400kHz to 2.2MHz Switching-Frequency Range
  - nMOS Input Protection Switch
- Multiple Diagnostic Features
  - LED-Current Measurement
  - Boost Output Voltage Measurement
  - LED Open/Short Detection and Protection
  - Boost Output Undervoltage and Overvoltage
- Versatile Dimming Scheme Allows Hybrid or PWM-Only Dimming Using DIM Input or I<sup>2</sup>C
  - Dimming Ratio > 10,000:1 Using Hybrid Dimming
  - 10,000:1 Dimming Ratio at 200Hz Using PWM Dimming
- Compact (4mm x 4mm) 24-Pin TQFN and SWTQFN Packages

**Ordering Information appears at end of data sheet.**

Simplified Block Diagram



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## Absolute Maximum Ratings

IN, EN to GND .....	-0.3V to +40V	NDRV Continuous Current.....	-100mA to +100mA
OUT_, NGATE, BSTMON, BOOST to GND.....	-0.3V to +52V	OUT_ Continuous Current .....	-150mA to +150mA
PGND, LEDGND to GND .....	-0.3V to +0.3V	Continuous Power Dissipation Multilayer Board (T <sub>A</sub> = +70°C).....	2.857W
V <sub>CC</sub> to GND when EN High.....	-0.3V to +6V	Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ).....	36°C/W
V <sub>CC</sub> to GND when EN Low .....	-0.3V to minimum of +6V and (V <sub>IN</sub> + 0.3)V	Package Thermal Resistance (θ <sub>JC</sub> ).....	3°C/W
FLTB, SCL, SDA, DIM to GND.....	-0.3V to +6V	Operating Temperature.....	-40°C to +125°C
FSEN, CS, RT, COMP, NDRV, IREF to GND .....	-0.3V to V <sub>CC</sub> + 0.3V	Junction Temperature .....	-40°C to +150°C
NDRV Peak Current (< 100ns).....	-5A to +5A	Storage Temperature Range .....	-65°C to +150°C
		Lead Temperature Range.....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### TQFN/SWTQFN

Package Code	T2444+4C
Outline Number	<a href="#">21-0139</a>
Land Pattern Number	<a href="#">90-0022</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	48°C/W
Junction to Case (θ <sub>JC</sub> )	3°C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	36°C/W
Junction to Case (θ <sub>JC</sub> )	3°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

(V<sub>IN</sub> = 12V, R<sub>RT</sub> = 76.8kΩ, C<sub>VCC</sub> = 2.2μF, T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted. ([Note 1](#)))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER INPUT</b>						
Operating Voltage Range, High Setting	V <sub>IN</sub>	Register bit UV_SEL = 0	3.2		36	V
Operating Voltage Range, Low Setting	V <sub>IN</sub>	Register bit UV_SEL = 1	2.5		36	V
Quiescent Supply Current	I <sub>QIN</sub>	V <sub>DIM</sub> = 5V; V <sub>BSTMON</sub> = 1.3V, OUT1–OUT4 are unconnected		9.5	13	mA
Standby Supply Current	ISHDN <sub>IN</sub>	V <sub>IN</sub> = V <sub>BOOST</sub> = 12V, V <sub>EN</sub> = 0V		4	8	μA
IN Undervoltage Lockout, Rising	UVLOR <sub>IN</sub>		3.8	4.15	4.45	V

**Electrical Characteristics (continued)**

( $V_{IN} = 12V$ ,  $R_{RT} = 76.8k\Omega$ ,  $C_{VCC} = 2.2\mu F$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Undervoltage Lockout, Falling	$UVLOF_{IN}$		3.2	3.75	4	V
IN Undervoltage Lockout Falling, High Setting	$UVLOF_{INCC}$	After completed boost soft-start. Register bit $UV\_SEL = 0$	2.65	2.9	3.15	V
IN Undervoltage Lockout Falling, Low Setting	$UVLOF_{INCC}$	After completed boost soft-start. Register bit $UV\_SEL = 1$	2.15	2.3	2.45	V
Startup Delay	$t_{STARTUP}$	From EN high to I <sup>2</sup> C ready			2	ms
IN to BOOST Switchover Voltage	$V_{SO}$	IN falling, if $V_{BOOST} > V_{IN} + 300mV$ (typ)	5.6	5.8	6.1	V
IN to BOOST Switchover Voltage Hysteresis	$V_{SO\_HYS}$			150		mV
BOOST Shutdown Input Current	$ISHDN_{BOOST}$	$V_{EN} = 0V$ , $V_{BOOST} = 12V$		0.1	1	$\mu A$
BOOST Input Current	$I_{BOOST}$	$V_{EN} = 5V$ , Register bit $ENA = 0$ , $V_{BOOST} = 24V$		3.5	7	$\mu A$
		$V_{EN} = 5V$ , Register bit $ENA = 1$ , $V_{BOOST} = 24V$		30	45	
<b>V<sub>CC</sub> REGULATOR</b>						
V <sub>CC</sub> Output Voltage	$V_{CC}$	$6V < V_{IN}$ , $V_{BOOST} < 36V$ , $I_{VCC} = 1mA$ to $10mA$	4.75	5	5.25	V
Dropout Voltage	$V_{CCDROP}$	$V_{IN} = 4.5V$ , $I_{VCC} = 5mA$			0.2	V
Short-Circuit Current Limit	$I_{VCC\_SC}$	$V_{CC}$ shorted to GND		60		mA
V <sub>CC</sub> Undervoltage-Lockout Threshold, Rising	$UVLOR_{VCC}$		4.05	4.2	4.35	V
V <sub>CC</sub> Undervoltage-Lockout Threshold, Falling	$UVLOF_{VCC}$		3.75	3.9	4.04	V
<b>RT OSCILLATOR</b>						
Switching-Frequency Range	$f_{SW}$	Frequency dithering disabled	400		2200	kHz
Maximum Duty Cycle	$D_{MAX}$	$f_{SW} = 400kHz$	90	94.5	98.5	%
		$f_{SW} = 2200kHz$	86	90.5	95	
Oscillator-Frequency Accuracy	$f_{SW1}$	$R_{RT} = 76.8k\Omega$ , dither disabled	348	400	444	kHz
	$f_{SW2}$	$R_{RT} = 13.3k\Omega$ , dither disabled	2013	2200	2387	
Frequency Dither	SS	Register bit $SSL = 1$		$\pm 3$		%
RT Output Voltage	$V_{RT}$	$R_{RT} = 76.8k\Omega$ or $R_{RT} = 13.3k\Omega$	1.22	1.25	1.28	V
Sync Rising Threshold	$V_{SYNCTH}$		2.1			V



**Electrical Characteristics (continued)**

( $V_{IN} = 12V$ ,  $R_{RT} = 76.8k\Omega$ ,  $C_{VCC} = 2.2\mu F$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Sync-Frequency Duty-Cycle Range	$D_{SYNC}$			50		%	
Sync-Frequency Range	$f_{SYNC}$		1.2 x $f_{SW}$		1.5 x $f_{SW}$	kHz	
<b>MOSFET DRIVER</b>							
NDRV On-Resistance, High Side	$R_{NDRV\_H}$	$I_{SINK} = 30mA$		1.5	3	$\Omega$	
NDRV On-Resistance, Low Side	$R_{NDRV\_L}$	$I_{SOURCE} = 30mA$		0.8	1.6	$\Omega$	
NDRV Rise Time	$t_{NDRV\_R}$	$C_{LOAD} = 1nF$ , ( <i>Note 2</i> )		8		ns	
NDRV Fall Time	$t_{NDRV\_F}$	$C_{LOAD} = 1nF$ , ( <i>Note 2</i> )		8		ns	
<b>SLOPE COMPENSATION</b>							
Peak Slope-Compensation Current-Ramp Magnitude	$I_{SLOPE}$	Current ramp added to CS	42	50	58	$\mu A$	
<b>CURRENT-SENSE COMPARATOR</b>							
Current-Limit Threshold	$V_{CL\_MAX}$	$V_{CL} = V_{CS} + \text{slope-compensation voltage}$	385	420	455	mV	
Current-Limit Threshold During Low-Voltage Operation, Low Setting	$V_{CLCC\_MAX}$	Register bit ILIM = 0, $V_{CC}$ regulator input switched to BOOST	565	600	635	mV	
Current-Limit Threshold During Low-Voltage Operation, High Setting	$V_{CLCC\_MAX}$	Register bit ILIM bit = 1, $V_{CC}$ regulator input switched to BOOST	785	825	856	mV	
<b>ERROR AMPLIFIER</b>							
OUT_ Regulation, High Threshold	$V_{OUT\_H}$	$V_{OUT\_falling}$	0.95	1.03	1.1	V	
OUT_ Regulation, Low Threshold	$V_{OUT\_L}$	$V_{OUT\_rising}$	0.7	0.78	0.85	V	
Transconductance	GM		420	600	840	$\mu S$	
COMP Sink Current	$I_{COMP\_SINK}$	$V_{COMP} = 2V$	200	480	800	$\mu A$	
COMP Source Current	$I_{COMP\_SRC}$	$V_{COMP} = 1V$	200	480	800	$\mu A$	
<b>LED CURRENT SINKS</b>							
IREF Voltage	$V_{IREF}$	$R_{IREF} = 49.9k\Omega$	1.22	1.25	1.28	V	
IREF Resistor IREFOOR Fault Detection Range	$R_{IREFOOR}$	Outside this range a fault will be detected	27.5		83.5	k $\Omega$	
OUT_ Output Current	$I_{OUT\_}$	$R_{IREF} = 49.9k\Omega$	120mA setting	115	120	125	mA
		$R_{IREF} = 49.9k\Omega$	100mA setting	96	100	104	
			50mA setting	48	50	52	
		$R_{IREF} = 40.2k\Omega$	150mA setting	143	149	155	

**Electrical Characteristics (continued)**

( $V_{IN} = 12V$ ,  $R_{RT} = 76.8k\Omega$ ,  $C_{VCC} = 2.2\mu F$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Channel-to-Channel Matching	$I_{OUT\_M}$	$I_{OUT\_} = 120mA$	-2		+2	%
		$I_{OUT\_} = 50mA$	-2.5		+2.5	
Total OUT_ Leakage Current to IN	$I_{OUTLEAK}$	$V_{OUT\_} = 48V$ , $V_{DIM} = 0V$ , all OUT_ are shorted together		8	15	$\mu A$
OUT_ Current, Rise Time	$t_{IOUT\_R}$	10% to 90% $I_{OUT\_}$ , ( <i>Note 2</i> )		150		ns
OUT_ Current, Fall Time	$t_{IOUT\_F}$	90% to 10% $I_{OUT\_}$ , ( <i>Note 2</i> )		50		ns
DIM Sampling Frequency	$f_{DIM}$			20		MHz
<b>OVERVOLTAGE AND UNDERVOLTAGE PROTECTION</b>						
BSTMON Overvoltage-Trip Threshold	$V_{BSTMONTH}$	$V_{BSTMON}$ rising	1.18	1.23	1.28	V
BSTMON Hysteresis	$V_{BSTMONHY}$			70		mV
BSTMON Input Bias Current	$I_{BSTMON}$	$0V < V_{BSTMON} < 1.3V$	-500		+500	nA
BSTMON Undervoltage-Detection Threshold, Rising	$V_{BSTMONUVR}$		0.47	0.5	0.53	V
BSTMON Undervoltage-Detection Threshold, Falling	$V_{BSTMONUVF}$	NGATE latched off	0.4	0.43	0.46	V
BSTMON Undervoltage-Blanking Time	$t_{BSTMON\_BL}$	After ENA is written to '1', Register bit FAST_SS = 0	47.8	52	56.2	ms
BSTMON Undervoltage-Detection Delay	$t_{BSTMON\_UV}$	BSTMON falling	4	10	18	$\mu s$
<b>LOGIC INPUT AND OUTPUTS</b>						
EN, SDA, SCL, DIM Input, Logic-High	$V_{IH}$		2.1			V
EN, SDA, SCL, DIM Input, Logic-Low	$V_{IL}$				0.8	V
EN Input Current	$I_{EN}$	$V_{EN} = 12V$		7.25	12	$\mu A$
SDA, SCL Input Current	$I_{SDA}$ , $I_{SCL}$	$V_{SDA} = V_{SCL} = 5V$	-1		+1	$\mu A$
DIM Input Frequency	$f_{DIM\_IN}$		90			Hz
DIM Input Pullup Current	$I_{DIM}$			5		$\mu A$
FSEN Input, Logic High	$V_{FSEN\_TH}$	FSEN Rising	2.2			V
FSEN Input Current	$I_{FSEN}$	$V_{FSEN} = 1V$	14.2	15	15.8	$\mu A$
SDA, FLTB Output Low Voltage	$V_{OL}$	Sinking 3mA			0.4	V
FLTB Output-Leakage Current	$I_{FLTB\_LKG}$	$V_{FLTB} = 5.5V$	-1		+1	$\mu A$

**Electrical Characteristics (continued)**

( $V_{IN} = 12V$ ,  $R_{RT} = 76.8k\Omega$ ,  $C_{VCC} = 2.2\mu F$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>NGATE OUTPUT</b>						
NGATE Source Current	$I_{NGATE\_SRC}$	$V_{IN} = 12V$ , $V_{NGATE} = V_{IN} - 7V$	37.5	50	62.5	$\mu A$
NGATE Sink Current	$I_{NGATE\_SINK}$	$V_{IN} = 12V$ , $V_{NGATE} = V_{IN} + 7V$	4.5	9		mA
NGATE Output Voltage	$V_{NGATE}$	Above $V_{IN}$ , $4.5V < V_{IN} < 36V$	4.5	7.5	11	V
NGATE Start Delay	$t_{NGATE}$	Delay between NGATE charge-pump turning on and the boost converter starting		2	2.2	ms
<b>LED FAULT DETECTION</b>						
LED Short-Detection Threshold	$V_{LED\_THR}$	Register bits SLDET[1:0] = 11, Rising	7.5	8	8.5	V
		Register bits SLDET[1:0] = 10, Rising	5.6	6	6.4	
		Register bits SLDET[1:0] = 01, Rising	2.8	3	3.25	
Short-Detection Comparator Delay	$t_{LEDS}$			6.5		$\mu s$
OUT_ Check LED Source Current	$I_{OUT\_CKLED}$		50	60	70	$\mu A$
OUT_ Short to GND Detection Threshold	$V_{OUT\_GND}$	Before boost converter startup	250	300	365	mV
OUT_ Unused-Detection Threshold	$V_{OUT\_UN}$		1.15	1.25	1.35	V
OUT_ Open-LED Detection Threshold	$V_{OUT\_OPEN}$	During operation	250	300	365	mV
<b>ANALOG-TO-DIGITAL CONVERTER</b>						
ADC Measurement Resolution	ADCBIT	( <i>Note 2</i> )		8		Bits
Total Measurement Error, Current	$E_{ADCOUT}$	150mA setting	-8		+8	mA
Total Measurement Error, BSTMON	$E_{ADCBSTMON}$	$V_{BSTMON} = 1V$	-70		70	mV
ADC Gain Error	ADCGAIN	150mA setting	-4		+6	%
ADC Offset Error	ADCOFF	150mA setting	-4		+4	LSB
Measurement Resolution, Current	LSBOUT	$R_{IREF} = 49.9k\Omega$		0.505		mA
		$R_{IREF} = 40.2k\Omega$		0.625		
Measurement Resolution, BSTMON	LSBBSTMON			5.1		mV
<b>THERMAL SHUTDOWN</b>						
Thermal Warning	$T_{WARN}$			125		$^\circ C$
Thermal-Shutdown Threshold	$T_{SHDN}$			165		$^\circ C$
Thermal-Shutdown Hysteresis	$T_{SHDN\_HY}$			15		$^\circ C$

**Electrical Characteristics (continued)**

( $V_{IN} = 12V$ ,  $R_{RT} = 76.8k\Omega$ ,  $C_{VCC} = 2.2\mu F$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted. (*Note 1*))

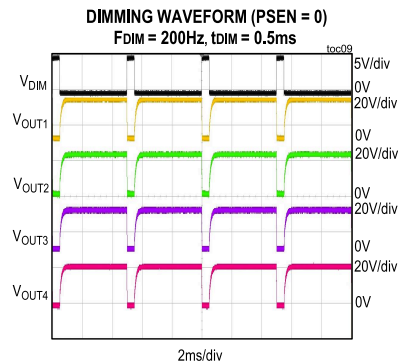
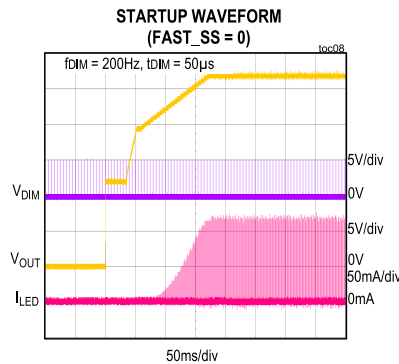
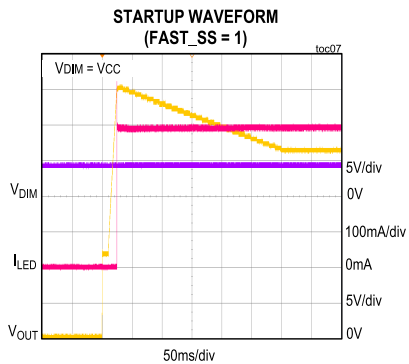
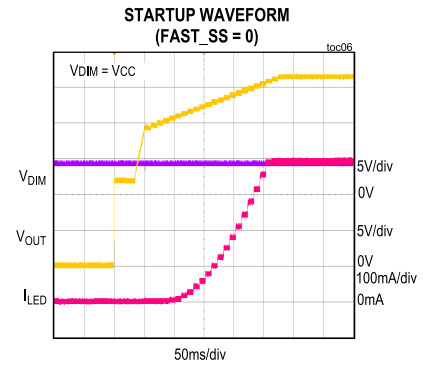
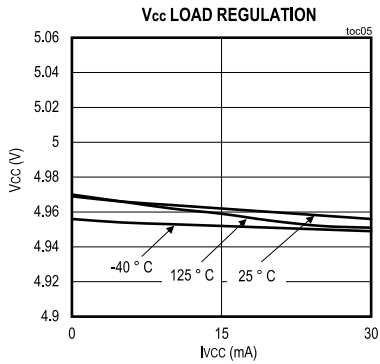
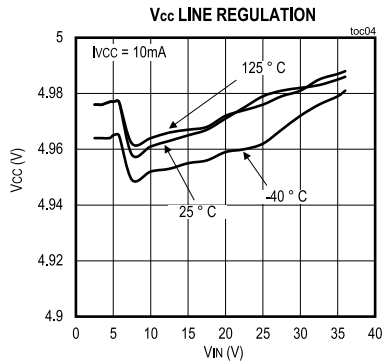
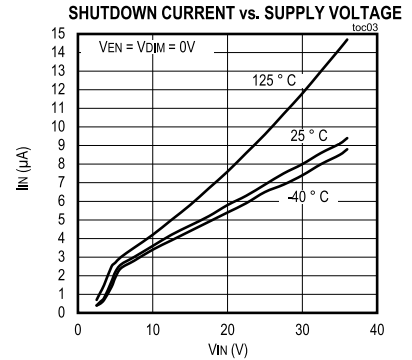
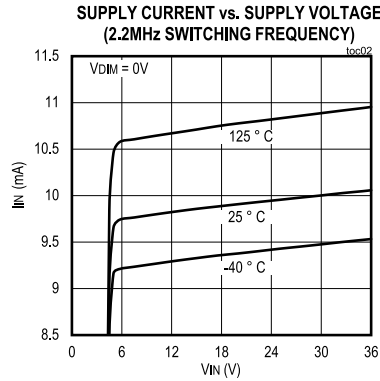
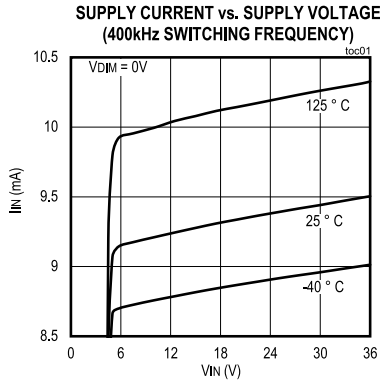
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>I<sup>2</sup>C INTERFACE</b>						
Serial-Clock Frequency	$f_{SCL}$				400	kHz
Bus-Free Time Between STOP and START Condition	$t_{BUF}$		1.3			$\mu s$
START Condition Setup Time	$t_{SU:STA}$		0.6			$\mu s$
START Condition Hold Time	$t_{HD:STA}$		0.6			$\mu s$
STOP Condition Setup Time	$t_{SU:STO}$		0.6			$\mu s$
Clock Low Period	$t_{LOW}$		1.3			$\mu s$
Clock High Period	$t_{HIGH}$		0.6			$\mu s$
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	Measured from 50% point on SCL falling edge to SDA edge	0			$\mu s$
Pulse Width of Spike Suppressed	$t_{SP}$			50		ns

**Note 1:** Limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

**Note 2:** Guaranteed by design.

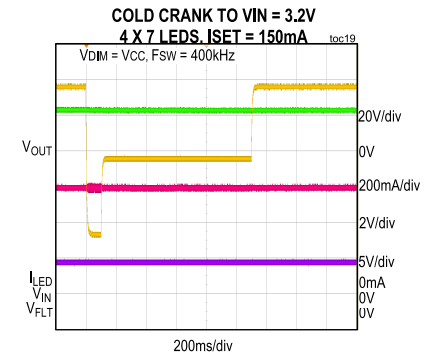
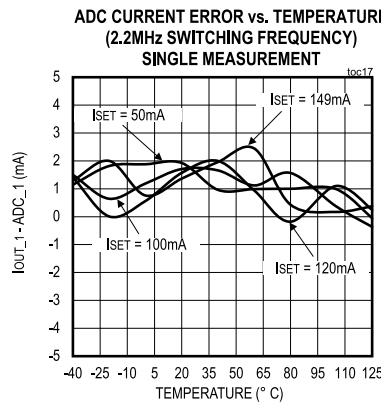
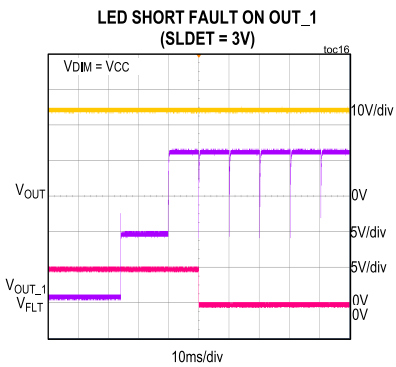
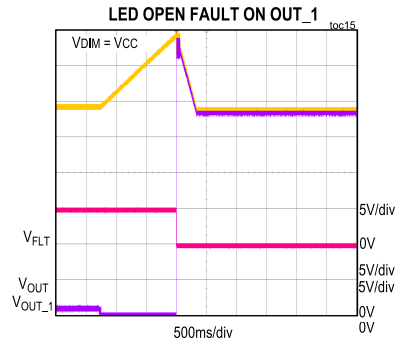
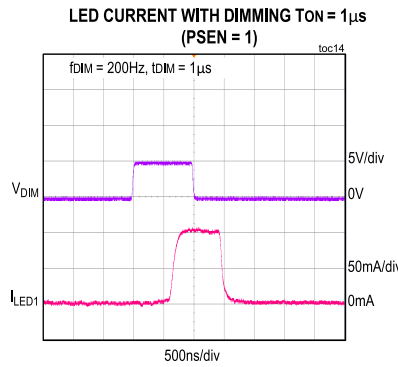
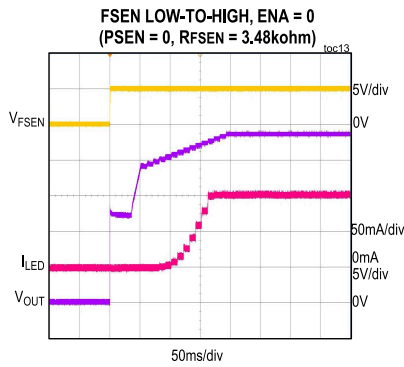
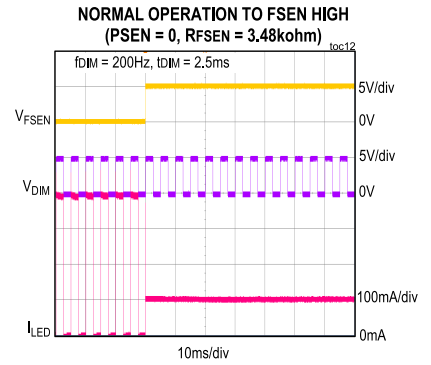
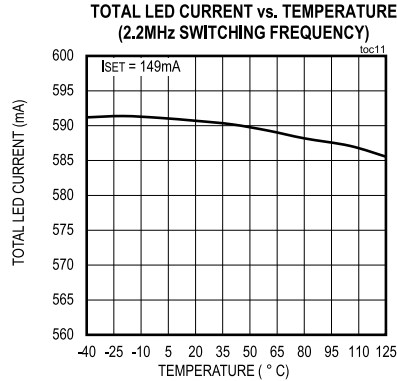
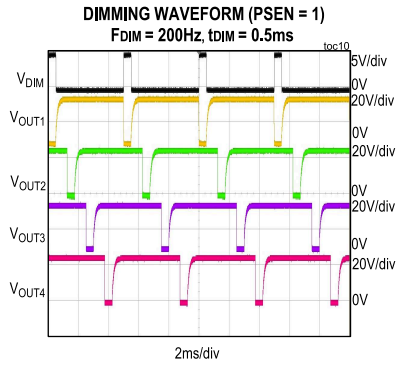
Typical Operating Characteristics

(V<sub>IN</sub> = 12V, T<sub>A</sub> = 25°C unless otherwise noted.)



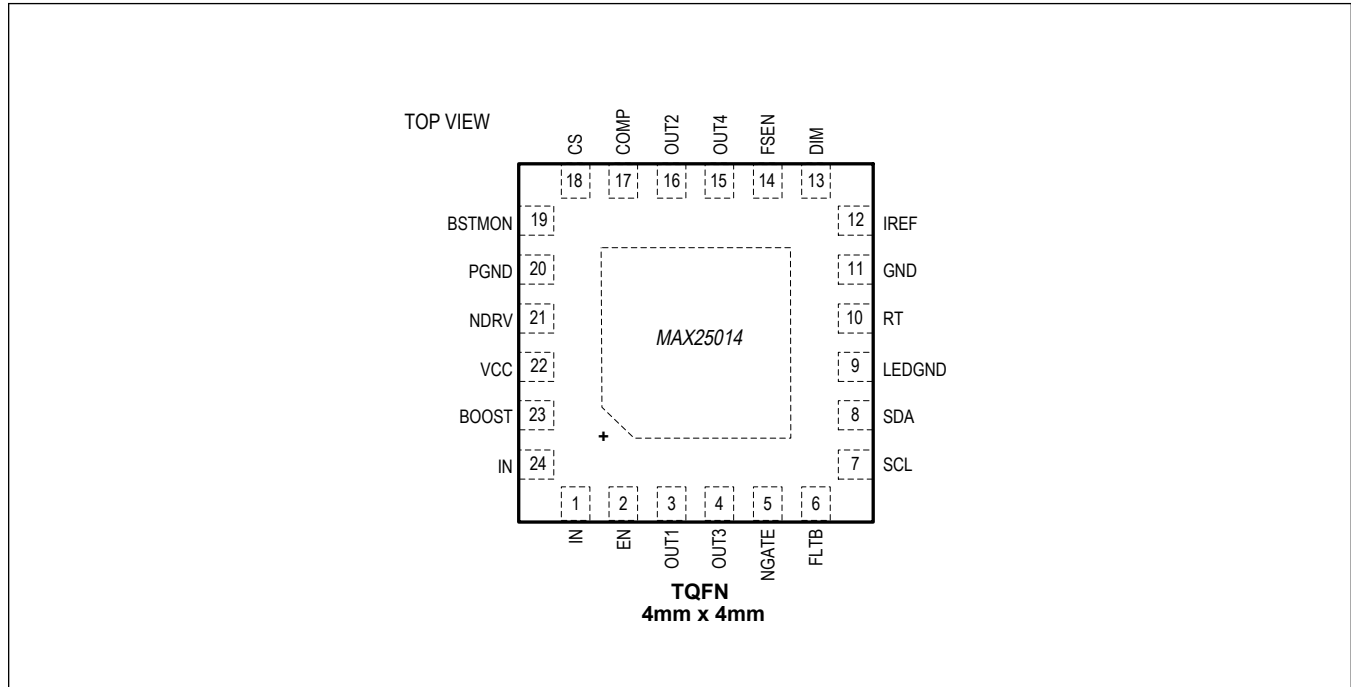
Typical Operating Characteristics (continued)

(V<sub>IN</sub> = 12V, T<sub>A</sub> = 25°C unless otherwise noted.)



Pin Configuration

MAX25014



Pin Description

PIN	NAME	FUNCTION
1	IN	Bias Supply Input. Connect a 2.5V to 36V supply to IN. Bypass IN to GND with a 2.2µF ceramic capacitor.
2	EN	Enable Input. Connect EN to ground to shut down the device. Connect EN to logic-high or IN for normal operation. EN has an internal clamp at 3V; when EN is above this voltage, an input current of $(V_{EN} - 3V)/1.2M\Omega$ will flow.
3	OUT1	LED String Cathode Connection 1. OUT1 is the open-drain output of the linear current sink, which controls the current through the LED string connected to OUT1. OUT1 sinks up to 150mA.
4	OUT3	LED String Cathode Connection 3. OUT3 is the open-drain output of the linear current sink, which controls the current through the LED string connected to OUT3. OUT3 sinks up to 150mA.
5	NGATE	Gate Connection for External Series nMOSFET driven by the internal charge pump.
6	FLT B	Open-Drain Fault Output. FLT B asserts low when any diagnostic bit that is not masked is asserted. See the <a href="#">Fault Protection</a> section for more details. Connect a pullup resistor from FLT B to V <sub>CC</sub> or to a logic supply of maximum 5V.
7	SCL	I <sup>2</sup> C Clock Input. Connect a pullup resistor from SCL to the logic supply.
8	SDA	I <sup>2</sup> C Data I/O Pin. Connect a pullup resistor from SDA to the logic supply.
9	LEDGND	LED Ground. LEDGND is the return-path connection for the linear current sinks. Connect GND, LEDGND, and PGND at a single point.
10	RT	Oscillator-Timing Resistor Connection. Connect a timing resistor (R <sub>RT</sub> ) from RT to GND to program the switching frequency. Also connect a 100pF capacitor from RT to GND. To synchronize the switching frequency with an external clock, apply an AC-coupled external clock at RT. When the oscillator is synchronized with the external clock, spread spectrum is disabled.

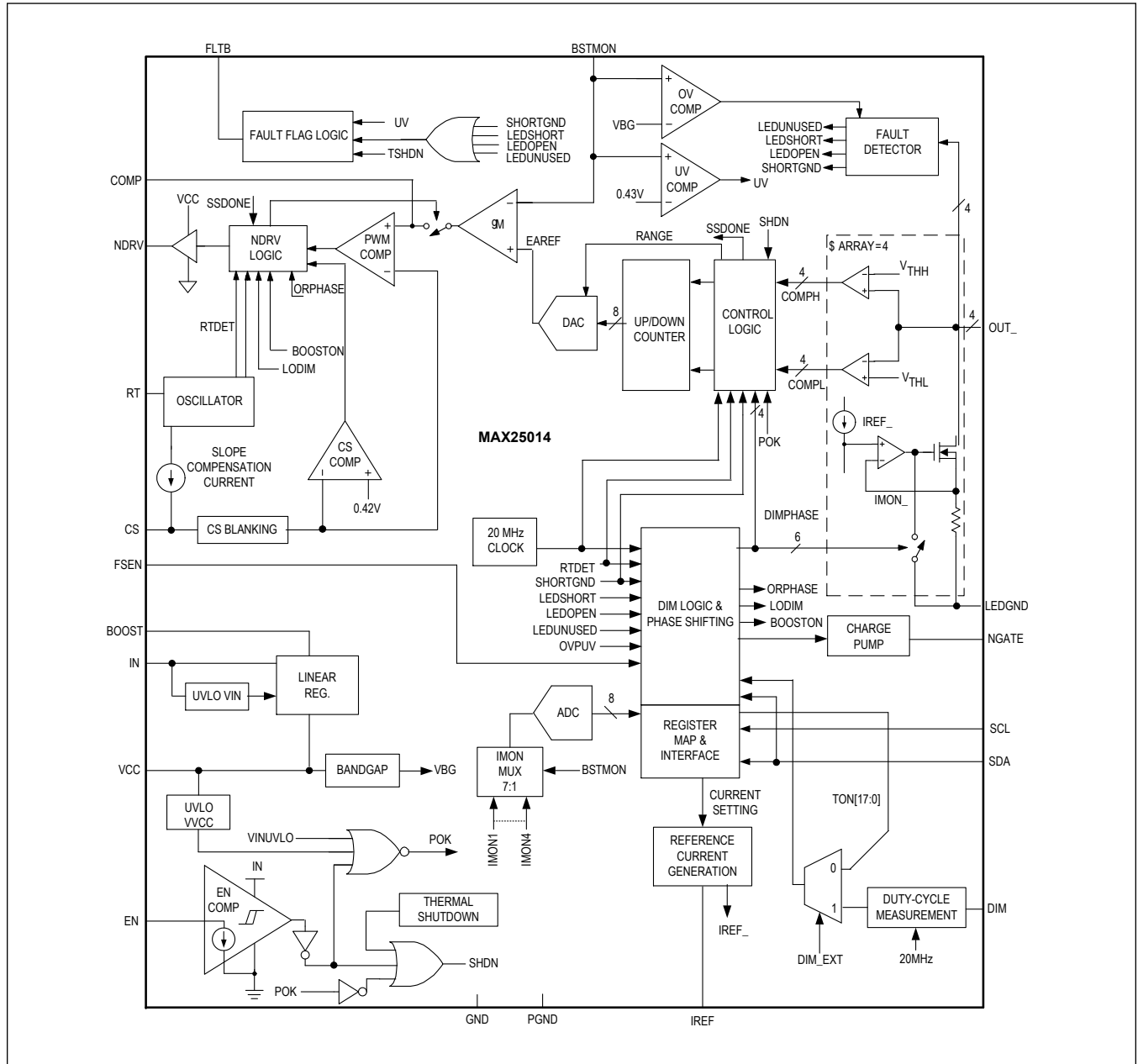
## Pin Description (continued)

PIN	NAME	FUNCTION
11	GND	Signal Ground. GND is the current return-path connection for the low-noise analog signals. Connect GND, LEDGND, and PGND at a single point.
12	IREF	LED Current-Reference Input. Connect a resistor ( $R_{IREF} = 40.2k\Omega$ ) from IREF to GND to set the reference current. Place the resistor as close as possible to the pin using the shortest possible trace.
13	DIM	PWM Dimming Input. Apply a PWM signal to DIM for LED dimming control unless I <sup>2</sup> C dimming is used. Connect DIM to V <sub>CC</sub> if dimming control is not used (100% brightness). Connect DIM to GND if dimming will be controlled through I <sup>2</sup> C.
14	FSEN	Fail-Safe Enable Pin. When FSEN is taken high the boost converter is enabled and the outputs OUT1–OUT4 are enabled at 100% duty cycle, independently of all register settings. Connect a resistor from FSEN to GND to set the LED current when FSEN is active and the device I <sup>2</sup> C address (see <a href="#">FSEN Pin Function</a> ). If the FSEN function is not needed connect the pin directly to GND.
15	OUT4	LED String Cathode Connection 4. OUT4 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT4. OUT4 sinks up to 150mA.
16	OUT2	LED String Cathode Connection 2. OUT2 is the open-drain output of the linear current sink that controls the current through the LED string connected to OUT2. OUT2 sinks up to 150mA.
17	COMP	Switching-Converter Compensation Input. Connect the compensation network from COMP to GND for current-mode control (see the <a href="#">Feedback Compensation</a> section).
18	CS	Current-Sense Input for the Switching Regulator. A sense resistor connected from the source of the external power MOSFET to PGND sets the switching current limit. A resistor connected between the source of the power MOSFET and CS sets the slope-compensation ramp rate (see the <a href="#">Slope Compensation and Current-Sense Resistor</a> section).
19	BSTMON	Overvoltage Threshold-Adjust Input. Connect a resistor-divider from the switching converter output to BSTMON and GND. The OVP comparator reference is internally set to 1.23V.
20	PGND	Power Ground. PGND is the switching current-return-path connection. Connect GND, LEDGND, and PGND at a single point.
21	NDRV	Switching nMOSFET Gate-Driver Output. Connect NDRV to the gate of the external switching-power nMOSFET using a 10 $\Omega$ to 22 $\Omega$ resistor. This decreases the slew rate of the gate driver and reduces switching noise.
22	V <sub>CC</sub>	5V Regulator Output. Bypass V <sub>CC</sub> to GND with a 1 $\mu$ F (min) ceramic capacitor as close as possible to the device.
23	BOOST	Connect to the Output of the Boost Converter. This pin serves as the input to the V <sub>CC</sub> regulator when IN drops below 5.8V.
24	IN	Bias Supply Input. Connect a 2.5V to 36V supply to IN. Bypass IN to GND with a 2.2 $\mu$ F ceramic capacitor.
—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP must be connected to GND.



Functional Diagrams

MAX25014 Block Diagram



## Detailed Description

The MAX25014 is a 4-channel backlight driver IC with boost controller for automotive displays. The integrated current outputs can sink up to 150mA LED current each. The device accepts a wide 2.5V to 36V input voltage range. The IC provides load-dump voltage protection up to 40V in automotive applications and incorporates three major blocks: a DC-DC controller with peak current-mode control to implement a boost or SEPIC-type switched-mode power supply, a 4-channel LED driver with 45mA to 150mA constant-current sink capability per channel, and a control block with I<sup>2</sup>C interface.

The internal current-mode switching DC-DC controller supports boost or SEPIC topologies and operates in the 400kHz to 2.2MHz frequency range. Integrated spread spectrum helps reduce EMI. An adaptive output-voltage-control scheme minimizes power dissipation in the LED current-sink paths.

The device features I<sup>2</sup>C-controlled pulse-width-modulation (PWM) dimming and hybrid dimming. In either case, the minimum pulse width is 500ns. Phase-shifted dimming of the strings is incorporated for lower EMI.

### Enable

The internal regulator is enabled when the EN pin is high. To shut down the device drive EN low, and the current consumption is reduced to 8 $\mu$ A (max).

### Low-Voltage Operation

After the boost soft-start is completed the MAX25014 continues to operate with IN voltages lower than 5V while maintaining 5V drive for the external MOSFET at NDRV. When the IN voltage drops to  $V_{\text{SWITCHOVER}}$  the  $V_{\text{CC}}$  regulator switches its input from IN to BOOST, the output of the boost converter. Switchover occurs as long as the voltage on BSTMON is above the undervoltage lockout level of 430mV and BOOST is greater than IN. When IN returns to a voltage above 5.95V the  $V_{\text{CC}}$  regulator resumes operation from IN. Bypass IN and BOOST with ceramic capacitors of value 2.2 $\mu$ F placed close to the respective pins.

At very low input voltages the efficiency of the boost converter reduces and the input current can reach very high levels as a consequence. When the input voltage falls below  $V_{\text{SWITCHOVER}}$  the boost converter current limit is automatically increased to 600mV or 825mV (typ), the value is set using the ILIM bit in the SETTING register. The external boost converter components must be selected for worst-case operation. Alternatively, it may be necessary to reduce the output power at low input voltages. If the voltage at IN drops below the level programmed by the UV\_SEL bit in register DISABLE the boost converter is disabled.

### Undervoltage Lockout

The IC features three undervoltage lockouts (UVLOs) that monitor the input voltage at IN and the output of the internal LDO regulator at  $V_{\text{CC}}$ . The device turns on when EN is taken high if both IN and  $V_{\text{CC}}$  are higher than their respective UVLO thresholds.

### Current-Mode DC-DC Controller

The IC has a constant-frequency, current-mode controller designed to drive the LEDs in a boost, SEPIC, or coupled-inductor buck-boost configuration. The IC features multi-loop control to regulate the peak current in the inductor, as well as the voltage across the LED current sinks, to minimize power dissipation.

The switching frequency can be programmed over the 400kHz to 2.2MHz range using a resistor connected from RT to GND.

Adjustable slope compensation is provided to compensate for subharmonic oscillations that occur at above 50% duty cycles in continuous-conduction mode.

The external MOSFET is turned on at the beginning of every switching cycle. The inductor current ramps up linearly until it is turned off at the peak current level set by the feedback loop. The peak inductor current is sensed from the voltage across the current-sense resistor ( $R_{\text{CS}}$ ) connected from the source of the external MOSFET to ground with the addition of the slope-compensation voltage due to  $R_{\text{SC}}$ .

The IC features leading-edge blanking to suppress the MOSFET switching noise. A PWM comparator compares the current-sense voltage plus the slope-compensation signal with the output of the transconductance error amplifier. The controller turns off the MOSFET when the voltage at CS exceeds the error amplifier's output voltage, which is also the voltage on the COMP pin. This process repeats every switching cycle to achieve peak current-mode control.

In addition to the peak current-mode-control loop, the IC has two other feedback loops for control. The converter output voltage is sensed through the BSTMON input, which goes to the inverting input of the error amplifier. The other feedback comes from the OUT\_ current sinks. This loop controls the headroom of the current sinks to minimize total power dissipation while still ensuring accurate LED current matching. Each current sink has a window comparator with a low threshold of 0.78V and a high threshold of 1.03V. The outputs of these comparators control an up/down counter. The up/down counter is updated on every falling edge of the DIM input and drives an 8-bit DAC that sets the reference to the error amplifier. When dimming is set to 100%, the counter is updated at intervals of 10ms.

### Output Undervoltage Protection

At the end of the boost converter soft-start, an undervoltage threshold is activated on the output of the DC-DC converter, which is set at 430mV. If the BSTMON pin is below 430mV after the soft-start period of the DC-DC converter, the converter is turned off and the NGATE output discharges the gate of the external nMOSFET. The FLTB pin is asserted low whenever undervoltage protection is activated. The ENA bit in the ISET (0x02) register must be toggled to start up again once the fault condition has been removed. Alternatively, the EN pin or power supply can be toggled.

### 8-Bit Digital-to-Analog Converter

The error amplifier's reference input is controlled with an 8-bit digital-to-analog converter (DAC). The DAC output is ramped up slowly during startup to implement a soft-start function (see the [Startup Sequence](#) section). During normal operation, the DAC output range is limited to 0.6V to 1.25V. Because the DAC output is limited to no less than 0.6V during normal operation, the overvoltage threshold for the output should be set to a value less than twice the minimum LED forward voltage. The DAC LSB determines the minimum step-in output voltage according to the equation below.

#### Equation 1:

$$V_{STEP\_MIN} = V_{DAC\_LSB} \times A_{OVP}$$

where:

$V_{STEP\_MIN}$  = Minimum output-voltage step

$V_{DAC\_LSB}$  = DAC least significant bit size (2.5mV)

$A_{OVP}$  = BSTMON resistor-divider gain (1 + R6/R7)

### FSEN Pin Function

The FSEN pin can be used to enable the device in situations where I<sup>2</sup>C control is temporarily impossible or the interface has stopped functioning (even if the ENA bit is not set). When FSEN is taken high, the boost converter is turned on and the current sinks are enabled at 100% duty cycle. When FSEN returns low, the values programmed in the I<sup>2</sup>C registers are applied at the beginning of the next dimming cycle.

The OUT\_ current, when FSEN is high, is set by a resistor from FSEN to GND according to [Table 1](#). The resistor value is read at power-up and the set OUT\_ current value and I<sup>2</sup>C address cannot subsequently be changed.

If FSEN is not used connect the pin to GND unless the alternative I<sup>2</sup>C address is to be used.

**Table 1. FSEN RESISTOR VALUES**

FSEN RESISTOR VALUE (kΩ)	OUT_ CURRENT (mA)	7-BIT I <sup>2</sup> C ADDRESS
0	Fail-safe disabled	0x69
3.48	25	0x69
7.15	25	0x6F
12	50	0x69
18.7	50	0x6F

**Table 1. FSEN RESISTOR VALUES (continued)**

FSEN RESISTOR VALUE (kΩ)	OUT_ CURRENT (mA)	7-BIT I <sup>2</sup> C ADDRESS
27.4	75	0x69
39	75	0x6F
59	100	0x69
84.5	100	0x6F

### Dimming

Dimming can be performed either using an external PWM signal applied to the DIM pin, or by programming the desired dimming level through I<sup>2</sup>C.

When using internal dimming, set the DIM\_EXT bit in the IMODE register (0x03) to 1 (the default value is 0, the DIM pin is the default dimming input) before setting the ENA bit to turn on the backlight. The signal on the DIM pin is sampled with a 20MHz internal clock.

In internal dimming, write up to 18 bits to the TON\_<sub>[17:0]</sub> bits (see registers 0x04 to 0x0C in the *Register Map* section). The value to be written is calculated using the following formula.

#### Equation 2:

$$TON = \frac{t_{ON}}{50ns}$$

where  $t_{ON}$  is the desired on-time. If a value is written that corresponds to an on-time less than 500ns ( $\leq 0x09$ ), the corresponding OUT\_ will stay on for 500ns. If the value written is longer than the dimming period, the output will be on at 100% duty cycle. To set zero current in any channel, write all the corresponding TON\_ bits to 0.

### Hybrid Dimming

In hybrid dimming mode, the external LEDs are dimmed by first reducing their current as the dimming duty-cycle decreases from 100% (see [Figure 1](#)). At the crossover level set by the HDIM\_THR\_1\_0[1:0] bits dimming transitions to PWM dimming where the LED current is chopped. To select hybrid dimming, set the HDIM bit in the IMODE (0x03) register and select the desired crossover level between analog and PWM dimming using the HDIM\_THR\_1\_0[1:0] bits in the same register. Depending on the DIM\_EXT bit, the device functions in one of two ways:

- (DIM\_EXT = 1) measures the duty cycle on the DIM pin and translates it into a combined LED current value and PWM setting.
- (DIM\_EXT = 0) takes the 18-bit value from the TON\_ registers and translates it into a combined LED current value and PWM setting.

**Note:** When hybrid dimming is used with an internal dimming setting (DIM\_EXT = 0), only the value TON1[17:0] is used. It is not possible to have individual dimming settings for each of the channels in this mode but the TON\_ settings for all the channels must be non-zero.

In summary, there are four possible dimming modes:

- External PWM dimming.
- Internal PWM dimming with the pulse-width set through I<sup>2</sup>C and the PWM frequency generated internally.
- External hybrid dimming with a PWM signal applied to the DIM pin; the pulsed current on the OUT\_ pins follows the DIM frequency.
- Internal hybrid dimming with the dimming ratio set through I<sup>2</sup>C and the PWM frequency generated internally. The TON1[17:0] setting is valid for all channels. Any channels with a TON\_<sub>[17:0]</sub> setting of 0 will be turned off.

[[Hybrid Dimming Operation]] illustrates the difference between standard and hybrid dimming with phase-shifting enabled.

**Hybrid Dimming Operation**

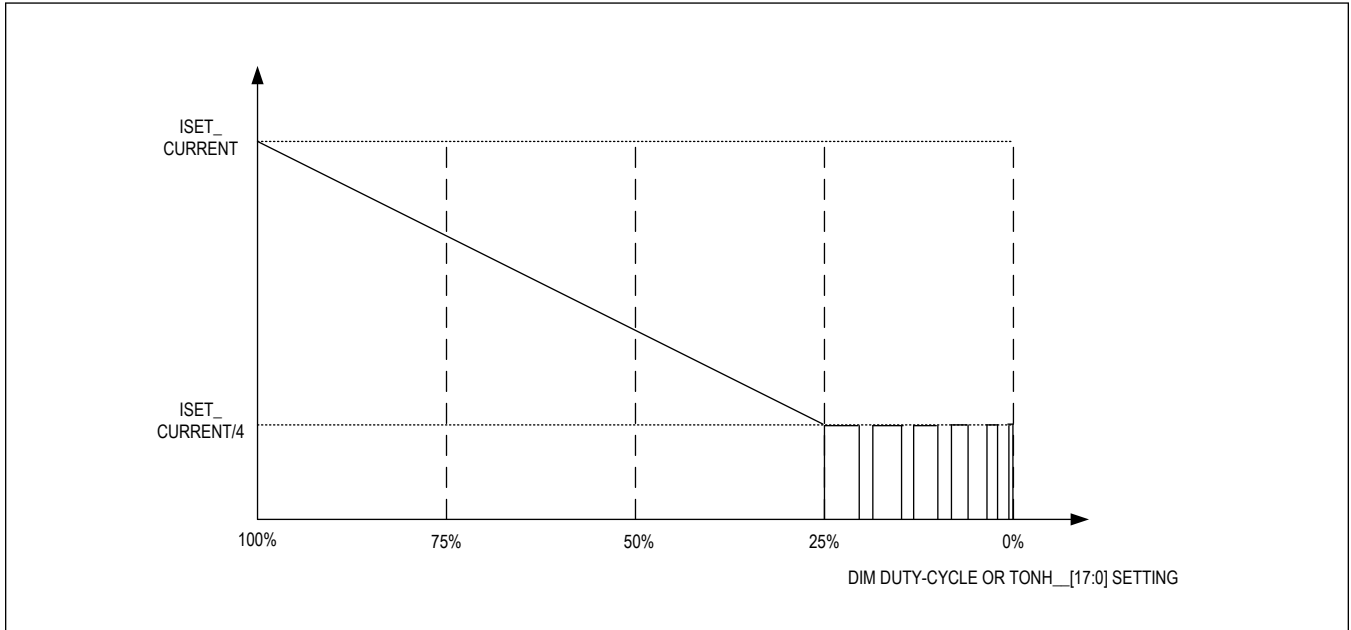


Figure 1. Hybrid Dimming Operation with HDIM[1:0] = 10 (25%)

**Hybrid Dimming Operation Modes**

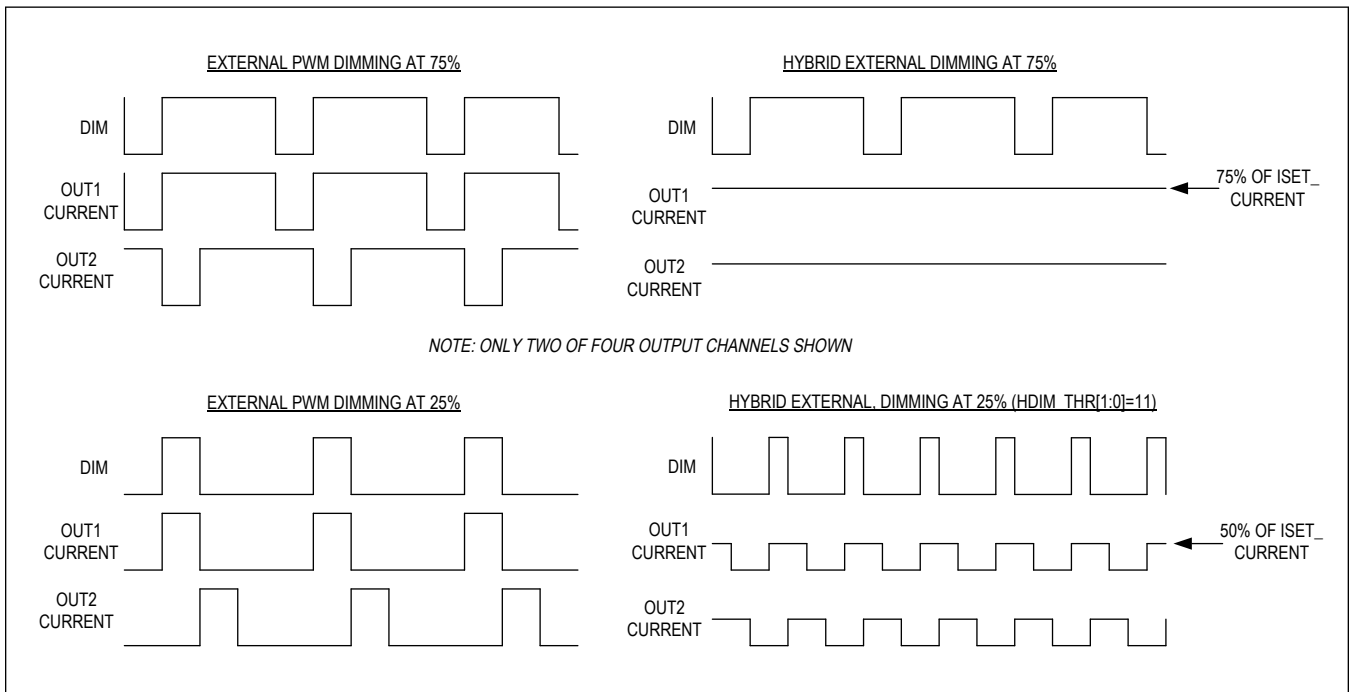


Figure 2. Hybrid Dimming Operation Modes

### Low-Dimming Mode

The IC's operation changes at very narrow dimming pulses to ensure a consistent dimming response of the LEDs. If the dimming on-time (from either the DIM input or the TON\_ value, depending on which is selected) is lower than 50 $\mu$ s (typ), the device enters low-dimming mode. In this state, the converter switches continuously and LED short detection is disabled. When the DIM input is greater than 51 $\mu$ s (typ) the device goes back into normal operation, enabling the short-LED detection and switching the power FET only when the effective dimming signal is high. OUT\_ current monitoring does not operate in low-dim mode although the BSTMON voltage can still be measured.

When internal dimming is used some channels may be in low-dim mode while others are not. If any channel is in low-dim mode, the boost converter runs continuously.

### Phase-Shift Dimming

When the PSEN bit in register 0x02 is set phase shifting of the LED strings is enabled. The device automatically sets the phase shift between strings to 90, 120, or 180 degrees, depending on the number of strings enabled.

### Disabling Individual Strings

To disable an unused LED string, connect the unused OUT\_ to ground through a 12k $\Omega$  resistor, or set the corresponding DIS\_ bit to 1 in the DISABLE (0x13) register before the ENA bit is set. During startup, the device sources 60 $\mu$ A (typ) current through the OUT\_ pins and measures the corresponding voltage. For the string to be properly disabled, the OUT\_ voltage should measure between 365mV and 1.15V during this check. 365mV is the maximum threshold for the OUT\_ short-to-ground check and 1.15V is the minimum unused string-detection threshold.

**Note:** When disabling unused strings, it is necessary to start by disabling the highest-numbered current sinks first (e.g., if two strings need to be disabled, disable OUT4 and OUT3. Do not disable any two strings at random). During normal operation, strings can be selectively turned off by changing the corresponding TON\_ setting to 0. This is only possible when internal dimming is used (not when using the DIM input pin).

### Startup Sequence

When the EN pin is taken high (assuming the IN voltage is above its undervoltage-lockout value), the internal regulator and the I<sup>2</sup>C interface are turned on and the device checks the OUT\_ channels. If any of the OUT\_ pins are detected as shorted to GND, the boost converter does not start (to avoid possible damage) and the corresponding OUT\_SG bit(s) are set. The device also detects and disconnects any unused current-sink channels connected to GND by means of a 12k $\Omega$  resistor. Alternatively, individual channels can be disabled using the DIS[4:1] bits. The total duration of this phase of the startup is 2ms (max). After this phase, the I<sup>2</sup>C interface can be used and the device registers can be written. The ENA bit should be set to 1 to enable the boost and subsequently the OUT\_ current sinks. Before setting the ENA bit to 1 fast soft-start can be chosen by setting the FAST\_SS bit to 1. When the ENA bit is set high, the startup sequence occurs in three stages:

#### Stage 1

Once the ENA bit is high, the controller begins the soft-start of the boost. First, the driver of the external nMOSFET is turned on. A typical current of 50 $\mu$ A is provided by the internal charge pump at the NGATE pin to turn on the external nMOSFET. Do not connect anything other than the MOSFET gate to the NDRV pin. After a 2ms timeout expires, Stage 2 of the startup begins.

#### Stage 2

After the checks in Stage 1 have been performed, the converter starts switching and the output begins to ramp. The DAC reference to the error amplifier is stepped up 1 bit at a time until the voltage at BSTMON reaches 600mV (or 1.1V when the FAST\_SS bit is set to 1). This stage duration is fixed at approximately 50ms (typ) or 23ms when the FAST\_SS bit is set to 1. The BSTMON pin is then sampled, and if its voltage is less than 500mV (typ), FLTB is asserted low, the power converter is turned off, the external nMOSFET on NGATE is turned off, and they all remain off until the ENA bit, input power, or EN pin is toggled.

**Stage 3**

The third stage begins once Stage 2 is complete and the DIM input goes high (with DIM\_EXT = 1), or internal dimming is enabled by setting a PWM value greater than 0 on any of the channels. During Stage 3, the output of the converter is adjusted until the minimum OUT\_ voltage falls within 0.78V (typ) and 1.03V (typ) comparator limits. The output adjustment is again controlled by the DAC, which provides the reference for the error amplifier. The DAC output is updated on each rising edge of the DIM input pin (or internal dimming signal). If the DIM input (or the internal dimming signal when DIM\_EXT = 1) is at 100% duty cycle (DIM = high), the DAC output is updated once every 10ms.

The total soft-start time can be calculated using Equation 3.

**Equation 3:**

$$t_{SS} = 52\text{ms} + \frac{(V_{LED} + 0.91) - (0.6 \times A_{OVP})}{f_{DIM} \times 0.01 \times A_{OVP}}$$

where:

$t_{SS}$  = Total soft-start time

52ms = Fixed Stage 1 + Stage 2 duration

$V_{LED}$  = Total forward voltage of the LED strings

0.91V = Midpoint of the window comparator

$f_{DIM}$  = Dimming frequency (use 100Hz for  $f_{DIM}$  when input duty cycle is 100%)

0.01V = 4 times the 2.5mV LSB of the DAC

$A_{OVP}$  = Gain of the BSTMON resistor-divider or  $1 + R6/R7$

When the FAST\_SS bit is set to 1 the soft-start is accelerated and the final value of the voltage on the BSTMON pin is 1.1V. The equation for the total soft-start time then becomes:

$$t_{SS} = 25\text{ms} + \frac{1.1 \times A_{OVP} - (V_{LED} + 0.91)}{f_{DIM} \times 0.01 \times A_{OVP}}$$

After the soft-start period, a fault is detected whenever the BSTMON pin falls below 430mV (typ). When this occurs, the power converter is latched off and the NGATE output discharges the gate of the external nMOSFET, disconnecting the input voltage from the boost converter. The FLTB pin is asserted low whenever the undervoltage protection is activated. Cycling the ENA bit, EN pin, or the supply is required to start up again, once the fault condition has been removed.

**Boost Startup**

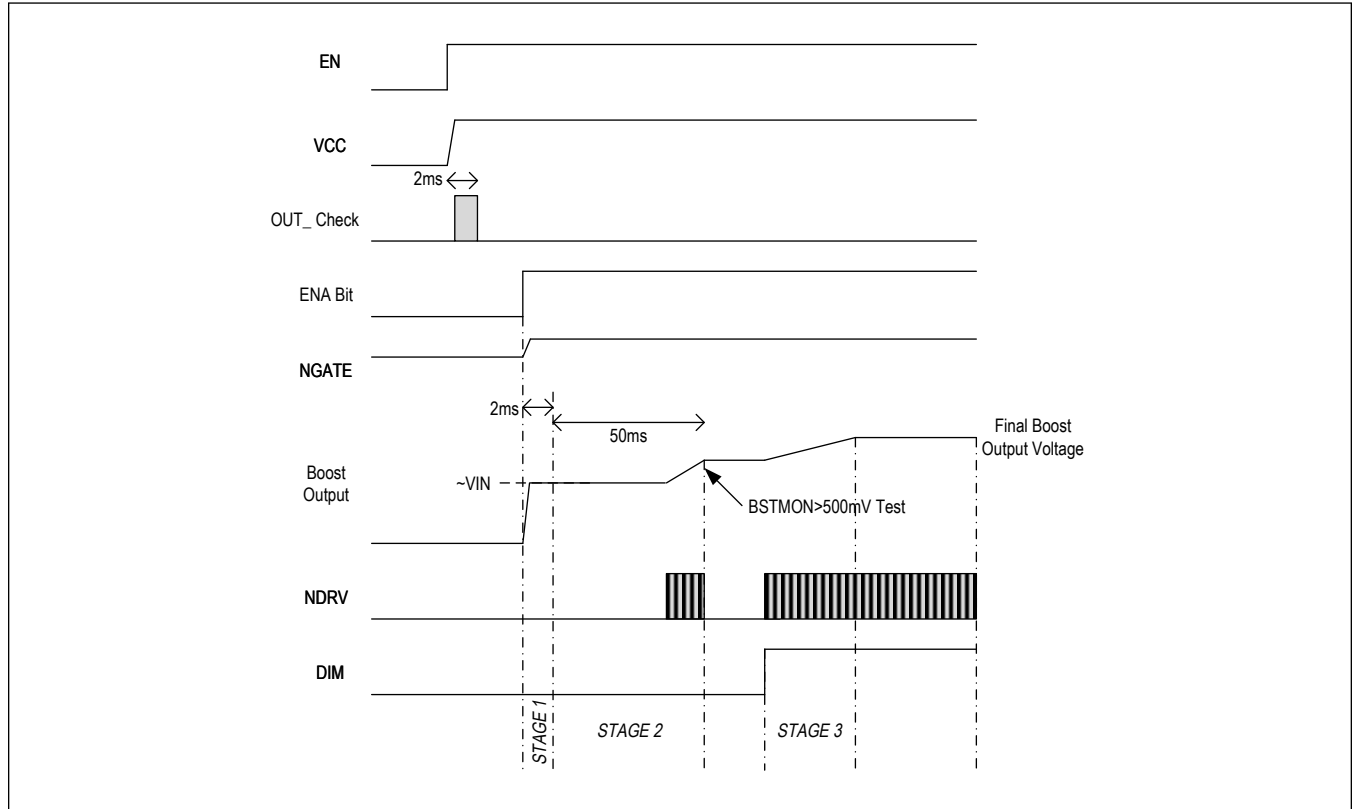


Figure 3. Boost Startup Waveform with FAST\_SS = 0

**Oscillator Frequency/External Synchronization**

The internal oscillator frequency is programmable between 400kHz and 2.2MHz using a timing resistor ( $R_{RT}$ ) connected from the RT pin to GND. Use Equation 4 to calculate the value of  $R_{RT}$  for the desired switching frequency ( $f_{SW}$ ).

**Equation 4:**

$$R_{RT} = \frac{29260 + (2200 - f_{SW}) \times 0.81}{f_{SW}}$$

where  $R_{RT}$  is in k $\Omega$  and  $f_{SW}$  is in kHz.

Synchronize the oscillator with an external clock by AC-coupling the external clock to the RT input. The value of the capacitor used for AC-coupling is  $C_{SYNC} = 10pF$  and the duty cycle of the external clock should be 50%.

At low input voltages and when the switching frequency is above 1MHz, the switching frequency is automatically reduced by a factor of 30% to enable high-duty-cycle operation and maintain output-voltage regulation.

**Spread-Spectrum Modulation**

The IC includes spread-spectrum modulation that reduces peak electromagnetic interference (EMI) at the switching frequency and its harmonics.

The spread spectrum uses a pseudorandom dithering technique where the switching frequency is varied in the 97% range (or 94% when the SSL bit is 1) of the programmed switching frequency, to 103% (or 106% when the SSL bit is 1) of the programmed switching frequency set through the external resistor from RT to GND. When spread spectrum is used, the total energy at the fundamental and each harmonic is spread over a wider bandwidth, reducing the peak energy



at the relevant frequency.

Spread spectrum is disabled if external synchronization is used. Optionally, spread spectrum can also be disabled by setting the SS\_OFF bit in the SETTING (0x12) register to 1. The amount of spread spectrum can also be varied between  $\pm 3\%$  and  $\pm 6\%$  using the SSL bit in the same register.

### 5V LDO Regulator (V<sub>CC</sub>)

The internal LDO regulator converts the input voltage at IN (or the voltage at the BOOST pin when IN is below V<sub>SWITCHOVER</sub>) to a 5V output voltage at V<sub>CC</sub>. The LDO regulator supplies current to the internal control circuitry and the gate driver. Bypass V<sub>CC</sub> to GND with a 1 $\mu$ F (min) ceramic capacitor as close as possible to the device.

### LED Current Control

The full-scale sink current for the outputs (OUT1–OUT4) is set using the four ISET[3:0] bits in the ISET register (0x02). The OUT\_ current value is also directly related to the reference current in the resistor on the IREF pin (R<sub>IREF</sub>). If the R<sub>IREF</sub> value is not in the 27.5k $\Omega$  to 83.5k $\Omega$  range, the device will not operate and an IREF0OR error is indicated (see the *Register Map*).

When PWM dimming is used, the current in the OUT\_ channels switches between zero and the full-scale sink current at the set duty cycle.

When hybrid dimming is used, the sink current in OUT1–OUT4 is reduced linearly from the full-scale value until the level set by HDIM\_THR\_1\_0[1:0] is reached; dimming at lower levels is then accomplished using PWM (see [Figure 1](#)).

The LED current when using a 40.2k $\Omega$  IREF resistor is shown in [Table 2](#).

**Table 2. LED CURRENT WITH 40.2k $\Omega$  IREF RESISTOR**

ISET[3:0]	LED CURRENT PER OUTPUT (mA)
0000	56
0001	62
0010	68
0011	74
0100	81
0101	87
0110	93
0111	99
1000	106
1001	112
1010	118
1011	124
1100	130
1101	137
1110	143
1111	149

### Fault Protection

Fault protection in the IC includes cycle-by-cycle current limiting in the PWM controller, DC-DC converter output undervoltage protection, output overvoltage protection, open-LED detection, short-LED detection and protection, and overtemperature shutdown. The open-drain fault flag output (FLTB) goes low when an open-LED string is detected, a short-LED string is detected, an output undervoltage, or during thermal shutdown. Certain faults can be inhibited from causing FLTB to go low using the bits in the MASK[7:0] register. FLTB is cleared when the fault condition is removed.

during thermal shutdown and shorted LEDs. FLTB is latched low for an open-LED and can be reset by cycling power or toggling the EN pin. The thermal-shutdown threshold is +165°C and has +15°C hysteresis.

### Open-LED Management and Overvoltage Protection

After the soft-start of the boost converter, the IC detects open-LED strings and disconnects any such strings from the internal minimum OUT\_ voltage detector. This keeps the DC-DC converter output voltage within safe limits and maintains high efficiency. The current in strings that have been detected open is not measured by the ADC and reads as zero.

During normal operation, the DC-DC converter output-regulation loop uses the minimum OUT\_ voltage as the feedback input. If any LED string is open, the voltage at the opened OUT\_ goes to V<sub>LEDGND</sub>. The DC-DC converter output voltage then increases to the overvoltage-protection threshold set by the voltage-divider network connected between the converter output, the BSTMON input, and GND. The overvoltage-protection threshold at the DC-DC converter output is determined using the equation below.

#### Equation 5:

$$V_{OUT\_BSTMON} = 1.23 \times \left(1 + \frac{R6}{R7}\right)$$

where 1.23V (typ) is the overvoltage threshold on BSTMON (see the Functional Diagram). Select V<sub>OUT\\_BSTMON</sub> according to the formula below.

#### Equation 6:

$$1.1 \times (V_{LED\_MAX} + 1.1) < V_{OUT\_BSTMON} < 2 \times (V_{LED\_MIN} + 0.7)$$

where:

V<sub>LED\\_MAX</sub> = Maximum expected LED string voltage

V<sub>LED\\_MIN</sub> = Minimum expected LED string voltage

Select R6 and R7 such that the voltage at OUT\_ does not exceed the absolute maximum rating. As soon as the DC-DC converter output reaches the overvoltage-protection threshold, the internal MOSFET is switched off.

The overvoltage threshold should be set to less than twice the minimum LED voltage to ensure proper operation and that the BSTMON minimum regulation point of 600mV (typ) is not breached. Connect a 12kΩ resistor between OUT\_ and LEDGND for each unused channel to avoid overvoltage triggering at startup. When an open-LED overvoltage condition occurs, FLTB is latched low. Any current-sink output with V<sub>OUT\_</sub> < 300mV (typ) is permanently disconnected from the minimum voltage detector. Toggle the EN pin to clear an open-LED condition.

### Short-LED Detection

The IC checks for shorted LEDs after the current in any channel is turned on. A shorted-LED is detected at OUT\_ if the condition below is met.

#### Equation 7:

$$V_{OUT\_} > RSDT$$

where:

RSDT = Programmable short-LED-detection threshold set by the SLDET[1:0] bits in the SETTING (0x12) register.

If a short is detected on any of the strings, the affected LED strings are disabled after a delay of one dimming cycle and the FLTB output flag asserts low after two dimming cycles until the device detects that the shorts are removed. Disable short-LED detection by setting SLDET[1:0] to 0x0. Short-LED detection is disabled in low-dimming mode. In external dimming mode with the DIM input connected continuously high, the OUT\_ pins are periodically scanned to detect shorted LEDs. The scan frequency is 100Hz.

Similarly, when DIM\_EXT = 0 and internal dimming is being used, shorted LEDs are still detected by periodically scanning the OUT\_ states at 100Hz.

Short-LED detection is also disabled in cases where all active OUT\_ channels rise above 2.5V. This can occur in a boost-converter application when the input voltage becomes higher than the total LED string voltage drop, such as during a

battery load dump. If a short-LED fault occurs during a load dump, the fault flag does not assert until the load dump is over and the minimum OUT\_ voltage has fallen below 2.35V. If a load dump occurs after a short LED is detected, the fault flag deasserts until the load dump is over and the minimum OUT\_ voltage has fallen below 2.35V, at which point, the fault flag reasserts.

#### **LED Short-to-Ground Protection**

During startup, a check is performed for OUT\_ pins shorted to ground by sourcing a current of 60 $\mu$ A into the OUT\_ pins. If the pin voltage does not exceed 300mV, a short to GND is declared. In this case the device does not start. Toggle the EN pin or power to clear this condition.

#### **Thermal Warning/Shutdown**

The IC includes thermal protection that operates at a temperature of 165°C. When the thermal-shutdown temperature is reached, the device is immediately disabled so it can cool. When the junction temperature falls by 15°C, the device is re-enabled with the same settings as before (the boost converter performs a soft-start). When a thermal shutdown occurs, the FLTB pin goes low and the OT bit, if read through the I<sup>2</sup>C, is set to 1.

A thermal warning bit (OTW) is implemented in the DIAG (0x1F) register and indicates that the junction temperature has exceeded 125°C. The OTWMASK bit in the MASK (0x1E) register is used to control whether or not an active OTW bit causes the FLTB pin to go low.

#### **MAX25014 Analog-to-Digital Converter**

The analog-to-digital converter (ADC) is used to measure the current in each of the strings and the voltage on the BSTMON pin.

A conversion cycle is started by setting the CONVERT bit in the ISET (0x02) register to 1. At the end of the cycle the CONVERT bit is reset to 0 to indicate a complete cycle, and the IOUT1–IOUT4 and VMON registers contain the updated values. The full-scale value of the current measurement is 127.5mA with an IREF resistor of 49.9k $\Omega$  or 158.3mA with R<sub>IREF</sub> = 40.2k $\Omega$ . Values higher than these read as full scale or 0xFF. Current measurements are not performed on channels that are in low-dim mode; before performing a conversion, this can be checked by reading the LoDIM\_ bits. If a conversion is attempted on a channel that is in low-dim mode, the current value returned will be 0x00. The duration of a complete conversion depends on whether or not phase shifting is enabled. With phase shifting enabled, a complete conversion can take up to two dimming cycles, worst-case. With phase shifting disabled, one dimming cycle is the worst-case latency (the conversion is initiated at the beginning of a DIM cycle and concluded < 50 $\mu$ s later).

Register Map

MAX25014

ADDRESS	NAME	MSB							LSB
<b>I2C</b>									
0x00	<a href="#">Dev_ID[7:0]</a>	Device_ID[7:0]							
0x01	<a href="#">Rev_ID[7:0]</a>	-	-	-	-	Revision_ID[3:0]			
0x02	<a href="#">ISET[7:0]</a>	-	CONVE RT	ENA	PSEN	ISET[3:0]			
0x03	<a href="#">IMODE[7:0]</a>	LoDIM4	LoDIM3	LoDIM2	LoDIM1	DIM_EX T	HDIM	HDIM_THR_1_0[1:0]	
0x04	<a href="#">TON1H[7:0]</a>	TON1H[7:0]							
0x05	<a href="#">TON1L[7:0]</a>	TON1L[7:0]							
0x06	<a href="#">TON2H[7:0]</a>	TON2H[7:0]							
0x07	<a href="#">TON2L[7:0]</a>	TON2L[7:0]							
0x08	<a href="#">TON3H[7:0]</a>	TON3H[7:0]							
0x09	<a href="#">TON3L[7:0]</a>	TON3L[7:0]							
0x0A	<a href="#">TON4H[7:0]</a>	TON4H[7:0]							
0x0B	<a href="#">TON4L[7:0]</a>	TON4L[7:0]							
0x0C	<a href="#">TON1-4LSB[7:0]</a>	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
0x12	<a href="#">SETTING[7:0]</a>	ILIM	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
0x13	<a href="#">DISABLE[7:0]</a>	UV_SEL	FAST_S S	CP_DIS	-	DIS4	DIS3	DIS2	DIS1
0x14	<a href="#">BSTMON[7:0]</a>	VBSTMON[7:0]							
0x15	<a href="#">IOUT1[7:0]</a>	IOUT1[7:0]							
0x16	<a href="#">IOUT2[7:0]</a>	IOUT2[7:0]							
0x17	<a href="#">IOUT3[7:0]</a>	IOUT3[7:0]							
0x18	<a href="#">IOUT4[7:0]</a>	IOUT4[7:0]							
0x1B	<a href="#">OPEN[7:0]</a>	-	-	-	-	OUT4O	OUT3O	OUT2O	OUT1O
0x1C	<a href="#">SHORTGND[7:0]</a>	-	-	-	-	OUT4SG	OUT3SG	OUT2SG	OUT1SG
0x1D	<a href="#">SHORTED LED[7:0]</a>	-	-	-	-	OUT4SL	OUT3SL	OUT2SL	OUT1SL
0x1E	<a href="#">MASK[7:0]</a>	-	-	-	BSTUVM ASK	OMASK	SGMAS K	OTWMA SK	SLMASK
0x1F	<a href="#">DIAG[7:0]</a>	-	-	IREFOO R	BSTUV	BSTOV	HW_RS T	OTW	OT

Register Details

[Dev\\_ID \(0x00\)](#)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[7:0]							
Reset	0x24							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
Device_ID	7:0	Reads 0x1424

**Rev\_ID (0x01)**

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Revision_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
Revision_ID	3:0	Device revision ID, reads 0x0.

**ISET (0x02)**

BIT	7	6	5	4	3	2	1	0
Field	–	CONVERT	ENA	PSEN	ISET[3:0]			
Reset	–	0b0	0b0	0b1	0b1011			
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION																																																																																					
CONVERT	6	Write a 1 to this bit to start a conversion cycle of the ADC. When the cycle is finished, this bit is automatically reset to indicate that data is ready.																																																																																					
ENA	5	Boost converter and LED outputs enable bit. Set to 1 to enable the device.																																																																																					
PSEN	4	When 0, phase shifting is disabled. When 1, phase shifting is enabled.																																																																																					
ISET	3:0	Table 3. LED CURRENT SETTING (VALUES WITH R <sub>IREF</sub> = 49.9kΩ)																																																																																					
		<table border="1"> <thead> <tr> <th>ISET3</th> <th>ISET2</th> <th>ISET1</th> <th>ISET0</th> <th>Current Setting</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>45mA</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50mA</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>55mA</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>60mA</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>65mA</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>70mA</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>75mA</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>80mA</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>85mA</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>90mA</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>95mA</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>100mA*</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>105mA</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>110mA</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>115mA</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>120mA</td></tr> </tbody> </table>	ISET3	ISET2	ISET1	ISET0	Current Setting	0	0	0	0	45mA	0	0	0	1	50mA	0	0	1	0	55mA	0	0	1	1	60mA	0	1	0	0	65mA	0	1	0	1	70mA	0	1	1	0	75mA	0	1	1	1	80mA	1	0	0	0	85mA	1	0	0	1	90mA	1	0	1	0	95mA	1	0	1	1	100mA*	1	1	0	0	105mA	1	1	0	1	110mA	1	1	1	0	115mA	1	1	1	1	120mA
		ISET3	ISET2	ISET1	ISET0	Current Setting																																																																																	
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1	1	1	1	120mA																																																																																			
		*default value																																																																																					

**IMODE (0x03)**

BIT	7	6	5	4	3	2	1	0
Field	LoDIM4	LoDIM3	LoDIM2	LoDIM1	DIM_EXT	HDIM	HDIM_THR_1_0[1:0]	
Reset	0x0	0x0	0x0	0x0	0b1	0b0	0b00	
Access Type	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
LoDIM4	7	When 1, indicates that channel 4 is in low-dim mode.
LoDIM3	6	When 1, indicates that channel 3 is in low-dim mode.
LoDIM2	5	When 1, indicates that channel 2 is in low-dim mode.
LoDIM1	4	When 1, indicates that channel 1 is in low-dim mode.
DIM_EXT	3	When 1, dimming through the DIM pin is enabled. When 0, dimming is controlled using the TON__ registers.
HDIM	2	When 1, hybrid dimming is enabled. Default value is 0.
HDIM_THR_1_0	1:0	Set hybrid-dimming threshold. Default value is 6.25% (00).

**TON1H (0x04)**

On-time setting for channel 1 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1H	7:0	High byte of 18-bit TON setting for channel 1.

**TON1L (0x05)**

On-time setting for channel 1 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON1L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON1L	7:0	Middle byte of 18-bit TON setting for channel 1.

**TON2H (0x06)**

On-time setting for channel 2 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2H	7:0	High byte of 18-bit TON setting for channel 2.

**TON2L (0x07)**

On-time setting for channel 2 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON2L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON2L	7:0	Middle byte of 18-bit TON setting for channel 2.

**TON3H (0x08)**

On-time setting for channel 3 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON3H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3H	7:0	High byte of 18-bit TON setting for channel 3.

**TON3L (0x09)**

On-time setting for channel 3 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON3L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON3L	7:0	Middle byte of 18-bit TON setting for channel 3.

**TON4H (0x0A)**

On-time setting for channel 4 with 50ns resolution, high byte.

BIT	7	6	5	4	3	2	1	0
Field	TON4H[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4H	7:0	High byte of 18-bit TON setting for channel 4.

**TON4L (0x0B)**

On-time setting for channel 4 with 50ns resolution, middle byte.

BIT	7	6	5	4	3	2	1	0
Field	TON4L[7:0]							
Reset	0b11111111							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TON4L	7:0	Middle byte of 18-bit TON setting for channel 4.

**TON1-4LSB (0x0C)**

LSBs of on-time setting for all channels with 50ns resolution.

BIT	7	6	5	4	3	2	1	0
Field	TON4LSB[1:0]		TON3LSB[1:0]		TON2LSB[1:0]		TON1LSB[1:0]	
Reset	0b11		0b11		0b11		0b11	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
TON4LSB	7:6	2 least significant bits of 18-bit TON setting for channel 4.
TON3LSB	5:4	2 least significant bits of 18-bit TON setting for channel 3.
TON2LSB	3:2	2 least significant bits of 18-bit TON setting for channel 2.
TON1LSB	1:0	2 least significant bits of 18-bit TON setting for channel 1.

**SETTING (0x12)**

BIT	7	6	5	4	3	2	1	0
Field	ILIM	FPWM[2:0]			SS_OFF	SSL	SLDET[1:0]	
Reset	0x0	0b001			0b0	0b0	0b11	
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION																																				
ILIM	7	This bit sets the current limit in low-voltage operating mode. When zero the current limit is increased to 600mV, when 1 the current limit becomes 820mV.																																				
FPWM	6:4	These bits set the PWM frequency in internal PWM mode.																																				
		<table border="1"> <thead> <tr> <th>FPWM2</th> <th>FPWM1</th> <th>FPWM0</th> <th>PWM FREQUENCY (Hz)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>153</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>203</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>305</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>610</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>980</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1220</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1401</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1634</td> </tr> </tbody> </table>	FPWM2	FPWM1	FPWM0	PWM FREQUENCY (Hz)	0	0	0	153	0	0	1	203	0	1	0	305	0	1	1	610	1	0	0	980	1	0	1	1220	1	1	0	1401	1	1	1	1634
		FPWM2	FPWM1	FPWM0	PWM FREQUENCY (Hz)																																	
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1	0	1	1220																																			
1	1	0	1401																																			
1	1	1	1634																																			
SS_OFF	3	When 1, spread-spectrum switching is disabled. Default value is 0.																																				



BITFIELD	BITS	DESCRIPTION															
SSL	2	When spread spectrum is enabled, the SSL bit chooses the amount of spread: When 0, the spread is nominally $\pm 6\%$ , and when 1, the spread is $\pm 3\%$ .															
SLDET	1:0	<table border="1"> <thead> <tr> <th>SLDET1</th> <th>SLDET0</th> <th>SETTING</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Disabled</td> </tr> <tr> <td>0</td> <td>1</td> <td>3V</td> </tr> <tr> <td>1</td> <td>0</td> <td>6V</td> </tr> <tr> <td>1</td> <td>1</td> <td>8V</td> </tr> </tbody> </table>	SLDET1	SLDET0	SETTING	0	0	Disabled	0	1	3V	1	0	6V	1	1	8V
		SLDET1	SLDET0	SETTING													
		0	0	Disabled													
		0	1	3V													
		1	0	6V													
1	1	8V															
<b>Shorted-LED-Threshold Settings</b>																	

**DISABLE (0x13)**

Channel-disable bits.

BIT	7	6	5	4	3	2	1	0
Field	UV_SEL	FAST_SS	CP_DIS	–	DIS4	DIS3	DIS2	DIS1
Reset	0x0	0x0	0x0	–	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
UV_SEL	7	Selects IN undervoltage lockout level. Set to 1 to set the lower option.
FAST_SS	6	Selects slow or fast boost soft-start. Set to 1 for fast soft-start.
CP_DIS	5	When 1 this bit disables the internal charge pump which drives the NGATE pin. Set to 1 when an external series switch is not used. The setting of CP_DIS should not be changed during device operation as it will cause the device to latch off.
DIS4	3	Set this bit to 1 to disable OUT4. This must be done before ENA is written to 1.
DIS3	2	Set this bit to 1 to disable OUT3. This must be done before ENA is written to 1.
DIS2	1	Set this bit to 1 to disable OUT2. This must be done before ENA is written to 1.
DIS1	0	Set this bit to 1 to disable OUT1. This must be done before ENA is written to 1.

**BSTMON (0x14)**

BIT	7	6	5	4	3	2	1	0
Field	VBSTMON[7:0]							
Reset	0b00000000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VBSTMON	7:0	Result of voltage measurement on BSTMON pin. The full-scale is 1.3V and 1 LSB is 5.1mV.

**IOUT1 (0x15)**

OUT1 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT1	7:0	OUT1 output current. Full scale is 128.8mA or 159.4mA, depending on the IREF resistor value.

**IOUT2 (0x16)**

OUT2 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT2	7:0	OUT2 output current, Full scale is 128.8mA or 159.4mA, depending on the IREF resistor value.

**IOUT3 (0x17)**

OUT3 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT3	7:0	OUT3 output current. Full scale is 128.8mA or 159.4mA, depending on the IREF resistor value.

**IOUT4 (0x18)**

OUT4 current readback.

BIT	7	6	5	4	3	2	1	0
Field	IOUT4[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
IOUT4	7:0	OUT4 output current. Full scale is 128.8mA or 159.4mA, depending on the IREF resistor value.

**OPEN (0x1B)**

Open-string diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4O	OUT3O	OUT2O	OUT1O
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4O	3	If 1, an open has been detected on channel 4.
OUT3O	2	If 1, an open has been detected on channel 3.
OUT2O	1	If 1, an open has been detected on channel 2.
OUT1O	0	If 1, an open has been detected on channel 1.

**SHORTGND (0x1C)**

Short-to-ground diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4SG	OUT3SG	OUT2SG	OUT1SG
Reset	–	–	–	–	0x0b0	0x0b0	0x0b0	0x0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4SG	3	If 1, a short-to-ground has been detected on channel 4 at startup.
OUT3SG	2	If 1, a short-to-ground has been detected on channel 3 at startup.
OUT2SG	1	If 1, a short-to-ground has been detected on channel 2 at startup.
OUT1SG	0	If 1, a short-to-ground has been detected on channel 1 at startup.

**SHORTED LED (0x1D)**

Shorted-LED diagnostics,

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUT4SL	OUT3SL	OUT2SL	OUT1SL
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OUT4SL	3	If 1, a shorted-LED condition has been detected on channel 4.
OUT3SL	2	If 1, a shorted-LED condition has been detected on channel 3.
OUT2SL	1	If 1, a shorted-LED condition has been detected on channel 2.
OUT1SL	0	If 1, a shorted-LED condition has been detected on channel 1.

**MASK (0x1E)**

Mask register for the FLTB pin.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BSTUVMASK	OMASK	SGMASK	OTWMASK	SLMASK
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
BSTUVMASK	4	When 1, a boost fault (undervoltage or overvoltage) does not cause the FLTB pin to assert low.
OMASK	3	When 1, an open-LED fault does not cause the FLTB pin to assert low.
SGMASK	2	When 1, a short-to-ground LED fault does not cause the FLTB pin to assert low.
OTWMASK	1	When 1, an overtemperature warning does not cause the FLTB pin to assert low.
SLMASK	0	When 1, a shorted-LED fault does not cause the FLTB pin to assert low.

**DIAG (0x1F)**

Boost state, overtemperature-warning/shutdown diagnostics.

BIT	7	6	5	4	3	2	1	0
Field	–	–	IREFOOR	BSTUV	BSTOV	HW_RST	OTW	OT
Reset	–	–	0b0	0b0	0b0	0b1	0x0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
IREFOOR	5	When 1, this bit indicates that the IREF current is out of range. This is probably due to an incorrect resistor value on IREF. In this condition, the IC stops operation.
BSTUV	4	If 1, an undervoltage has been detected on the boost output and the boost was disabled.
BSTOV	3	If 1, the boost converter is at its overvoltage limit.
HW_RST	2	If 1, the device has just emerged from a hardware reset (power-up). This bit is reset after the first read from this register.
OTW	1	If 1, the junction temperature of the device is over 125°C.
OT	0	If 1, the junction temperature of the device exceeded 165°C and the device was shut down.

## Applications Information

### DC-DC Converter

Three different converter topologies are possible with the DC-DC converter in the MAX25014 that have the ground-referenced outputs necessary to use the constant-current sink drivers. If the LED string forward voltage is always greater than the input supply voltage range, use the boost-converter topology. If the LED string forward voltage falls within the supply voltage range, use a buck-boost converter topology. The possible buck-boost topologies are SEPIC or a coupled-inductor buck-boost topology. The latter is basically a flyback converter with 1:1 turns ratio. 1:1-coupled inductors are available with tight coupling suitable for this application.

The boost-converter topology provides the highest efficiency among the above-mentioned topologies. The coupled-inductor topology has the advantage of not using a coupling capacitor, but does require tightly coupled windings to avoid additional snubber components. The SEPIC configuration requires two inductors (or a coupled inductor) and a coupling capacitor. Furthermore, the feedback-loop compensation for SEPIC becomes complex if the coupling capacitor is not large enough.

### Power-Circuit Design

First, select a converter topology based on the factors listed in the [DC-DC Converter](#) section. Determine the required input supply voltage range, the maximum voltage needed to drive the LED strings, including the minimum 0.85V across the constant LED current sink ( $V_{LED}$ ), and the total output current needed to drive the LED strings ( $I_{LED}$ ), as shown below in Equation 8.

#### Equation 8:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

where  $I_{STRING}$  is the current per string and  $N_{STRING}$  is the number of strings used.

Next, calculate the maximum duty cycle ( $D_{MAX}$ ) using one of the equations below, depending on the configuration.

#### Equation 9 (for the boost configuration):

$$D_{MAX} = \frac{(V_{LED} + V_{D1} - V_{IN\_MIN})}{(V_{LED} + V_{D1} - V_{DS} - 0.3)}$$

#### Equation 10 (for SEPIC and coupled-inductor buck-boost configurations):

$$D_{MAX} = \frac{V_{LED} + V_{D1}}{(V_{IN\_MIN} - V_{DS} - 0.3 + V_{LED} + V_{D1})}$$

where:

- $V_{D1}$  = Forward drop of the rectifier diode in volts (approximately 0.6V)
- $V_{IN\_MIN}$  = Minimum input supply voltage
- $V_{DS}$  = Drain-to-source voltage of the external MOSFET when it is on

Select the switching frequency ( $f_{SW}$ ) depending on space, noise, and efficiency constraints.

### Boost and Coupled-Inductor Configurations

In all three converter configurations, the average inductor current varies with the input voltage; the maximum average current occurs at the lowest input voltage. For the boost converter, the average inductor current is equal to the input current. Select the maximum peak-to-peak ripple on the inductor current ( $\Delta I_L$ ). The recommended maximum peak-to-peak ripple is 60% of the average inductor current, but lower and higher values of ripple are also acceptable.

Use the following equations to calculate the maximum average inductor current ( $I_{L\_AVG}$ ) and peak inductor current ( $I_{L\_P}$ ) in amperes.

#### Equation 11:

$$I_{L_{AVG}} = \frac{I_{LED}}{(1 - D_{MAX})}$$

Allowing the peak-to-peak inductor ripple ( $\Delta I_L$ ) to be  $\pm 30\%$  of the average inductor current:

**Equations 12:**

$$\Delta I_L = I_{L_{AVG}} \times 0.3 \times 2$$

and:

$$I_{L_P} = I_{L_{AVG}} + \frac{\Delta I_L}{2}$$

Calculate the minimum inductance value ( $L_{MIN}$ ), in henries (H), with the inductor current ripple set to the maximum value:

**Equation 13:**

$$L_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

Choose an inductor with a minimum inductance greater than the calculated  $L_{MIN}$  and current rating greater than  $I_{L_P}$ . The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current for boost configuration. For the coupled-inductor, the saturation limit of the inductor with only one winding conducting should be 10% higher than  $I_{L_P}$ .

### SEPIC Configuration

Power-circuit design for the SEPIC configuration is very similar to a conventional design with the output voltage referenced to the input supply voltage. For SEPIC, the output is referenced to ground and the inductor is split into two parts. One of the inductors ( $L_2$ ) takes LED current as the average current, and the other ( $L_1$ ) takes input current as the average current.

Use the following equations to calculate the average inductor currents ( $I_{L1_{AVG}}$ ,  $I_{L2_{AVG}}$ ) and peak inductor currents ( $I_{L1_P}$ ,  $I_{L2_P}$ ) in amperes.

**Equation 14:**

$$I_{L1_{AVG}} = \frac{I_{LED} \times D_{MAX} \times 1.1}{1 - D_{MAX}}$$

The factor 1.1 provides a margin of 10% to account for the converter losses.

**Equation 15:**

$$I_{L2_{AVG}} = I_{LED}$$

Assuming the peak-to-peak inductor ripple  $\Delta I_L$  is  $\pm 30\%$  of the average inductor current.

**Equations 16:**

$$\Delta I_{L1} = I_{L1_{AVG}} \times 0.3 \times 2$$

and:

$$I_{L1_P} = I_{L1_{AVG}} + \frac{\Delta I_{L1}}{2}$$

and:

$$\Delta I_{L2} = I_{L2_{AVG}} \times 0.3 \times 2$$

and:

$$I_{L2_P} = I_{L2_{AVG}} + \frac{\Delta I_{L2}}{2}$$

Calculate the minimum inductance values ( $L_{1_{MIN}}$  and  $L_{2_{MIN}}$ ) in henries with the inductor current ripple set to the values previously calculated.

**Equations 17:**

$$L1_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3) \times D_{MAX}}{f_{SW} \times \Delta IL1}$$

$$L2_{MIN} = \frac{(V_{IN\_MIN} - V_{DS} - 0.3) \times D_{MAX}}{f_{SW} \times \Delta IL2}$$

Choose inductors with a minimum inductance greater than the calculated  $L1_{MIN}$  and  $L2_{MIN}$ , and current rating greater than  $IL1_P$  and  $IL2_P$ , respectively. The recommended saturation current limit of the selected inductor is 10% higher than the inductor peak current.

To simplify further calculations, consider L1 and L2 as a single inductor with L1 and L2 connected in parallel. The combined inductance value and current is calculated as shown below.

**Equations 18:**

$$L = \frac{L1 \times L2}{L1 + L2}$$

and:

$$IL_{AVG} = IL1_{AVG} + IL2_{AVG}$$

where  $IL_{AVG}$  represents the total average current through both the inductors in the SEPIC configuration. Use these values in the calculations in the following sections.

Select coupling-capacitor  $C_S$  so peak-to-peak ripple on it is less than 2% of the minimum input supply voltage. This ensures that the second-order effects created by the series-resonant circuit comprising L1,  $C_S$ , and L2 do not affect the normal operation of the converter. Use the following equation to calculate the minimum value of  $C_S$ .

**Equation 19:**

$$C_S = \frac{I_{LED} \times D_{MAX}}{V_{IN\_MIN} \times 0.02 \times f_{SW}}$$

where:

- $C_S$  = Minimum value of the coupling capacitor in farads
- 0.02 = 2% ripple factor

**Slope Compensation and Current-Sense Resistor**

The IC generates a current ramp for slope compensation. This ramp current is synchronized with the switching frequency and starts from zero at the beginning of every clock cycle, rising linearly to reach 50 $\mu$ A at the end of the clock cycle. The slope-compensating resistor ( $R_{SC}$ ) is connected between the CS input and the source of the external switching MOSFET. This adds a programmable ramp voltage to the CS input voltage to provide slope compensation.

Use one of the following equations to calculate the value of  $R_{SC}$ .

**Equation 20 (for the boost configuration):**

$$R_{SC} = \frac{(V_{LED} - 2 \times V_{IN\_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

**Equation 21 (for SEPIC and coupled-inductor configurations):**

$$R_{SC} = \frac{(V_{LED} - V_{IN\_MIN}) \times R_{CS} \times 3}{L_{MIN} \times 50\mu A \times f_{SW} \times 4}$$

where:

- $V_{LED}$  and  $V_{IN\_MIN}$  are in volts
- $R_{SC}$  and  $R_{CS}$  are in  $\Omega$
- $L_{MIN}$  is in henries

- $f_{SW}$  is in hertz

The value of the switch current-sense resistor ( $R_{CS}$ ) can be calculated as shown below.

**Equation 22 (for the boost configuration):**

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.385 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times (V_{LED} - 2 \times V_{IN\_MIN}) \times 3}$$

**Equation 23: (for SEPIC and coupled-inductor configurations):**

$$R_{CS} = \frac{4 \times L_{MIN} \times f_{SW} \times 0.385 \times 0.9}{I_{LP} \times 4 \times L_{MIN} \times f_{SW} + D_{MAX} \times (V_{LED} - V_{IN\_MIN}) \times 3}$$

where 0.385 is the minimum value of the peak current-sense threshold. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold of 0.385 is multiplied by 0.9 to take tolerances into account.

### Output Capacitor Selection

For all three converter topologies, the output capacitor supplies the load current when the main switch is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across the constant-current sink outputs because the LED-string voltages are stable due to the constant current. For the MAX25014, limit peak-to-peak output-voltage ripple to 200mV to get stable output current.

The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESR and ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise during PWM dimming, the amount of ceramic capacitors on the output is usually minimized. In this case, an additional electrolytic or aluminum organic polymer capacitor can provide most of the bulk capacitance.

### External Switching-MOSFET Selection

The external switching MOSFET should have a voltage rating sufficient to withstand the maximum boost output voltage, together with the rectifier diode drop and any possible overshoot due to ringing caused by parasitic inductance and capacitance. The recommended MOSFET VDS voltage rating is 30% higher than the sum of the maximum output voltage and the rectifier diode drop.

The continuous-drain current rating of the MOSFET ( $I_D$ ), when the case temperature is at the maximum operating ambient temperature, should be greater than that calculated below,

**Equation 24:**

$$I_{DRMS} = \left( \sqrt{I_{L\_AVG}^2 \times D_{MAX}} \right) \times 1.3$$

The MOSFET dissipates power due to both switching losses and conduction losses. Use the following equation to calculate the conduction losses in the MOSFET

**Equation 25:**

$$P_{COND} = I_{L\_AVG}^2 \times D_{MAX} \times R_{DS(ON)}$$

where  $R_{DS(ON)}$  is the on-state drain-to-source resistance of the MOSFET. Use the following equation to calculate the switching losses in the MOSFET.

**Equation 26:**

$$P_{SW} = \frac{I_{L\_AVG} \times V_{LED}^2 \times C_{GD} \times f_{SW}}{2} \times \left( \frac{1}{I_{GON}} + \frac{1}{I_{GOFF}} \right)$$

where  $I_{GON}$  and  $I_{GOFF}$  are the gate currents of the MOSFET in amperes when it is turned on and turned off, respectively.  $C_{GD}$  is the gate-to-drain MOSFET capacitance in farads.



**Rectifier Diode Selection**

Using a Schottky rectifier diode produces less forward drop and puts the least burden on the MOSFET during reverse recovery. A diode with considerable reverse-recovery time increases the MOSFET switching loss. Select a Schottky diode with a voltage rating 20% higher than the maximum boost-converter output voltage and current rating greater than that shown below.

**Equation 27:**

$$I_{L\_AVG} \times (1 - D_{MAX}) \times 1.2$$

**Feedback Compensation**

During normal operation, the feedback control loop regulates the minimum OUT\_ voltage to fall within the window comparator limits of 0.78V and 1.03V when LED string currents are enabled during PWM dimming. When LED currents are off during PWM dimming, the control loop turns off the converter and stores the previous boost output-voltage value for use during the next on cycle.

The switching converter small-signal-transfer function has a right-half plane (RHP) zero in the boost configuration if the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate.

**Equation 28: (worst-case RHP zero frequency (f<sub>ZRHP</sub>) is calculated using):**

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED}}$$

**Equation 29: (for the SEPIC and coupled-inductor configurations):**

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2 \times \pi \times L \times I_{LED} \times D_{MAX}}$$

The standard way to avoid this zero is to roll off the loop gain to 0dB at a frequency of less than 1/5 of the RHP zero frequency with a -20dB/decade slope.

The switching converter small-signal transfer function also has an output pole. The effective output impedance, together with the output filter capacitance, determines the output pole frequency (f<sub>P1</sub>) that is calculated for the boost configuration, as shown in the following equation.

**Equation 30:**

$$f_{P1} = \frac{I_{LED}}{\pi \times V_{LED} \times C_{OUT}}$$

**Equation 31: (for SEPIC and coupled-inductor use this formula:**

$$f_{P1} = \frac{I_{LED} \times D_{MAX}}{\pi \times V_{LED} \times C_{OUT}}$$

Compensation components R<sub>COMP</sub> and C<sub>COMP</sub> perform two functions. C<sub>COMP</sub> introduces a low-frequency pole that presents a -20dB/decade slope to the loop gain. R<sub>COMP</sub> flattens the gain of the error amplifier for frequencies above the zero formed by R<sub>COMP</sub> and C<sub>COMP</sub>. For compensation, this zero is placed at f<sub>P1</sub> to provide a -20dB/decade slope for frequencies above f<sub>P1</sub> to the combined modulator and compensator response.

The value of R<sub>COMP</sub> needed to fix the total loop gain at f<sub>P1</sub> so the total loop gain crosses 0dB with -20dB/decade slope at 1/5 the RHP zero frequency, is calculated for the boost configuration below.

**Equation 32:**

$$R_{COMP} = \frac{f_{ZRHP} \times R_{CS} \times I_{LED} \times A_{OVP}}{5 \times f_{P1} \times GM_{COMP} \times V_{LED} \times (1 - D_{MAX})}$$

**Equation 33: (for SEPIC and coupled-inductor buck-boost configurations):**

$$R_{\text{COMP}} = \frac{f_{\text{ZRHP}} \times R_{\text{CS}} \times I_{\text{LED}} \times A_{\text{OVP}} \times D_{\text{MAX}}}{5 \times f_{\text{P1}} \times \text{GM}_{\text{COMP}} \times V_{\text{LED}} \times (1 - D_{\text{MAX}})}$$

where:

- $R_{\text{COMP}}$  = Compensation resistor in  $\Omega$
- $A_{\text{OVP}}$  = BSTMON resistor-divider gain (a value  $\gg 1$ )
- $R_{\text{CS}}$  = Current-sense resistor in  $\Omega$
- $\text{GM}_{\text{COMP}}$  = Transconductance of the error amplifier (600 $\mu$ S)

The value of  $C_{\text{COMP}}$  is calculated as shown below.

**Equation 34:**

$$C_{\text{COMP}} = \frac{1}{2 \times \pi \times f_{\text{Z1}} \times R_{\text{COMP}}}$$

where  $f_{\text{Z1}}$  is the compensation zero placed at 1/5 the crossover frequency, which is, in turn, set at 1/5 the  $f_{\text{ZRHP}}$ . If the output capacitors do not have low ESR, the ESR zero frequency could fall below the 0dB crossover frequency. An additional pole may be required to cancel out this zero placed at the same frequency. This can be added by connecting a capacitor from the COMP pin directly to GND with a value shown below.

**Equation 35:**

$$C_{\text{PAR}} = \text{GM}_{\text{COMP}} \times R_{\text{ESR}} \times C_{\text{OUT}}$$

where  $R_{\text{ESR}}$  is the capacitor ESR value and  $C_{\text{OUT}}$  is the output-capacitor value.

### External Disconnect-MOSFET Selection

An external nMOSFET can be used to disconnect the boost output from the battery in the event of an output overload or short condition. In the case of the SEPIC or buck-boost, this protection is not necessary so there is no need for the nMOSFET. Leave the NGATE pin unconnected when an external nMOSFET is not used and set the CP\_DIS bit to 1. If it is necessary to have output-short protection for the boost even at power-up, then the current through the nMOSFET (refer to the MAX25014EVKIT for a reference circuit) has to be sensed. Once the current-sense voltage exceeds a certain threshold, it should limit the input current to the programmed threshold. This threshold should be set at a sufficiently high level so it never trips at startup or under normal operating conditions. Check the safe operating area (SOA) of the nMOSFET so the current-limit-trip threshold and voltage on the MOSFET do not exceed the limits of the SOA curve of the nMOSFET at the highest operating temperature.

Ensure that the maximum value of the nMOSFET gate threshold voltage is lower than 4V for reliable operation.

### V<sub>OUT</sub> to OUT\_ Bleed Resistors

The OUT\_ pins have a leakage specification of 15 $\mu$ A (max) in cases where all OUT\_ pins are shorted to 48V (see  $I_{\text{OUTLEAK}}$  in the [Electrical Characteristics](#) table). This leakage current is dependent on the OUT\_ voltage and is higher at higher voltages. Therefore, in cases where large numbers of LEDs are connected in series, a 100k $\Omega$  (or larger) bleed resistor can be placed in parallel with the LED string to prevent the OUT\_ leakage current from very dimly turning on the LEDs, even when the DIM signal is low (see resistors R8–R11 in the [Typical Application Circuit](#)).

### Thermal Considerations

The on-chip power dissipation of the MAX25014 comprises three main factors:

1. Current-sink power loss:  $1.1\text{V} \times I_{\text{LED}}$
2. Device operating current power loss:  $V_{\text{IN}} \times 11\text{mA}$
3. Gate-drive current for the external MOSFET:  $V_{\text{IN}} \times Q_{\text{gd}} \times f_{\text{SW}}$ , where  $Q_{\text{gd}}$  is the total gate charge of the selected MOSFET and  $f_{\text{SW}}$  is the switching frequency.

Calculate the total power dissipation by adding the two values calculated above. The junction temperature at the maximum ambient temperature can then be calculated as follows.

**Equation 37:**

$$T_J = T_A + P_{TOT} \times \theta_{JA}$$

where  $T_A$  is the ambient temperature and  $\theta_{JA}$  is the junction-to-ambient thermal resistance of the package (36°C/W on a four-layer board). Ensure that the junction temperature does not exceed 150°C.

As an example, consider an application with an operating voltage of 14V and a total output current of 600mA. The selected MOSFET has a total gate charge of 5nC and the switching frequency is 400kHz. The total power dissipation is shown in the following equation.

**Equation 38:**

$$P_{TOT} = 1.1 \times 0.4 + 14 \times 0.011 + 14 \times 5\text{nC} \times 400000 = 0.622\text{W}$$

The maximum junction temperature at an ambient temperature of 85°C is shown in the following equation.

**Equation 39:**

$$T_J = 85 + 0.622 \times 36 = 107^\circ\text{C}$$

### PCB Layout Considerations

LED driver circuits based on the MAX25014 use a high-frequency switching converter to generate the voltage for LED strings. Take proper care while laying out the circuit to ensure correct operation. The switching-converter portion of the circuit has nodes with very fast voltage changes that could lead to undesirable effects on the sensitive parts of the circuit. Follow the guidelines below to reduce noise as much as possible:

- Connect the IREF resistor to the IREF pin using the shortest possible trace to avoid noise pickup.
- Connect the bypass capacitor on  $V_{CC}$  as close as possible to the device and connect the capacitor ground to the analog ground plane using vias close to the capacitor terminal. Connect the GND of the device to the analog ground plane using a via placed close to GND. Lay the analog ground plane on the inner layer, preferably next to the top layer. Use the analog ground plane to cover the entire area under critical signal components for the power converter.
- Have a power-ground plane for the switching-converter power circuit under the power components (i.e., input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power-ground plane closest to PGND. Connect all other ground connections to the power ground plane using vias placed close to the terminals.
- There are two loops in the power circuit that carry high-frequency switching currents. One loop is when the MOSFET is on (from the input filter capacitor positive terminal, through the inductor, the internal MOSFET and the current-sense resistor, to the input capacitor negative terminal). The other loop is when the MOSFET is off (from the input capacitor positive terminal, through the inductor, the rectifier diode, output filter capacitor, to the input capacitor negative terminal). Analyze these two loops and make the loop areas as small as possible. Wherever possible, have a return path on the power ground plane for the switching currents on the top layer copper traces, or through power components. This reduces the loop area considerably and provides a low-inductance path for the switching currents. Reducing the loop area also reduces radiation during switching.
- Connect the power-ground plane for the constant-current LED-driver portion of the circuit to LEDGND as close as possible to the device. Connect GND to PGND at the same point.
- Add a small bypass capacitor (22pF to 47pF) to the BSTMON input. Place the capacitor as close as possible to the pin to suppress high-frequency noise.
- Boost output voltage for the LED strings should be taken directly from the output capacitors and not from the boost diode anode.
- Input and output capacitors need good grounding with wide traces and multiple vias to the ground plane.
- See [Figure 4](#) for a symbolic sample layout of the power section.

Sample Layout

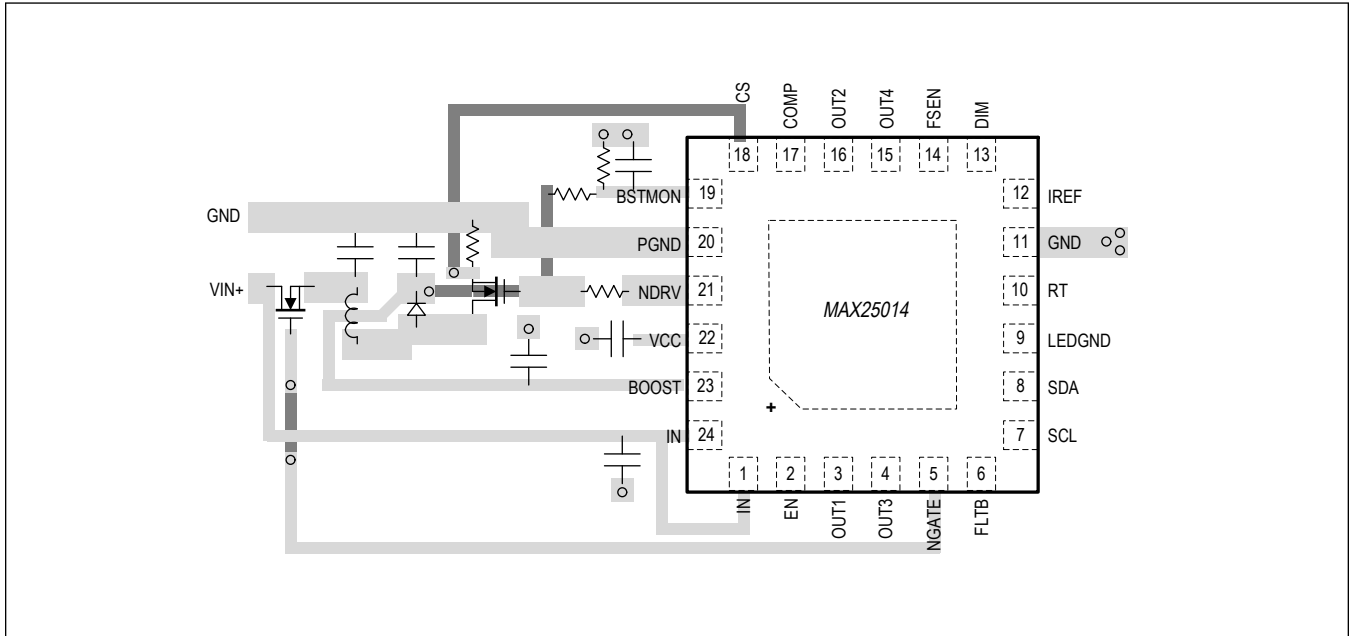
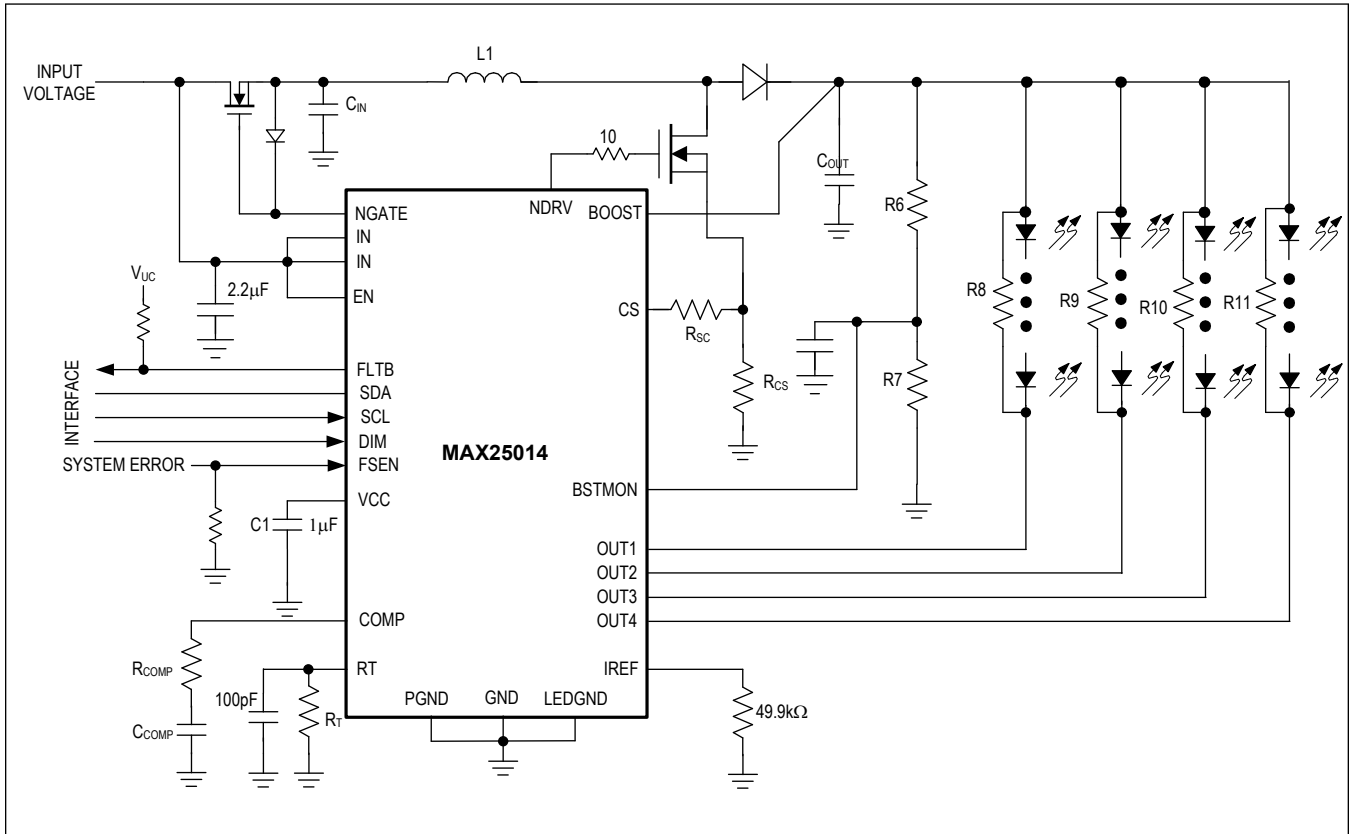


Figure 4. Sample Layout

Typical Application Circuits

MAX25014 Applications Circuit



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX25014ATG/V+	-40°C to +125°C	24 TQFN-EP*
MAX25014ATG/VY+	-40°C to +125°C	24 SWTQFN-EP*

List all notes at the end of the table on each page if the table runs onto more than one page:

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

Y = Side-wettable package.

\*EP = Exposed pad.

MAX25014

Automotive Low Input Voltage I<sup>2</sup>C 4-Channel  
150mA Backlight Driver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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