MAX25205 Gesture Sensor for Automotive Applications

General Description

The MAX25205 is a low-cost data-acquisition system for gesture and proximity sensing. The MAX25205 recognizes the following independent gestures:

- Hand swipe gestures (left, right, up, and down)
- Finger and hand rotation (CW and CCW)
- Proximity detection

The proximity, hand detection, and gesture recognition functions of the MAX25205 operate by detecting the light reflected from the controlled IR-LED light source with an integrated 6x10-element optical sensor array. The MAX25205 can detect these gestures even when exposed to bright ambient light. A low-power, low-cost CPU, such as the MAX32630, is required to process the data from the sensor.

This discrete light source is created externally with one or more FETs driven directly from the MA25205. The light source's PWM duty cycle is programmable from 1/16 to 16/16. The LEDs are pulsed on one or more times in a programmable sequence that is repeated for every sample.

For flexibility, the MAX25205 supports two different serial communication protocols: I^2C (400kHz) and SPI (6MHz).

The MAX25205 is available in a 4mm x 4mm, 20-pin, optical QFN package.

Applications

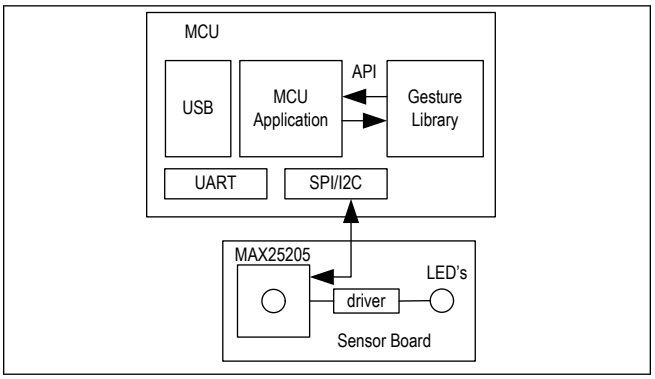
- Central Information Display Control
- Rear-Seat Entertainment Systems
- Door, Moon Roof, and Trunk Control
- Mechanical Switch Replacement
- Occupant Detection

Benefits and Features

- Low-Cost, Flexible Gesture-Sensing Solution for Automotive Applications
- Low-Power, Low-Cost External CPU Processes Sensor Output
- Supports Swipe, Rotation, and Proximity Gestures
- Highly Integrated
  - 60-Pixel IR Photodiode Array
  - Integrated LED Driver
  - 400kHz I^2C and 6MHz SPI Serial Interfaces
- Operates in 120k Lux Ambient Light
- AEC-Q100 Qualified
  - -40°C to +85°C Operation
  - MSL1
- Ultra-Low-Power Operation
  - 1mA at 3.3V
- Compact 4mm x 4mm x 1.35mm, 20-Pin, Side-Wettable QFN Package

Ordering Information appears at end of datasheet.

Simplified System Diagram



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LDO_OUT to GND..... -0.3V to 2.2V
V_{DD} to GND..... -0.3V to 2.2V
V_{DDIO} to GND ..... -0.3V to 6V
CS, SCL, SDA, $\overline{INT}$, SYNC, SEL to GND . -0.3V to V_{DDIO} + 0.3V
DOUT, ELED to GND ..... -0.3V to V_{DDIO} + 0.3V

Short-Circuit Between DRV and GND ..... Continuous
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 39.8 mW/°C above +70°C.) ..... 0mW to 2191mW
Operating Temperature Range ..... -40°C to 85°C
Operating Junction Temperature ..... +125°C
Storage Temperature Range ..... -40°C to +150°C
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Lead Temperature (soldering, 10s)..... 300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

4mm x 4mm QFN

Package Code	Q2044Y+2
Outline Number	21-100404
Land Pattern Number	90-100083
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25.1 (C/W)
Junction to Case (θ_{JC})	4.7 (C/W)

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(MAX25205 Typical Application Circuit, V_{DDIO} = 1.7V to 5.5V, LDO_IN = 2.7V to 5.5V, V_{LED} = 2.7V to 3.6V, LDO_OUT connected to V_{DD}. T_A = -40°C to +85°C. Typ values: V_{DDIO} = 3.3V, LDO_IN = 3.3V, V_{LED} = 3.3V, T_A = +25°C. (Note 1) Default register settings (Note 3).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
LDO_IN Supply Voltage	LDO IN	*Note 2*	2.7	3.3	5.5	V
LDO_OUT Supply Voltage	LDO_OUT		1.7	1.8	2.0	V
V_{DD} Supply Voltage	V_{DD}	*Note 2*	1.7	1.8	2.0	V
Logic Supply Voltage	V_{DDIO}	*Note 2*	1.7	3.3	5.5	V
LDO_IN Current	I_{LDO_IN}	LDO_OUT connected to V_{DD}.		0.8		mA
Shutdown Current	I_{SHDN}	Register 0x02 Bit 7 = 1		6		µA
Power-Up Time	T_{ON}	*Note 4*, V_{LDO_OUT} = V_{DD} = 1.7V, V_{LDO_IN} = V_{DDIO} = 2.7V		6		ms

Electrical Characteristics (continued)

(MAX25205 Typical Application Circuit, V_{DDIO} = 1.7V to 5.5V, LDO_IN = 2.7V to 5.5V, V_{LED} = 2.7V to 3.6V, LDO_OUT connected to V_{DD}. T_A = -40°C to +85°C. Typ values: V_{DDIO} = 3.3V, LDO_IN = 3.3V, V_{LED} = 3.3V, T_A = +25°C. (Note 1) Default register settings (Note 3).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IR LED DRIVER							
LED Current	I_{LED}	DRV Voltage = 1.8V	DRV[3:0] = 0000		0		mA
			DRV[3:0] = 0001		13.3		
			DRV[3:0] = 0010		26.7		
			DRV[3:0] = 0011		40		
			DRV[3:0] = 0100		53.3		
			DRV[3:0] = 0101		66.7		
			DRV[3:0] = 0110		80		
			DRV[3:0] = 0111		93.3		
			DRV[3:0] = 1000		106.7		
			DRV[3:0] = 1001		120		
			DRV[3:0] = 1010		133.3		
			DRV[3:0] = 1011		146.7		
			DRV[3:0] = 1100		160		
			DRV[3:0] = 1101		173.3		
			DRV[3:0] = 1110		186.7		
			DRV[3:0] = 1111	180	200	220	
LED Current Accuracy		I_{LED} = 200mA, V_{DRV} = 0.8V to 3.6V		-10		10	%
IR RECEIVER CHARACTERISTICS							
Optical Response		External 940nm collimated light source with irradiance = 175 µW/cm^2. ADC full scale = 16384 counts. Optical response is the average response of the center four pixels. *Note 5*			8000		Counts
DIGITAL CHARACTERISTICS							
Output Low-Voltage SDA, $\overline{INT}$	V_{OL}	I_{SINK} = 6mA, open-drain outputs				0.4	V
Output Low-Voltage DOUT, SYNC, ELED	V_{OL}	I_{SINK} = 1mA, CMOS outputs				0.4	V
Output High Voltage DOUT, SYNC, ELED	V_{OH}	I_{SOURCE} = 1mA, CMOS outputs		0.75 x V_{DDIO}			V
Leakage Current						1.0	µA
Input Low Voltage SDA/ DIN, SCL, SEL, $\overline{CS}$, SYNC	V_{IL}					0.3 x V_{DDIO}	V
Input High Voltage SDA/ DIN, SCL, SEL, $\overline{CS}$, SYNC	V_{IH}			0.7 x V_{DDIO}			V
Input Capacitance					3		pF

Electrical Characteristics (continued)

(MAX25205 Typical Application Circuit, V_{DDIO} = 1.7V to 5.5V, LDO_IN = 2.7V to 5.5V, V_{LED} = 2.7V to 3.6V, LDO_OUT connected to V_{DD}. T_A = -40°C to +85°C. Typ values: V_{DDIO} = 3.3V, LDO_IN = 3.3V, V_{LED} = 3.3V, T_A = +25°C. (Note 1) Default register settings (Note 3).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Oscillator Frequency			2.5	2.56	2.62	MHz
I²C TIMING CHARACTERISTICS SDA, SCL						
I²C Clock Rate	f_{SCL}	*Note 2*			400	kHz
SCL Pulse Width	t_{LOW}	*Note 4*	1.3			µs
	t_{HIGH}	*Note 4*	0.6			
Data Hold Time	t_{HD}	*Note 4*	0		900	ns
Data Setup Time	t_{SU}	*Note 4*	100			ns
SPI TIMING CHARACTERISTICS $\overline{CS}$, SCL, DIN and DOUT						
SCL Frequency	f_{CLK}	*Note 2*			6	MHz
SCL Pulse Width High	t_{CH}	*Note 4*	75			ns
SCL Pulse Width Low	t_{CL}	*Note 4*	75			ns
$\overline{CS}$ Fall to SCL Rise Setup Time	t_{CSS}	*Note 4*	25			ns
DIN to SCL Rise Setup Time	t_{DS}	*Note 4*	20			ns
DIN to SCL Rise Hold Time	t_{DH}	*Note 4*	10			ns

Note 1: Limits are 100% tested at T_A = +25°C and T_A = +85°C. Operation at T_A = -40°C is guaranteed by design and characterization.

Note 2: Condition of production test.

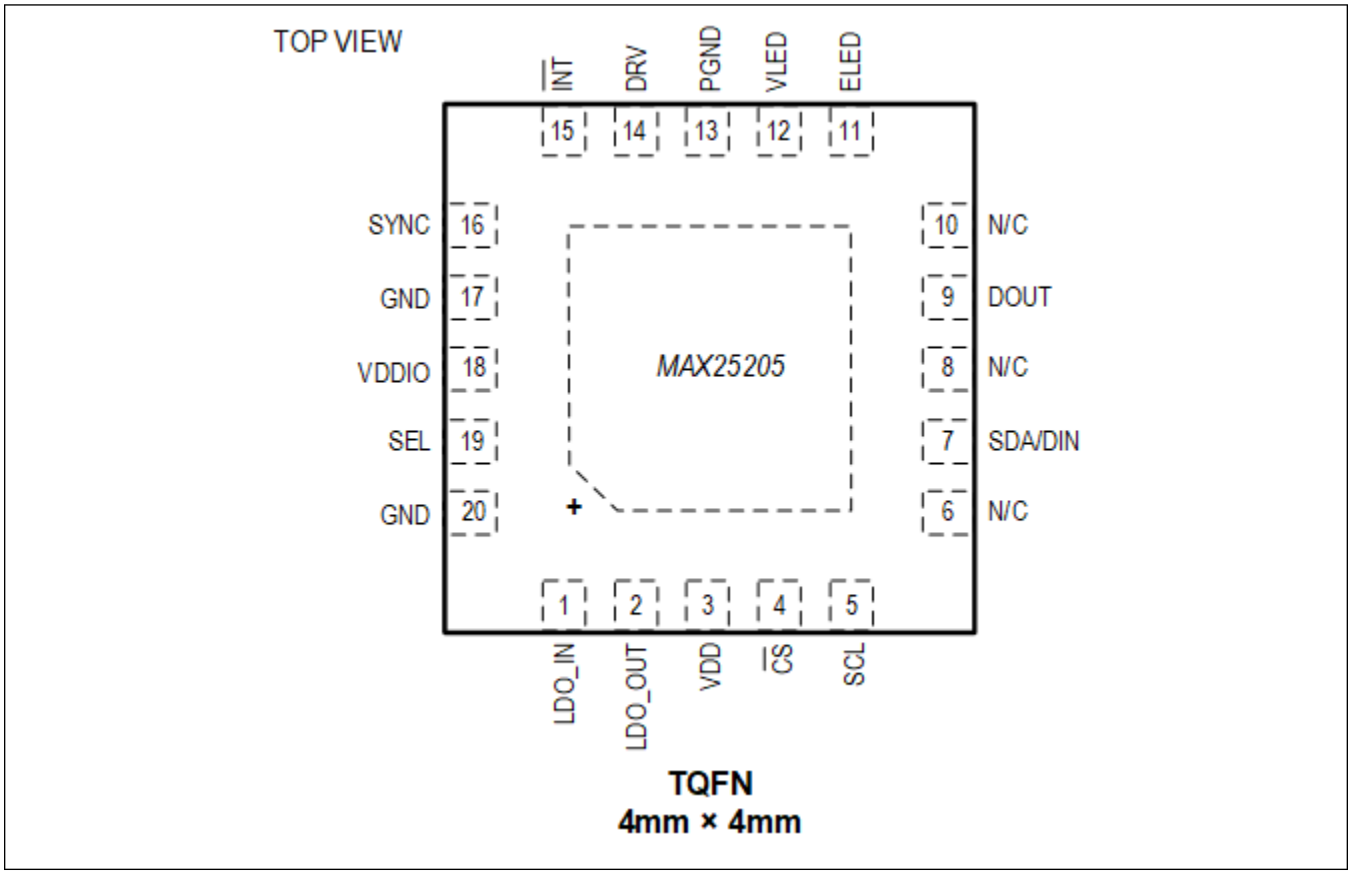
Note 3: Default register settings 0x01 = 0x04, 0x02 = 0x02, 0x03 = 0x04, 0x04 = 0xAC, 0x05 = 0x08, 0x06 = 0x0A, 0xC1 = 0x0A, 0xA5 = 0x88, 0xA5 = 0x88, 0xA6 = 0x88, 0xA7 = 0x88, 0xA8 = 0x88, 0xA9 = 0x88.

Note 4: Not production tested. Guaranteed by design and characterization.

Note 5: Count up A, eliminate B mode. Default register setting with the following exceptions: 0x04 = 0xAE, 0x05 = 0x00.

Pin Configuration

MAX25205



Pin Description

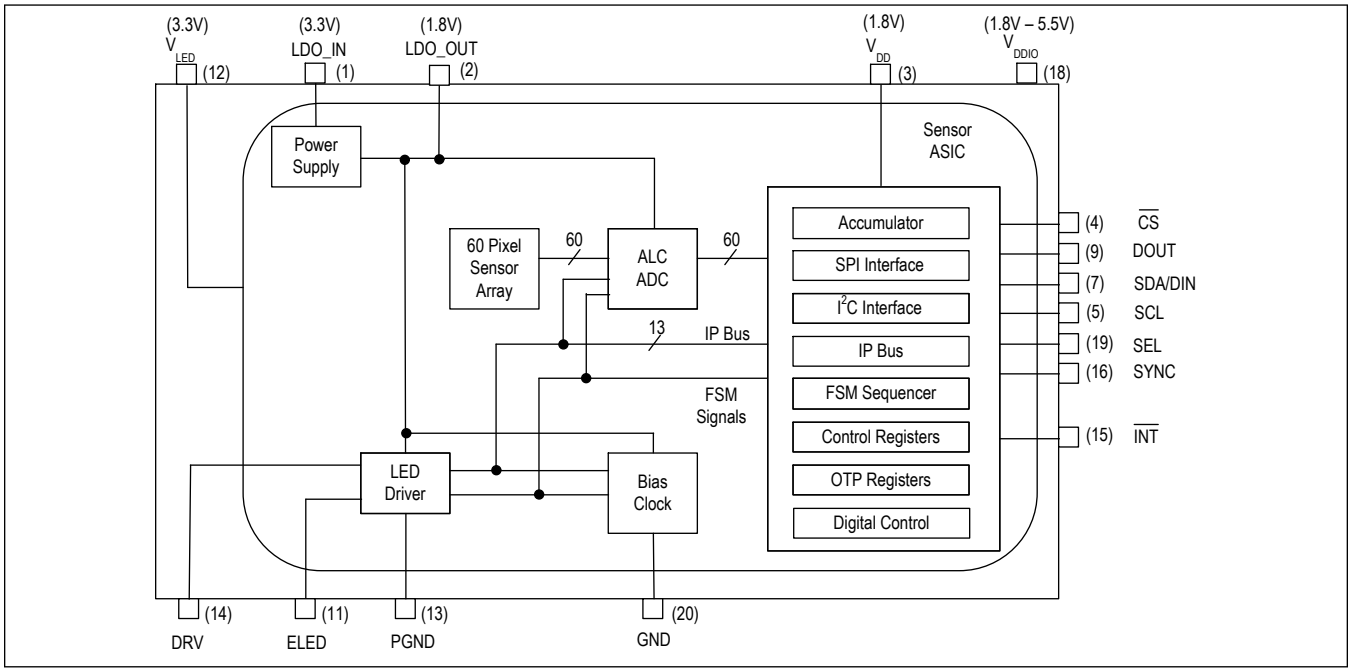
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
1	LDO_IN	Connect to low-noise (V_N <150mV_{PP}) 3.3V supply through a 390Ω resistor. Bypass with at least a 2.2µF ceramic capacitor. See *Typical Application Circuits*.	3.3V	Power
2	LDO_OUT	Bypass with a 1.0µF ceramic capacitor. See *Typical Application Circuits*. Connect to V_{DD} (Pin 3).	1.8V	Regulated Output
3	V_{DD}	Connect to LDO_OUT(Pin 2). V_{DD} is the supply for the internal digital circuitry.	1.8V	Power
4	$\overline{CS}$	SPI Chip Select/I²C Address Select $\overline{CS}$ = 0: Write Address 9E, Read Address 9F $\overline{CS}$ = 1: Write Address A0, Read Address A1	V_{DDIO}	Input

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
5	SCL	I^2C Serial Clock. For I^2C operation, pull up to V_{DDIO} with 4.7kΩ.	V_{DDIO}	Input
6, 8, 10	NC	Connect to ground.		No Connect
7	SDA/DIN	When the SEL pin is connected to V_{DD}, Pin 7 becomes SDA for I^2C communication. When the SEL pin is connected to GND, Pin 7 becomes DIN or SPI communication. For I^2C operation, pull SDA up to V_{DDIO} with 4.7kΩ.	V_{DDIO}	Input/Output
9	DOUT	SPI Data Out	V_{DDIO}	Output
11	ELED	External LED CMOS Level Voltage PWM Drive Output. This pin drives the gate of either a p-channel FET or an n-channel FET. A resistor in series with the FET's drain limits the maximum pulse current supplied to the external LED. ELED output level for a logic low is 0V and for a logic high is V_{DDIO}. **Note**: When using a 1.8V V_{DDIO}, a MOSFET with very low threshold voltage (V_{TH}<1V), should be used to ensure minimal $R_{DS(ON)}$.	V_{DDIO}	Output
12	V_{LED}	ESD Protection for DRV Pin. Internal protection diodes clamp negative pulses to ground and positive pulses to the same supply used to supply the external LED. Bias V_{LED} at 3.3V for typical applications. If the DRV pin is not used, it should be grounded to PGND.	V_{LED}	Power
13	PGND	LED driver ground when DRV pin is used to drive LED		GND
14	DRV	Direct LED Current Drive. When the MAX25205 is configured for direct LED drive, connect the DRV pin to the cathode of the LED. Connect the LED's anode to the LED supply to V_{LED} for ESD protection. When external current drive is not used, DRV should be grounded along with the V_{LED} pin.	VLED	Output
15	$\overline{INT}$	Interrupt Signal. At the end of a conversion sample sequence, the $\overline{INT}$ pin goes low. The host µP can monitor this pin to determine when the ADC output registers are ready to be read. $\overline{INT}$ pin should be pulled up with a 4.7kΩ resistor to V_{DDIO}. The status register 0x00 must be read once for the $\overline{INT}$ pin to become active.	V_{DDIO}	Input/Output
16	SYNC	External Synchronization Pin. Driving SYNC with a controlled logic signal prevents simultaneous flashing of LEDs in systems configured with two MAX25205 sensors.	V_{DDIO}	Input/Output
18	V_{DDIO}	Digital I/O Supply Pin. The digital I/O is compatible with 1.8V, 3.3V, or 5V CMOS logic levels.	V_{DDIO}	Power
19	SEL	Serial Interface Mode Select: SEL = V_{DD}: I^2C SEL = GND: SPI	V_{DDIO}	Input
17, 20	GND	Ground		GND
EP	Backside Paddle	This pin must be connected to ground.		Backside Paddle

Functional Diagrams

Block Diagram



Detailed Description

The proximity, hand-detection, and gesture-recognition functions are achieved by detecting the light reflected from the controlled IR-LED light source while rejecting ambient light. An integrated 6x10-element optical sensor array performs the light measurements. This discrete light source is created externally with one or more FETs driven directly from the MA25205. The light source's PWM duty cycle is programmable from 1/16 to 16/16. The LEDs are pulsed on one or more times in a programmable sequence. This pulse sequence is repeated for every sample. A low-power, low-cost CPU such as the MAX32630 is required to process the data from the sensor.

Recommended Operating Conditions

Table 1. Recommended Operating Conditions

PARAMETER	PIN NAME	MIN	TYP	MAX	UNIT
Supply Range	LDO_IN	2.7	3.3	5.5	V
	V_{DD}	1.7	1.8	2	
	V_{DDIO}	1.7	3.3	5.5	
Bias Range	V_{LED}	2.7	3.3	3.6	
Maximum Supply Noise	LDO_IN		150		mV_{P-P}
	V_{DD}		50		

Register Map

MAX25205

ADDRESS	NAME	MSB							LSB
STATUS									
0x00	INTERRUPT STATUS[7:0]	–	–	–	PWRON	–	EOCINTS	–	–
CONFIGURATION									
0x01	MAIN CONFIGURATION 1[7:0]	–	EXSYNC[2:0]			–	EOCINTE	–	–
0x02	MAIN CONFIGURATION 2[7:0]	SHDN	RESET	–	SYNC	OSEN	OSTRIG	–	–
0x03	SEQ CONFIGURATION 1[7:0]	SDLY[3:0]				TIM[2:0]			–
0x04	SEQ CONFIGURATION 2[7:0]	NRPT[2:0]			NCDS[2:0]			CDSMODE	–
0x05	AFE CONFIGURATION[7:0]	–	ALC_COARSE	–	–	ALCEN	–	PGA[1:0]	
0x06	LED CONFIGURATION[7:0]	–	–	–	–	DRV[3:0]			
ADC									
0x10	ADC00H[7:0]	–	–	–	–	–	–	–	–
0x11	ADC00L[7:0]	–	–	–	–	–	–	–	–
0x12	ADC01H[7:0]	–	–	–	–	–	–	–	–
0x13	ADC01L[7:0]	–	–	–	–	–	–	–	–
0x14	ADC02H[7:0]	–	–	–	–	–	–	–	–
0x15	ADC02L[7:0]	–	–	–	–	–	–	–	–
0x16	ADC03H[7:0]	–	–	–	–	–	–	–	–
0x17	ADC03L[7:0]	–	–	–	–	–	–	–	–
0x18	ADC04H[7:0]	–	–	–	–	–	–	–	–
0x19	ADC04L[7:0]	–	–	–	–	–	–	–	–
0x1A	ADC05H[7:0]	–	–	–	–	–	–	–	–
0x1B	ADC05L[7:0]	–	–	–	–	–	–	–	–
0x1C	ADC06H[7:0]	–	–	–	–	–	–	–	–
0x1D	ADC06L[7:0]	–	–	–	–	–	–	–	–
0x1E	ADC07H[7:0]	–	–	–	–	–	–	–	–
0x1F	ADC07L[7:0]	–	–	–	–	–	–	–	–
0x20	ADC08H[7:0]	–	–	–	–	–	–	–	–
0x21	ADC08L[7:0]	–	–	–	–	–	–	–	–
0x22	ADC09H[7:0]	–	–	–	–	–	–	–	–
0x23	ADC09L[7:0]	–	–	–	–	–	–	–	–
0x24	ADC10H[7:0]	–	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0x25	ADC10L[7:0]	–	–	–	–	–	–	–	–
0x26	ADC11H[7:0]	–	–	–	–	–	–	–	–
0x27	ADC11L[7:0]	–	–	–	–	–	–	–	–
0x28	ADC12H[7:0]	–	–	–	–	–	–	–	–
0x29	ADC12L[7:0]	–	–	–	–	–	–	–	–
0x2A	ADC13H[7:0]	–	–	–	–	–	–	–	–
0x2B	ADC13L[7:0]	–	–	–	–	–	–	–	–
0x2C	ADC14H[7:0]	–	–	–	–	–	–	–	–
0x2D	ADC14L[7:0]	–	–	–	–	–	–	–	–
0x2E	ADC15H[7:0]	–	–	–	–	–	–	–	–
0x2F	ADC15L[7:0]	–	–	–	–	–	–	–	–
0x30	ADC16H[7:0]	–	–	–	–	–	–	–	–
0x31	ADC16L[7:0]	–	–	–	–	–	–	–	–
0x32	ADC17H[7:0]	–	–	–	–	–	–	–	–
0x33	ADC17L[7:0]	–	–	–	–	–	–	–	–
0x34	ADC18H[7:0]	–	–	–	–	–	–	–	–
0x35	ADC18L[7:0]	–	–	–	–	–	–	–	–
0x36	ADC19H[7:0]	–	–	–	–	–	–	–	–
0x37	ADC19L[7:0]	–	–	–	–	–	–	–	–
0x38	ADC20H[7:0]	–	–	–	–	–	–	–	–
0x39	ADC20L[7:0]	–	–	–	–	–	–	–	–
0x3A	ADC21H[7:0]	–	–	–	–	–	–	–	–
0x3B	ADC21L[7:0]	–	–	–	–	–	–	–	–
0x3C	ADC22H[7:0]	–	–	–	–	–	–	–	–
0x3D	ADC22L[7:0]	–	–	–	–	–	–	–	–
0x3E	ADC23H[7:0]	–	–	–	–	–	–	–	–
0x3F	ADC23L[7:0]	–	–	–	–	–	–	–	–
0x40	ADC24H[7:0]	–	–	–	–	–	–	–	–
0x41	ADC24L[7:0]	–	–	–	–	–	–	–	–
0x42	ADC25H[7:0]	–	–	–	–	–	–	–	–
0x43	ADC25L[7:0]	–	–	–	–	–	–	–	–
0x44	ADC26H[7:0]	–	–	–	–	–	–	–	–
0x45	ADC26L[7:0]	–	–	–	–	–	–	–	–
0x46	ADC27H[7:0]	–	–	–	–	–	–	–	–
0x47	ADC27L[7:0]	–	–	–	–	–	–	–	–
0x48	ADC28H[7:0]	–	–	–	–	–	–	–	–
0x49	ADC28L[7:0]	–	–	–	–	–	–	–	–
0x4A	ADC29H[7:0]	–	–	–	–	–	–	–	–
0x4B	ADC29L[7:0]	–	–	–	–	–	–	–	–
0x4C	ADC30H[7:0]	–	–	–	–	–	–	–	–
0x4D	ADC30L[7:0]	–	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0x4E	ADC31H[7:0]	–	–	–	–	–	–	–	–
0x4F	ADC31L[7:0]	–	–	–	–	–	–	–	–
0x50	ADC32H[7:0]	–	–	–	–	–	–	–	–
0x51	ADC32L[7:0]	–	–	–	–	–	–	–	–
0x52	ADC33H[7:0]	–	–	–	–	–	–	–	–
0x53	ADC33L[7:0]	–	–	–	–	–	–	–	–
0x54	ADC34H[7:0]	–	–	–	–	–	–	–	–
0x55	ADC34L[7:0]	–	–	–	–	–	–	–	–
0x56	ADC35H[7:0]	–	–	–	–	–	–	–	–
0x57	ADC35L[7:0]	–	–	–	–	–	–	–	–
0x58	ADC36H[7:0]	–	–	–	–	–	–	–	–
0x59	ADC36L[7:0]	–	–	–	–	–	–	–	–
0x5A	ADC37H[7:0]	–	–	–	–	–	–	–	–
0x5B	ADC37L[7:0]	–	–	–	–	–	–	–	–
0x5C	ADC38H[7:0]	–	–	–	–	–	–	–	–
0x5D	ADC38L[7:0]	–	–	–	–	–	–	–	–
0x5E	ADC39H[7:0]	–	–	–	–	–	–	–	–
0x5F	ADC39L[7:0]	–	–	–	–	–	–	–	–
0x60	ADC40H[7:0]	–	–	–	–	–	–	–	–
0x61	ADC40L[7:0]	–	–	–	–	–	–	–	–
0x62	ADC41H[7:0]	–	–	–	–	–	–	–	–
0x63	ADC41L[7:0]	–	–	–	–	–	–	–	–
0x64	ADC42H[7:0]	–	–	–	–	–	–	–	–
0x65	ADC42L[7:0]	–	–	–	–	–	–	–	–
0x66	ADC43H[7:0]	–	–	–	–	–	–	–	–
0x67	ADC43L[7:0]	–	–	–	–	–	–	–	–
0x68	ADC44H[7:0]	–	–	–	–	–	–	–	–
0x69	ADC44L[7:0]	–	–	–	–	–	–	–	–
0x6A	ADC45H[7:0]	–	–	–	–	–	–	–	–
0x6B	ADC45L[7:0]	–	–	–	–	–	–	–	–
0x6C	ADC46H[7:0]	–	–	–	–	–	–	–	–
0x6D	ADC46L[7:0]	–	–	–	–	–	–	–	–
0x6E	ADC47H[7:0]	–	–	–	–	–	–	–	–
0x6F	ADC47L[7:0]	–	–	–	–	–	–	–	–
0x70	ADC48H[7:0]	–	–	–	–	–	–	–	–
0x71	ADC48L[7:0]	–	–	–	–	–	–	–	–
0x72	ADC49H[7:0]	–	–	–	–	–	–	–	–
0x73	ADC49L[7:0]	–	–	–	–	–	–	–	–
0x74	ADC50H[7:0]	–	–	–	–	–	–	–	–
0x75	ADC50L[7:0]	–	–	–	–	–	–	–	–
0x76	ADC51H[7:0]	–	–	–	–	–	–	–	–

ADDRESS	NAME	MSB							LSB
0x77	ADC51L[7:0]	–	–	–	–	–	–	–	–
0x78	ADC52H[7:0]	–	–	–	–	–	–	–	–
0x79	ADC52L[7:0]	–	–	–	–	–	–	–	–
0x7A	ADC53H[7:0]	–	–	–	–	–	–	–	–
0x7B	ADC53L[7:0]	–	–	–	–	–	–	–	–
0x7C	ADC54H[7:0]	–	–	–	–	–	–	–	–
0x7D	ADC54L[7:0]	–	–	–	–	–	–	–	–
0x7E	ADC55H[7:0]	–	–	–	–	–	–	–	–
0x7F	ADC55L[7:0]	–	–	–	–	–	–	–	–
0x80	ADC56H[7:0]	–	–	–	–	–	–	–	–
0x81	ADC56L[7:0]	–	–	–	–	–	–	–	–
0x82	ADC57H[7:0]	–	–	–	–	–	–	–	–
0x83	ADC57L[7:0]	–	–	–	–	–	–	–	–
0x84	ADC58H[7:0]	–	–	–	–	–	–	–	–
0x85	ADC58L[7:0]	–	–	–	–	–	–	–	–
0x86	ADC59H[7:0]	–	–	–	–	–	–	–	–
0x87	ADC59L[7:0]	–	–	–	–	–	–	–	–
CHANNEL GAIN TRIMS									
0xA5	COLUMN GAIN 2, 1[7:0]	CGAIN2[3:0]				CGAIN1[3:0]			
0xA6	COLUMN GAIN 4, 3[7:0]	CGAIN4[3:0]				CGAIN3[3:0]			
0xA7	COLUMN GAIN 6, 5[7:0]	CGAIN6[3:0]				CGAIN5[3:0]			
0xA8	COLUMN GAIN 8, 7[7:0]	CGAIN8[3:0]				CGAIN7[3:0]			
0xA9	COLUMN GAIN 10, 9[7:0]	CGAIN10[3:0]				CGAIN9[3:0]			
LED CONTROL									
0xC1	LED_CTRL[7:0]	–	–	–	–	GAINSEL	DRV_EN	ELED_EN	ELED_POL

Register Details

INTERRUPT STATUS (0x00)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PWRON	–	EOCINTS	–	–
Reset	–	–	–		–		–	–
Access Type	–	–	–	Read Only	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PWRON	4	Power On Reset	PWRON = 1 indicates that a power-up event occurred, either because the part was turned on, or because there was a power-supply voltage glitch. All interrupt threshold settings in the registers are reset to power-on-default states, and should be examined if necessary. The $\overline{INT}$ pin is also pulled low. Once this bit is set, the only way to clear this bit is to read this register. PWRON = 0 indicates normal operation; no interrupt event occurred.
EOCINTS	2	End Of Conversion Interrupt	EOCINTS = 1 indicates that the most recent sample cycle has ended, and the newest ADC values are readable. This bit will be cleared in one of the following ways: - Main Status Register is read. - Any of the four gesture/proximity ADC output registers is read. - A new sample cycle begins. The $\overline{INT}$ pin is also cleared when EOCINTS = 1 This bit is always set to 0 if the EOCINTE bit is set to 0, and the external $\overline{INT}$ will not react to an end of conversion. EOCINTS = 0 indicates that no interrupt trigger event occurred.

MAIN CONFIGURATION 1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	EXSYNC[2:0]			–	EOCINTE	–	–
Reset	–	0b000			–	0b1	–	–
Access Type	–	Write, Read			–	Write, Read	–	–

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td>EXSYNC</td><td>6:4</td><td>External Sync</td><td>The 3 bits of EXSYNC[2:0] control the external synchronization feature of the MAX25205. This is required for the case where two MAX25205 devices are used in a system, and a means is needed to avoid simultaneous flashing of the two LEDs. If the host processor is available to perform this function, then the internal SNYC and one-shot modes described later can be used. If the host processor is not available to coordinate the sample timing, then the two MAX25205 parts in the system must self-coordinate by communicating through the SYNC pin. The 3 bits of EXSYNC control the operation of the SYNC pin for this purpose.

<table>
<tr><th>EXSYNC[2:0]</th><th>Function</th></tr>
<tr><td>000</td><td>The SYNC pin is set to input, but has no function. The customer must tie the pin to a logic-high, low voltage, or to a pulldown or pullup resistor.</td></tr>
<tr><td>001</td><td>The SYNC pin is set to input, and this MAX25205 functions as an LED SYNC slave</td></tr>
<tr><td>010</td><td>The SYNC pin is set to output, and this MAX25205 functions as an LED SYNC master</td></tr>
<tr><td>011</td><td>Same as 000</td></tr>
<tr><td>100</td><td>Same as 000</td></tr>
<tr><td>101</td><td>Same as 000</td></tr>
<tr><td>110</td><td>Same as 000</td></tr>
<tr><td>111</td><td>Same as 000</td></tr>
</table>
</td></tr>
<tr><td>EOCINTE</td><td>2</td><td>End-of-Conversion Interrupt Enable</td><td>ECOINTE = 1 enables the end-of-conversion interrupt. An end-of-conversion event triggers a hardware interrupt in which the $\overline{INT}$ pin is pulled low and EOCINTS bit (register 0x00[2]) is set high.

Note: $\overline{INT}$ is cleared from the active state after six clock cycles if the processor does not clear it first by reading the status register.</td></tr>
</table>

MAIN CONFIGURATION 2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	SHDN	RESET	–	SYNC	OSEN	OSTRIG	–	–
Reset	0b0	0b0	–	0b0	0b0	0b0	–	–
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SHDN	7	Shutdown Control	SHDN = 1 places the MAX25205 into a power-save mode. While all registers remain accessible and retain data, ADC conversion data contained in them are previous values. Writable registers also remain accessible in shutdown. All interrupts are cleared. SHDN = 0 places the MAX25205 in normal operation. When the part returns from shutdown, the data in the registers is not current until the first conversion cycle is completed.
RESET	6	Reset Control	RESET = 1 triggers the power-on-reset sequence. All configuration, threshold, and data registers are reset to power-on state by writing a 1 to this bit, and an internal hardware reset pulse is generated. This bit then automatically becomes 0 after the RESET sequence is completed. Post-reset, the PWRON Interrupt is triggered. RESET = 0 configures the MAX25205 for normal operation.
SYNC	4	Master Slave Synchronize	This bit is used for synchronizing and staggering LED pulses when multiple devices are used in the system. This prevents two devices from flashing their LED at the same time. This is a self-clearing bit. When set to 1, it resets to 0 after one I^2C clock. The rising edge of this bit aborts the current ADC conversion cycle and starts a new ADC conversion cycle (ADC conversion cycle includes LED pulse, precharge, and ADC conversion/integration time). The ADC conversion cycles repeat after the delay set by SDLY[3:0]. Note 1: This scheme will not work for short SDLY settings. When multiple devices are used in a system, there is a limit on the minimum SDLY. The SDLY of the master must be larger than the integration time of the slave. Note 2: The software may periodically execute the sync sequence to take care of clock drift and mismatch on multiple devices.
OSEN	3	One-Shot Mode Enable	This bit enables one-shot mode. In this mode, the parameter SDLY is ignored, and no samples are automatically initiated. Instead, the system waits in idle mode until the bit OSTRIG (one-shot trigger) is set. This mode is used if the host processor requires full control over the timing of sample sequences, such as the case where there are multiple MAX25205 devices in one system. When combined with the EOCINT feature, the processor can be in full control of the start of a sample sequence, and then can be alerted when the sequence is done. When cleared to 0, the sequencer reverts to normal operation.

BITFIELD	BITS	DESCRIPTION	DECODE
OSTRIG	2	One-Shot Trigger	The bit OSTRIG is used for initiating one ADC conversion cycle under software control when OSEN is set to 1. When OSEN is set to 0, OSTRIG is ignored. This is a self-clearing bit. When set to 1, it resets to 0 after one I^2C clock. The rising edge of this bit starts an ADC conversion cycle. The cycle does not repeat until OSTRIG is cleared, and then set to 1 again.

SEQ CONFIGURATION 1 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	SDLY[3:0]				TIM[2:0]			–
Reset	0b0111				0b011			–
Access Type	Write, Read				Write, Read			–

BITFIELD	BITS	DESCRIPTION	DECODE
SDLY	7:4	End of Conversion Delay	See table below.

SDLY [3:0]	Clock Counts	Delay Between Samples (ms)
0000	0	0
0001	3998	1.56
0010	7995	3.12
0011	15990	6.25
0100	31980	12.49
0101	63960	24.98
0110	127920	49.97
0111	255840	99.94
1000	511680	199.98
1001	1023360	399.75
1010	2046720	799.5
1011-1111	4093440	1599

The 4 bits of SDLY[3:0] define 12 different sample-delay times for all channels. This added delay can be used to save power in power-sensitive applications where the 60 ADC do not need to be sampling continuously.

BITFIELD	BITS	DESCRIPTION	DECODE
TIM	3:1	Integration Time	The 3 bits of TIM[2:0] set the integration time for the ADC conversion, as shown below. **TIM[2:0] / LED Pulse Width (clock counts) / Integration Time (µs)** 000 / 16 / 6.25 001 / 32 / 12.5 010 / 64 / 25.0 011 / 128 / 50.0 100 / 256 / 100 101 / 512 / 200 110 / 1024 / 400 111 / 2048 / 800

SEQ CONFIGURATION 2 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	NRPT[2:0]			NCDS[2:0]			CDSMODE	–
Reset	0b100			0b100			0b0	–
Access Type	Write, Read			Write, Read			Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
NRPT	7:5	Number of Repeats	NRPT[2:0] sets the number of times the CDS sequence is repeated. Each repeat of the CDS sequence is identical to the previous—there is a single ALC pulse followed by one or more CDS A/B pairs, as set by NCDS[2:0]. The integration counters are not reset during this repetitive sequence; they continue to accumulate the count. **NRPT[2:0] / Number of CDS sequences** 000 / 1 001 / 2 010 / 4 011 / 8 100 / 16 101 / 32 110 / 64 111 / 128

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td>NCDS</td><td>4:2</td><td>Number of Coherent Double Samples</td><td>NCDS[2:0] sets the value of nCDS, the number of times that the CDS sequence is repeated within a single sample cycle after a single pulse of ALC. Setting nCDS to a value greater than 1 causes the programmed CDS sequence (Mode 0 or 1) to be repeated nCDS times after the single ALC pulse. The integration counters are not reset during the nCDS repeated sequences; they continue to accumulate the count.

<table><tr><th>NCDS[2:0]</th><th>Number of CDS sequences following a single ALC pulse</th></tr><tr><td>000</td><td>1</td></tr><tr><td>001</td><td>2</td></tr><tr><td>010</td><td>4</td></tr><tr><td>011</td><td>8</td></tr><tr><td>100</td><td>16</td></tr><tr><td>101</td><td>32</td></tr><tr><td>110</td><td>64</td></tr><tr><td>111</td><td>128</td></tr></table></td></tr>
<tr><td>CDSMODE</td><td>1</td><td>Coherent Double Sampling Mode</td><td><table><tr><th>CDSMODE</th><th>Description</th></tr><tr><td>0</td><td>Count up during sequence A and down during sequence B</td></tr><tr><td>1</td><td>Count up during sequence A, do not subtract sequence B</td></tr></table></td></tr>
</table>

AFE CONFIGURATION (0x5)

BIT	7	6	5	4	3	2	1	0
Field	–	ALC_COARSE	–	–	ALCEN	–	PGA[1:0]	
Reset	–	0b0	–	–	0b1	–	0b00	
Access Type	–	Write, Read	–	–	Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ALC_COARSE	6	ALC Coarse Current Correction	Factory use only. Set to 0.
ALCEN	3	Coarse Ambient Light Compensation Enable	ALCEN enables the coarse ambient light compensation circutis in the 60 analog front end channels. 0 = coarse ambient light compensation is not enabled. 1 = coarse ambient light compensation is enabled.

BITFIELD	BITS	DESCRIPTION	DECODE
PGA	1:0	Programable Gain Amplifier	The 2 bits PGA[1:0] set the gain range of the ADC channels according to the table below. **PGA[1:0]** / **Relative ADC Gain** / **I_{REF} (nA)** 00 / 1 / 16 01 / 1/4 / 64 10 / 1/16 / 256 11 / 1/32 / 512

LED CONFIGURATION (0x6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DRV[3:0]			
Reset	–	–	–	–	0b0000			
Access Type	–	–	–	–	Write, Read			

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td>DRV</td><td>3:0</td><td>One of the following:
• LED PWM drive setting when ELED_EN = 1 and DRV_EN = 0
• LED current drive setting when ELED_EN = 0 and DRV = 1.</td><td>
<table>
<tr><th>DRV[3:0]</th><th>DUTY CYCLE</th></tr>
<tr><td>0000</td><td>1/16</td></tr>
<tr><td>0001</td><td>2/16</td></tr>
<tr><td>0010</td><td>3/16</td></tr>
<tr><td>0011</td><td>4/16</td></tr>
<tr><td>0100</td><td>5/16</td></tr>
<tr><td>0101</td><td>6/16</td></tr>
<tr><td>0110</td><td>7/16</td></tr>
<tr><td>0111</td><td>8/16</td></tr>
<tr><td>1000</td><td>9/16</td></tr>
<tr><td>1001</td><td>10/16</td></tr>
<tr><td>1010</td><td>11/16</td></tr>
<tr><td>1011</td><td>12/16</td></tr>
<tr><td>1100</td><td>13/16</td></tr>
<tr><td>1101</td><td>14/16</td></tr>
<tr><td>1110</td><td>15/16</td></tr>
<tr><td>1111</td><td>16/16</td></tr>
</table>
<table>
<tr><th>DRV [3:0]</th><th>mA</th></tr>
<tr><td>0000</td><td>0</td></tr>
<tr><td>0001</td><td>13.3</td></tr>
<tr><td>0010</td><td>26.7</td></tr>
<tr><td>0011</td><td>40</td></tr>
<tr><td>0100</td><td>53.3</td></tr>
<tr><td>0101</td><td>66.7</td></tr>
<tr><td>0110</td><td>80</td></tr>
<tr><td>0111</td><td>93.3</td></tr>
<tr><td>1000</td><td>106.7</td></tr>
<tr><td>1001</td><td>120</td></tr>
<tr><td>1010</td><td>133.3</td></tr>
<tr><td>1011</td><td>146.7</td></tr>
<tr><td>1100</td><td>160</td></tr>
<tr><td>1101</td><td>173.3</td></tr>
<tr><td>1110</td><td>186.7</td></tr>
<tr><td>1111</td><td>200</td></tr>
</table>
</td></tr>
</table>

COLUMN GAIN 2, 1 (0xA5)

BIT	7	6	5	4	3	2	1	0
Field	CGAIN2[3:0]				CGAIN1[3:0]			
Reset	0b1000				0b1000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CGAIN2	7:4	Column Gain 2	There are ten different 4-bit column gains for the entire 60-channel array. Each trim value applies to one of the ten columns in the pixel array.

GAIN (hex)	I_{REF} Multiplication Factor	Gain Factor
0x00	3.06	0.33
0x01	2.71	0.37
0x02	2.35	0.43
0x03	2.06	0.49
0x04	1.77	0.56
0x05	1.55	0.65
0x06	1.33	0.75
0x07	1.17	0.86
0x08	1.00	1.00
0x09	0.88	1.14
0x0A	0.75	1.33
0x0B	0.66	1.53
0x0C	0.56	1.79
0x0D	0.49	2.04
0x0E	0.42	2.38
0x0F	0.37	2.70

BITFIELD	BITS	DESCRIPTION	DECODE
CGAIN1	3:0	Column Gain 1	There are ten different 4-bit column gains for the entire 60-channel array. Each trim value applies to one of the ten columns in the pixel array. **GAIN (hex) / I_{REF} Multiplication Factor / Gain Factor** 0x00 / 3.06 / 0.33 0x01 / 2.71 / 0.37 0x02 / 2.35 / 0.43 0x03 / 2.06 / 0.49 0x04 / 1.77 / 0.56 0x05 / 1.55 / 0.65 0x06 / 1.33 / 0.75 0x07 / 1.17 / 0.86 0x08 / 1.00 / 1.00 0x09 / 0.88 / 1.14 0x0A / 0.75 / 1.33 0x0B / 0.66 / 1.53 0x0C / 0.56 / 1.79 0x0D / 0.49 / 2.04 0x0E / 0.42 / 2.38 0x0F / 0.37 / 2.70

COLUMN GAIN 4, 3 (0xA6)

BIT	7	6	5	4	3	2	1	0
Field	CGAIN4[3:0]				CGAIN3[3:0]			
Reset	0b1000				0b1000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CGAIN4	7:4	Column Gain 4	See description in CGAIN1.
CGAIN3	3:0	Column Gain 3	See description in CGAIN1.

COLUMN GAIN 6, 5 (0xA7)

BIT	7	6	5	4	3	2	1	0
Field	CGAIN6[3:0]				CGAIN5[3:0]			
Reset	0b1000				0b1000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CGAIN6	7:4	Column Gain 6	See description in CGAIN1.
CGAIN5	3:0	Column Gain 5	See description in CGAIN1.

COLUMN GAIN 8, 7 (0xA8)

BIT	7	6	5	4	3	2	1	0
Field	CGAIN8[3:0]				CGAIN7[3:0]			
Reset	0b1000				0b1000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CGAIN8	7:4	Column Gain 8	See description in CGAIN1.
CGAIN7	3:0	Column Gain 7	See description in CGAIN1.

COLUMN GAIN 10, 9 (0xA9)

BIT	7	6	5	4	3	2	1	0
Field	CGAIN10[3:0]				CGAIN9[3:0]			
Reset	0b1000				0b1000			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CGAIN10	7:4	Column Gain 10	See description in CGAIN1.
CGAIN9	3:0	Column Gain 9	See description in CGAIN1.

LED_CTRL (0xC1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	GAINSEL	DRV_EN	ELED_EN	ELED_POL
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GAINSEL	3	Factory Gain Trim Selection	Value / Enumeration / Decode 0x0 / Gain Trim Register Select / Address 0xA5 - 0xA9 (default) 0x1 / Gain Trim Register Select / Internal Trim Value
DRV_EN	2	Current Drive Output Enable.	Value / Enumeration / Decode 0x0 / DRV Output / Disabled 0x1 / DRV Output / Enabled
ELED_EN	1	External LED Output Enable	ELED is an output pin design to drive a pMOS or nMOS switch with a PWM signal. Value / Enumeration / Decode 0x0 / Output / Disable 0x1 / Output / Enable

BITFIELD	BITS	DESCRIPTION	DECODE
ELED_POL	0	External LED Polarity Control	Value / Enumeration / Decode 0x0 / / Drive nMOS Switch 0x1 / / Drive pMOS Switch

Applications Information

Principle of Operation

Two electrical techniques are used to reject ambient light: coarse correction and fine correction. For coarse correction, the photo diode current is sampled and stored during time T1 when the IR LED is off. This current, which is a coarse measure of the ambient light, is then subtracted during the entire conversion cycle. The fine-correction method, however, uses coherent double sampling (CDS). An A pulse representing IR+ambient is measured when the IR LED is pulsed on. A second B pulse is measured with the LED off, representing ambient light. Subtracting the B pulse from the A pulse results in reflected IR with no common-mode ambient light (ambient-light compensation). The net reflected IR current is sampled with a 1-bit first-order sigma-delta ADC. The ADC is sampled with a 2.5MHz clock. Full scale of the ADC is given by:

N_{FS} = TIM x NCDS x NRPTS

The ratio of ADC sample count (N) to ADC full scale (N_{FS}) is porportional to the ratio of IR current to ADC reference current (I_{REF}),

$I_n / I_{REF} = N / N_{FS}$.

The maximum resolution of the sigma-delta ADC is 15 bits or N = 32,768 counts. Choosing large values for the full ADC scale will improve SNR while increasing integration time. The maximum current the ADC will clip at is I_{REF}, while the minimum current is:

$I_{min} = I_{REF} / N_{FS}$.

Operation Mode

The MAX25205 operates on a periodic sample schedule. When a sample is scheduled to occur, a sequence of digital signals activates the optical measurement circuits, i.e. pixels, and then collects the respective digital output data. When the sample sequence is finished, the pixels are disabled and placed in a low-power sleep mode. The register variable SDLY[3:0] controls the length of the sleep period. The pixels are held in this mode until the next scheduled sample sequence occurs. The timing of the periodic sampling schedule can be reset by setting the SYNC bit. In one-shot mode, (OSEN = 1), the periodic sampling is disabled, and the MAX25205 executes a sample sequence only when the OSTRIG bit is set.

The length and nature of the sampling sequence is controlled by the variables TIM[2:0], NRPT[2:0], and NCDS[2:0]. The variable CDSMODE selects one of the following methods to acquire the data during the sampling sequence.

CDS Mode 0

CDS Mode 0 is the default mode of operation. Every sample sequence consists of two measurements, A and B. In the A sequence, the LED is energized and the channel counters count up. The A sequence is then repeated in the subsequent B sequence, except the LED is not energized and the channel counters count down, which reduces the value stored. This algorithm removes slow-moving offsets and optical interference.

CDS Mode 1

CDS Mode 1 is similar to Mode 0, except that in the B sequence, the count down is not subtracted. Use Mode 1 if there is no need for the additional offset correction.

MAX25205 Sample-Sequence Timing

The timing specification is selectable with register variables, defined as follows:

- NCDS[2:0]: Number of CDS (A/B sequence) pairs, is also the number of LED pulses
- NRPT[2:0]: Number of ALC coarse correction + CDS pairs
- CRST: Enable the integrator reset between A/B sequences. The reset time is 16 clocks when CRST is high, or 0 when CRST is low.

The nominal clock frequency is 2.56MHz, so a 256-clock-cycle sample takes 100µs. Each cycle of the clock, T_{CK}, is 391ns.

Table 2. Sequence Timing Specification

PARAMETER	FUNCTION	# CLOCKS
T1	ALC duration time	256
D1	Delay time to start integration	32
T2	LED ON pulse	Defined by TIM[2:0]
T3	LED OFF pulse	T3 = T2
T4	Reset time between A/B, CRST = 0	0
T4	Reset time between A/B, CRST = 1	16
D2	Fixed delay	520

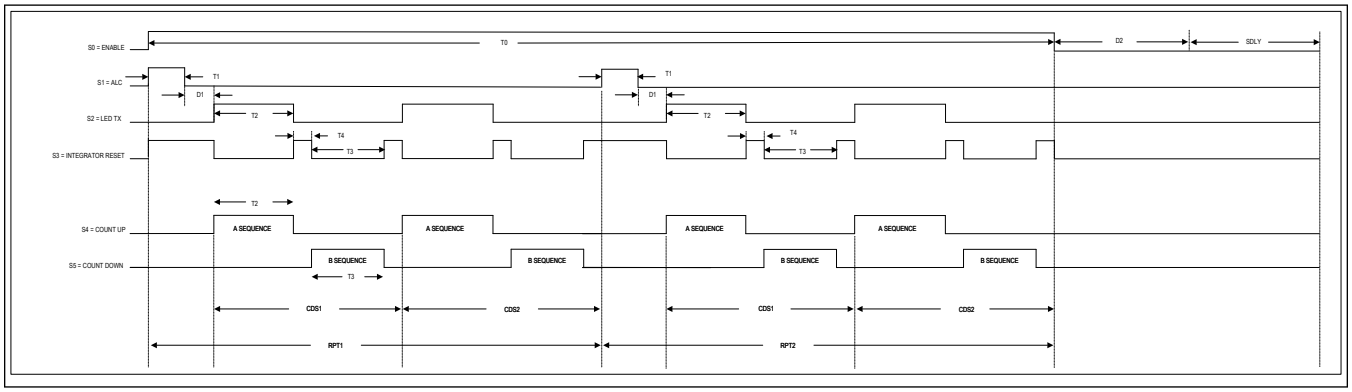


Figure 1. Timing Setting: NCDS = 2, NRPT = 2, CRST = 1

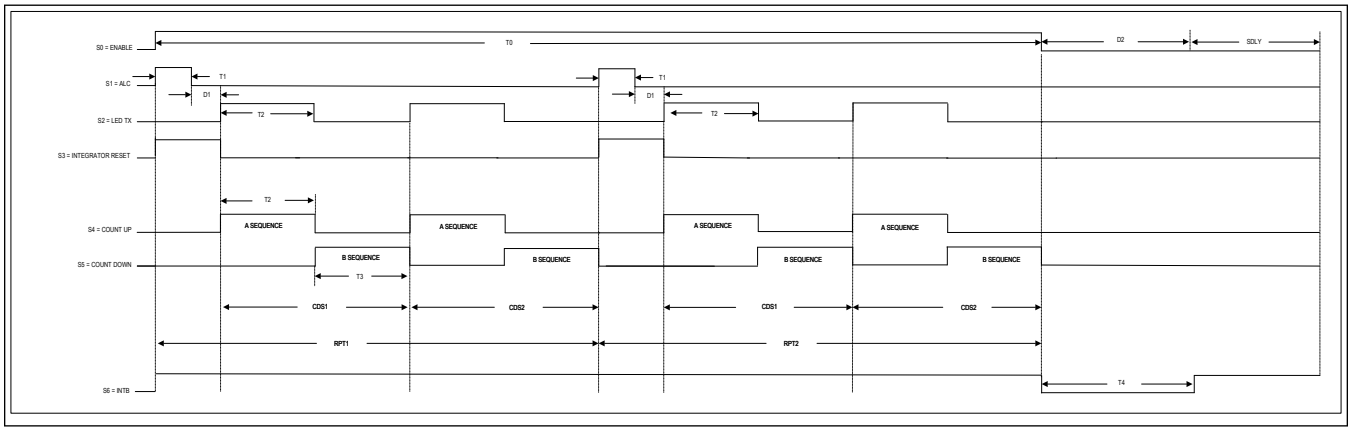


Figure 2. Timing Setting: NCDS = 2, NRPT = 2, CRST = 0

Array Orientation

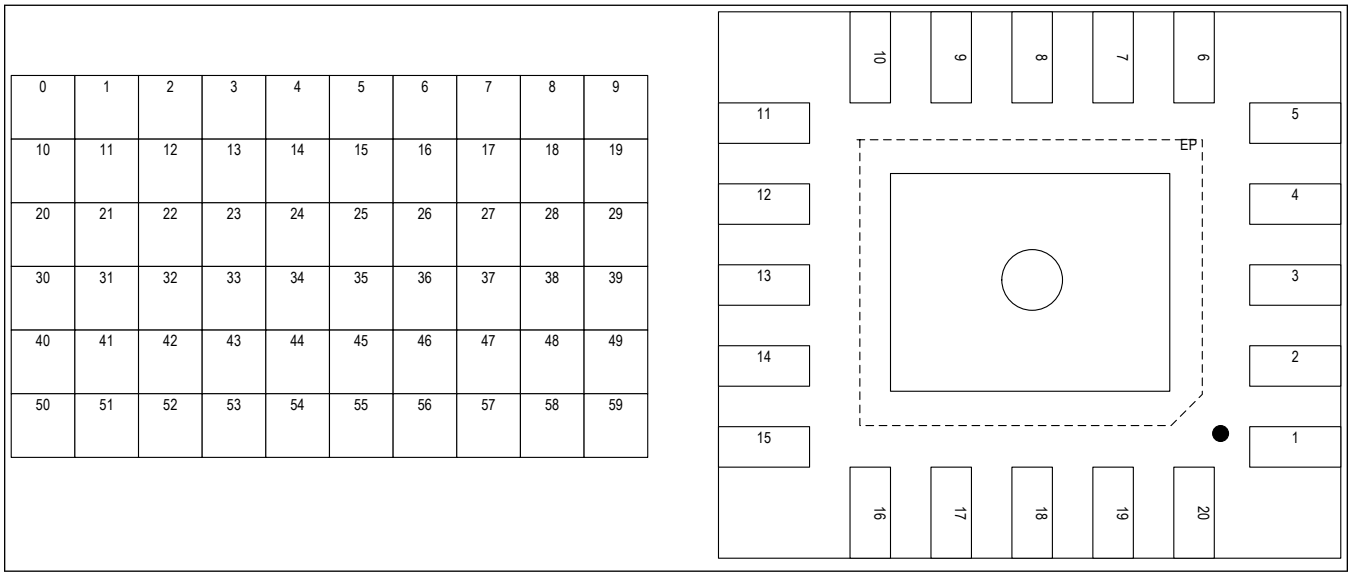


Figure 3. Array Orientation Relative to Pin 1

I²C Serial Interface

The MAX25205 IC features an I²C/SMBus-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. The master generates SCL and initiates data transfer on the bus. A master device writes data to the IC by transmitting the proper slave address, followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (S_R) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a NOT ACKNOWLEDGE, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor is required on the SDA bus. SCL operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high-voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signal.

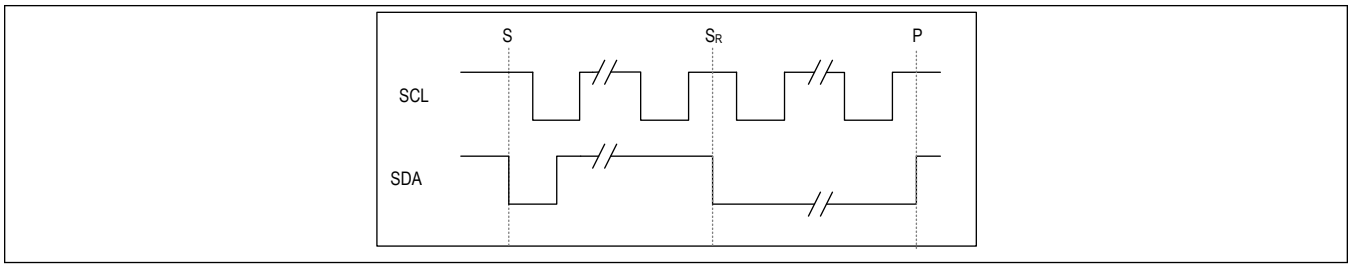


Figure 4. START, REPEAT START, STOP Conditions

Enabling I²C or SPI communications

When the SEL input is set to V_{DD}, the MAX25205 operates in I²C mode. In this mode, the $\overline{CS}$ input functions as the I²C address select pin. When $\overline{CS}$ = 0, the MAX25205 is pre-programmed with a slave address of 0x9E for write and 0x9F for

read. When $\overline{CS}$ is set to V_{DDIO}, the logic adds 2 to the programmed I^2C address. In this case, the I^2C address is 0xA0 for write and 0xA1 for read. The address is defined as the seven most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure MAX25205 to read mode. Set the read/write bit to 0 to configure the MAX25205 to write mode. The address is the first byte of information sent to MAX25205 after the START condition.

When the SEL pin is set to GND, the MAX25205 operates in SPI mode. There is no device address for SPI communications. A given part is selected by setting a low state on its $\overline{CS}$ pin. If there are multiple MAX25205 parts sharing the same SPI bus, then each must have its own $\overline{CS}$ signal, but the parts can share the SCL and DOUT nets. When a part is deselected by setting its $\overline{CS}$ signal high, the DOUT pin on that part is set to Hi-Z, permitting another part to drive the shared DOUT net. The shared SCL net is always driven from the master at the desired serial-clock frequency, and all of the slave devices share that signal.

Table 3. I^2C Slave Address

$\overline{CS}$ Pin	SLAVE ADDRESS FOR WRITING	SLAVE ADDRESS FOR READING
GND	1001 1110 (0X9E)	1001 1111 (0X9F)
V_{DD}	1010 0000 (0XA0)	1010 0001 (0XA1)

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the IC uses to handshake receipt of each byte of data when in write mode. The IC pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the IC is in read mode. An ACKNOWLEDGE is sent by the master after each read byte to allow data transfer to continue. A NOT ACKNOWLEDGE is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

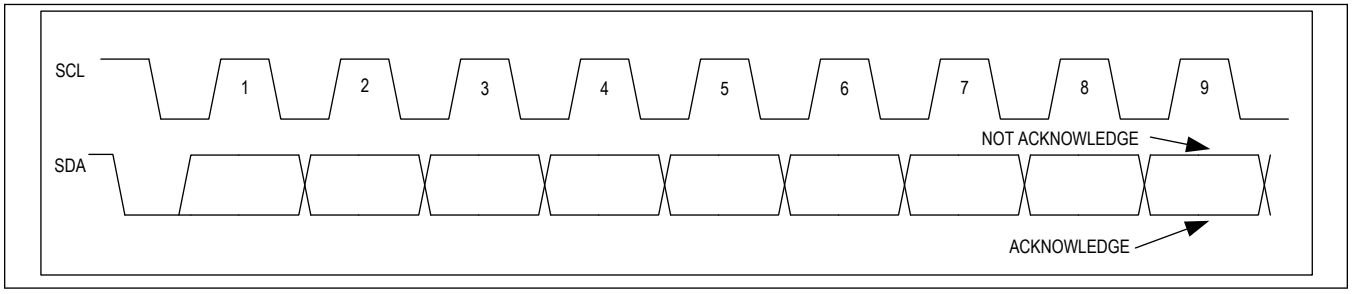


Figure 5. ACKNOWLEDGE

Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/W bit set to 0, 1 byte of data to

configure the internal register address pointer, one or more bytes of data, and a STOP condition. See figures illustrating the proper frame format for writing 1 byte of data to the IC and the frame format for writing n-bytes of data to the IC.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that is written to the chosen register. An ACKNOWLEDGE pulse from the IC signals receipt of the data byte. The address pointer automatically increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. Figure 6 and Figure 7 illustrate how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition.

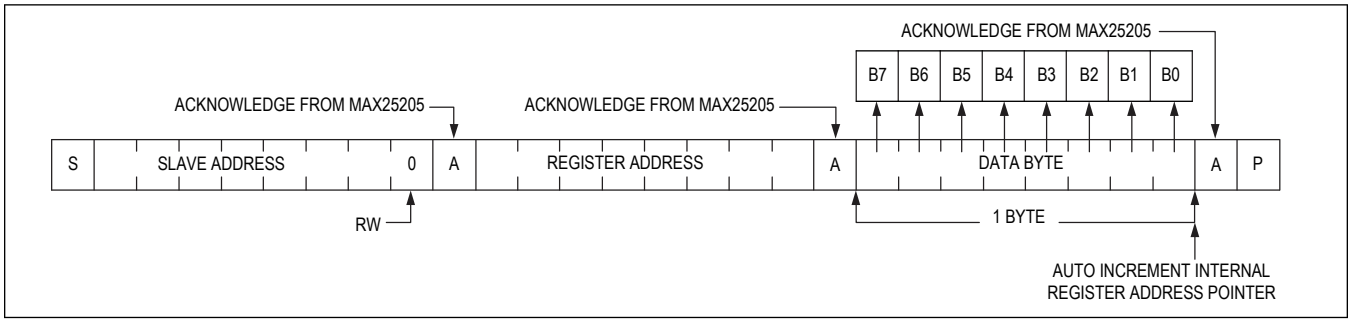


Figure 6. Write 1 Byte

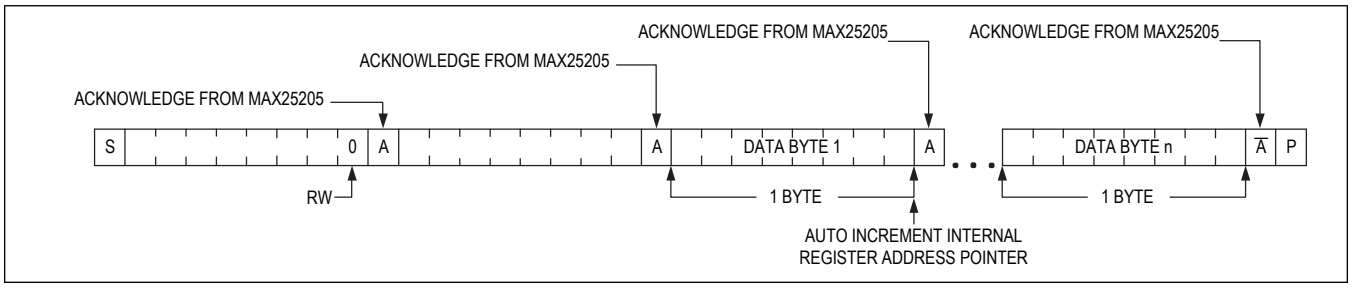


Figure 7. Write n Bytes

Read Data Format

Send the slave address with the R/W bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the ninth SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00. The first byte transmitted from the IC is the contents of register 0x00. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer automatically increments after each read-data byte. This automatic-increment feature allows all registers to be read sequentially within one continuous frame.

A STOP condition can be issued after any number of read-data bytes. If a STOP condition is issued and followed by another read operation, the first data byte to be read is from register 0x00, and subsequent reads automatically increment the address pointer until the next STOP condition. The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the IC's slave address with the R/W bit set to 0, followed by the register address. A REPEATED START condition is then sent, followed by the slave address with the R/W bit set to 1. The IC transmits the contents of the specified register. The address pointer automatically increments after transmitting the first byte. Attempting to read from register addresses higher than 0xFF results in repeated reads of 0xFF. Note that 0xB0–0xC0 are reserved registers. The master acknowledges receipt of each read byte during the

acknowledge clock pulse. The master must acknowledge all correctly received bytes except the final byte, which must be followed by a NOT ACKNOWLEDGE from the master and then a STOP condition.

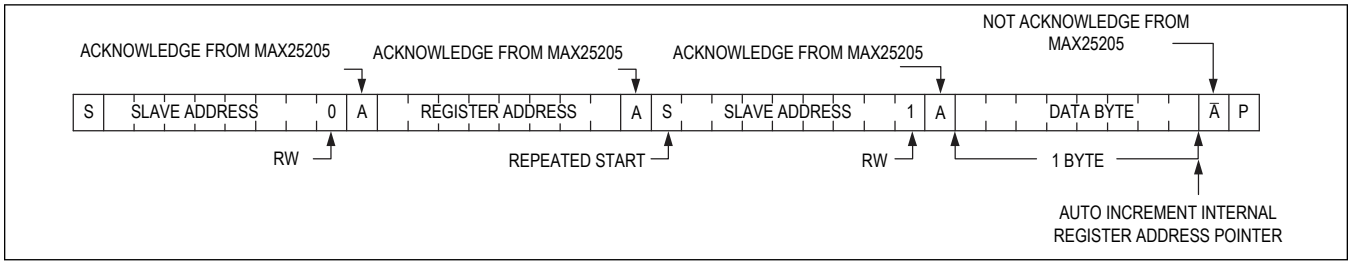


Figure 8. Reading 1 Byte of Indexed Data

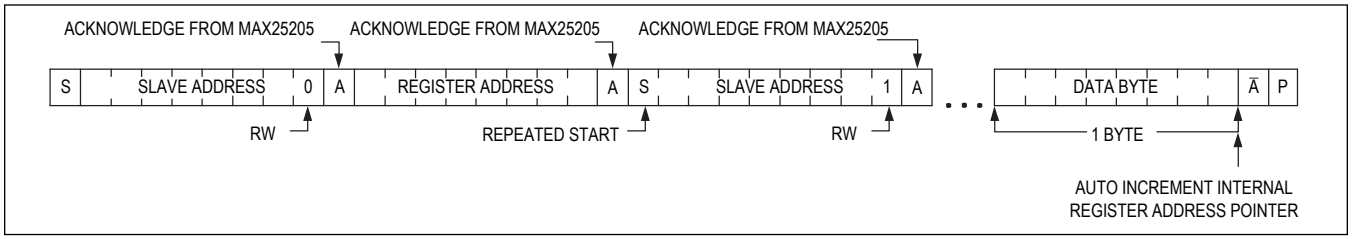


Figure 9. Reading n Bytes of Indexed Data

SPI Interface

The MAX25205 4-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSPs. The interface provides three inputs, SCL, $\overline{CS}$, and DIN, and one output, DOUT. The chip-select input ($\overline{CS}$, active-low) frames the data loaded through the serial-data input (DIN). Following a $\overline{CS}$ input high-to-low transition, the data is shifted in synchronously and latched into the input register on each rising edge of the serial-clock input (SCL).

The SPI interface in the MAX25205 has an 8-bit address, 8-bit command (but only 1-bit MSb is valid) and 8-bit data. The MAX25205 SPI only supports SPI mode 0, clock polarity CPOL = 0, clock phase CHPA = 0.

Each serial operation word is 24 bits long. The serial-input register transfers its contents to the destination registers after loading 24 bits of data on the 24th SCL rising edge. To initiate a new SPI operation, drive $\overline{CS}$ high and then low to begin the next operation sequence, ensuring that all relevant timing requirements are met. During $\overline{CS}$ high periods, SCL is ignored, allowing communication to other devices on the same bus. SPI operations consisting of more than 24 SCL cycles are executed on the 24th SCL falling edge, using the first 3 bytes of data available. SPI operations consisting of less than 24 SCL cycles will not be executed.

The SPI read operation is always operated in burst mode with bursts framed by $\overline{CS}$. Therefore, to read all 120 bytes of ADC values, initiate a read operation as follows:

$\overline{CS}$ High-Low Transition

1. Write 8-bit add (0x10 or 0x01 is the high byte of ADC 00's 2-byte value)
2. Write 8-bit read command (0x80)
3. Read 8-bit ADC_00_h, high byte data output for ADC00
4. Read 8-bit ADC_00_l, low byte data output for ADC00
5. Read 8-bit ADC_01_h, ...
6. Read 8-bit ADC_01_l
7. ...
8. Read 8-bit ADC_58_h
9. Read 8-bit ADC_58_l
10. Read 8-bit ADC_59_h
11. Read 8-bit ADC_59_l

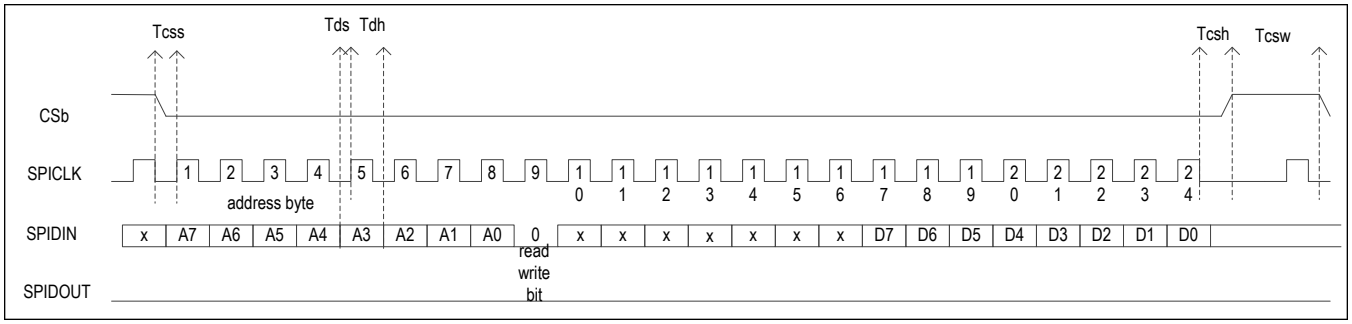


Figure 10. SPI Write

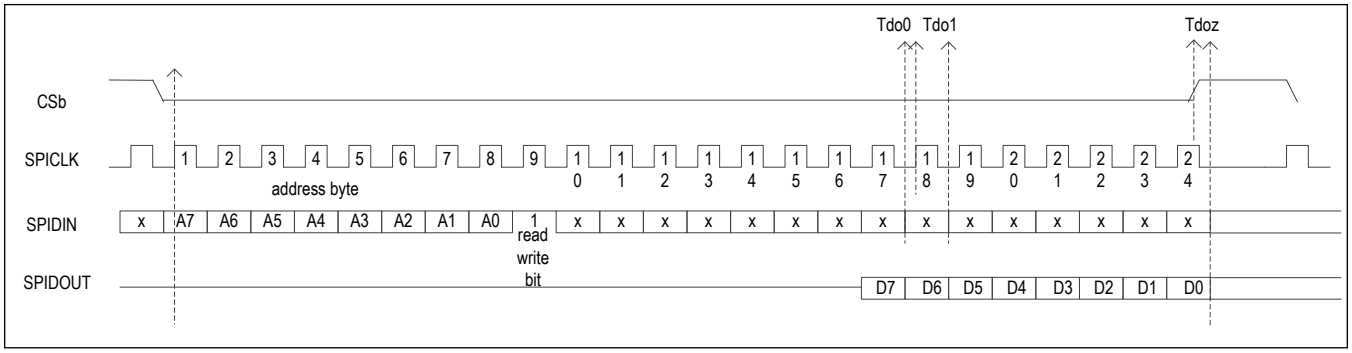
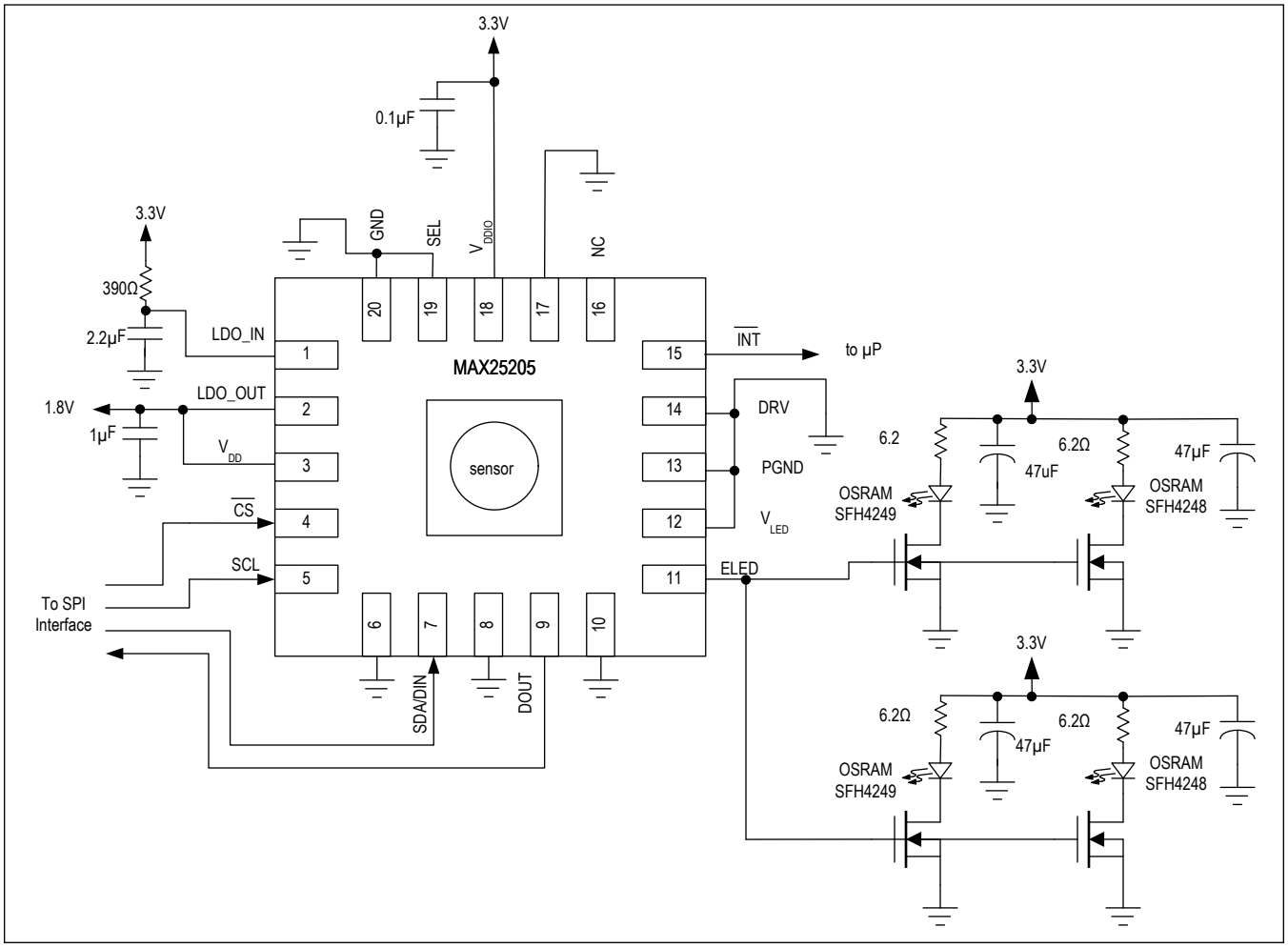


Figure 11. SPI Read

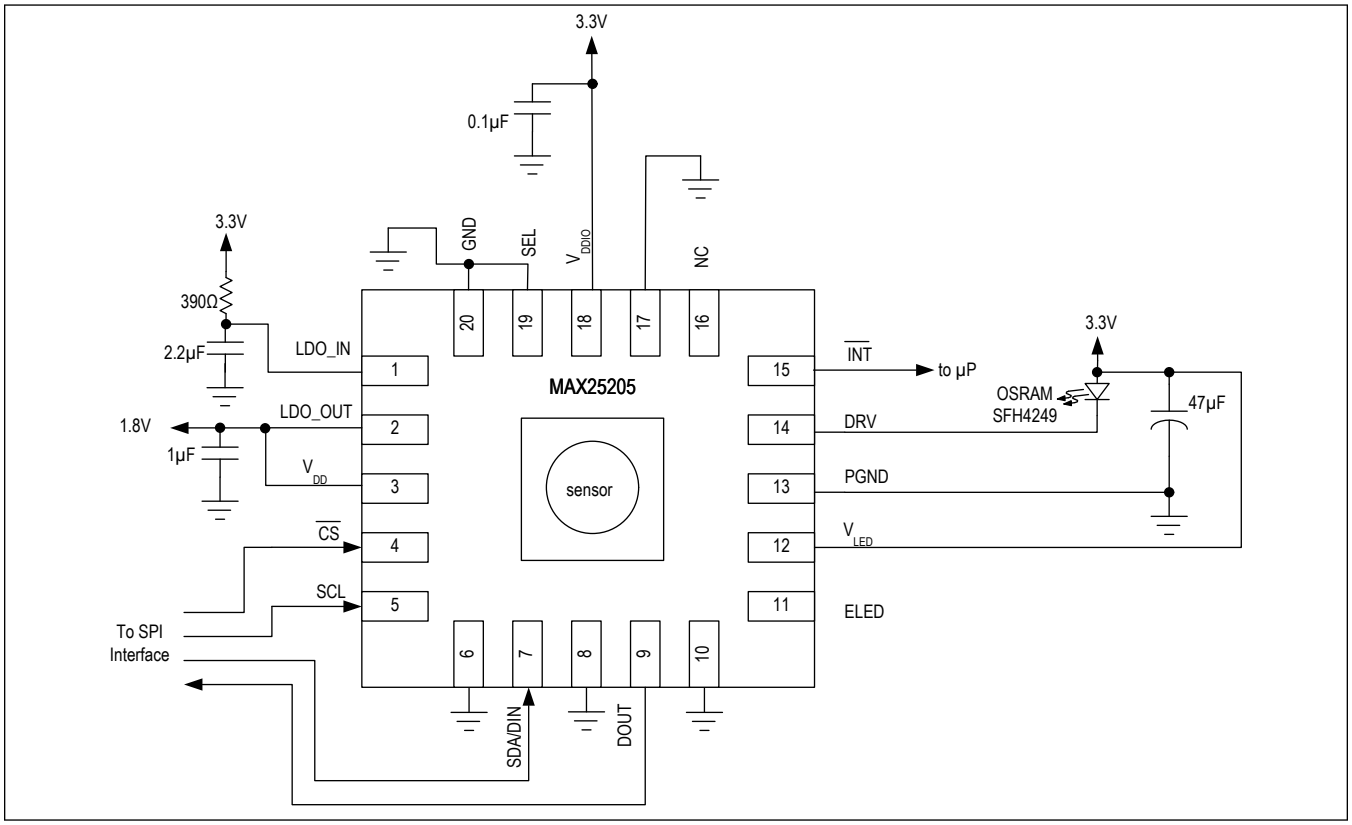
Typical Application Circuits

Typical Application Circuit with External FET LED Drive



Typical Application Circuits (continued)

Typical Application Circuit with Internal Current Drive



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	[TOP MARKING]
MAX25205EQP/VY+	-40°C to +85°C	20-pin 4mm x 4mm QFN	

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

The MAX25205 is an optical receiver and assembly should include a "no wash" approach to ensure contaminants are not deposited on the optical aperture.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/19	Initial release	—
1	9/20	Updated *Benefits and Features* and *Ordering Information*	1, 32

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