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MAX25220/MAX25221/ MAX25221B/MAX25221C

Automotive 4-Channel TFT-LCD Power Supplies with VCOM Buffer

General Description

The MAX25220/MAX25221/MAX25221B/MAX25221C are 4-channel TFT-LCD power ICs that provide symmetrical positive AVDD and negative NAVDD supplies as well as VG_{ON} and VG_{OFF} gate supplies. In addition, a VCOM buffer with output voltage range above and below ground and a temperature measurement block are integrated (MAX25221/B/C).

The devices contain non-volatile memory so that the values of all outputs can be calibrated for the lifetime of the device (maximum five times).

Programming is carried out using the built-in I²C interface, which can also be used to read back diagnostic information. A stand-alone mode is also available.

The temperature sensor interface block measures the temperature optionally, allowing the VCOM output voltage to be adjusted depending on the measured temperature.

The MAX25220/MAX25221/MAX25221B/MAX25221C are available in a TQFN package and operate in the -40 to +125°C temperature range.

Applications

- Infotainment Displays
- Central Information Displays
- Instrument Clusters

Benefits and Features

- High Integration
 - Synchronous Boost Provides AVDD of 4.2V to 10.5V at up to 200mA
 - NAVDD Inverter Output at up to -200mA
 - 15mA VG_{ON} Output (7.6V to 20.2V) from 3x Regulated Charge Pump
 - VG_{OFF} (-18.2V to -5.6V) from Regulated Charge Pump at up to -15mA (Charge-Pump Doubler)
 - Controlled Sequencing during Power-On and Power-Off of All Rails
 - VCOM Output Range +1V to -2.49V in 6.83mV Steps (MAX25221/B/C)
 - NTC Input for Temperature Measurement/ Compensation (MAX25221/B/C)
- Low EMI
 - 420kHz/2.1MHz Switching Frequency with Spread Spectrum
- I²C Control/Diagnostic Interface with FLT_B (Interrupt) Output
 - UV Diagnostics on All Outputs
- Versatile
 - Non-Volatile Output Voltage Settings on AVDD/ NAVDD, VG_{ON}, VG_{OFF}, VCOM, and Sequencing
 - Supports Stand-Alone Operation Mode after Programming
 - Compact 5mm x 5mm TQFN32 Package
- AEC-Q100 Grade 1

[Ordering Information](#) appears at end of data sheet.

Simplified Block Diagram

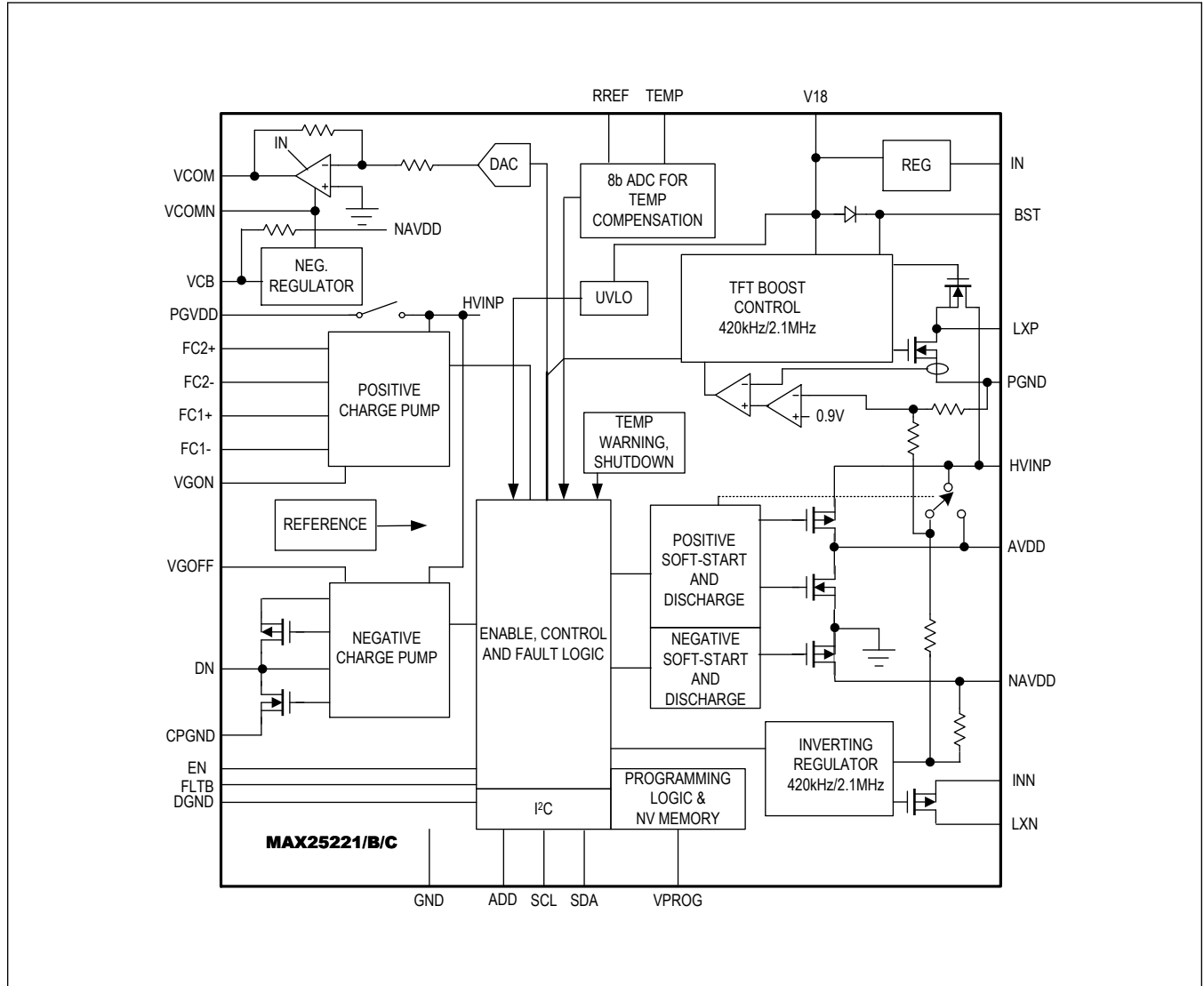


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Absolute Maximum Ratings

| | | | |
|-------------------------------|---|---|------------------------|
| IN, INN to GND..... | -0.3V to +6V | VCOMN to GND..... | V18 - 6V to V18 + 0.3V |
| IN to INN..... | -0.3V to +0.3V | PGVDD, FC1-, FC2-, DN to GND..... | -0.3V to HVINP + 0.3V |
| V18 to GND..... | -0.3V to +2.2V | FC1+ to GND..... | -0.3V to PGVDD + 0.3V |
| HVINP to GND..... | -0.3V to 16V | FC2+ TO FC1+..... | -0.3V to +22V |
| LXP, AVDD to GND..... | -0.3V to HVINP + 0.3V | VG _{ON} to FC2+..... | -0.3V to +22V |
| BST to GND..... | -0.3V to +16V | FC2+, VG _{ON} to GND..... | -0.3V to +24V |
| BST to LXP..... | -0.3V to +2.2V | EN, FLT, SCL, SDA to GND..... | -0.3V to +6V |
| LXN to INN..... | -22V to +0.3V | ADD, TEMP, RREF to GND..... | -0.3V to V18 + 0.3V |
| PGND, CPGND, DGND to GND..... | -0.3V to +0.3V | V _{PROG} to GND..... | -0.3V to +14V |
| VCB to GND..... | V18 - 22V to V18 + 0.3V | Continuous Power Dissipation (Multilayer Board) (T _A = +70°C, derate 21.3mW/°C above +70°C)..... | 2222mW |
| NAVDD to GND..... | V _{V18} - 16V to V _{V18} + 0.3V | Operating Temperature Range..... | -40°C to +125°C |
| VG _{OFF} to GND..... | V _{V18} - 22V to V _{V18} + 0.3V | | |
| VCOM to GND..... | VCOMN - 0.3V to IN + 0.3V | | |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

| | |
|--|-------------------------|
| Package Code | T3255+6C |
| Outline Number | 21-0140 |
| Land Pattern Number | 90-0603 |
| Thermal Resistance, Single-Layer Board: | |
| Junction to Ambient (θ _{JA}) | 47°C/W |
| Junction to Case (θ _{JC}) | 3°C/W |
| Thermal Resistance, Four-Layer Board: | |
| Junction to Ambient (θ _{JA}) | 36°C/W |
| Junction to Case (θ _{JC}) | 3°C/W |

TQFN-SW

| | |
|--|---------------------------|
| Package Code | T3255Y+6C |
| Outline Number | 21-100041 |
| Land Pattern Number | 90-100066 |
| Thermal Resistance, Single-Layer Board: | |
| Junction to Ambient (θ _{JA}) | 47°C/W |
| Junction to Case (θ _{JC}) | 3°C/W |
| Thermal Resistance, Four-Layer Board: | |
| Junction to Ambient (θ _{JA}) | 36°C/W |
| Junction to Case (θ _{JC}) | 3°C/W |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

($V_{IN} = 3.3V$, $V_{INN} = 3.3V$, Limits are 100% guaranteed between $T_A = -40^\circ C$ and $T_A = +125^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------|---|--------------|---------|-------|----------|
| INPUT SUPPLY | | | | | | |
| IN Voltage Range | | | 2.65 | | 5.5 | V |
| IN UVLO Threshold | IN_UVLO_R | Rising | 2.4 | 2.5 | 2.57 | V |
| IN UVLO Hysteresis | IN_UVLO_HYS | | | 100 | | mV |
| IN Shutdown Current | I_{IN_SHDN} | EN = GND, $V_{IN} = 3.3V$, $T_A = +25^\circ C$ | | 7 | 12 | μA |
| IN Quiescent Current | I_{IN_Q} | $V_{EN} = V_{IN} = 3.3V$, no switching. | | 1.5 | 2.5 | mA |
| V18 REGULATOR | | | | | | |
| V18 Output Voltage | | | 1.72 | 1.8 | 1.88 | V |
| V18 Current Limit | | | 60 | | | mA |
| V18 Undervoltage Lockout | | V18 rising | 1.6 | 1.65 | 1.7 | V |
| V18 Undervoltage Hysteresis | | | | 150 | | mV |
| OSCILLATOR | | | | | | |
| Operating Frequency | f_{BOOSTH} | f_{SW} bit = 0, dither disabled. Switching frequency for boost, inverter, and charge pumps. | 1950 | 2100 | 2250 | kHz |
| | f_{BOOSTL} | f_{SW} bit = 1, dither disabled. Switching frequency for boost, inverter, and charge pumps. | 385 | 420 | 455 | |
| Frequency Dither | f_{BOOSTD} | | | ± 6 | | % |
| BOOST REGULATOR | | | | | | |
| HVINP Output Voltage Range | V_{HVINP} | | $V_{IN} + 1$ | | 10.5 | V |
| AVDD Output Voltage Range | | | 4.2 | | 10.5 | V |
| AVDD Adjustment Step Size | | | | 0.1 | | V |
| AVDD Output Regulation | V_{AVDD} | avdd[5:0] = 0x1A, full load current and input voltage range | 6.664 | 6.8 | 6.936 | V |
| Oscillator Maximum Duty Cycle | | 420kHz switching frequency | 87 | 88.5 | 90 | % |
| | | 2.1MHz switching frequency | 84 | 87 | 90 | |
| Low-Side Switch On-Resistance | LXP_RON_LS | $I_{LXP} = 0.1A$ | | 0.1 | 0.2 | Ω |
| Synchronous Rectifier On-Resistance | | | | 0.1 | 0.2 | Ω |
| Synchronous Rectifier Zero-Crossing Threshold | ZX_TH | | | 70 | | mA |
| LXP Leakage Current | LXP_L_LEAK | $V_{EN} = 0V$, $V_{LXP} = 10.5V$ | | | 20 | μA |
| LXP Current Limit | I_{LIMPH} | Duty cycle = 50% | 1.7 | 2 | 2.3 | A |
| Soft-Start Period | t_{BOOST_SS} | Current-limit ramp | | 5 | | ms |

Electrical Characteristics (continued)

($V_{IN} = 3.3V$, $V_{INN} = 3.3V$, Limits are 100% guaranteed between $T_A = -40^{\circ}C$ and $T_A = +125^{\circ}C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------------|---|-------|-----------------|------|-----------|
| INVERTING REGULATOR | | | | | | |
| Oscillator Maximum Duty Cycle | | 2.1MHz switching frequency | 92 | 95 | | % |
| | INV_MAXDC | 420kHz switching frequency | 88 | 90 | | |
| $V_{AVDD} + V_{NAVDD}$ Regulation Voltage | V_{NAVDD_AVD} D_REG | $V_{INN} = 2.65V$ to $5.5V$, $V_{AVDD} = 6.8V$, $1mA < I_{NAVDD} < 200mA$, $I_{AVDD} =$ same load as NAVDD | -34 | 0 | 34 | mV |
| LXN On-Resistance | LXN_RON | INN to LXN, $I_{LXN} = 0.1A$ | | 0.25 | 0.5 | Ω |
| LXN Leakage Current | LXN_LEAK | $V_{IN} = 3.6V$, $V_{LXN} = V_{NAVDD} = -6.8V$, $T_A = +25^{\circ}C$ | | | 20 | μA |
| LXN Current Limit | I_{LIMNH} | Duty cycle = 80% | 1.55 | 1.9 | 2.25 | A |
| Soft-Start Period | t_{INV_SS} | Current-limit ramp | | 5 | | ms |
| NAVDD Discharge Resistance | | | | 2 | | $k\Omega$ |
| POSITIVE CHARGE-PUMP REGULATOR | | | | | | |
| V_{GON} Threshold for Charge-Pump Switching Enable | | | | $V_{HVINP-0.8}$ | | V |
| FC1-, FC2- Switches Current Limit, High-side | | | 90 | 120 | | mA |
| FC1-, FC2- Switches Current Limit, Low-side | | | 72 | 100 | | mA |
| FC1-, FC2- to CPGND On-Resistance | | | | 4 | 6.5 | Ω |
| FC1-, FC2- to HVINP On-Resistance | | | | 6 | 10.5 | Ω |
| FC2+ to PGVDD, FC1+ to FC2+ and V_{GON} to FC1+ Switches On-Resistance | | | | 2.5 | 4.5 | Ω |
| V_{GON} Voltage Range, I ² C Mode | | | 7.6 | | 20.2 | V |
| V_{GON} Adjustment Step Size, I ² C Mode | | | | 0.2 | | V |
| V_{GON} Output Voltage | V_{VGON} | $vgon[5:0] = 0x16$, full load current and $V_{HVINP} > 5V$, charge-pump tripler | 11.7 | 12 | 12.3 | V |
| V_{GON} Discharge Resistance | | | 2.2 | 3 | 3.8 | $k\Omega$ |
| NEGATIVE CHARGE-PUMP REGULATOR | | | | | | |
| DN Current Limit | | | 75 | 100 | | mA |
| V_{GOFF} Voltage Range, I ² C Mode | | | -18.2 | | -5.6 | V |
| V_{GOFF} Adjustment Step Size, I ² C Mode | | | | 0.2 | | V |
| V_{GOFF} Output-Voltage Accuracy | | $vgoff[5:0] = 0x16$, full load current and input voltage range, 420kHz operation. | -10.3 | -10 | -9.7 | V |

Electrical Characteristics (continued)

($V_{IN} = 3.3V$, $V_{INN} = 3.3V$, Limits are 100% guaranteed between $T_A = -40^{\circ}C$ and $T_A = +125^{\circ}C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------|---|------|-------------------|------|-----------|
| DN On-Resistance, High-Side | | | | 6 | 10 | Ω |
| DN On-Resistance, Low-Side | | $I_{DN} = -10mA$ | | 3.5 | 6.5 | Ω |
| $V_{G\text{OFF}}$ Discharge Current | | | | 1.5 | | mA |
| SEQUENCE SWITCHES | | | | | | |
| AVDD ON Resistance | R_{ONAVDD} | Between HVINP and AVDD, $I_{AVDD} = 200mA$ | | 0.5 | 1 | Ω |
| AVDD Current Limit | I_{LIMPOS} | | 300 | | 600 | mA |
| AVDD Discharge Resistance | | | | 1.2 | | $k\Omega$ |
| PGVDD On resistance | | (HVINP-PGVDD), $I_{PGVDD} = 3mA$ | | 6 | 9 | Ω |
| PGVDD Current Limit | | Expires when PGVDD charging is completed | 80 | 100 | | mA |
| FAULT PROTECTION | | | | | | |
| Fault Timeout | | $tfault[1:0] = 10$ | | 60 | | ms |
| Fault Retry Time | | $tretry[1:0] = 10$ or 11 | | 1.9 | | s |
| FLTB Output Frequency | | Stand-alone mode only | 0.88 | 1 | 1.12 | kHz |
| FLTB Output Duty Cycle, $V_{G\text{ON}}$ or $V_{G\text{OFF}}$ Fault | | Stand-alone mode only | | 75 | | % |
| FLTB Output Duty Cycle with AVDD, NAVDD or HVINP Fault | | Stand-alone mode only | | 50 | | % |
| FLTB Output Duty Cycle, VCOM Fault | | Stand-alone mode only | | 25 | | % |
| AVDD Undervoltage Fault Threshold | | Relative measurement between HVINP and AVDD | 80 | 85 | 90 | % |
| AVDD Short-Circuit Fault Threshold | | Relative measurement between HVINP and AVDD | 35 | 40 | 45 | % |
| NAVDD Undervoltage Fault Threshold | | Measured with respect to AVDD | 80 | 85 | 90 | % |
| NAVDD Short-Circuit Fault Threshold | | Measured with respect to AVDD | 35 | 40 | 45 | % |
| $V_{G\text{ON}}$ Undervoltage Fault Threshold | | Of set value | 80 | 85 | 90 | % |
| $V_{G\text{ON}}$ Short-Circuit Fault Threshold | | $V_{G\text{ON}}$ Falling, MAX25220ATJ/MAX25221ATJ/MAX25221BATJ only | | $V_{HVINP} - 1.1$ | | V |
| $V_{G\text{OFF}}$ Undervoltage Fault Threshold | | Of set value | 80 | 85 | 90 | % |
| $V_{G\text{OFF}}$ Short-Circuit Fault Threshold | | MAX25220ATJ/MAX25221ATJ/MAX25221BATJ only | 35 | 40 | 45 | % |
| Short-Circuit and Overload Fault Delay | | | | 10 | | μs |

Electrical Characteristics (continued)

($V_{IN} = 3.3V$, $V_{INN} = 3.3V$, Limits are 100% guaranteed between $T_A = -40^{\circ}C$ and $T_A = +125^{\circ}C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------|--|-------|------------|------|------------------|
| VCOM BUFFER | | | | | | |
| VCOMN Output Voltage | | $I_{VCOM} = 120mA$, $V_{NAVDD} = -10.5V$ | | -3.5 | -3.2 | V |
| VCB Output Current | | | 5 | 12 | 21 | mA |
| VCOM Output Current Limit, Sinking | | Dynamic output current, $t < t_{FAULT}$ | 120 | 200 | 300 | mA |
| VCOM Output Current Limit, Sourcing | $I_{LIMCOMP}$ | Dynamic output current, $t < t_{FAULT}$ | 120 | 200 | 300 | mA |
| VCOM Overcurrent Detection Threshold | | | 60 | 70 | 85 | of $I_{LIMCOMP}$ |
| VCOM Offset Voltage, Complete Range | | $V_{VCOM} = -2.49V$ and $V_{VCOM} = +1V$, no load | -20 | | +20 | mV |
| VCOM Offset Voltage, 25°C | | $T_A = +25^{\circ}C$, $V_{COM} = -0.5V$ | -6 | | +6 | mV |
| VCOM Offset Voltage | | $V_{COM} = -0.5V$ | -10 | | +10 | mV |
| VCOM Output Voltage Range | | Temperature compensation disabled | -2.49 | | 1 | V |
| VCOM DAC Step Size | | | | 6.83 | | mV |
| VCOM Buffer Slew Rate | | $C_{VCOM} = 10nF$, VCOM from -2.49V to +1V | | 0.72 | | V/ μs |
| VCOM Fault Threshold | | Deviation from set voltage | | ± 0.25 | | V |
| VCOM Fault Detection Filter Time | | $t_{fault}[1:0] = 10$ | | 60 | | ms |
| VCOM Discharge Resistance | | to GND | 9 | 14 | 22 | k Ω |
| RREF INPUT | | | | | | |
| RREF Input Voltage Range | | | 0 | | 1.25 | V |
| RREF ADC Resolution | | | | 4.88 | | mV |
| RREF Conversion Rate | | | | 128 | | kHz |
| TEMP Voltage | V_{TEMP} | $I_{TEMP} = 10$ to $500\mu A$ | | 625 | | mV |
| TEMP Current Mirror Gain | | $I_{TEMP} = 10$ to $500\mu A$ | | 1 | | $\mu A/\mu A$ |
| Internal Temperature Sensor Voltage | | $T_A = +25^{\circ}C$ | | 620 | | mV |
| RREF DAC Offset | | | | 5 | | mV |
| RREF DAC Full-Scale Error | | | | 5 | | mV |
| RREF DAC Gain Error | | | -0.4 | | +0.4 | % |
| RREF DAC Differential Non-linearity | | | | 0.5 | | LSB |
| RREF DAC Integral Non-Linearity | | | | 0.5 | | LSB |
| LOGIC INPUTS and OUTPUTS (EN, SCL, ADD, SDA) | | | | | | |
| EN Glitch Filter | EN_BLK | | | 10 | | μs |

Electrical Characteristics (continued)

($V_{IN} = 3.3V$, $V_{INN} = 3.3V$, Limits are 100% guaranteed between $T_A = -40^{\circ}C$ and $T_A = +125^{\circ}C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|---|------|-----|------|-------------|
| EN Minimum Low Time For Reset | | $C_{V18} = 1\mu F$ | 1 | | | ms |
| EN Input Logic-High | | | 1.22 | | | V |
| EN Input Logic-Low | | | | | 0.6 | V |
| ADD Input Logic-High | | | 1.22 | | | V |
| ADD Input Logic-Low | | | | | 0.66 | V |
| ADD Input Pulldown Current | | | | 10 | 12 | μA |
| SCL, SDA Input, Logic-High | | | 1.22 | | | V |
| SCL, SDA Input, Logic-Low | | | | | 0.6 | V |
| SCL Input Leakage Current | | | -1 | | +1 | μA |
| FLTB, SDA Output Low Voltage | V_{OL} | Sinking 5mA | | | 0.4 | V |
| FLTB, SDA Output Leakage Current | I_{LEAK} | 5.5V | -1 | | +1 | μA |
| PROGRAMMING VOLTAGE | | | | | | |
| V _{PROG} Voltage | | | 8.2 | 8.5 | 8.8 | V |
| V _{PROG} Voltage Undervoltage Threshold | | V _{PROG} rising | | 8 | 8.2 | V |
| V _{PROG} Voltage Overvoltage Threshold | | V _{PROG} falling | 8.8 | 9 | | V |
| V _{PROG} Input Current | | During NV programming, $T_A = +25^{\circ}C$ | | 9 | 25 | mA |
| NV Programming Time | | | | 16 | 20 | ms |
| THERMAL SHUTDOWN | | | | | | |
| Thermal Warning Threshold | | | | 125 | | $^{\circ}C$ |
| Thermal-Shutdown Threshold | T_{SHDN} | | | 160 | | $^{\circ}C$ |
| Thermal-Shutdown Hysteresis | T_{SHDN_HYS} | | | 15 | | $^{\circ}C$ |
| I²C INTERFACE | | | | | | |
| Clock Frequency | f_{SCL} | | | | 0.4 | MHz |
| Hold Time (Repeated) START | $t_{HD:STA}$ | | 600 | | | ns |
| SCL Low Time | t_{LOW} | | 1300 | | | ns |
| SCL High Time | t_{HIGH} | | 600 | | | ns |
| Setup Time (Repeated) START | $t_{SU:STA}$ | | 600 | | | ns |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | | ns |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |

Electrical Characteristics (continued)

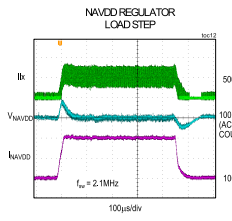
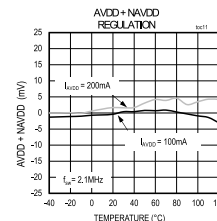
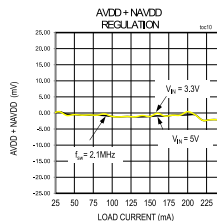
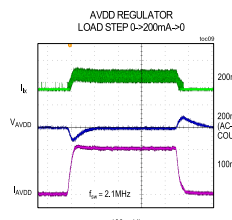
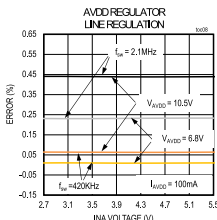
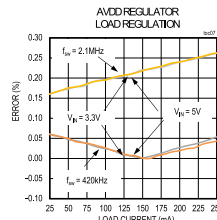
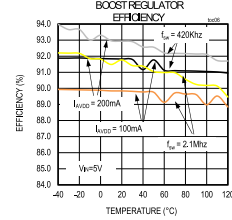
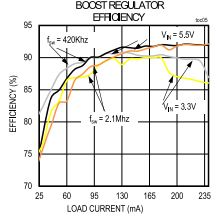
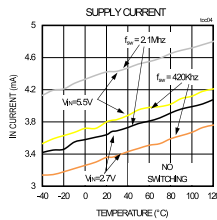
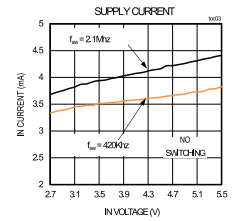
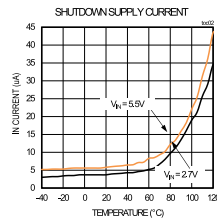
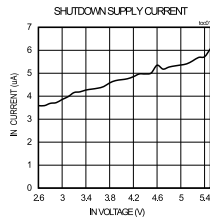
($V_{IN} = 3.3V$, $V_{INN} = 3.3V$, Limits are 100% guaranteed between $T_A = -40^{\circ}C$ and $T_A = +125^{\circ}C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|--------------|------------|-----|-----|-----|-------|
| Setup Time for STOP Condition | $t_{SU:STO}$ | | 600 | | | ns |
| Spike Suppression | | | | 50 | | ns |

Note 1: Note 1: Limits are 100% tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

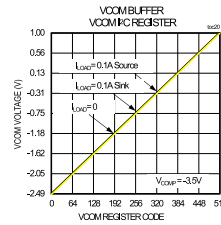
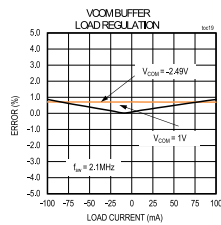
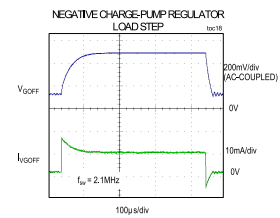
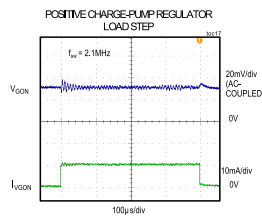
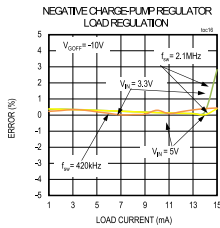
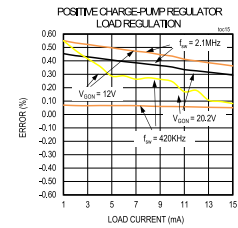
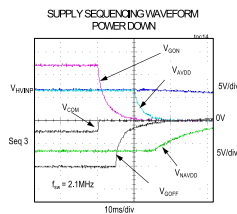
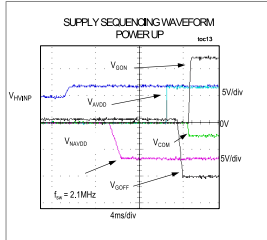
Typical Operating Characteristics

($V_{IN} = +3.3V$, $F_{SW} = 2.1MHz$, $T_A = +25\text{ C}$ unless otherwise noted.)



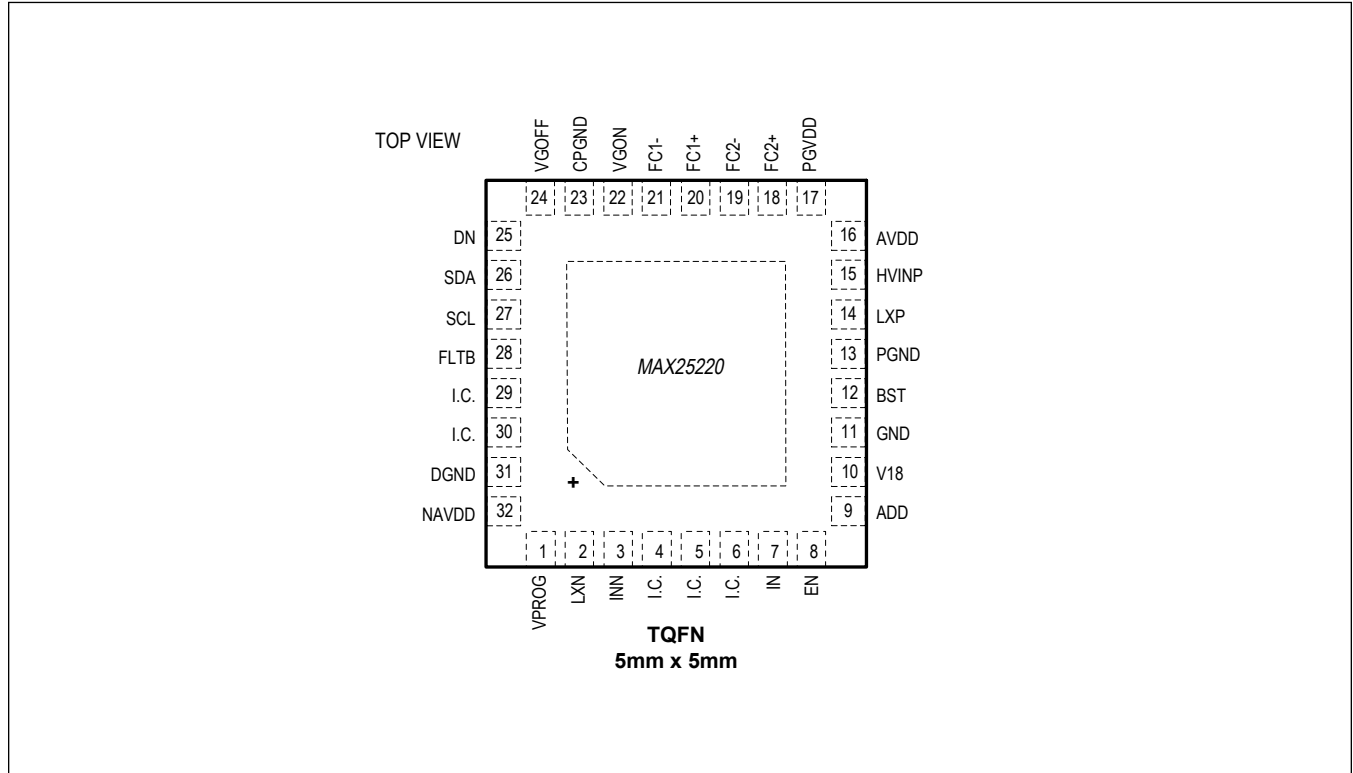
Typical Operating Characteristics (continued)

($V_{IN} = +3.3V$, $F_{SW} = 2.1MHz$, $T_A = +25\text{ C}$ unless otherwise noted.)

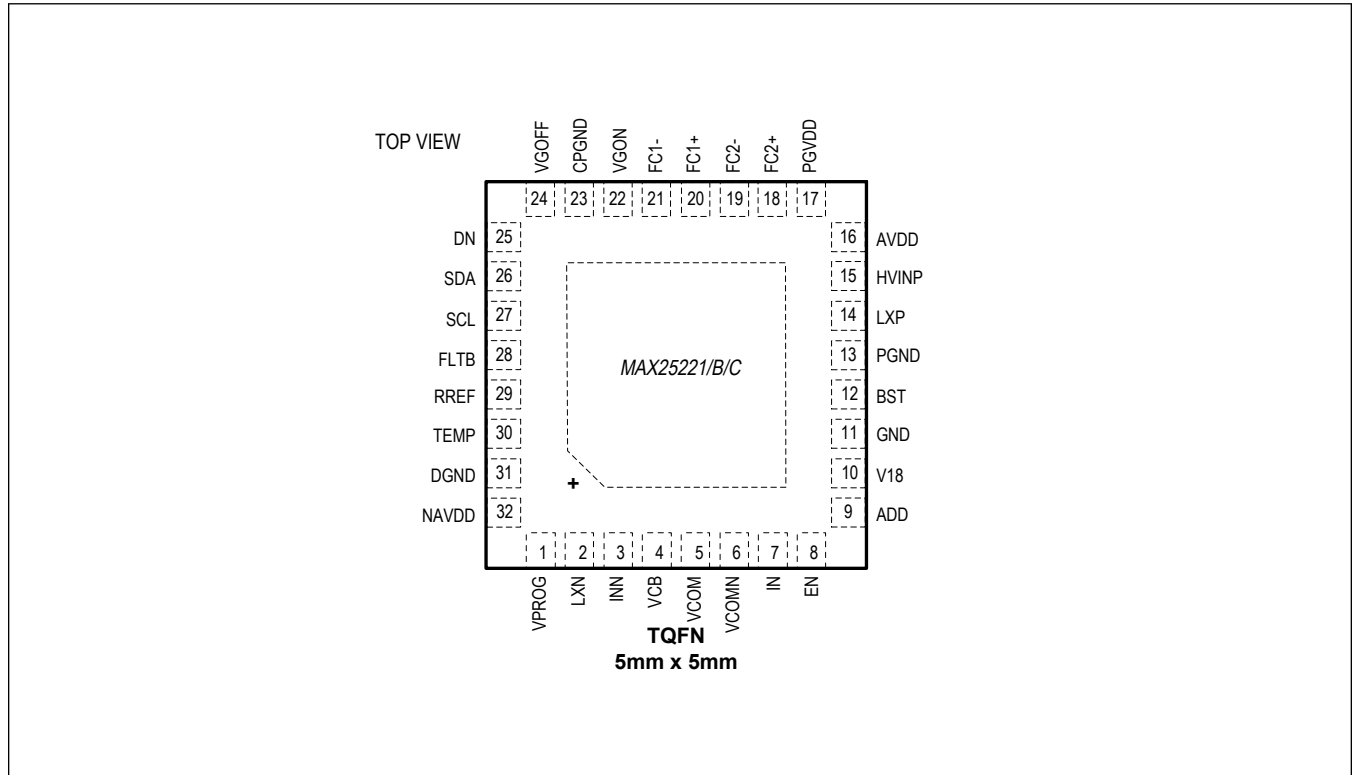


Pin Configurations

MAX25220



MAX25221/B/C



Pin Description

| PIN | | NAME | FUNCTION |
|----------|------------------|-------------------|---|
| MAX25220 | MAX25221/ B/C | | |
| 1 | 1 | V _{PROG} | Programming Voltage. Apply a voltage of 8.5V to this pin during the programming of non-volatile registers. Connect to GND through a resistor during normal operation. |
| 2 | 2 | LXN | DC-DC Inverting Converter Inductor/Diode Connection. |
| 3 | 3 | INN | Inverting Converter Input. Connect 10µF + 0.1µF ceramic capacitors from this pin to ground for proper operation. |
| 4 | — | IC | Internally connected. Leave this pin open. |
| — | 4 | VCB | Drive Output for External npn Pass Transistor for VCOMN regulator. Connect to the base of the external npn transistor. |
| 5 | — | IC | Internally Connected. Leave this pin open. |
| — | 5 | VCOM | Output of VCOM amplifier. |
| 6 | — | IC | Internally Connected. Connect this pin to GND. |
| — | 6 | VCOMN | Negative Supply for VCOM Buffer. Connect a ceramic capacitor of at least 1µF from VCOMN to GND. |
| 7 | 7 | IN | Supply Connection for Display Bias Circuitry. Bypass IN with local 10µF and 0.1µF capacitors. |

Pin Description (continued)

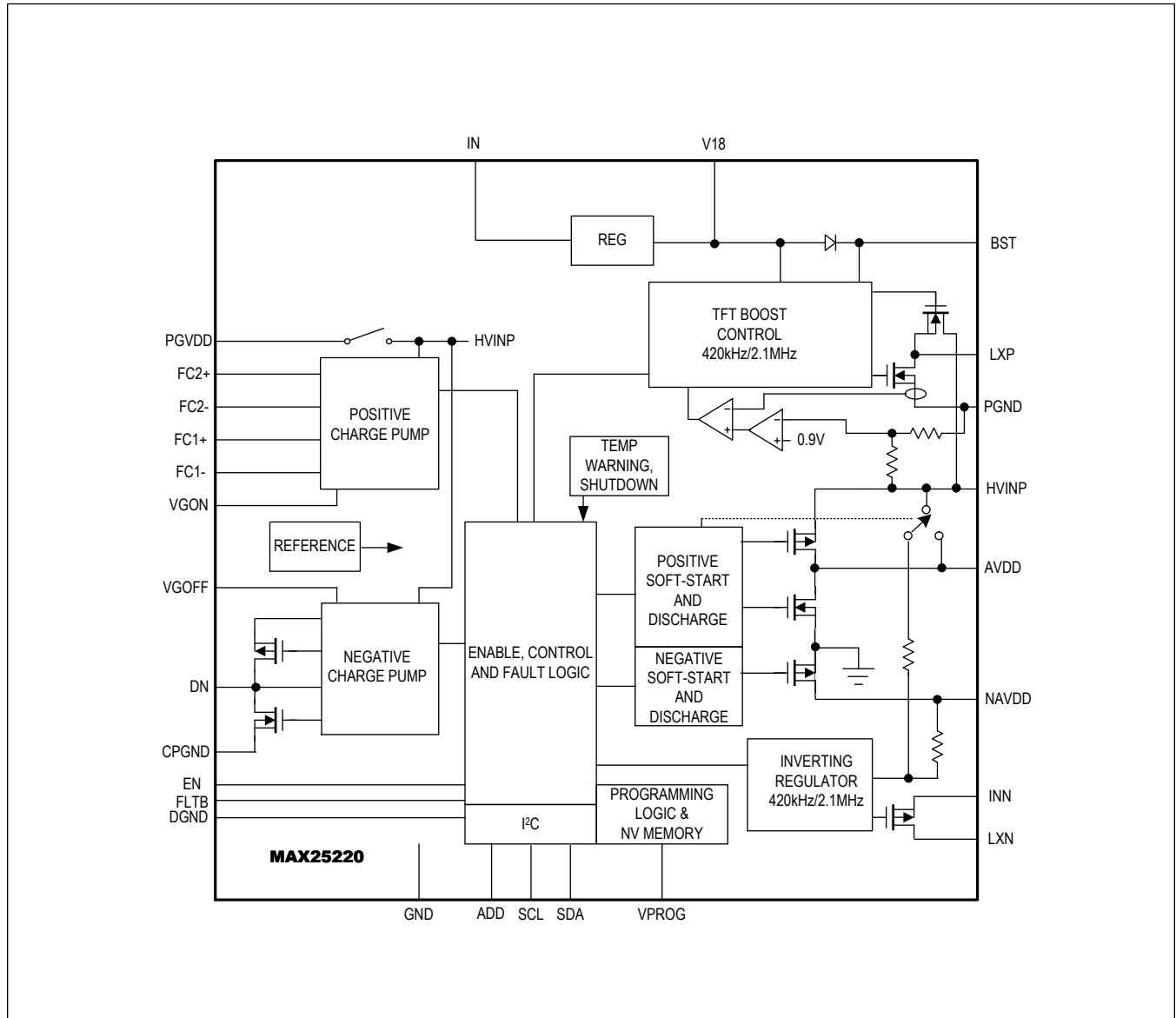
| PIN | | NAME | FUNCTION |
|----------|------------------|-------------------|---|
| MAX25220 | MAX25221/ B/C | | |
| 8 | 8 | EN | Enable Input Pin. When EN is low, the device is in shutdown. When EN is taken high, the device is active. In stand-alone mode, the outputs are turned on in the stored sequence when EN goes high. |
| 9 | 9 | ADD | Device Address Select pin. Connect to GND or V18 to Select the Device I ² C Address. See the I ² C address table. To use stand-alone mode (without I ² C) leave the ADD pin open. In this mode, the device turns on all outputs in the programmed sequence when EN is taken high. |
| 10 | 10 | V18 | Output of Internal 1.8V Regulator. Connect a 1μF capacitor from V18 to GND. |
| 11 | 11 | GND | Ground Connection |
| 12 | 12 | BST | Bootstrap Capacitor Connection for Synchronous Rectifier Driver. Connect a 0.1μF ceramic capacitor between BST and LXP. |
| 13 | 13 | PGND | Ground Connection for Boost Switching Device and VCOM Buffer. Connect to GND using a low-impedance trace. |
| 14 | 14 | LXP | Switching Node of Boost Converter. Connect the boost inductor between LXP and IN. |
| 15 | 15 | HVINP | Boost Output and Input to Positive and Negative Charge-Pump Drivers. Bypass HVINP with a 10μF output capacitor placed close to the pin. |
| 16 | 16 | AVDD | Switched Output of Boost Converter. Connect a bypass capacitor of value 2.2μF from AVDD to PGND. |
| 17 | 17 | PGVDD | Supply Voltage for Positive Charge Pump. PGVDD is connected to HVINP by means of an internal switch when the positive charge pump is enabled. Bypass PGVDD with a ceramic capacitor of 1μF to GND. |
| 18 | 18 | FC2+ | Positive Connection for Second Flying Capacitor. Connect a 22nF capacitor from FC2- to FC2+. |
| 19 | 19 | FC2- | Negative Connection for Second Flying Capacitor. Connect a 22nF capacitor from FC2- to FC2+. |
| 20 | 20 | FC1+ | Positive Connection for First Flying Capacitor. Connect a 22nF capacitor from FC1- to FC1+. |
| 21 | 21 | FC1- | Negative Connection for First Flying Capacitor. Connect a 22nF capacitor from FC1- to FC1+. |
| 22 | 22 | VG _{ON} | Output of Positive Charge-Pump Block. Connect a 1μF capacitor from VG _{ON} to GND. |
| 23 | 23 | CPGND | Ground Connection for Charge Pumps. |
| 24 | 24 | VG _{OFF} | Output of Negative Charge-Pump Block. Connect a 1μF capacitor from this pin to GND. |
| 25 | 25 | DN | Negative Charge-Pump Push-Pull Drive Output. |
| 26 | 26 | SDA | Bidirectional I ² C Data Pin. |
| 27 | 27 | SCL | I ² C Clock Pin. |
| 28 | 28 | FLT _B | Open-Drain, Active-Low Fault Output. Connect a pullup resistor from FLT _B to a logic supply ≤5V. In stand-alone mode, the duty cycle of the FLT _B pin indicates an error condition, if present (see Table 4). When the serial interface is used, FLT _B is either a 0 (indicating data to be read from the internal registers) or a 1. |
| 29 | — | IC | Internally Connected. Leave this pin open. |
| — | 29 | R _{REF} | Reference Resistor Pin. When using the temperature compensation function, connect a resistor from R _{REF} to GND. If unused, leave R _{REF} unconnected. |

Pin Description (continued)

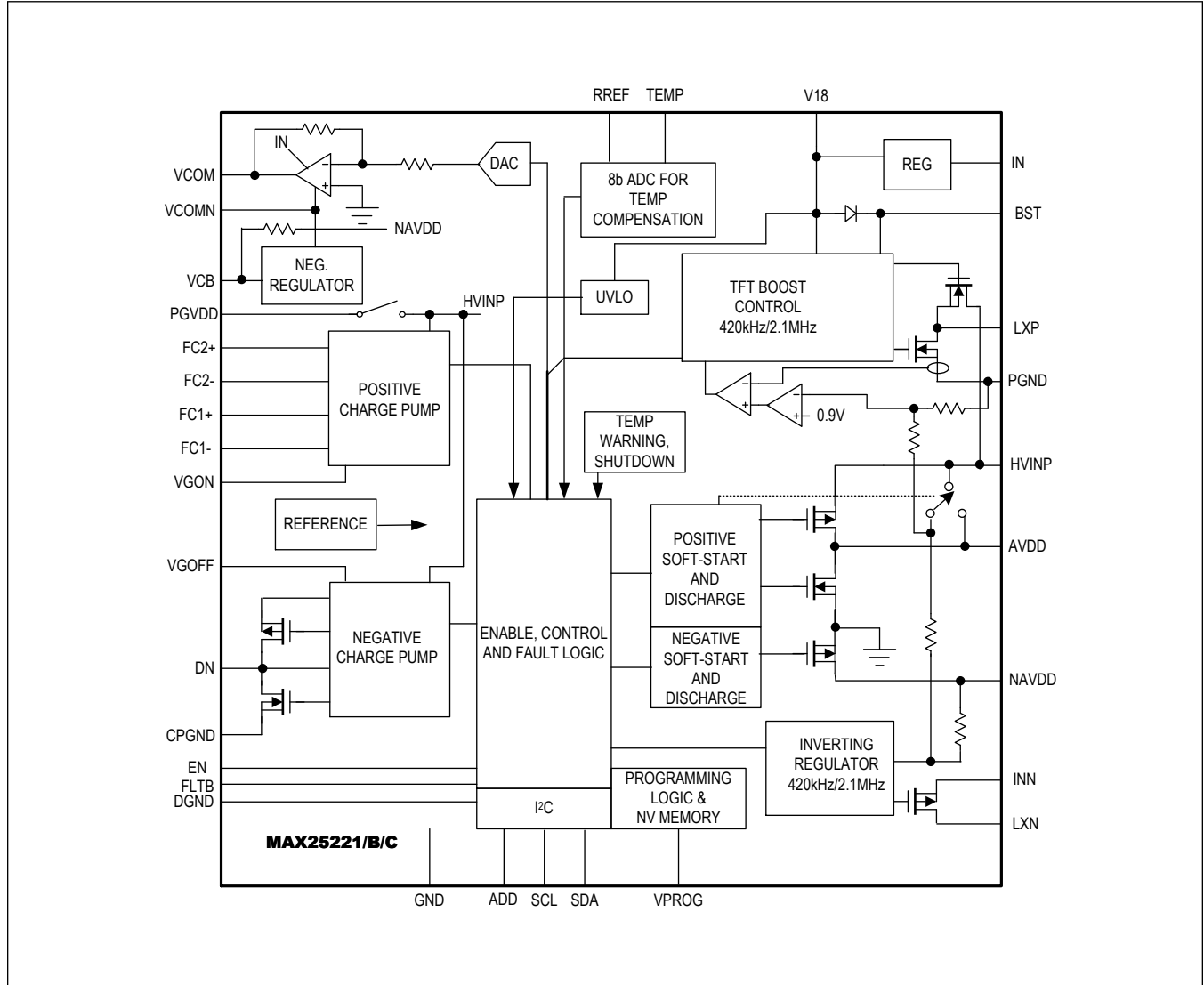
| PIN | | NAME | FUNCTION |
|----------|------------------|-------|--|
| MAX25220 | MAX25221/ B/C | | |
| 30 | — | IC | Internally Connected. Leave this pin open. |
| — | 30 | TEMP | Temperature Sensor Pin. When using the temperature compensation function, connect an NTC from TEMP to GND. If unused, leave TEMP unconnected. |
| 31 | 31 | DGND | Logic Ground. |
| 32 | 32 | NAVDD | Negative Source-Driver Output Voltage. Connect ceramic capacitors of value 0.1 μ F and 10 μ F from this pin to GND with the smallest capacitor closest to the pin. |

Functional Diagrams

MAX25220



MAX25221/B/C



Detailed Description

The MAX25220/MAX25221/MAX25221B/MAX25221C are 4-channel TFT-LCD power ICs that provide symmetrical positive AVDD and negative NAVDD supplies as well as V_{GON} and V_{GOFF} gate supplies. In addition, a VCOM buffer with output voltage range above and below ground and a temperature-measurement block are integrated in the MAX25221, MAX25221B, and MAX25221C.

The devices contain non-volatile memory so that the values of all outputs can be calibrated for the lifetime of the device. Programming is carried out using the built-in I²C interface, which can also be used to read back diagnostic information. Operation in stand-alone mode is also possible.

The temperature-sensor interface block in the MAX25221, MAX25221B, and MAX25221C determines the temperature by measuring the voltage on the R_{REF} pin when a temperature-sensitive component, such as an NTC, is connected to TEMP. The VCOM output voltage can be adjusted as a function of the measured temperature.

Power-Up State

When power is applied, the MAX25220/21/21B/21C are in low-quiescent-current mode until the EN pin is taken high. When EN is taken high (if the device supply voltage on IN exceeds the undervoltage lockout voltage of 2.5V) the 1.8V regulator is turned on and the device is functional after a delay of 1ms. Subsequent operation depends on the device configuration and type as follows:

Table 1. Device Behavior after Start-Up

| DEVICE | ADD = 0 | ADD PIN FLOATING | ADD = V18 |
|-------------|--|---|--|
| MAX25220/1 | Outputs turned on when start bit in register REG_CTRL is written to 1. | Outputs turned on immediately when EN high. | Outputs turned on when start bit in register REG_CTRL is written to 1. |
| MAX25221B/C | Outputs turned on immediately when EN high. | Outputs turned on immediately when EN high. | Outputs turned on immediately when EN high. |

If the non-volatile memory has been written to previously the stored values are read and the outputs are turned on in the programmed sequence. If the device has not been programmed previously it powers up with the default voltages of 6.8V (AVDD), 12V (V_{GON}) and -10V (V_{GOFF}).

When I²C is used, all values can be programmed and the outputs turned on using the start bit in the REG_CTRL register. The values can subsequently be stored in non-volatile memory using the burn_otp command, if required.

If at any time the internal 1.8V regulator is out of range, the v18oor bit is set in register FAULT2 and the FLTB pin is asserted low, assuming the device is being used in I²C mode. No other action is taken unless the V18 voltage is below its undervoltage lockout level.

Switching Frequency

The switching frequency of the boost and inverting converters and the charge pumps is set using the f_{SW} bit in register CONFIG. When f_{SW} is 0, the switching frequency is 2.1MHz. When f_{SW} is set to 1, the switching frequency is 420kHz. The switching frequency can have spread-spectrum applied to improve EMI performance using the en_ss bit in register CONFIG.

Stand-Alone Operation

Stand-alone operation is used when the device has already been programmed and should start up with the pre-programmed values when power is applied and the EN pin taken high. In stand-alone mode, leave the ADD pin unconnected.

I²C Read-Only Mode

The MAX25221B/C starts up immediately with the preprogrammed values when power is applied and the EN pin taken high. If the ADD pin is connected to V18 the I²C interface is in read-only mode and can only be used to read the device registers, writing is not possible. The 7-bit I²C address of the device is 0x29 (0x53 when the read bit is added) in this

mode.

Source Driver Power Supplies

The source-driver power supplies consist of a boost converter with output switch and an inverting buck-boost converter that generate up to +10.5V maximum and down to -10.5V minimum, respectively, and can deliver up to 200mA on the positive regulator and -200 mA on the negative regulator. The positive source-driver power supply's regulation voltage (AVDD) is set by writing the avdd[5:0] value in the AVDD_SET register using the I²C interface, and can be programmed into non-volatile memory. The default AVDD output voltage is 6.8V.

The negative source-driver supply voltage (NAVDD) is automatically tightly regulated to -AVDD within ±34mV. NAVDD cannot be adjusted independently of AVDD.

The AVDD boost converter is a current-mode converter with two internal switches and internal compensation. The direct output of the converter is HVINP while AVDD is a switched-output version. The NAVDD converter is a current-mode converter with one internal switch, an external diode and internal compensation.

Gate-Driver Power Supplies

The positive gate-driver power supply (VG_{ON}) is a regulated charge-pump tripler and generates up to +20.2V. Note also that the maximum output voltage is $3 \times AVDD - R_{ONTOTAL} \times I_{VGON} \times K$, where $R_{ONTOTAL}$ is typically 30Ω and K is a factor 0.75. In cases where a doubler charge pump is sufficient, set the cp_2stage bit and leave pins FC1- and FC1+ unconnected in order to increase efficiency.

The negative gate-driver power supply (VG_{OFF}) generates a maximum negative voltage of -18.2V and requires external diodes and capacitors. The VG_{ON} and VG_{OFF} blocks switch at the same frequency as the AVDD and NAVDD converters.

Both supplies are capable of output currents up to 15mA, assuming sufficient headroom. The VG_{ON} and VG_{OFF} regulation voltages are set by writing the vgon[5:0] and vgo[5:0] values in the register map using the I²C interface, and can be stored in the non-volatile section of the register map.

Sequencing

The power-on and power-off sequences are controlled by the seq_set[2:0] bits in the VCOM_L register. The setting should be written before the sequence is to be executed and should not be changed during the turn-on or turn-off sequences. The sequence options are as follows:

Table 2. Available Sequences

| Sequence No. | SEQUENCE SET BITS | | | POWER-ON | | | | POWER-OFF (REVERSE-ORDER OF POWER-ON) | | | | NOTES |
|--------------|-------------------|----------|----------|-------------------|-------------------|----------------------------|-----------------------------|---------------------------------------|-------------------|-------------------|-------------------|-----------------|
| | seq_set2 | seq_set1 | seq_set0 | 1st | 2nd after t1 ms | 3rd after t2 ms | 4th after t3 ms | 1st | 2nd after t3 ms | 3rd after t2 ms | 4th after t1 ms | |
| 1 | 0 | 0 | 0 | AVDD | NAVDD | VG _{OFF} | VG _{ON} / VCOM | VG _{ON} / VCOM | VG _{OFF} | NAVDD | AVDD | |
| 2 | 0 | 0 | 1 | AVDD | NAVDD | VG _{ON} | VG _{OFF} / VCOM | VG _{OFF} / VCOM | VG _{ON} | NAVDD | AVDD | |
| 3 | 0 | 1 | 0 | NAVDD | AVDD | VG _{OFF} | VG _{ON} / VCOM | VG _{ON} / VCOM | VG _{OFF} | AVDD | NAVDD | Default setting |
| 4 | 0 | 1 | 1 | NAVDD | AVDD | VG _{ON} | VG _{OFF} / VCOM | VG _{OFF} / VCOM | VG _{ON} | AVDD | NAVDD | |
| 5 | 1 | 0 | 0 | NAVDD | VG _{OFF} | AVDD | VG _{ON} / VCOM | VG _{ON} / VCOM | AVDD | VG _{OFF} | NAVDD | |
| 6 | 1 | 0 | 1 | VG _{OFF} | VG _{ON} | NAVDD | AVDD/ VCOM | AVDD/ VCOM | NAVDD | VG _{ON} | VG _{OFF} | |
| 7 | 1 | 1 | 0 | AVDD/ NAVDD | VG _{OFF} | VG _{ON} / VCOM | - | VG _{ON} / VCOM | VG _{OFF} | AVDD/ NAVDD | - | |

Table 2. Available Sequences (continued)

| | | | | | | | | | | | | |
|---|---|---|---|----------------|------|-----------------------------|---|-----------------------------|------|----------------|---|--|
| 8 | 1 | 1 | 1 | AVDD/ NAVDD | VGON | VG _{OFF} / VCOM | - | VG _{OFF} / VCOM | VGON | AVDD/ NAVDD | - | |
|---|---|---|---|----------------|------|-----------------------------|---|-----------------------------|------|----------------|---|--|

The times in the above table are determined by the delay1, delay2 and delay3 settings in the DELAY-VCOM_LSB register. The fastest power-up is obtained by setting the delays to 0.

The output voltages are not monitored during off sequencing; each output is turned off in turn using the programmed delays. When the delays are set to zero, outputs are turned off in sequence with 1ms delays. A sequence can be stored in non-volatile memory by writing to the burn_otp_reg register.

The V18 linear regulator is powered down 200ms after the power-down sequence is complete. After this time, the device is in shut-down mode and can be restarted by setting the EN input high.

Sequencing Diagram

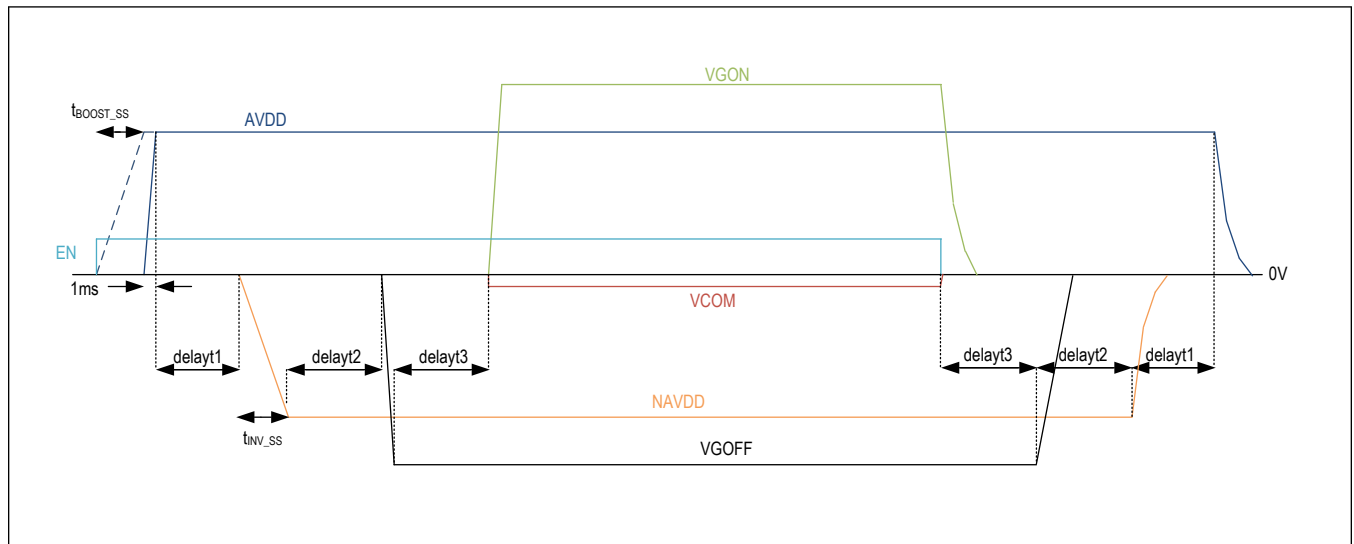


Figure 1. Sequencing Example (Sequence 1, Not to Scale)

VCOM Buffer

The VCOM output voltage is programmed using I²C to a value between -2.49V and +1V. The 9-bit value can also be stored in non-volatile memory. The most-significant bits of the VCOM voltage setting are in the VCOM25 register while the least-significant bit is the vcom25_0 bit in the DELAY-DELAYVCOM_LSB register.

The VCOM buffer can output peak currents up to ±120mA. If the VCOM output voltage deviates from the set value by more than 0.25V, a VCOM fault is detected and flagged with the vcom_flt bit in the FAULT2 register. When this fault is detected, the VCOM buffer continues to function—it is not automatically disabled. Note that a fault condition can lead to high power dissipation in the VCOM buffer and could lead to thermal shutdown of the entire device. If the VCOM buffer is continuously in current limit for more than the time set by tfault[1:0], it is disabled together with the AVDD, NAVDD, VG_H and VG_L outputs to avoid damage to the IC. Also in this case the vcom_flt bit is set.

The maximum capacitive load on the VCOM output is 10nF. If higher capacitance loads are used, a series resistor should be employed to maintain stability.

To calculate the value to write to the VCOM25 register use the following equation:

$$VCOM25 = \frac{V_{COM} + 2.49}{0.00683}$$

The correspondence between the VCOM set value and the VCOM voltage is shown in table 2.

Table 3. VCOM Settings

| VCOM25 REGISTER VALUE | VCOM VOLTAGE (V) |
|-----------------------|------------------|
| 0x1FF | 1 |
| 0x1FE | 0.9932 |
| ... | ... |
| 0x16E | +0.0098 |
| 0x16D | +0.003 |
| 0x16C | -0.0039 |
| ... | ... |
| 0x002 | -2.4763 |
| 0x001 | -2.4832 |
| 0x000 | -2.49 |

VCOMN Negative Power Supply

A linear regulator is implemented to derive a regulated -3.5V for the VCOM buffer from the NAVDD supply. The npn transistor connected to the VCB pin acts as the pass transistor of the regulator. The peak output current of the regulator is the same as the peak negative drive current from the VCOM output, or at least 120mA. The device senses the voltage at VCOMN and regulates it to -3.5V by driving VCB. The peak drive current for the base of the external npn is at least 5mA.

Limiting the Range of VCOM Voltage

When temperature compensation is not enabled, it is possible to limit the excursion of VCOM to a range between the values set in the VCOM_MIN and VCOM_MAX registers. If an attempt is made to write a value outside the set range to VCOM25, the VCOM output voltage is not updated and the I²C interface issues a NACK.

VCOM Temperature Compensation

The VCOM output voltage can be compensated for temperature changes using a temperature-sensitive component (e.g. an NTC thermistor) connected to the TEMP input or an internal temperature sensor. Select the sensor to be used with the int_sensor bit in the CONFIG register (the default configuration is to use the external sensor). The TEMP pin is forced to 625mV and the current drawn from it is mirrored on the RREF pin. The voltage generated due to the resistor on RREF is fed to the internal 8-bit ADC, which has a reference voltage of 1.25V. The input to the ADC is therefore as follows:

$$V_{ADC} = \frac{0.625 \times R_{RREF}}{R_{TEMP}}$$

With reference to [Figure 2](#): $R_{TEMP} = (R_{NTC} \parallel R1) + R2$

The highly non-linear NTC characteristic can be modified depending on which temperature (cold, room, or hot) necessitates the highest resolution. As an example in [Figure 2](#), a reference resistor is connected to RREF while a combination of the NTC and two low-TC resistors R1 and R2 are connected to TEMP. In this way, an ADC reading that is steeper at higher temperatures is obtained, enhancing the resolution of the ADC there. When temperature compensation is enabled, the value of the voltage on the RREF pin is available in the TEMP (0x01) register.

Temperature compensation is enabled by setting the T_comp_en bit in the DELAY-VCOM_LSB register. When T_comp_en is high, the voltage on the RREF pin is measured and the VCOM output voltage is updated at a rate of 1Hz. At start-up, even with temperature compensation enabled, there is a delay before compensation becomes active due to the time needed to sample the temperature. For this reason, the device always starts up with the VCOM25 voltage value on VCOM.

The VCOM value at 25°C is the value written in the VCOM25 register together with the LSB from DELAY-VCOM_LSB register. This value serves as the reference for all other VCOM values. The 5-bit values in the VCOM_L, and VCOM_H1 registers represent the change in VCOM from the VCOM25 value at the temperature represented by an ADC reading of VTEMP_L and VTEMP_H1. The value in the VCOM_H2 register represents the positive shift in VCOM from VCOM_H1. The VCOM_L value represents a negative shift in VCOM while VCOM_H1 and VCOM_H2 represent positive shifts.

NTC Connection Diagram

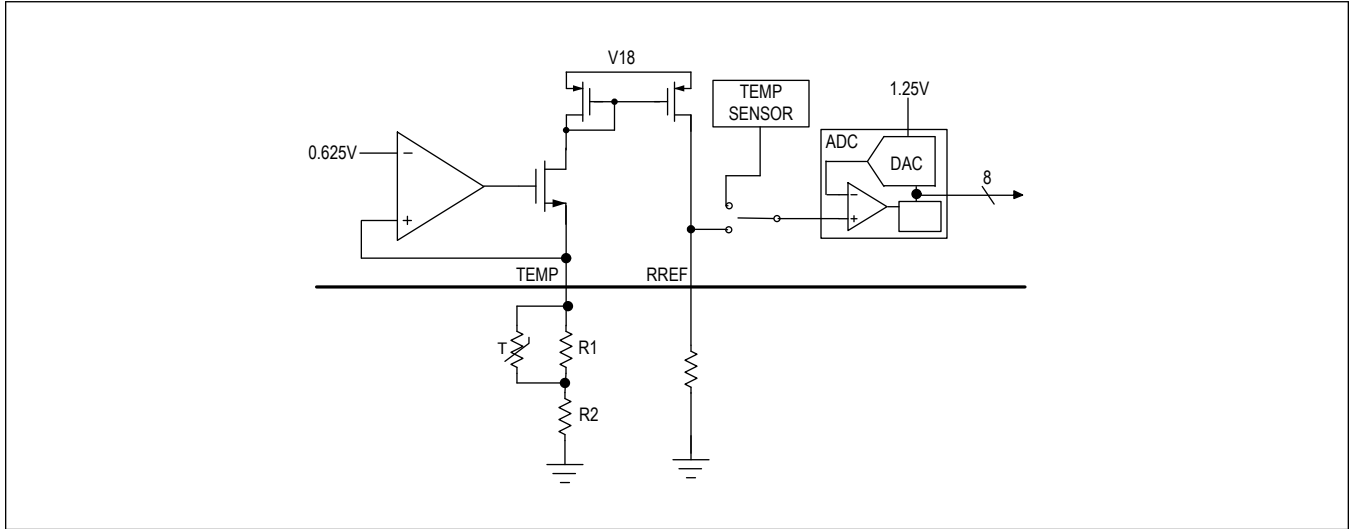


Figure 2. Possible NTC Connection

Internal Temperature Sensor

The internal temperature sensor senses the junction temperature of the IC which may be significantly different from the ambient temperature. To use the internal sensor, set the int_sensor bit in the CONFIG register to 1. The internal temperature sensor has a temperature coefficient of 2mV/°C and a nominal output voltage of 620mV at 25°C.

When the internal temperature sensor is selected, it is connected directly to the ADC input.

Temperature Compensation Curve

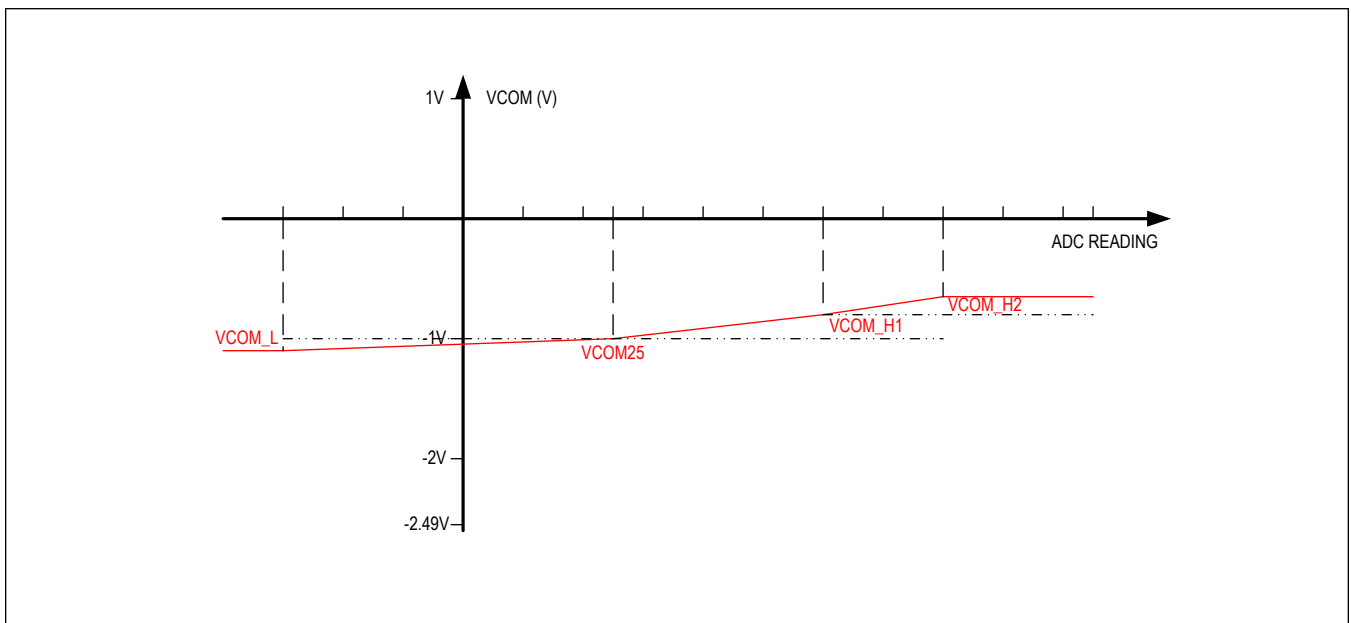


Figure 3. Temperature Compensation Curve

Fault Handling

The reaction to faults is dependent on whether the device is in I²C or stand-alone mode.

In I²C mode, the following faults, if not masked, cause the FLTB pin to assert low: avdd_uv, navdd_uv, vgon_uv, vgoff_uv, vcom_flt, nv_flt, th_shdn, vin_uvlo, and par_err. The th_warn fault is masked by default and must be explicitly enabled using the th_warn_mask bit.

When the ADD pin is left floating (I²C interface not used) the FLTB pin outputs a pulse train of varying duty cycle depending on the detected fault as shown in [Table 4](#).

Table 4. FLTB Duty Cycle in Stand-Alone Mode

| DUTY-CYCLE | FAULT |
|-----------------------|---|
| 75% | VG _{ON} or VG _{OFF} fault |
| 50% | AVDD, NAVDD or HVINP fault |
| 25% | VCOM fault |
| 0% (continuously low) | NV fault or thermal shutdown |

The frequency at the FLTB pin is 1kHz when indicating a fault. If multiple faults are present, the highest-priority fault is indicated. The list above is in order of priority with the highest priority listed last.

Undervoltage Faults on Source and Gate Outputs

When an undervoltage is detected on any of the AVDD, NAVDD, VG_{ON}, or VG_{OFF} outputs, all of the outputs are turned off and the appropriate fault bit is set in the FAULT1 register. At the same time, the FLTB pin asserts low. Depending on the setting of the tretry[1:0] bits, the subsequent behavior of the device is as follows:

- tretry = 01, 10 or 11: After 0.95s or 1.9s a retry is performed where all outputs are turned on in the appropriate sequence. If the fault is still present, the output will be disabled again after tfault[1:0]. A total of three retries are performed, after which no further retry attempts are performed (the device can be restarted by toggling power or the EN pin or by using the RESTART command). If tretry = 11 retries continue until the fault is removed and normal function can resume.
- tretry = 00: No retry is attempted (the device can be restarted by toggling power or the EN pin or by using the RESTART command).

If a short-circuit is encountered during start-up, device operation is halted, all outputs are disabled, and the subsequent behavior depends on the setting of retry[1:0] as described above. The short-circuit checks on VG_{ON} and VG_{OFF} are enabled 1ms after the pins are enabled. The C version does not have short-circuit checks on VG_{ON} and VG_{OFF}.

During retry, faults are no longer monitored and the fault or faults which caused retry are indicated using the corresponding fault bits. During retry, the FLTB pin asserts low unless the fault which caused the retry is masked.

Thermal Warning and Shutdown

When the junction temperature reaches 125°C, the thermal warning bit is set. The device takes no further action.

If the device junction temperature reaches 160°C, all outputs are turned off immediately. When the junction temperature drops by 15°C, the outputs are re-enabled using the stored sequence.

NV Memory

The MAX25220/MAX25221/MAX25221B/MAX25221C include six blocks of one-time-programmable memory (the number of writes performed so far can be read from nv_count[2:0] in the REG_CTRL register). The user can store the block of volatile registers from 0x07 to 0x15 in non-volatile memory which is in turn mapped to register locations 0x17 to 0x25. Note that before the non-volatile memory has been programmed, a read from the locations 0x17 to 0x25 yields the result 0xFF.

The contents of the non-volatile memory are protected by a single-error correction/double-error detection (SECEDED) redundant code while data transfer from non-volatile memory to registers 0x07 to 0x15 is protected by a parity check. If the parity check fails, a retry is performed two times. If all three attempts are unsuccessful, the device does not start up, the nv_flt bit is set, and the FLTB pin is asserted low. If the SECEDED check fails, the device does not start up, the nv_flt bit is set, and the FLTB pin is asserted low.

If there are no errors, the outputs are turned on with the stored values and in the stored sequence.

To store the contents of registers 0x07 to 0x15 to non-volatile memory a voltage source of 8.5V ±2% capable of supplying more than 25mA should be connected to the V_{PROG} pin. When the V_{PROG} voltage is stable an I²C NV write command can be performed by writing to the burn_otp_reg register. If the NV write is unsuccessful (because the V_{PROG} voltage was out of range or because of a general memory error) the nv_flg bit is set, FLTB pin goes low. After an NV write command is executed, the nv_flg bit should be checked. If nv_flg is high another NV write can be attempted.

Connect V_{PROG} to GND if non-volatile memory is not used.

Ensure that temperature compensation is disabled when programming VCOM.

Auto-Refresh Function

When the refresh bit in register CONFIG is set, the device reads from the non-volatile registers at intervals of 1s and writes the data into the corresponding volatile registers. This avoids the effect of possible corruption of the volatile registers. Auto-refresh reads are subject to error correction in the same way as the initial read after device power-up.

When programming the non-volatile memory, the auto-refresh function should be enabled immediately before performing the burn_otp_reg write. See the section *Using the NV Memory* in [Applications Information](#).

BURN, REBOOT and RESTART Commands

The BURN and REBOOT commands are used to store the contents of registers 0x07 to 0x15 in non-volatile memory or to fetch the contents of non-volatile memory and load them into registers 0x07 to 0x15, respectively. The RESTART command is used to restart the device from a latched-fault mode. When a RESTART command is performed, all fault bits are cleared.

A BURN command is performed by writing to register address 0x78 (burn_otp_reg).

A REBOOT command is performed by writing to register address 0x79 (reboot_otp_reg).

A RESTART command is performed by writing to register address 0x7A (soft_restart).

When parity checking is enabled and one of these user commands is sent to the device, the third byte should be such as to have even parity over the 3 bytes sent.

I²C Interface

The MAX25220/MAX25221/MAX25221B/MAX25221C include an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus.

The Slave ID of the MAX25220/MAX25221/MAX25221B/MAX25221C depends on the connection of the ADD pin according to Table 4.

A master device communicates with the MAX25220/MAX25221/MAX25221B/MAX25221C by transmitting the correct Slave ID with appended R/W bit, followed by the register address and data word (for a write transaction only). Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition, and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The IC's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 1kΩ is required on the SDA bus. In general, the resistor should be selected as a function of bus capacitance such that the rise time on the bus is not greater than 120ns. The IC's SCL line operates as an input only. A pullup resistor greater than 1kΩ is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. In general, for the SCL-line resistor selection, the same recommendations as for SDA apply. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

I²C Slave Addresses

Table 5. I²C Slave Addresses

| ADD PIN CONNECTION | DEVICE ADDRESS | | | | | | | WRITE ADDRESS | READ ADDRESS |
|--------------------|----------------|----|----|----|----|----|----|---------------|--------------|
| | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| | | | | | | | | | |

Table 5. I²C Slave Addresses (continued)

| | | | | | | | | | |
|-----|---|---|---|---|---|---|---|-------|------|
| GND | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0x42 | 0x43 |
| V18 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0x52* | 0x53 |

* On the MAX25221B/C, writing to the device is not possible when ADD is connected to V18.

Parity Checking

Even parity checking for write transactions can be enabled by setting the par_en bit in REG_CTRL to 1. The parity bit is the most-significant bit of the register address byte and should be set to attain even parity. The parity check is performed over all 3 bytes received by the device: the slave address, the register address, and the data payload. Burst-mode write is not supported when parity checking is enabled; a complete I²C transaction is needed to write to each single register. When a parity bit error is detected the par_err bit is set, the I²C interface issues a NACK and no write is performed.

When writing any of the BURN, REBOOT, and RESTART commands, parity must be adjusted by changing the third or payload byte; the command byte must not be changed.

Register Map

MAX25220/MAX25221/MAX25221B/MAX25221C

| ADDRESS | NAME | MSB | | | | | | | LSB |
|-----------------------|--|------------------|--------------|-----------------|-----------------|-----------------|--------------|----------------|---------------|
| USER REGISTERS | | | | | | | | | |
| 0x00 | DEVICE[7:0] | - | - | dev_id[5:0] | | | | | |
| 0x01 | TEMP[7:0] | temp[7:0] | | | | | | | |
| 0x02 | REG_CTRL[7:0] | par_en | start | nv_count[2:0] | | | rev_id[2:0] | | |
| 0x03 | FLTMASK1[7:0] | - | avdd_uv_mask | - | navdd_uv_mask | - | vgon_uv_mask | - | vgoff_uv_mask |
| 0x04 | FLTMASK2[7:0] | - | par_err_mask | vin_uvlo_mask | hvinp_uv_mask | - | - | vcom_fit_mask | th_warn_mask |
| 0x05 | FAULT1[7:0] | - | avdd_uv | - | navdd_uv | - | vgon_uv | - | vgoff_uv |
| 0x06 | FAULT2[7:0] | v18oor | par_err | vin_uvlo | hvinp_uv | th_shdn | nv_fit | vcom_fit | th_warn |
| 0x07 | CONFIG[7:0] | int_sensor | refresh | en_ss | fSW | tretry[1:0] | | tfault[1:0] | |
| 0x08 | DELAY-VCOM_LSB[7:0] | delayt1[1:0] | | delayt2[1:0] | | delayt3[1:0] | | T_comp_en | vcom25_0 |
| 0x09 | VCOM25[7:0] | vcom25[7:0] | | | | | | | |
| 0x0A | VCOM_L[7:0] | seq_set[2:0] | | | vcom_l[4:0] | | | | |
| 0x0B | VCOM_H1[7:0] | - | - | - | vcom_h1[4:0] | | | | |
| 0x0C | VCOM_H2[7:0] | - | - | - | vcom_h2[4:0] | | | | |
| 0x0D | VTEMP25[7:0] | vtemp25[7:0] | | | | | | | |
| 0x0E | VTEMP_L[7:0] | vtemp_l[7:0] | | | | | | | |
| 0x0F | VTEMP_H1[7:0] | vtemp_h1[7:0] | | | | | | | |
| 0x10 | VTEMP_H2[7:0] | vtemp_h2[7:0] | | | | | | | |
| 0x11 | VCOM_MIN[7:0] | vcom_min[7:0] | | | | | | | |
| 0x12 | VCOM_MAX[7:0] | vcom_max[7:0] | | | | | | | |
| 0x13 | AVDD_SET[7:0] | - | - | avdd[5:0] | | | | | |
| 0x14 | VGON[7:0] | - | cp_2stage | vgon[5:0] | | | | | |
| 0x15 | VGOFF[7:0] | - | - | vgoff[5:0] | | | | | |
| 0x17 | NV_CONFIG[7:0] | nv_int_sensor | nv_refresh | nv_en_ss | nv_fSW | nv_retry[1:0] | | nv_tfault[1:0] | |
| 0x18 | NV_DELAY-VCOM_LSB[7:0] | nv_delayt1[1:0] | | nv_delayt2[1:0] | | nv_delayt3[1:0] | | nv_T_comp_en | nv_vcom25_0 |
| 0x19 | NV_VCOM25[7:0] | nv_vcom25[7:0] | | | | | | | |
| 0x1A | NV_VCOM_L[7:0] | nv_seq_set[2:0] | | | nv_vcom_l[4:0] | | | | |
| 0x1B | NV_VCOM_H1[7:0] | - | - | - | nv_vcom_h1[4:0] | | | | |
| 0x1C | NV_VCOM_H2[7:0] | - | - | - | nv_vcom_h2[4:0] | | | | |
| 0x1D | NV_VTEMP25[7:0] | nv_vtemp25[7:0] | | | | | | | |
| 0x1E | NV_VTEMP_L[7:0] | nv_vtemp_l[7:0] | | | | | | | |
| 0x1F | NV_TEMP_H1[7:0] | nv_vtemp_h1[7:0] | | | | | | | |
| 0x20 | NV_TEMP_H2[7:0] | nv_vtemp_h2[7:0] | | | | | | | |

| ADDRESS | NAME | MSB | | | | | | LSB |
|----------------------|-------------------------------------|-----|------------------|--|--|--|--|-------------------|
| 0x21 | NV_VCOM_MIN[7:0] | | | | | | | nv_vcom_min[7:0] |
| 0x22 | NV_VCOM_MAX[7:0] | | | | | | | nv_vcom_max[7:0] |
| 0x23 | NV_AVDD_SET[7:0] | – | – | | | | | nv_avdd[5:0] |
| 0x24 | NV_VGON[7:0] | – | nv_cp_2 stage | | | | | nv_vgon[5:0] |
| 0x25 | NV_VGOFF[7:0] | – | – | | | | | nv_vgoff[5:0] |
| USER COMMANDS | | | | | | | | |
| 0x78 | burn_otp_reg[7:0] | | | | | | | burn_otp[7:0] |
| 0x79 | reboot_otp_reg[7:0] | | | | | | | reboot_otp[7:0] |
| 0x7A | soft_restart[7:0] | | | | | | | soft_restart[7:0] |

Register Details

[DEVICE \(0x00\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------------|---|------|---|--------------------------|---|---|---|-------------|--|
| Field | – | – | | | | | | dev_id[5:0] | |
| Reset | – | – | | | | | | | |
| Access Type | – | – | | | | | | Read Only | |
| BITFIELD | | BITS | | DESCRIPTION | | | | | |
| dev_id | | 5:0 | | Device ID. Reads 0x20/21 | | | | | |

[TEMP \(0x01\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------------|---|------|---|--|---|---|---|-----------|--|
| Field | | | | | | | | temp[7:0] | |
| Reset | | | | | | | | 0x0 | |
| Access Type | | | | | | | | Read Only | |
| BITFIELD | | BITS | | DESCRIPTION | | | | | |
| temp | | 7:0 | | Voltage reading from R _{REF} pin. | | | | | |

[REG_CTRL \(0x02\)](#)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------------|-------------|-------------|---|--|---|---|-------------|---|--|
| Field | par_en | start | | nv_count[2:0] | | | rev_id[2:0] | | |
| Reset | 0x0 | 0x0 | | | | | 0x1 | | |
| Access Type | Write, Read | Write, Read | | Read Only | | | Read Only | | |
| BITFIELD | | BITS | | DESCRIPTION | | | | | |
| par_en | | 7 | | Parity enable bit. When 1 this bit enables parity checking on write transactions to the device. | | | | | |
| start | | 6 | | Enable bit. When this bit is set to 1, the turn-on sequence set using the seq_set bits is executed. The default value of this bit is 0, except in the B/C version where it is 1. | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---|
| nv_count | 5:3 | This field indicates the total number of writes to non-volatile memory. The maximum value is 6. |
| rev_id | 2:0 | Revision ID. Reads 0x1. |

FLTMASK1 (0x03)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------|---|---------------|---|--------------|---|---------------|
| Field | – | avdd_uv_mask | – | navdd_uv_mask | – | vgon_uv_mask | – | vgoff_uv_mask |
| Reset | – | 0x0 | – | 0x0 | – | 0x0 | – | 0x0 |
| Access Type | – | Write, Read | – | Write, Read | – | Write, Read | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|--|
| avdd_uv_mask | 6 | When 1 this bit prevents an undervoltage on AVDD from asserting FLTB low. |
| navdd_uv_mask | 4 | When 1 this bit prevents an undervoltage on NAVDD from asserting FLTB low. |
| vgon_uv_mask | 2 | When 1 this bit prevents an undervoltage on VGON from asserting FLTB low. |
| vgoff_uv_mask | 0 | When 1 this bit prevents an undervoltage on VGOFF from asserting FLTB low. |

FLTMASK2 (0x04)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------|---------------|---------------|---|---|---------------|--------------|
| Field | – | par_err_mask | vin_uvlo_mask | hvinp_uv_mask | – | – | vcom_fit_mask | th_warn_mask |
| Reset | – | 0x0 | 0x0 | 0x0 | – | – | 0x0 | 0x1 |
| Access Type | – | Write, Read | Write, Read | Write, Read | – | – | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---------------|------|--|
| par_err_mask | 6 | When 1 prevents parity errors from asserting the FLTB pin. |
| vin_uvlo_mask | 5 | When 1 this bit prevents an undervoltage on IN from asserting the FLTB pin. |
| hvinp_uv_mask | 4 | Mask bit for hvinp_uv diagnostic. When 1 an undervoltage on HVINP does not cause FLTB to assert. |
| vcom_fit_mask | 1 | When 1 this bit prevents a fault on VCOM from asserting FLTB low. |
| th_warn_mask | 0 | When 1 this bit prevents an overtemperature warning from asserting FLTB low. |

FAULT1 (0x05)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------------|---|--------------------|---|--------------------|---|--------------------|
| Field | – | avdd_uv | – | navdd_uv | – | vgon_uv | – | vgoff_uv |
| Reset | – | 0x0 | – | 0x0 | – | 0x0 | – | 0x0 |
| Access Type | – | Read Clears All | – | Read Clears All | – | Read Clears All | – | Read Clears All |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| avdd_uv | 6 | When 1 this bit indicates an undervoltage on AVDD. |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| navdd_uv | 4 | When 1 this bit indicates an undervoltage on NAVDD. |
| vgon_uv | 2 | When 1 this bit indicates an undervoltage on VG _{ON} . |
| vgoff_uv | 0 | When 1 this bit indicates an undervoltage on VG _{OFF} . |

FAULT2 (0x06)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Field | v18oor | par_err | vin_uvlo | hvinp_uv | th_shdn | nv_fit | vcom_fit | th_warn |
| Reset | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 |
| Access Type | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All | Read Clears All |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| v18oor | 7 | Indicates that the 1.8V output is out of range, either above its overvoltage level or below its undervoltage level. |
| par_err | 6 | Indicates that a parity error was detected on an I ² C transaction. |
| vin_uvlo | 5 | Indicates an undervoltage condition on the IN pin. When this happens the device turns off all outputs and waits for IN to return above the IN UVLO level, after which the outputs are re-enabled in the programmed sequence. |
| hvinp_uv | 4 | When 1 this bit indicates an undervoltage on the boost output, HVINP. |
| th_shdn | 3 | When 1 this bit indicates an overtemperature shutdown. |
| nv_fit | 2 | Non-volatile memory failure - unsuccessful transfer of the contents of NV memory to working memory or more than one error detected. |
| vcom_fit | 1 | When 1 indicates a fault on the VCOM output either due to it being 0.25V away from its set value (unfiltered) or because the VCOM buffer was in current limit for a time t _{fault} . |
| th_warn | 0 | When 1 this bit indicates a thermal warning. |

CONFIG (0x07)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|---|-------------|---|
| Field | int_sensor | refresh | en_ss | fSW | tretry[1:0] | | tfault[1:0] | |
| Reset | 0x0 | 0x0 | 0x0 | 0x0 | 0x1 | | 0x0 | |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|------------|------|--|---|
| int_sensor | 7 | Set this bit to 1 to use the internal temperature sensor. | |
| refresh | 6 | When this bit is 1 the contents of the NV registers are automatically copied to the volatile registers every second. | 0x0: Refresh disabled. 0x1: Refresh enabled. |
| en_ss | 5 | Enable spread-spectrum by setting this bit to 1. | |
| fSW | 4 | Sets switching frequency. | 0x0: 2.1MHz 0x1: 420kHz |
| tretry | 3:2 | Sets retry time after a fault. | 0x0: Retry disabled 0x1: Retry after 0.95s, total 3 retries. 0x2: Retry after 1.9s, total 3 retries. 0x3: Retry after 1.9s |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|------------------------|--|
| tfault | 1:0 | Sets fault delay time. | 0x0: 15ms 0x1: 30ms 0x2: 60ms 0x3: 90ms |

DELAY-VCOM_LSB (0x08)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|-------------|---|-------------|---|-------------|-------------|
| Field | delay1[1:0] | | delay2[1:0] | | delay3[1:0] | | T_comp_en | vcom25_0 |
| Reset | 0x2 | | 0x2 | | 0x2 | | 0x0 | 0x0 |
| Access Type | Write, Read | | Write, Read | | Write, Read | | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|-----------|------|---|
| delay1 | 7:6 | Set delay t1 in the start-up sequence. Choose between 0, 5ms, 10ms and 15ms. |
| delay2 | 5:4 | Set delay t2 in the start-up sequence. Choose between 0, 5ms, 10ms and 15ms. |
| delay3 | 3:2 | Set delay t3 in the start-up sequence. Choose between 0, 5ms, 10ms and 15ms. |
| T_comp_en | 1 | When 1 this bit enables temperature compensation of the output of the VCOM amplifier. |
| vcom25_0 | 0 | LSB of VCOM setting at 25°C. |

VCOM25 (0x09)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field | vcom25[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-----------------------|
| vcom25 | 7:0 | VCOM setting at 25°C. |

VCOM_L (0x0A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|-------------|---|---|---|---|
| Field | seq_set[2:0] | | | vcom_l[4:0] | | | | |
| Reset | 0x2 | | | 0x00 | | | | |
| Access Type | Write, Read | | | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|--|
| seq_set | 7:5 | Sequence selection bits. | 0x0: Sequence 1. 0x1: Sequence 2. 0x2: Sequence 3. 0x3: Sequence 4. 0x4: Sequence 5. 0x5: Sequence 6. 0x6: Sequence 7. 0x7: Sequence 8. |
| vcom_l | 4:0 | Delta VCOM at the temperature corresponding to VTEMP_L. This value sets the difference between the VCOM value at 25°C and that at VTEMP_L. | |

VCOM_H1 (0x0B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|--------------|---|---|---|---|
| Field | – | – | – | vcom_h1[4:0] | | | | |
| Reset | – | – | – | 0x00 | | | | |
| Access Type | – | – | – | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---|
| vcom_h1 | 4:0 | Delta VCOM at VTEMP_H1. This value sets the difference between the VCOM value at 25°C and that at VTEMP_H1. |

VCOM_H2 (0x0C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|--------------|---|---|---|---|
| Field | – | – | – | vcom_h2[4:0] | | | | |
| Reset | – | – | – | 0x0 | | | | |
| Access Type | – | – | – | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|---|
| vcom_h2 | 4:0 | Delta VCOM at VTEMP_H2. This value sets the difference between the VCOM value at VTEMP_H1 and that at VTEMP_H2. |

VTEMP25 (0x0D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field | vtemp25[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|------------------------------|
| vtemp25 | 7:0 | Voltage at TEMP pin at 25°C. |

VTEMP_L (0x0E)

| | | | | | | | | |
|--------------------|--------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | vtemp_l[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-----------------|-------------|---|
| vtemp_l | 7:0 | Voltage at TEMP pin corresponding to low-temperature breakpoint in VCOM compensation curve. |

VTEMP_H1 (0x0F)

| | | | | | | | | |
|--------------------|---------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | vtemp_h1[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-----------------|-------------|--|
| vtemp_h1 | 7:0 | Voltage at TEMP pin corresponding to first high-temperature breakpoint in VCOM compensation curve. |

VTEMP_H2 (0x10)

| | | | | | | | | |
|--------------------|---------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | vtemp_h2[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-----------------|-------------|---|
| vtemp_h2 | 7:0 | Voltage at TEMP pin corresponding to second high-temperature breakpoint in VCOM compensation curve. |

VCOM_MIN (0x11)

| | | | | | | | | |
|--------------------|---------------|----------|----------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | vcom_min[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-----------------|-------------|-------------------------------|
| vcom_min | 7:0 | Lower limit for VCOM setting. |

VCOM_MAX (0x12)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Field | vcom_max[7:0] | | | | | | | |
| Reset | 0xFF | | | | | | | |
| Access Type | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|-------------------------------|
| vcom_max | 7:0 | Upper limit for VCOM setting. |

AVDD_SET (0x13)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------|---|---|---|---|---|
| Field | – | – | avdd[5:0] | | | | | |
| Reset | – | – | 0x1A | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------------------------|---|
| avdd | 5:0 | Sets AVDD and NAVDD voltages. | 0x0: 4.2 0x1: 4.3 0x2: 4.4 0x3: 4.5 0x4: 4.6 0x5: 4.7 0x6: 4.8 0x7: 4.9 0x8: 5 0x9: 5.1 0xA: 5.2 0xB: 5.3 0xC: 5.4 0xD: 5.5 0xE: 5.6 0xF: 5.7 0x10: 5.8 0x11: 5.9 0x12: 6 0x13: 6.1 0x14: 6.2 0x15: 6.3 0x16: 6.4 0x17: 6.5 0x18: 6.6 0x19: 6.7 0x1A: 6.8 0x1B: 6.9 0x1C: 7V 0x1D: 7.1 0x1E: 7.2 0x1F: 7.3 0x20: 7.4 0x21: 7.5 0x22: 7.6 0x23: 7.7 0x24: 7.8 0x25: 7.9 0x26: 8 0x27: 8.1 0x28: 8.2 0x29: 8.3 0x2A: 8.4 0x2B: 8.5 0x2C: 8.6 0x2D: 8.7 0x2E: 8.8 0x2F: 8.9 0x30: 9 0x31: 9.1 0x32: 9.2 0x33: 9.3 0x34: 9.4 0x35: 9.5 0x36: 9.6 0x37: 9.7 0x38: 9.8 0x39: 9.9 0x3A: 10 |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 0x3B: 10.1 0x3C: 10.2 0x3D: 10.3 0x3E: 10.4 0x3F: 10.5 |

VGON (0x14)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|------|---|-------------|---|---|---|---|---|
| Field | – | cp_2stage | vgon[5:0] | | | | | |
| Reset | – | 0x0 | 0x16 | | | | | |
| Access Type | – | Write, Read | Write, Read | | | | | |
| BITFIELD | BITS | DESCRIPTION | DECODE | | | | | |
| cp_2stage | 6 | Set this bit to 1 when using a two-stage charge-pump. | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--------------------------------|--|
| vgon | 5:0 | Sets VG _{ON} voltage. | 0x0: 7.6 0x1: 7.8 0x2: 8 0x3: 8.2 0x4: 8.4 0x5: 8.6 0x6: 8.8 0x7: 9 0x8: 9.2 0x9: 9.4 0xA: 9.6 0xB: 9.8 0xC: 10 0xD: 10.2 0xE: 10.4 0xF: 10.6 0x10: 10.8 0x11: 11 0x12: 11.2 0x13: 11.4 0x14: 11.6 0x15: 11.8 0x16: 12 0x17: 12.2 0x18: 12.4 0x19: 12.6 0x1A: 12.8 0x1B: 13 0x1C: 13.2 0x1D: 13.4 0x1E: 13.6 0x1F: 13.8 0x20: 14 0x21: 14.2 0x22: 14.4 0x23: 14.6 0x24: 14.8 0x25: 15 0x26: 15.2 0x27: 15.4 0x28: 15.6 0x29: 15.8 0x2A: 16 0x2B: 16.2 0x2C: 16.4 0x2D: 16.6 0x2E: 16.8 0x2F: 17 0x30: 17.2 0x31: 17.4 0x32: 17.6 0x33: 17.8 0x34: 18 0x35: 18.2 0x36: 18.4 0x37: 18.6 0x38: 18.8 0x39: 19 0x3A: 19.2 |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|--|
| | | | 0x3B: 19.4 0x3C: 19.6 0x3D: 19.8 0x3E: 20 0x3F: 20.2 |

VG OFF (0x15)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------|---|---|---|---|---|
| Field | – | – | vgoff[5:0] | | | | | |
| Reset | – | – | 0x16 | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|--|---|
| vgoff | 5:0 | Sets V _{G_{OFF}} voltage. | 0x0: -5.6 0x1: -5.8 0x2: -6 0x3: -6.2 0x4: -6.4 0x5: -6.6 0x6: -6.8 0x7: -7 0x8: -7.2 0x9: -7.4 0xA: -7.6 0xB: -7.8 0xC: -8 0xD: -8.2 0xE: -8.4 0xF: -8.6 0x10: -8.8 0x11: -9 0x12: -9.2 0x13: -9.4 0x14: -9.6 0x15: -9.8 0x16: -10 0x17: -10.2 0x18: -10.4 0x19: -10.6 0x1A: -10.8 0x1B: -11 0x1C: -11.2 0x1D: -11.4 0x1E: -11.6 0x1F: -11.8 0x20: -12 0x21: -12.2 0x22: -12.4 0x23: -12.6 0x24: -12.8 0x25: -13 0x26: -13.2 0x27: -13.4 0x28: -13.6 0x29: -13.8 0x2A: -14 0x2B: -14.2 0x2C: -14.4 0x2D: -14.6 0x2E: -14.8 0x2F: -15 0x30: -15.2 0x31: -15.4 0x32: -15.6 0x33: -15.8 0x34: -16 0x35: -16.2 0x36: -16.4 0x37: -16.6 0x38: -16.8 0x39: -17 0x3A: -17.2 |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|----------|------|-------------|---|
| | | | 0x3B: -17.4 0x3C: -17.6 0x3D: -17.8 0x3E: -18 0x3F: -18.2 |

NV_CONFIG (0x17)

Non-volatile configuration register

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---------------|------------|-----------|-----------|---------------|---|----------------|---|
| Field | nv_int_sensor | nv_refresh | nv_en_ss | nv_fSW | nv_retry[1:0] | | nv_tfault[1:0] | |
| Reset | | | | | | | | |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | | Read Only | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---------------|------|--|----------------------------|
| nv_int_sensor | 7 | When this bit is 1 the internal temperature sensor is used. | |
| nv_refresh | 6 | When this bit is 1 the contents of the NV registers are automatically copied to the volatile registers every second. | |
| nv_en_ss | 5 | When this bit is 1 spread-spectrum is enabled. | |
| nv_fSW | 4 | Sets switching frequency. | 0x0: 2.2MHz 0x1: 440kHz |
| nv_retry | 3:2 | Sets retry time after a fault. | |
| nv_tfault | 1:0 | Sets retry time after a fault. | |

NV_DELAY-VCOM_LSB (0x18)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|----------------|---|----------------|---|----------------|---|--------------|-------------|
| Field | nv_delay1[1:0] | | nv_delay2[1:0] | | nv_delay3[1:0] | | nv_T_comp_en | nv_vcom25_0 |
| Reset | | | | | | | 0x0 | |
| Access Type | Read Only | | Read Only | | Read Only | | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION |
|--------------|------|---|
| nv_delay1 | 7:6 | Set delay t1 in the start-up sequence. Choose between 0, 5ms, 10ms and 15ms. |
| nv_delay2 | 5:4 | Set delay t2 in the start-up sequence. Choose between 0, 5ms, 10ms and 15ms. |
| nv_delay3 | 3:2 | Set delay t3 in the start-up sequence. Choose between 0, 5ms, 10ms and 15ms. |
| nv_T_comp_en | 1 | When 1 this bit enables temperature compensation of output of the VCOM amplifier. |
| nv_vcom25_0 | 0 | When 1 this bit enables temperature compensation of output of the VCOM amplifier. |

NV_VCOM25 (0x19)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---|---|---|---|---|---|
| Field | nv_vcom25[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-----------|------|-----------------------|
| nv_vcom25 | 7:0 | VCOM setting at 25°C. |

NV_VCOM_L (0x1A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|---|----------------|-----------|---|---|---|
| Field | nv_seq_set[2:0] | | | nv_vcom_l[4:0] | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | Read Only | | | |

| BITFIELD | BITS | DESCRIPTION |
|------------|------|--|
| nv_seq_set | 7:5 | Sequence selection bits. |
| nv_vcom_l | 4:0 | Delta VCOM at the temperature corresponding to VTEMP_L. This value sets the difference between the VCOM value at 25°C and that at VTEMP_L. |

NV_VCOM_H1 (0x1B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|-----------------|---|---|---|---|
| Field | – | – | – | nv_vcom_h1[4:0] | | | | |
| Reset | – | – | – | | | | | |
| Access Type | – | – | – | Read Only | | | | |

| BITFIELD | BITS | DESCRIPTION |
|------------|------|---|
| nv_vcom_h1 | 4:0 | Delta VCOM at VTEMP_H1. This value sets the difference between the VCOM value at 25°C and that at VTEMP_H1. |

NV_VCOM_H2 (0x1C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|-----------------|---|---|---|---|
| Field | – | – | – | nv_vcom_h2[4:0] | | | | |
| Reset | – | – | – | | | | | |
| Access Type | – | – | – | Read Only | | | | |

| BITFIELD | BITS | DESCRIPTION |
|------------|------|---|
| nv_vcom_h2 | 4:0 | Delta VCOM at VTEMP_H2. This value sets the difference between the VCOM value at VTEMP_H1 and that at VTEMP_H2. |

NV_VTEMP25 (0x1D)

| | | | | | | | | |
|--------------------|-----------------|----------|------------------------------|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | nv_vtemp25[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| nv_vtemp25 | 7:0 | | Voltage at TEMP pin at 25°C. | | | | | |

NV_VTEMP_L (0x1E)

| | | | | | | | | |
|--------------------|-----------------|----------|---|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | nv_vtemp_l[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| nv_vtemp_l | 7:0 | | Voltage at TEMP pin corresponding to low-temperature breakpoint in VCOM compensation curve. | | | | | |

NV_TEMP_H1 (0x1F)

| | | | | | | | | |
|--------------------|------------------|----------|--|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | nv_vtemp_h1[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| nv_vtemp_h1 | 7:0 | | Voltage at TEMP pin corresponding to first high-temperature breakpoint in VCOM compensation curve. | | | | | |

NV_TEMP_H2 (0x20)

| | | | | | | | | |
|--------------------|------------------|----------|---|----------|----------|----------|----------|----------|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | nv_vtemp_h2[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| nv_vtemp_h2 | 7:0 | | Voltage at TEMP pin corresponding to second high-temperature breakpoint in VCOM compensation curve. | | | | | |

NV_VCOM_MIN (0x21)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field | nv_vcom_min[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-------------|------|-------------------------------|
| nv_vcom_min | 7:0 | Lower limit for VCOM setting. |

NV_VCOM_MAX (0x22)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------------------|---|---|---|---|---|---|---|
| Field | nv_vcom_max[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|-------------|------|-------------------------------|
| nv_vcom_max | 7:0 | Upper limit for VCOM setting. |

NV_AVDD_SET (0x23)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|--------------|---|---|---|---|---|
| Field | – | – | nv_avdd[5:0] | | | | | |
| Reset | – | – | | | | | | |
| Access Type | – | – | Read Only | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|----------|------|--|
| nv_avdd | 5:0 | Sets AVDD and NAVDD voltages. See table for register 0x13. |

NV_VGON (0x24)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|--------------|--------------|---|---|---|---|---|
| Field | – | nv_cp_2stage | nv_vgon[5:0] | | | | | |
| Reset | – | | | | | | | |
| Access Type | – | Read Only | Read Only | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|--------------|------|---|
| nv_cp_2stage | 6 | When this bit is set to 1 a two-stage charge-pump is used. |
| nv_vgon | 5:0 | Sets VG _{ON} voltage. See table for register 0x14. |

NV_VGOFF (0x25)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|---|--|---|---|---|---|---|
| Field | – | – | nv_vgoff[5:0] | | | | | |
| Reset | – | – | | | | | | |
| Access Type | – | – | Read Only | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| nv_vgoff | 5:0 | | Sets VGOFF voltage. See table for register 0x15. | | | | | |

burn_otp_reg (0x78)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|--|---|---|---|---|---|
| Field | burn_otp[7:0] | | | | | | | |
| Reset | 0x0 | | | | | | | |
| Access Type | Write Only | | | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| burn_otp | 7:0 | | Command to copy the contents of registers 0x07-0x15 to the non-volatile registers 0x17-0x25. | | | | | |

reboot_otp_reg (0x79)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------------|---|--|---|---|---|---|---|
| Field | reboot_otp[7:0] | | | | | | | |
| Reset | | | | | | | | |
| Access Type | Write Only | | | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| reboot_otp | 7:0 | | Command to copy the contents of the non-volatile registers 0x17-0x15 to the working registers 0x17-0x25. | | | | | |

soft_restart (0x7A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|-------------------|---|--|---|---|---|---|---|
| Field | soft_restart[7:0] | | | | | | | |
| Reset | 0x00 | | | | | | | |
| Access Type | Write Only | | | | | | | |
| BITFIELD | BITS | | DESCRIPTION | | | | | |
| soft_restart | 7:0 | | Command used to re-start the device from a latched fault mode. All faults are cleared when this command is executed. | | | | | |

Applications Information

Boost Converter

Boost Converter Inductor Selection

Three key inductor parameters must be specified for operation with the device: Inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). Use a 2.2 μ H inductor when the boost converter operates at 2.1MHz and 10 μ H at 420kHz.

The inductor's saturation rating must exceed the maximum current limit of 2.3A.

Boost Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determine the amplitude of the high-frequency ripple seen on the output voltage. For stability, the boost output-filter capacitor should have a value of 10 μ F or greater when using 2.1MHz switching.

To avoid a large drop on HVINP when AVDD is enabled, the capacitance on the HVINP node should be at least three times larger than that on AVDD.

Boost Input Filter Capacitor

Sufficient input capacitance must be used to avoid input voltage drop when transients are encountered on the AVDD or NAVDD outputs and when the AVDD switch is closed. If the IN voltage drops below 2.57V, the device is likely to reset so input capacitance must prevent this. The total value of capacitance depends on the expected transients and the series resistance in the IN connection. A good starting point is a total input capacitance of 2 x 22 μ F ceramic capacitors in parallel with 2 x 10 μ F ceramic capacitors. Depending on the particular application circumstances more or less capacitance may be needed.

Input capacitance requirements are significantly relaxed when an input voltage of 5V is used.

Setting the AVDD Voltage

The AVDD output voltage is set by writing a 6-bit value to the AVDD_SET register.

The NAVDD converter outputs a negative voltage whose absolute value is the same as AVDD.

NAVDD Inverting Regulator

NAVDD Regulator Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DC}). Use a 2.2 μ H inductor when the converter operates at 2.1MHz and 10 μ H at 420kHz.

The inductor's saturation current rating must exceed the maximum current limit of 2.25A.

NAVDD External Diode Selection

Select a diode with a peak current rating of at least the LXN current limit (I_{LIMNH}) for use with the NAVDD output. The diode breakdown-voltage rating should exceed the sum of the maximum INN voltage and the absolute value of the NAVDD voltage. A Schottky diode improves the overall efficiency of the converter but should be selected to have low leakage at the maximum operating temperature.

NAVDD Output Capacitor Selection

The primary criterion for selecting the output filter capacitor is low ESR and capacitance value, as the NAVDD capacitor provides the load current when the internal switch is on. The voltage ripple on the NAVDD output has two components:

1. Ripple due to ESR which is the product of the peak inductor current and the output filter capacitor's ESR
2. Ripple due to bulk capacitance that can be determined as follows.

$$\Delta V_{\text{BULK}} = \frac{I_{\text{NAVDD}} \times \frac{D}{f_{\text{SW}}}}{C_{\text{NAVDD}}}$$

For stability, the NAVDD output capacitor should have a value of 10µF or greater when using 2.1MHz switching frequency.

Setting the V_{GON} and V_{G_{OFF}} Output Voltages

The internal positive charge pump can output a voltage approximately three times AVDD. If a voltage of twice the HVINP voltage is sufficient leave the FC1+ and FC1- pins unconnected and set the cp_2stage bit.

For V_{G_{OFF}}, the number of charge-pump stages should be chosen to ensure sufficient output voltage while maintaining the V_{G_{OFF}} voltage within its permitted operating range.

The V_{G_{ON}} output voltage is set by writing a 6-bit value to the vgon[5:0] field in the V_{G_{ON}} register.

The V_{G_{OFF}} voltage is set by writing a 6-bit value to the vgo[5:0] field in the V_{G_{OFF}} register.

V_{G_{ON}} Voltage Higher than Three Times AVDD

In exceptional cases, it may be necessary to produce a V_{G_{ON}} voltage greater than three times AVDD. In such cases, an external charge-pump circuit can be used as shown in [Figure 4](#). When using the device in this way, leave the FC1-, FC1+ and FC2+ pins unconnected and set the cp_2stage bit to 1.

4x Charge Pump

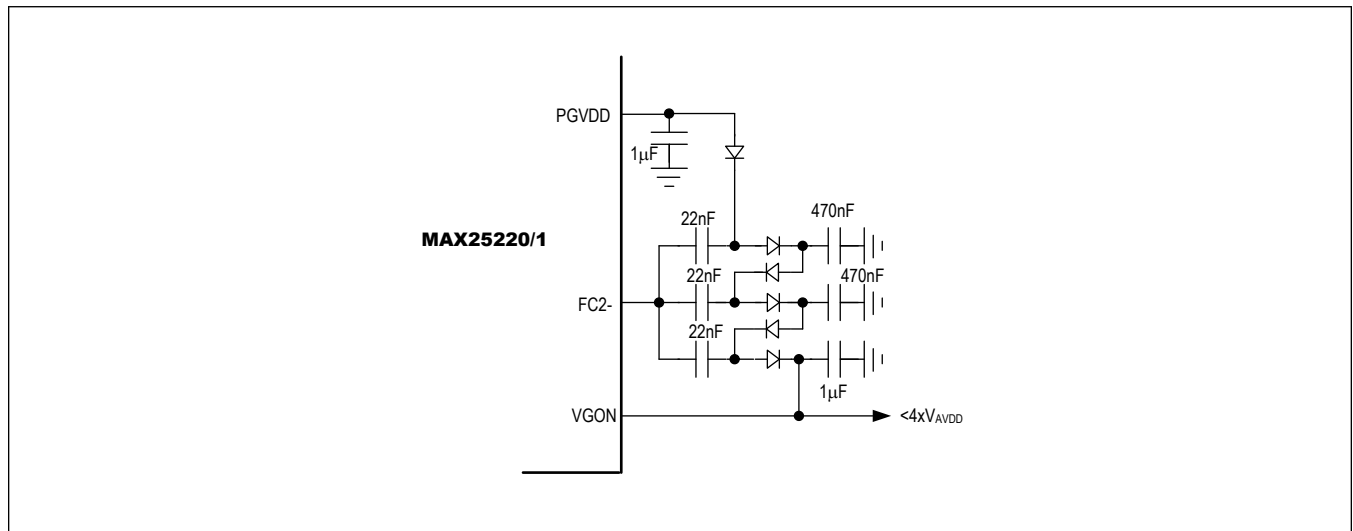


Figure 4. Quadrupler Charge-Pump at 2.1MHz

VCOM Block

V_{CB} Transistor

Select an external npn transistor with a minimum current gain of 30. When designing the PCB, ensure that the parasitic capacitance between the base and collector of the npn is minimized to avoid oscillation. Note that high continuous DC current on VCOM causes very high power dissipation in the npn device and a device with low thermal resistance should therefore be selected.

VCOM Temperature Compensation Example

Assume that an NTC with 10kΩ resistance at 25°C is connected from TEMP to GND and that the R_{REF} resistor is of value 2400Ω. At various temperatures, the following voltages will be observed on R_{REF} and the ADC measurement result

will be as follows:

Table 6. ADC Result vs Temperature

| TEMPERATURE | NTC RESISTANCE | R _{REF} VOLTAGE | ADC RESULT | DESIRED VCOM VOLTAGE |
|-------------|----------------|--------------------------|------------|----------------------|
| -30°C | 113kΩ | 13mV | 0x02 | -1.09V |
| 25°C | 10kΩ | 150mV | 0x1F | -1V |
| 60°C | 3kΩ | 500mV | 0x66 | -0.98V |
| 85°C | 1.5kΩ | 1V | 0xCD | -0.91V |

The rightmost column of the previous table indicates the desired VCOM output voltage at each temperature, which will be the inflection points in the temperature compensation curve. The following values are written to the relevant registers (remembering that each LSB of the VCOM setting represents 6.83mV):

Table 7. VCOM Setting Example

| REGISTER | FIELD | SETTING | NOTES |
|--------------------|---------------|---------|---|
| DELAYVCOM_LSB[7:0] | vcom25_0 | 0 | 9-bit value is 011011010 or 0xDA which corresponds to -1V |
| VCOM25 | vcom25[7:0] | 0x6D | |
| VCOM_L | vcom_l[4:0] | 0x0D | Represents shift of -89mV from VCOM25 |
| VCOM_H1 | vcom_h1[4:0] | 0x03 | Represents shift of +20mV from VCOM25 |
| VCOM_H2 | vcom_h2[4:0] | 0x0A | Represents shift of +68mV from VCOM_H1 |
| VTEMP25 | vtemp25[7:0] | 0x1F | ADC result at 25°C |
| VTEMP_L | vtemp_l[7:0] | 0x02 | ADC result at -30°C |
| VTEMP_H1 | vtemp_h1[7:0] | 0x66 | ADC result at 60°C |
| VTEMP_H2 | vtemp_h2[7:0] | 0xCD | ADC result at 85°C |

With these settings, the VCOM output voltage at 25°C is -1V, while at the temperature represented by 13mV at the R_{REF} pin the VCOM voltage decreases to -1.09V as set by the VCOM_L register. Similarly, the VCOM_H1 and VCOM_H2 values are output on VCOM when the TEMP voltage is 500mV and 1V, respectively. In between these values the device interpolates the correct VCOM voltage value with a resolution of 6.83mV. The complete curve is shown in [Figure 5](#).

When setting the values VTEMP_{xx} and VCOM_{xx}, it is important to avoid values which can cause wraparound in the temperature compensation algorithm thus possibly leading to sudden changes in the value of VCOM.

Sample VCOM Temperature Compensation Curve

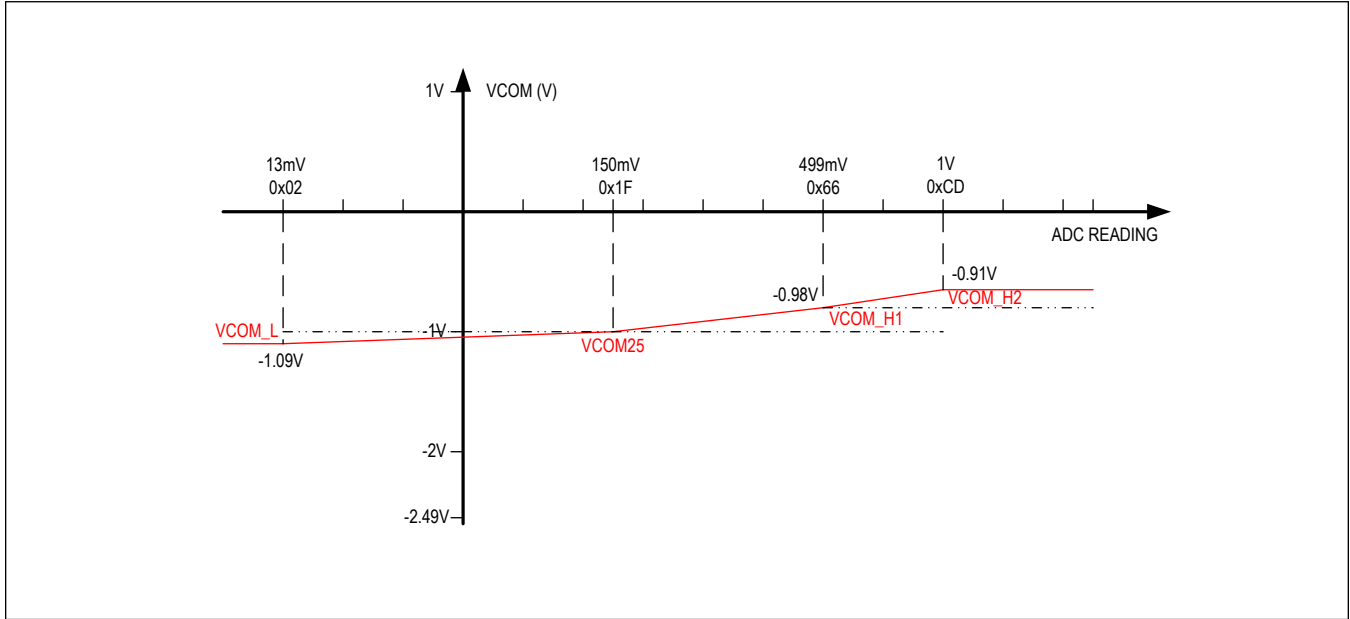


Figure 5. Sample VCOM Temperature Compensation Curve

Using the NV Memory

Follow the sequence below to perform non-volatile programming of the device when the auto-refresh function is not used:

1. Apply a voltage between 3.3V and 5V to the IN and INN pins with the device in I²C mode
2. Write the desired values to be stored in OTP to the registers from 0x07 to 0x15
3. Apply 8.5V to V_{PROG}
4. Optionally wait to ensure the 8.5V at V_{PROG} is stable
5. Send burn_otp_reg (write any value to 0x78) command. If parity is enabled ensure the overall parity is even by altering the final byte if necessary.
6. Wait 20ms
7. If the nv_flg bit is 0, the write was successful, go to next step. If nv_flg = 1, perform re-try (steps 5,6).
8. Send reboot_otp (write any value to 0x79) command.

Special care is required when performing non-volatile programming with the auto-refresh feature enabled. In such cases follow the sequence below when at least one calibration has already been performed:

1. Apply a voltage between 3.3V and 5V to the IN and INN pins
2. Write the desired values to be stored in NV memory to the registers from 0x07 to 0x15 (keep auto-refresh bit disabled until here)
3. Enable the auto-refresh feature
4. Start polling one of the registers from 0x07 to 0x15 which has changed its value until that value gets refreshed to the older one (auto-refresh is active)
5. The following steps from #6 to #10 must be completed within 1s
6. Write the desired values to be stored in OTP to the registers from 0x07 to 0x15 (including auto-refresh bit).
7. Apply 8.5V to V_{PROG}
8. Optionally wait to ensure the 8.5V at V_{PROG} is stable
9. Send burn_otp_reg (write any value to 0x78) command. If parity is enabled ensure the overall parity is even by

altering the final byte if necessary

10. Wait 20ms
11. If the `nv_flg` bit is 0, the write was successful, go to next step. If `nv_flg` = 1, perform retry from step 2.
12. Send `reboot_otp` (write any value to 0x79) command

The non-volatile memory can be written to a total of six times.

Layout Considerations

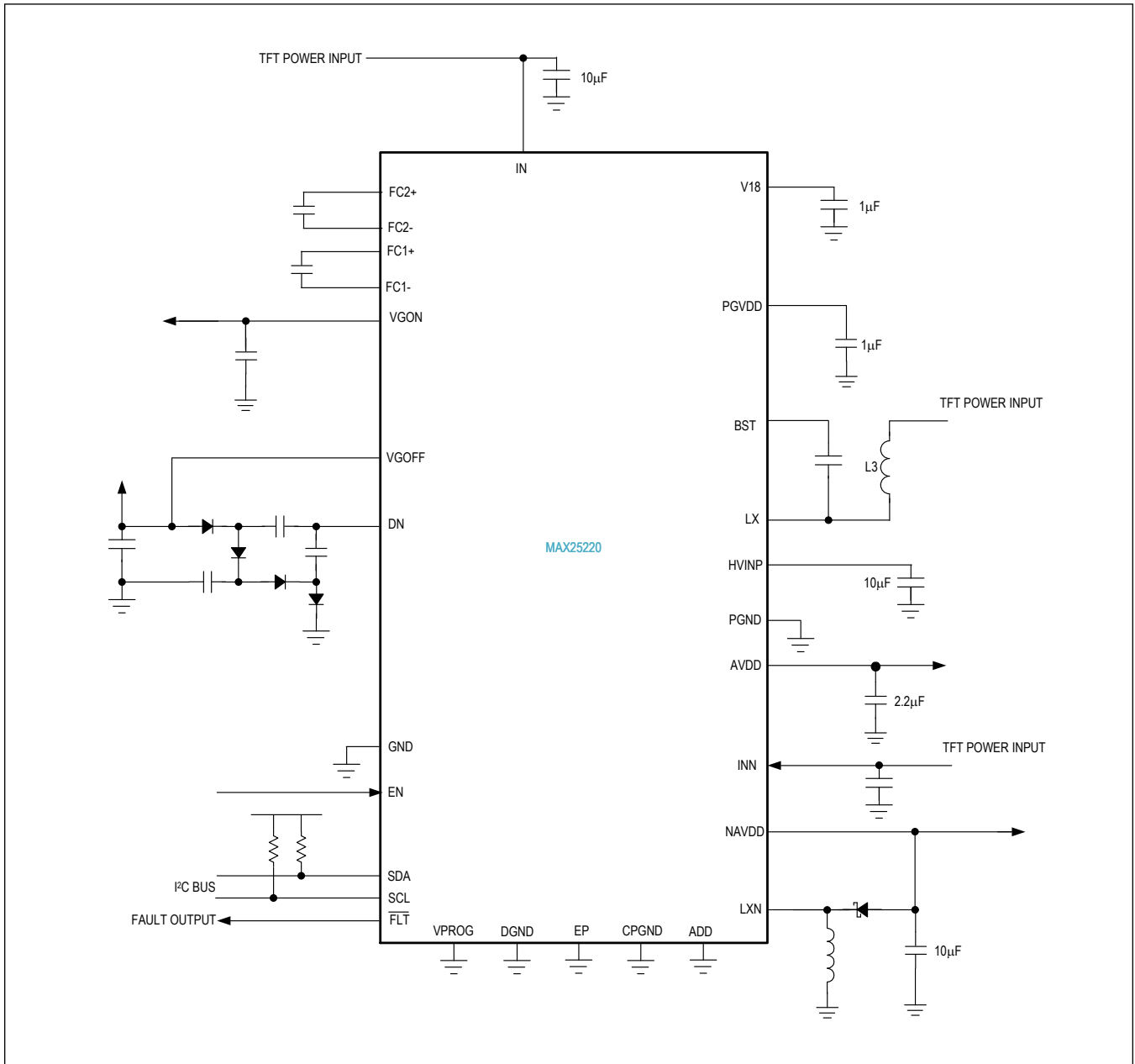
The MAX25220/MAX25221/MAX25221B/MAX25221C include high-frequency switching converters to generate the voltages for TFT-LCDs. Take proper care while laying out the circuit board to ensure correct operation. The switching-converter portions of the circuit have nodes with very fast voltage changes that could lead to undesirable effects on the sensitive parts of the circuit as well as electromagnetic interference (EMI). Follow the guidelines below to reduce noise as much as possible:

- Connect the bypass capacitors on IN and INN as close as possible to the device and connect the capacitor ground to the analog ground plane using vias close to the capacitor terminal. Ensure that the power connection to IN and INN uses a very wide trace or complete board layer to avoid input undervoltage problems.
- Connect the GND pin of the device to the analog ground plane using a via close to GND. Lay the analog ground plane on the inner layer, preferably next to the top layer. Use the analog ground plane to cover the entire area under critical signal components for the power converter.
- Have a power-ground plane for the switching-converter power circuit under the power components (i.e., input filter capacitor, output filter capacitor, inductor, MOSFET, rectifier diode, and current-sense resistor). Connect PGND to the power-ground plane closest to PGND. Connect all other ground connections to the power ground plane using vias close to the terminals.
- Minimize the copper area of all switching nodes to avoid EMI. Minimize the loop areas for the AVDD and NAVDD converters by placing all components close to the LXP and LXN pins. Place the input and output capacitor grounds close to each other. In the case of AVDD the input/output capacitor grounds should also connect directly to the PGND pin.
- Connect GND, CPGND and PGND at the exposed pad of the device.
- Refer to the evaluation kit (EV kit) data sheet for a sample layout.

In addition, when using an external NTC temperature sensor for temperature compensation connect the grounded end directly to the grounded end of the RREF resistor. This avoids possible differences in ground potential between different points on the circuit board.

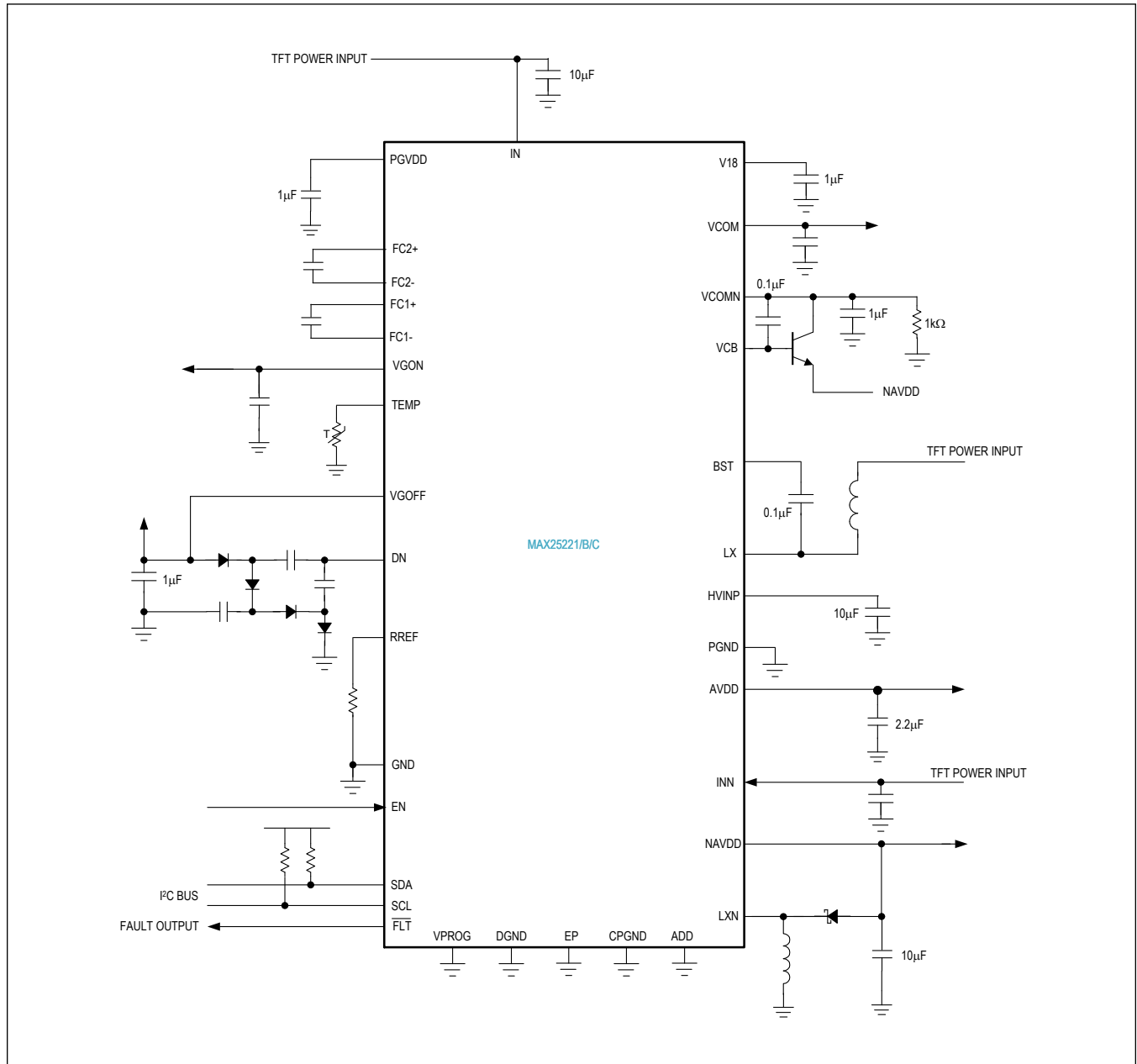
Typical Application Circuits

MAX25220 Applications Diagram



Typical Application Circuits (continued)

MAX25221 Applications Diagram



Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PIN-PACKAGE | FEATURES |
|----------------------|-------------------|--------------|---|
| MAX25220ATJ/V+ | -40 to +125°C | 32 TQFN-EP | Without VCOM buffer |
| MAX25221ATJ/V+ | -40 to +125°C | 32 TQFN-EP | With VCOM buffer |
| MAX25220ATJ/ VY+ | -40 to +125°C | 32 SWTQFN-EP | Without VCOM buffer |
| MAX25221ATJ/ VY+* | -40 to +125°C | 32 SWTQFN-EP | With VCOM buffer |
| MAX25221BATJ/ V+ | -40 to +125°C | 32 TQFN-EP | EN pin turn-on, VCOM buffer |
| MAX25221CATJ/ V+ | -40 to +125°C | 32 TQFN-EP | EN pin turn-on, VCOM buffer, short-circuit check disabled on VGON/VGOFF |

+ Denotes a lead(Pb)-free/RoHS-compliant package.

/V denotes an automotive qualified part.

Y = Side-wettable package.

T Denotes tape-and-reel.

*Future product - contact factory for availability.

MAX25220/MAX25221/
MAX25221B/MAX25221C

Automotive 4-Channel TFT-LCD Power Supplies
with VCOM Buffer

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|-------------------------|
| 0 | 5/20 | Initial release | — |
| 1 | 6/20 | Removed future product notation from MAX25221ATJ/V+ in Ordering Information | 54 |
| 2 | 6/20 | Added Typical Operating Characteristics | 14, 15 |
| 3 | 10/20 | Updated Package Information and Electrical Characteristics ; removed future product notation for MAX25220ATJ/VY+ in Ordering Information | 7, 11, 54 |
| 4 | 11/20 | Updated Pin Descriptions and Ordering Information . | 19, 54 |
| 5 | 8/21 | Added information on non-volatile memory writes; updated Absolute Maximum Ratings ; added C version; updated inductor selection content | 2, 6, 27, 29-31, 43, 51 |

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