

MAX25307/MAX25308

Two/Three Output Low-Noise LDO Linear Regulators

General Description

The MAX25307/MAX25308 are a two/three output linear regulator family that deliver up to 600mA on channel 1 and up to 300mA on channels 2 and 3 with only $37\mu V_{RMS}$ of output noise from 10Hz to 100kHz. These regulators maintain $\pm 1.25\%$ output accuracy over a wide input voltage range, requiring only 155mV (max) of input-to-output headroom at full load. The 1.95mA maximum no-load supply current is independent of dropout voltage. Each output is factory programmable between 0.6V to 3.7875V in 12.5mV steps. No external components are needed except for the input, output, and bypass capacitors. Each output has an independent enable input and \overline{RESET} output.

Applications

- Infotainment Systems
- Point of Load
- Advanced Driver-Assistance Systems (ADAS)

Benefits and Features

- 1.7V to 5.5V Input Voltage Range
- Factory Selectable Output Voltage of 0.6V to 3.7875V in 12.5mV Steps
- $37\mu V_{RMS}$ Output Noise, 10Hz to 100kHz
- 1.95mA (Max) Operating Supply Current
- 70dB PSRR at 10kHz
- 600mA Maximum Output Current (OUT1)
- 300mA Maximum Output Current (OUT2/3)
- $\pm 1.25\%$ DC Accuracy Over Load, Line, and Temperature
- 155mV (Max) Dropout at $I_{MAX1/2/3}$ Load ($3.3V_{IN}$)
- $< 1\mu A$ Shutdown Supply Current
- Overcurrent and Overtemperature Protection
- Output-to-Input Reversed Current Protection
- Individual \overline{RESET} Outputs
- 3mm x 3mm 16 pin TQFN Package
- $-40^{\circ}C$ to $125^{\circ}C$ Grade 1 Automotive Temperature Range

Ordering Information appears at end of data sheet.

Simplified Block Diagram

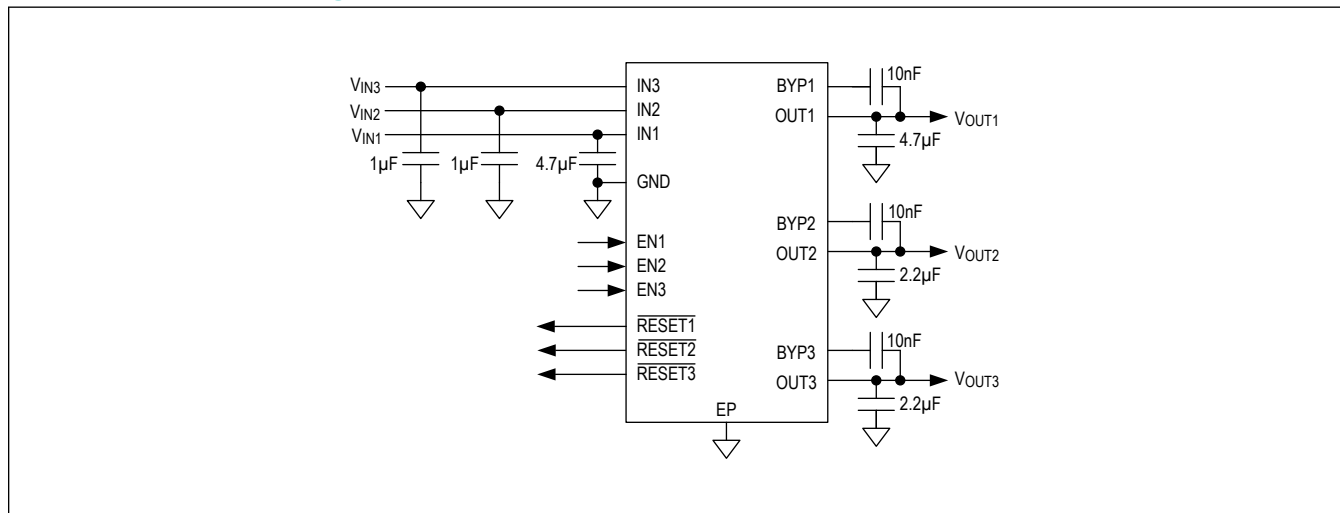


TABLE OF CONTENTS

General Description	1
Applications	1
Benefits and Features	1
Simplified Block Diagram	1
Absolute Maximum Ratings	3
Recommended Operating Conditions	3
Package Information	3
TQFN	3
Electrical Characteristics	3
Typical Operating Characteristics	6
Pin Configurations	9
MAX25308	9
MAX25307	9
Pin Description	9
Functional Diagrams	11
Simplified Functional Diagram	11
Detailed Description	12
Supply Inputs (IN1-3)	12
Enable (EN1-3)	12
Bypass (BYP)	12
Overcurrent Protection	12
Overtemperature Protection	12
Output-to-Input Reverse Current Protection	12
RESET Outputs	13
Input Capacitor	13
Output Capacitor	13
Thermal Considerations	13
Typical Application Circuits	14
Circuit 1 (MAX25308)	14
Circuit 2 (MAX25307)	14
Ordering Information	14
Revision History	15

Absolute Maximum Ratings

IN1, IN2, IN3, EN1, EN2, EN3 to GND	-0.3V to +6V
OUT1 to GND	-0.3V to IN1 + 0.3V
OUT2 to GND	-0.3V to IN2 + 0.3V
OUT3 to GND	-0.3V to IN3 + 0.3V
BYP1, BYP2, BYP3 to GND	-0.3V to +6V
RESET1, RESET2, RESET3 to GND	-0.3V to +6V
Output Short-Circuit Duration	Continuous

Package Thermal Characteristics
T1633+7C

Continuous Power Dissipation	
TQFN (derate 21.52mW/°C above 70°C)	1721.69mW
Operating Junction Temperature	-40°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	°C

Note: These limits are not guaranteed.

Package Information

TQFN

Package Code	T1633+7C
Outline Number	21-0136
Land Pattern Number	90-0032
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	46.47°C/W
Junction to Case (θ_{JC})	5.58°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(VIN1,2 = 3.3V, VIN3 = 3.6V, COUT1 = 4.7µF, COUT2,3 = 2.2µF, CBYP_ = 10nF, TJ = -40°C to +150°C, unless otherwise noted. Typical values are at TA = +25°C under normal conditions, unless otherwise specified. (Note 1) (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	VIN_	Guaranteed by Output Accuracy	1.7		5.5	V
Input Undervoltage Lockout	VIN_UVLO	VIN_ rising	1.5		1.69	V
Input Undervoltage Lockout Hysteresis	VIN_UVLO_HYS	VIN_ UVLO Hysteresis		100		mV
Supply Current	IQ_	All outputs off		1		µA
		IOUT = 0mA, VIN1,2 = 3.3V, VIN3 = 3.6V, VEN_ = VIN_		1.2	1.95	mA

Electrical Characteristics (continued)

(VIN1,2 = 3.3V, VIN3 = 3.6V, COUT1 = 4.7μF, COUT2,3 = 2.2μF, CBYP_ = 10nF, TJ = -40°C to +150°C, unless otherwise noted. Typical values are at TA = +25°C under normal conditions, unless otherwise specified. (Note 1) (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Range (Note 4)	VOUT_	VIN_ ≥ VOUT_ + 0.3V, VIN_ ≥ 1.7V	0.6		3.7875	V
Output Accuracy	ACC	IOUT_ from 0.1mA to IMAX_, VIN_ from VOUT_ + 0.3V to 5.5V, VIN_ ≥ 1.7V, -40°C < TJ < 125°C	-1.25		+1.25	%
		IOUT_ from 0.1mA to IMAX_, VIN_ from VOUT_ + 0.3V to 5.5V, VIN_ ≥ 1.7V, -40°C < TJ < 150°C	-1.5		+1.5	
Load Regulation		IOUT_ from 0.1mA to IMAX_, VIN_ = VOUT_ + 0.3V, VOUT1,2,3 = Factory setting		0.07		%
Line Regulation		VIN_ from VOUT_ + 0.3V to 5.5V, VIN_ ≥ 1.7V, IOUT1,2,3 = 0.1mA		0.06		%
LDO_ Dropout Voltage (Note 2)		VIN_ = 3.3V, IOUT_ = IMAX_		65	155	mV
Current Limit	ILIM1_HI	IMAX1 = 600mA, VIN1 ≥ 1.7V, VOUT1 = 95% of regulation, VIN1 ≥ VOUT1 + 0.3V	650	790	930	mA
	ILIM2,3_HI	IMAX2,3 = 300mA, VIN2,3 ≥ 1.7V, VOUT2,3 = 95% of regulation, VIN2,3 ≥ VOUT2,3 + 0.3V	390	490	590	
Output Noise		VOUT_ = 1.2V, IOUT_ = 100mA, 10Hz to 100kHz, CBYP_ = 47nF		37		μVRMS
Power Supply Rejection Ratio	PSRR	IOUT1 = 100mA, IOUT2,3 = 50mA, 10kHz		70		dB
EN_ Input Threshold		VIN_ from 1.7V to 5.5V	EN_ rising		1.2	V
			EN_ falling	0.4		
EN_ Hysteresis				75		mV
EN_ Input Resistance		VIN_ from 1.7V to 5.5V		TJ = +25°C	2	MΩ
Input Reverse Current Threshold		Peak reverse current before IIN_ falls to less than 50μA		200		mA
Thermal Shutdown Threshold		TJ rising		170		°C
Thermal Shutdown Hysteresis				15		°C
Discharge Resistance		VEN_ = 0V		800		Ω
Startup Time		Delay from VEN_ high to VOUT_ starts rising		220		μs
RESET						
RESET_ OV Threshold		VOUT_ rising	104.6	108.3	111.7	%
RESET_ UV Threshold		VOUT_ falling	88.3	91.7	94.7	%
RESET_ Voltage, Low		IRESET_ = 1mA		10	100	mV
RESET_ Filter Time				5		μs

Electrical Characteristics (continued)

(VIN1,2 = 3.3V, VIN3 = 3.6V, C_{OUT1} = 4.7μF, C_{OUT2,3} = 2.2μF, C_{BYP_} = 10nF, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise specified. (Note 1) (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET_ Leakage Current			-0.1	+0.001	+0.1	μA
RESET_ Hold Time		Option 1	0.425	0.5	0.575	ms
		Option 2	2.805	3.7	4.255	
		Option 3	6.29	7.4	8.51	
		Option 4	12.665	14.9	17.135	

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design and characterization.

Note 2: Dropout voltage is defined as (V_{in}-V_{out}) when FET is fully turned ON.

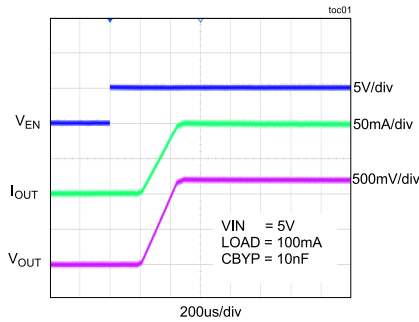
Note 3: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 4: Not Production Tested, Characterized by ATE.

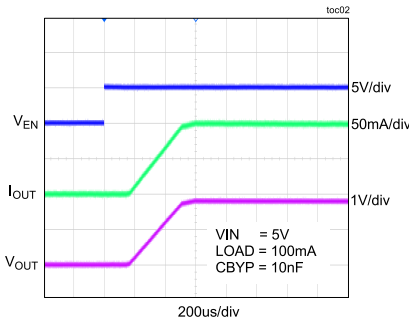
Typical Operating Characteristics

($V_{IN_} = 3.3V$, $V_{OUT1/2/3} = 1.2V/1.8V/3.3V$, $T_A = 25^\circ C$, $C_{IN1} = 4.7\mu F$, $C_{IN2,3} = 1\mu F$, $C_{OUT1} = 4.7\mu F$, $C_{OUT2,3} = 2.2\mu F$, $C_{BYP_} = 10nF$, unless otherwise noted.)

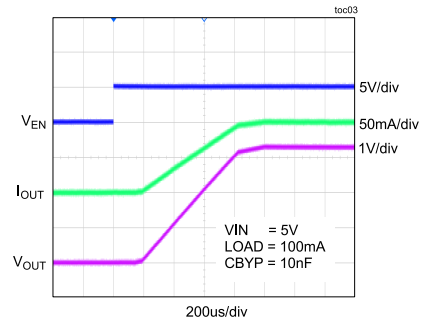
CH1 STARTUP WAVEFORM



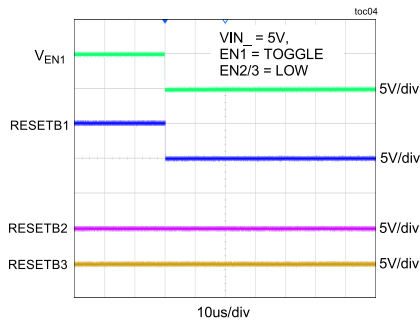
CH2 STARTUP WAVEFORM



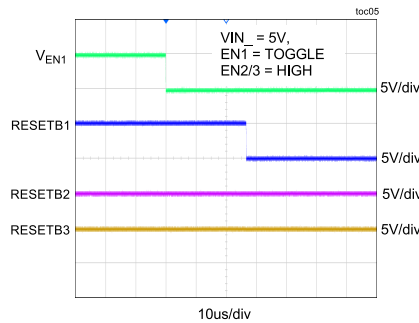
CH3 STARTUP WAVEFORM



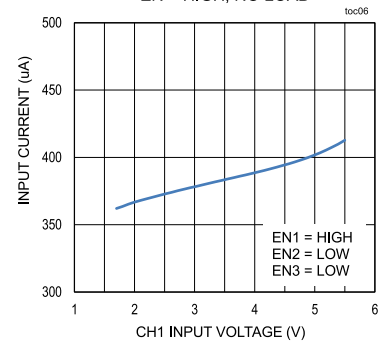
CH1 RESETB TOGGLE WAVEFORM



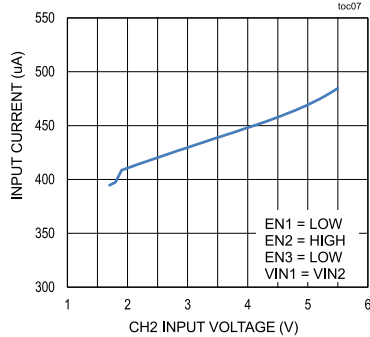
CH1 RESETB TOGGLE WAVEFORM



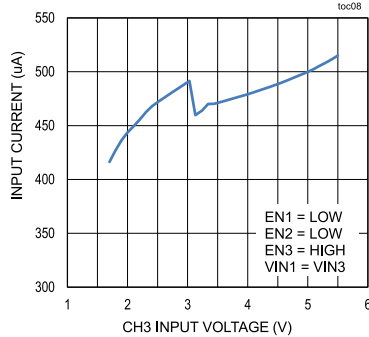
CH1 QUIESCENT CURRENT EN = HIGH, NO LOAD



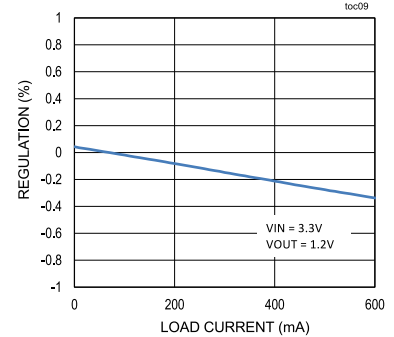
CH2 QUIESCENT CURRENT EN = HIGH, NO LOAD



CH3 QUIESCENT CURRENT EN = HIGH, NO LOAD

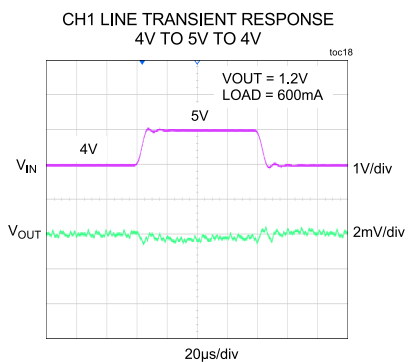
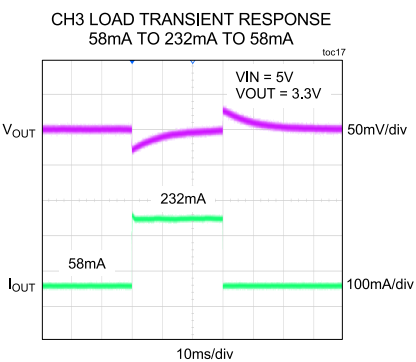
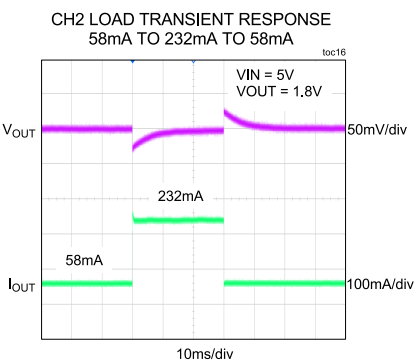
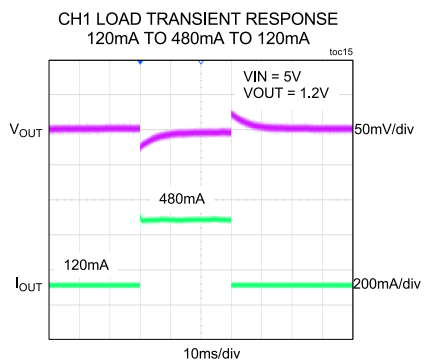
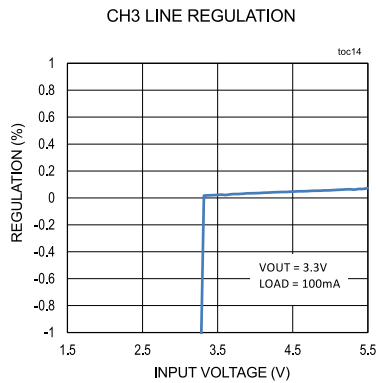
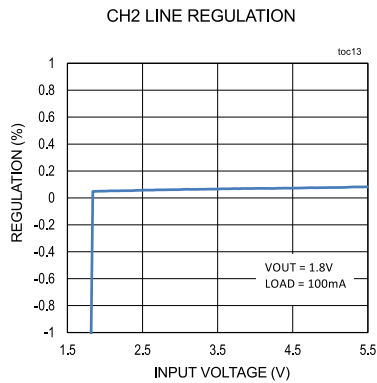
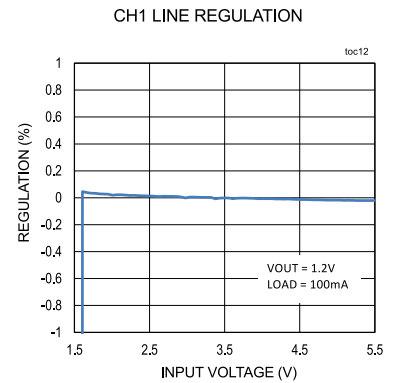
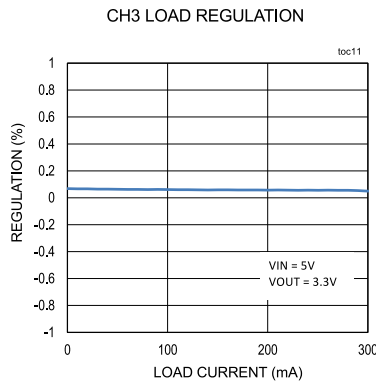
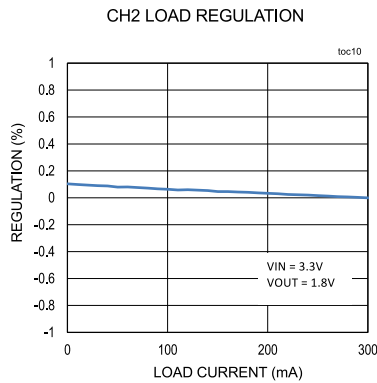


CH1 LOAD REGULATION



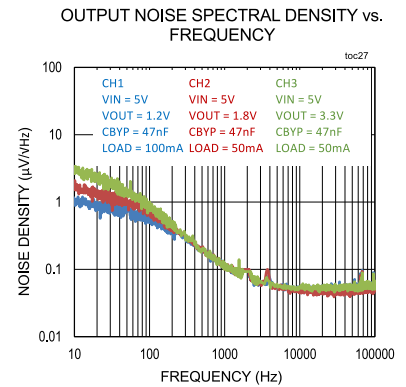
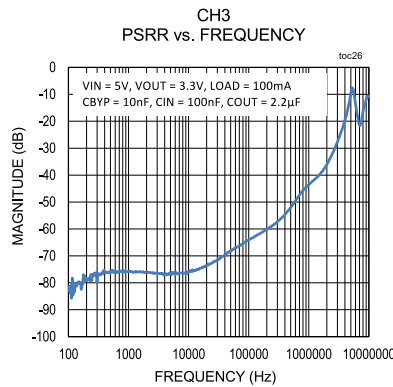
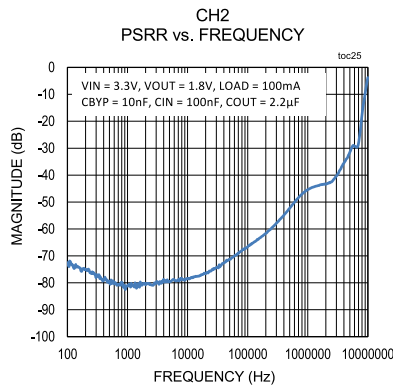
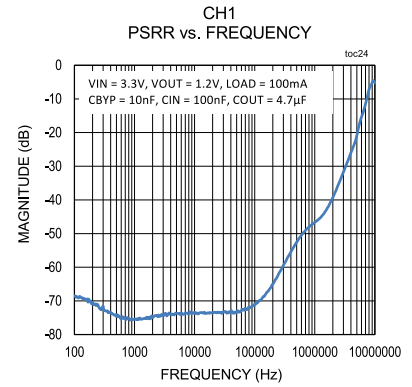
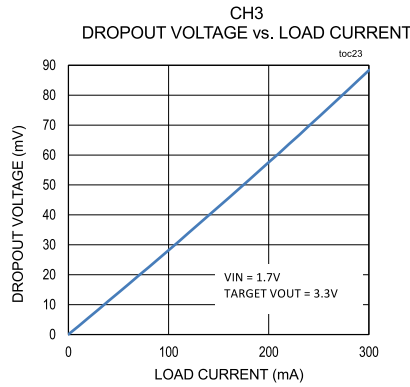
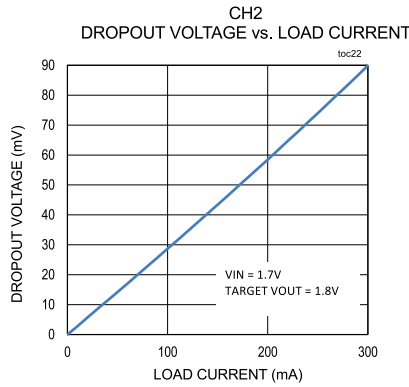
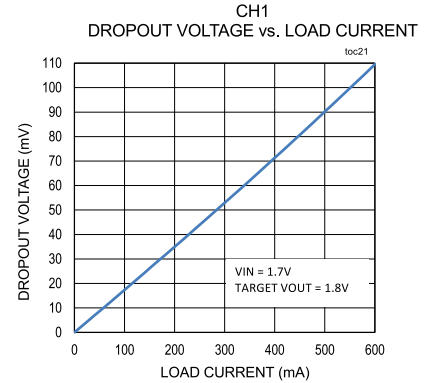
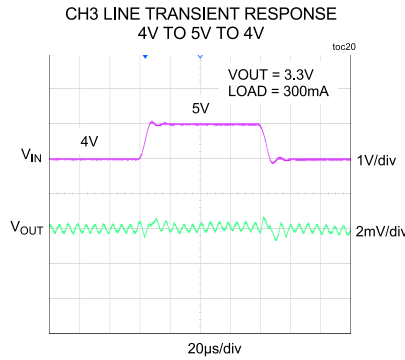
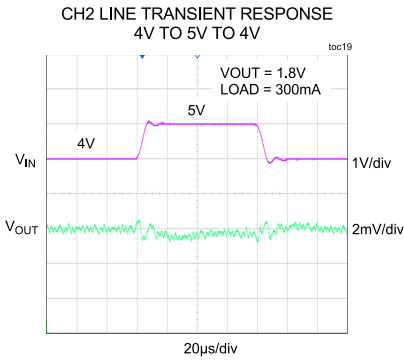
Typical Operating Characteristics (continued)

($V_{IN_} = 3.3V$, $V_{OUT1/2/3} = 1.2V/1.8V/3.3V$, $T_A = 25^\circ C$, $C_{IN1} = 4.7\mu F$, $C_{IN2,3} = 1\mu F$, $C_{OUT1} = 4.7\mu F$, $C_{OUT2,3} = 2.2\mu F$, $C_{BYP_} = 10nF$, unless otherwise noted.)



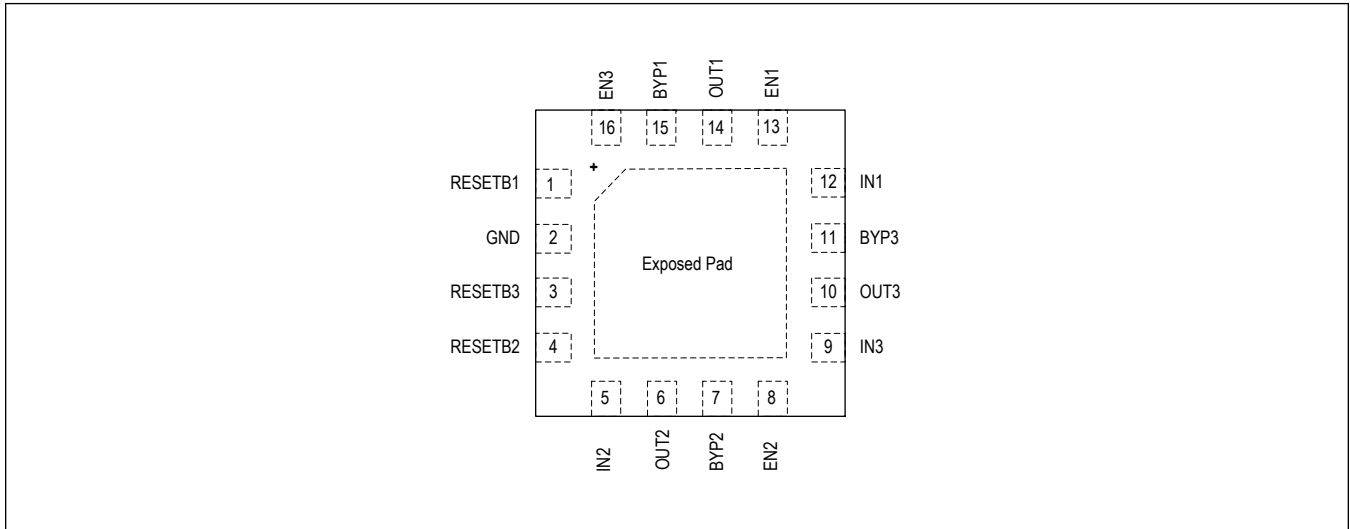
Typical Operating Characteristics (continued)

($V_{IN_} = 3.3V$, $V_{OUT1/2/3} = 1.2V/1.8V/3.3V$, $T_A = 25^\circ C$, $C_{IN1} = 4.7\mu F$, $C_{IN2,3} = 1\mu F$, $C_{OUT1} = 4.7\mu F$, $C_{OUT2,3} = 2.2\mu F$, $C_{BYP_} = 10nF$, unless otherwise noted.)

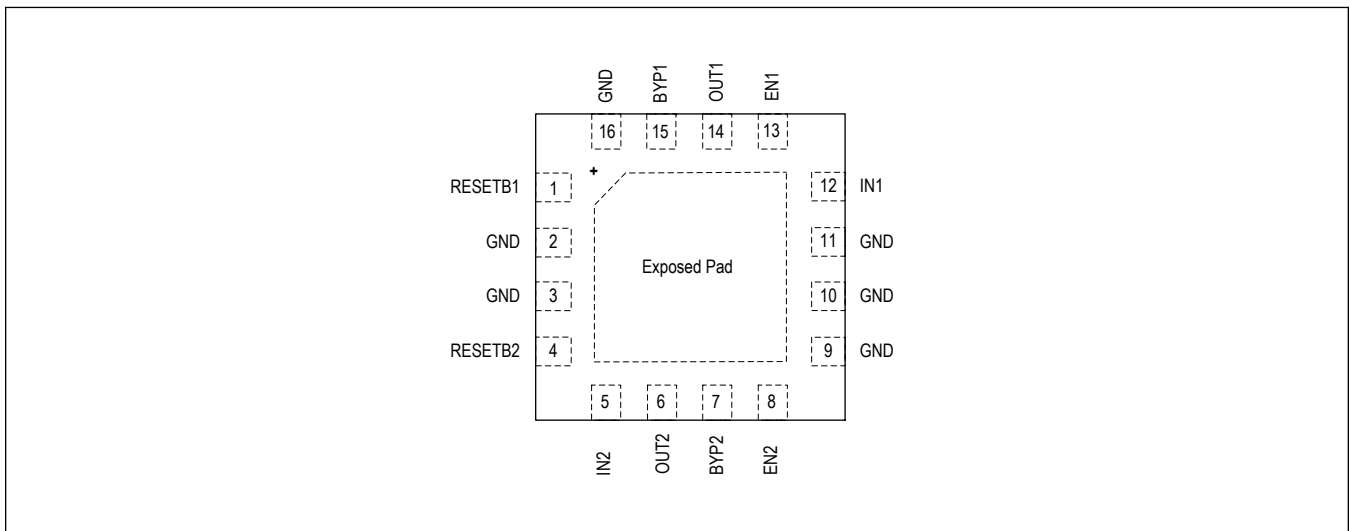


Pin Configurations

MAX25308



MAX25307



Pin Description

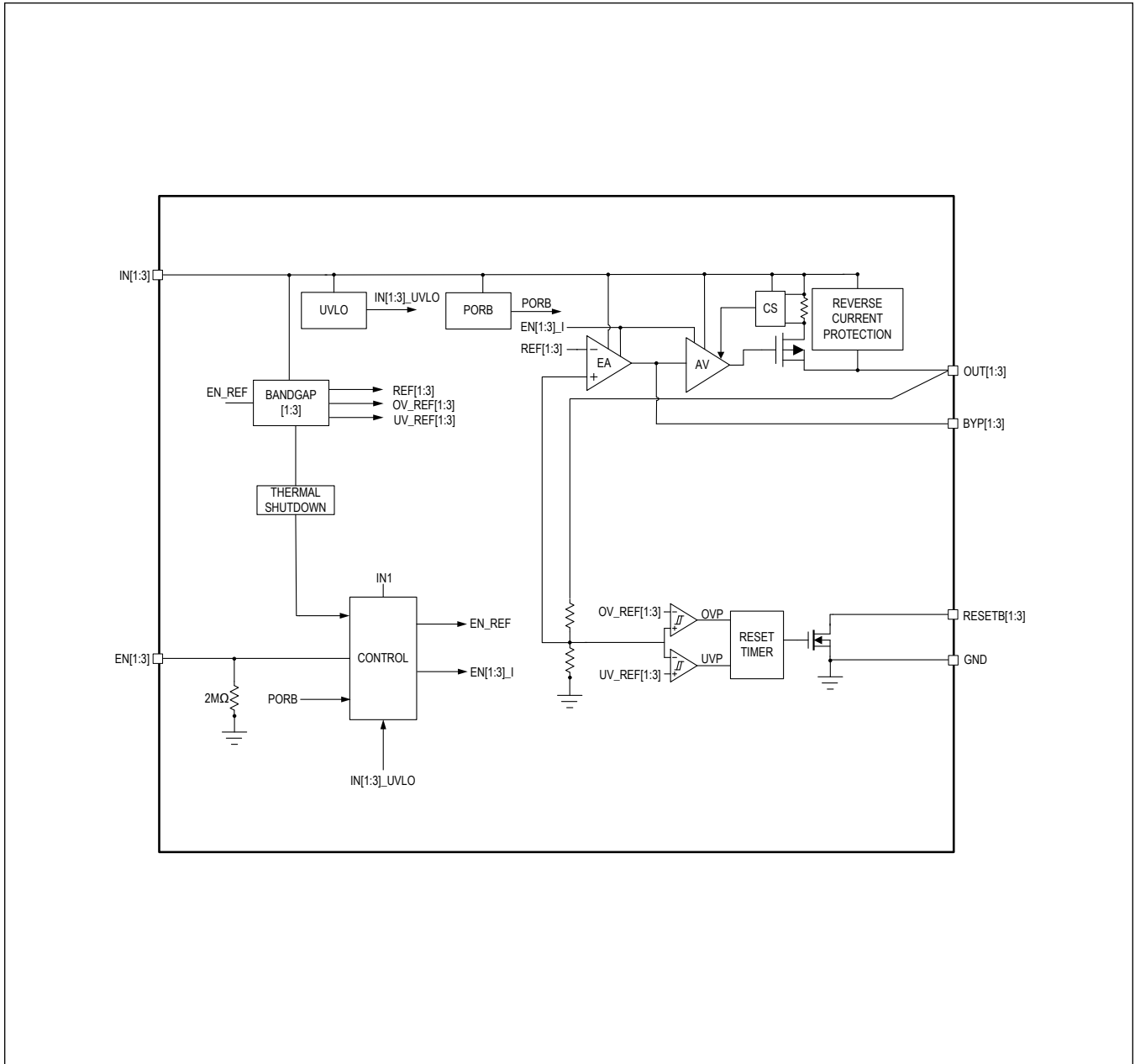
PIN		NAME	FUNCTION
MAX25308	MAX25307		
1	1	RESET1	Active Low RESET for Output 1. RESET1 becomes high impedance when OUT1 is in regulation. Actively pulled down if OUT1 is outside the regulation window. To obtain a logic signal, connect a pullup resistor from this pin to a supply.
2	2	GND	Regulator Ground. Bring IN_ and OUT_ bypass capacitor GND connections to this pin.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX25308	MAX25307		
3	—	$\overline{\text{RESET3}}$	Active Low RESET for Output 3. $\overline{\text{RESET3}}$ becomes high impedance when OUT3 is in regulation. Actively pulled down if OUT3 is outside the regulation window. To obtain a logic signal, connect a pullup resistor from this pin to a supply.
4	4	$\overline{\text{RESET2}}$	Active Low RESET for Output 2. $\overline{\text{RESET2}}$ becomes high impedance when OUT2 is in regulation. Actively pulled down if OUT2 is outside the regulation window. To obtain a logic signal, connect a pullup resistor from this pin to a supply.
5	5	IN2	Regulator Supply Input. Connect to a voltage between 1.7V and 5.5V, and bypass with a 1 μ F capacitor from IN2 to GND.
6	6	OUT2	Channel 2 Output. Sources maximum up to 300mA at output regulation voltage. Bypass with 2.2 μ F low ESR capacitor from OUT2 to GND.
7	7	BYP2	Bypass Capacitor Input 2. Connect 1nF to 100nF capacitor between OUT2 and BYP2 to reduce output noise and set the regulator soft-start rate.
8	8	EN2	Enable Input for Channel 2. Connect this pin to a logic signal to enable (V_{EN2} high) or disable (V_{EN2} low) the regulator output. Connect to IN_ with 10k Ω pullup resistor to keep the output enabled whenever a valid supply voltage is present.
9	—	IN3	Regulator Supply Input. Connect to a voltage between 1.7V and 5.5V and bypass with a 1 μ F capacitor from IN3 to GND.
10	—	OUT3	Channel 3 Output. Sources maximum up to 300mA at output regulation voltage. Bypass with 2.2 μ F low ESR capacitor from OUT3 to GND.
11	—	BYP3	Bypass Capacitor Input 3. Connect 1nF to 100nF capacitor between OUT3 and BYP3 to reduce output noise and set the regulator soft-start rate.
12	12	IN1	Regulator Supply Input. Connect to a voltage between 1.7V and 5.5V, and bypass with a 4.7 μ F capacitor from IN1 to GND.
13	13	EN1	Enable Input for Channel 1. Connect this pin to a logic signal to enable (V_{EN1} high) or disable (V_{EN1} low) the regulator output. Connect to IN_ with a 10k Ω pullup resistor to keep the output enabled whenever a valid supply voltage is present.
14	14	OUT1	Channel 1 Output. Sources up to 600mA at output regulation voltage. Bypass with 4.7 μ F low ESR capacitor from OUT1 to GND.
15	15	BYP1	Bypass Capacitor Input 1. Connect 1nF to 100nF capacitor between OUT1 and BYP1 to reduce output noise and set the regulator soft-start rate.
16	—	EN3	Enable Input for Channel 3. Connect this pin to a logic signal to enable (V_{EN3} high) or disable (V_{EN3} low) the regulator output. Connect to IN_ with a 10k Ω pull up resistor to keep the output enabled whenever a valid supply voltage is present.
—	3,9,10,11,16	N.C.	Connect to Ground
EP	EP	EP	Exposed Pad. Connect the exposed pad to a ground plane with low thermal resistance to ambient to provide best heat sinking.

Functional Diagrams

Simplified Functional Diagram



Detailed Description

The MAX25307/MAX25308 are a two/three output linear regulator family that deliver up to 600mA on channel 1 and 300mA on channels 2 and 3 with only $37\mu\text{V}_{\text{RMS}}$ of output noise from 10Hz to 100kHz. These regulators maintain $\pm 1.25\%$ output accuracy over a wide input voltage range, requiring only 155mV (max) of input-to-output headroom at full load. The 1.95mA maximum no-load supply current is independent of dropout voltage. Each output is factory programmable between 0.6V to 3.7875V in 12.5mV steps. No external components are needed except for the input, output, and bypass capacitors. Each output has an independent enable input and RESET outputs. A simplified functional diagram is shown in [Simplified Functional Diagram](#).

Supply Inputs (IN1-3)

There is a separate supply input for each LDO. However, IN1 powers the common circuitry of the device. This requires power to the IN1 to be supplied before OUT2 and/or OUT3 can be turned on. If the supply for IN1 comes up last, this delays the soft-start for the other outputs until after IN1 is above the UVLO. It is acceptable that the enable inputs are high prior to the input supply being applied.

Enable (EN1-3)

The MAX25307/MAX25308 include individual enable inputs for each output (EN1/EN2/EN3). Pull EN_ low to shut down the output, or drive EN_ high to enable the output. If a separate enable signal is not available, connect EN_ to IN_ to keep the output enabled whenever a valid supply voltage is present.

Bypass (BYP)

The capacitor connected from BYP_ to OUT_ filters the noise of the reference, feedback resistors, and regulator input stage. The slew rate of the output voltage during startup is also determined by the BYP capacitor. A $0.01\mu\text{F}$ capacitor sets the slew rate to 5V/ms.

The BYP capacitor value can be adjusted from $0.001\mu\text{F}$ to $0.1\mu\text{F}$ to change the startup slew rate according to the following formula:

$$\text{StartupSlewRate} = (5\text{V} / \text{ms}) \times \left(\frac{0.01\mu\text{F}}{C_{\text{BYP}_-}} \right)$$

where C_{BYP_-} is in μF .

Overcurrent Protection

The MAX25307/MAX25308 current limit provides protection during output overload or short circuit conditions. If the output is shorted to GND, the output current is limited to the selected current limit. In such cases, the output falls out of regulation, and is $V_{\text{OUT}} = I_{\text{LIM}} \times R_{\text{LOAD}}$. In this condition, the pass element dissipates power equals to $(V_{\text{IN}} - V_{\text{OUT}}) \times I_{\text{LIM}}$, which increases junction temperature. When the junction temperature reaches approximately 170°C (typ), a thermal overload circuit turns off the device. When the junction cools to 155°C (typ), the device is turned on to reestablish regulation. While the fault persists, the device cycles between the current limit and thermal shutdown.

Overtemperature Protection

Overtemperature protection turns off the device when junction temperature rises to approximately 170°C (typ). When junction temperature cools to approximately 155°C (typ), the output turns back on to reestablish regulation. The thermal protection circuit can cycle on and off depending on power dissipation, thermal resistance, and ambient temperature. This cycling limits the power dissipation and protects the device from damage due to overheating.

Output-to-Input Reverse Current Protection

The MAX25307/MAX25308 are also protected against reverse current when the output voltage is higher than the input. If extra output capacitance is used at the output, a power-down transient at the input would normally cause a large reverse current through a conventional regulator. The MAX25307/MAX25308 include a reverse voltage detector that trips when

IN_ drops 10mV below OUT_, shutting off the regulator and opening the PMOS body diode connection, preventing any reverse current.

RESET Outputs

The MAX25307/MAX25308 include an open-drain output, $\overline{\text{RESET}}$ for each output that goes low to indicate the output voltage is out of regulation. Connect a pullup resistor from this pin to an external supply. When the associated EN_ is low the $\overline{\text{RESET}}$ is asserted. The hold time of all reset outputs is factory selectable between 0.5ms and 14.9ms.

Input Capacitor

A 4.7 μ F ceramic capacitor for channel 1 and 1 μ F ceramic capacitor for channels 2 and 3 are recommended for the input. Select a capacitor that maintains its capacitance over temperature and DC bias. Capacitors with X7R temperature characteristics generally perform well.

Output Capacitor

The minimum output capacitance for stability depends on the current configuration of the channel. See the following table for the capacitance requirements based on the output current capability.

OUTPUT CURRENT (I_{MAX})	$C_{\text{OUT(MIN)}}$ (μ F)	$C_{\text{OUT(TYP)}}$ (μ F)
600mA	2.35	4.7
300mA	1.1	2.2

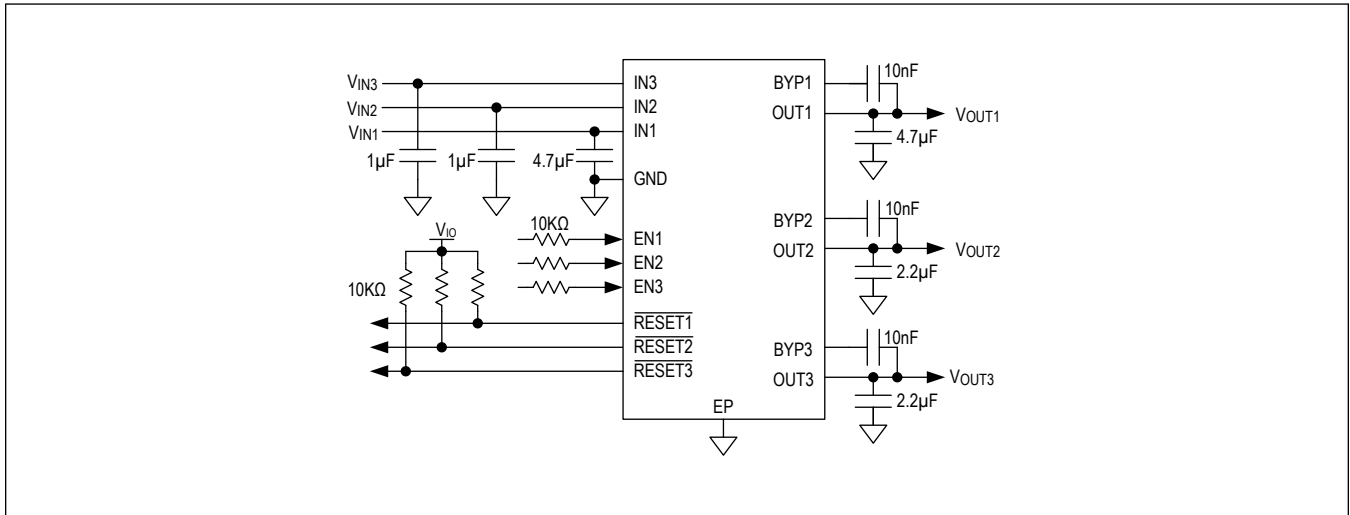
The typical output capacitance assumes an X7R capacitor with a working voltage high enough such that the fully derated output capacitance is greater than $C_{\text{OUT(MIN)}}$.

Thermal Considerations

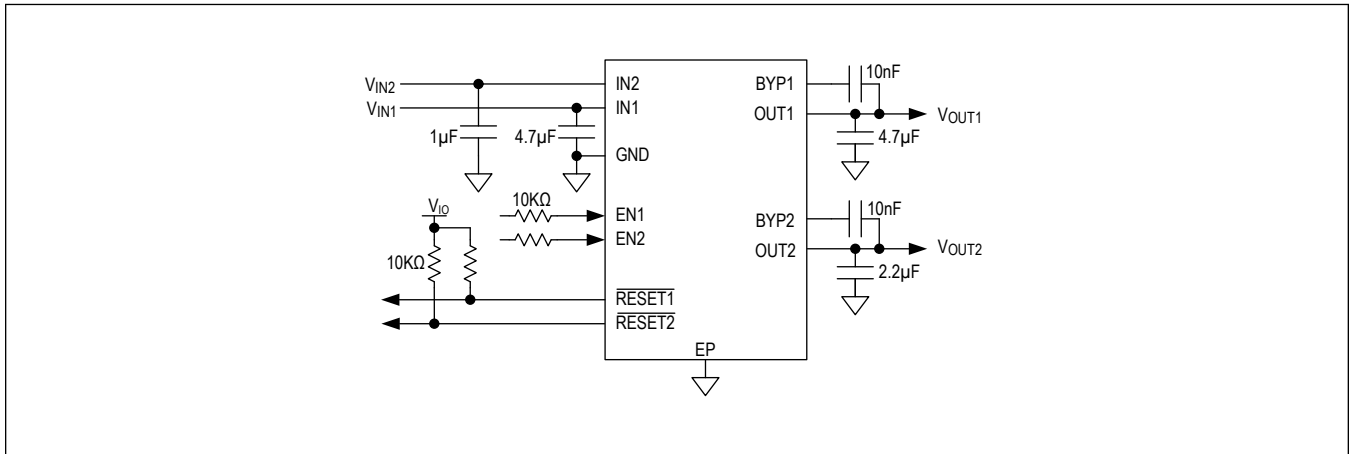
The MAX25307/MAX25308 are packaged in an 16-pin 3mm x 3mm TQFN package with an exposed pad. The exposed pad is the main path for heat to leave the IC, and therefore must be connected to a ground plane with thermal vias to allow heat to dissipate from the device. Thermal properties of the IC package are given in the *Package Information* section.

Typical Application Circuits

Circuit 1 (MAX25308)



Circuit 2 (MAX25307)



Ordering Information

PART NUMBER	V _{OUT1} (V)	I _{MAX1} (A)	V _{OUT2} (V)	I _{MAX2} (A)	V _{OUT3} (V)	I _{MAX3} (A)	HOLD (ms)
MAX25308AATEA/V+	1.2	0.6	1.8	0.3	3.3	0.3	0.5
MAX25307AATEA/V+*	3.3	0.6	1.8	0.3	-	-	3.7

*Future product—Contact factory for availability.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/21	Release for market intro	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Linear Voltage Regulators](#) category:

Click to view products by [Maxim](#) manufacturer:

Other Similar products are found below :

[LV56831P-E](#) [LV5684PVD-XH](#) [MCDTSA6-2R](#) [L7815ACV-DG](#) [LV56801P-E](#) [TCR3DF13,LM\(CT](#) [TCR3DF39,LM\(CT](#) [TLE42794G](#)
[L78L05CZ/1SX](#) [L78LR05DL-MA-E](#) [LM317T](#) [636416C](#) [714954EB](#) [LV5680P-E](#) [L78M15CV-DG](#) [L79M05T-E](#) [TLS202A1MBVHTSA1](#)
[L78LR05D-MA-E](#) [NCV317MBTG](#) [NTE7227](#) [NCV78M09BDTRKG](#) [LV5680NPVC-XH](#) [LT1054CN8](#) [ME6208A50M3G](#) [SL7533-8](#)
[ME6231A50M3G](#) [ME6231A50PG](#) [ME6231C50M5G](#) [AMS1117S-3.3](#) [AMS1117-5.0](#) [AMS1117S-5.0](#) [AMS1117-3.3](#) [MD5118](#) [MD5121](#)
[MD5127](#) [MD5128](#) [MD5130](#) [MD5144](#) [MD5150](#) [MD5115](#) [MD5125](#) [MD5136](#) [MD5140](#) [MD5110](#) [MD52E18WB6](#) [MD52E33WB6](#)
[MD52E15QA3](#) [MD52E21QA3](#) [MD52E25QA3](#) [MD52E28QA3](#)