MAX31328

±3.5ppm, I²C RTC with Integrated Crystal and Power Management

General Description

The MAX31328 is a low-cost, extremely accurate, I²C real-time clock (RTC) with an integrated temperature-compensated crystal oscillator (TCXO) and crystal. The device incorporates a battery input and maintains accurate timekeeping when main power to the device is interrupted. The integration of the crystal resonator enhances the long-term accuracy of the device and eliminates the external crystal requirement in the system. The MAX31328 is available in a 10-pin LGA package.

The RTC maintains seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either 24-hour or 12-hour format with an AM/PM indicator. Two programmable time-of-day alarms and a programmable square-wave output are provided. Address and data are transferred serially through an I²C bidirectional bus. A precision temperature-compensated voltage reference and comparator circuit monitors the status of V_{CC} to detect power failures and automatically switch to the backup supply when necessary. Additionally, the $\overline{RST}$ pin is monitored as a pushbutton input for generating a microprocessor reset.

Applications

- Servers
- Power Meters
- Telematics
- Global Positioning System

Benefits and Features

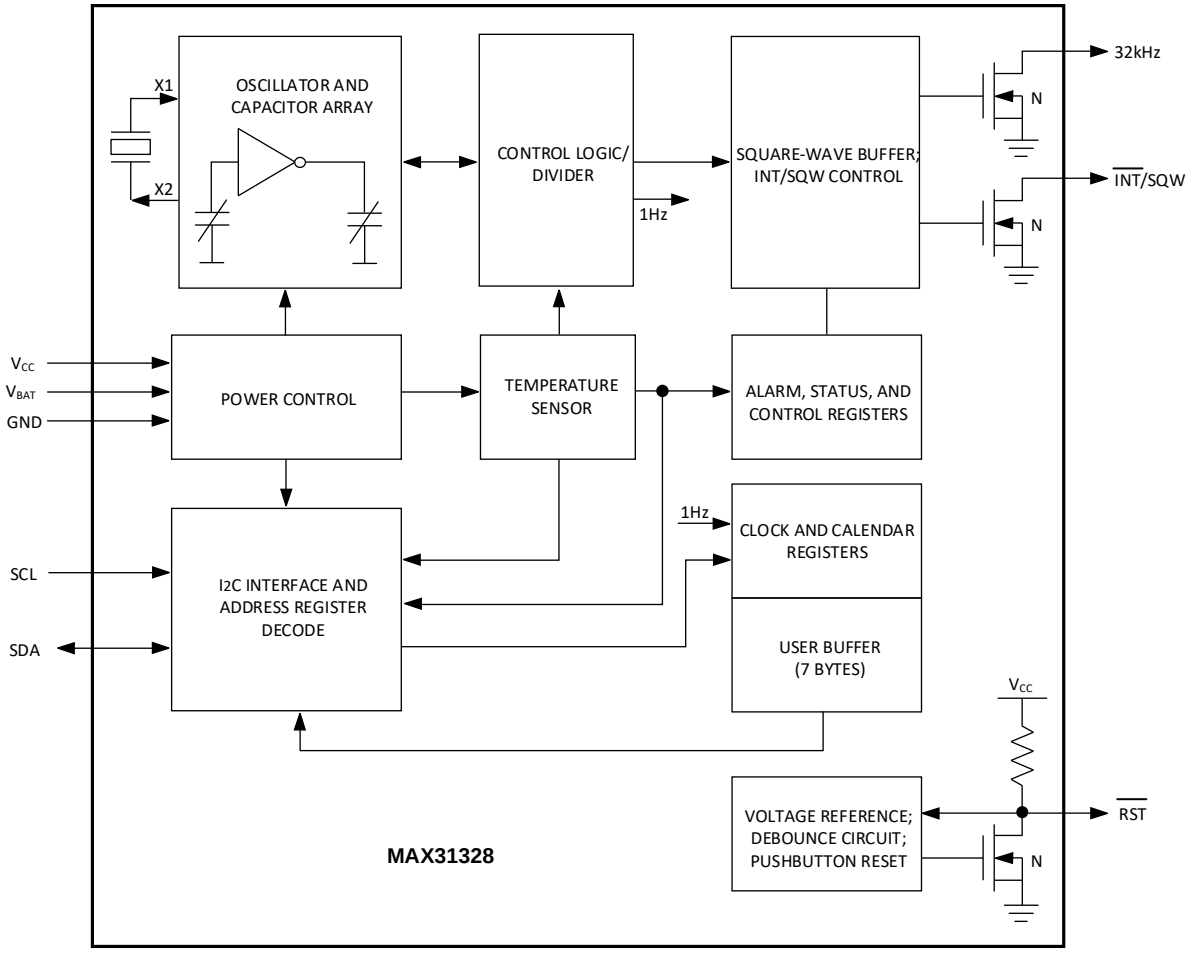
- Highly Accurate RTC Completely Manages All Timekeeping Functions
  - Complete Clock Calendar Functionality, Including Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap-Year Compensation Up to 2100
  - Low Timekeeping Battery Current of 660nA
  - Timekeeping Accuracy ±3.5ppm (±0.302 seconds/day) from -40°C to +85°C
  - Two Time-of-Day Alarms
  - Temperature-Compensated Programmable Square-Wave Output
  - Register for Aging Trim
  - $\overline{RST}$ Output/Pushbutton Reset Debounce Input
  - Digital Temperature Sensor with ±3°C Accuracy
  - +2.3V to +5.5V Supply Voltage
- Simple Serial Interface Connects to Most Microcontrollers
  - I²C Interface (400kHz)
- Battery-Backup Input for Continuous Timekeeping
  - Low-Power Operation Extends Battery-Backup Run Time
  - 3.3V Operation
- Operating Temperature Range: -40°C to +85°C
- 5mm x 5mm 10-Pin LGA Package

***Ordering Information** and package information appear at end of data sheet.*

19-100978; Rev 0; 2/21

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground .....-0.3V to +6V
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+125°C
Storage Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow, 2 times max.) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} or V_{BAT} = +2.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS (Note 1)							
Supply Voltage	V_{CC}			2.3	3.3	5.5	V
	V_{BAT}			2.3	3.0	5.5	
Logic 1 Input (SDA, SCL)	V_{IH}			0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0 Input (SDA, SCL)	V_{IL}			-0.3		0.3 x V_{CC}	V
FREQUENCY AND TIMEKEEPING							
Frequency Stability vs. Temperature	$\Delta f/f_{OUT}$	V_{CC} = 3.3V or V_{BAT} = 3.3V, aging offset = 00h	-40°C to +85°C			±3.5	ppm
Frequency Stability vs. Voltage	$\Delta f/V$				1		ppm/V
Timekeeping Accuracy	Tk_a	V_{CC} = 3.3V				±0.302	seconds/ day
Aging Performance	$\Delta f/f_0$	Not production tested	First year		±1		ppm
			Ten years		±5		
Temperature Accuracy	Temp	V_{CC} = 3.3V or V_{BAT} = 3.3V			±3		°C
GENERAL							
Active Supply Current	I_{CCA}	(Notes 3, 4)	V_{CC} = +3.3V			200	µA
			V_{CC} = 5.5V			300	
Standby Supply Current	I_{CCS}	I²C bus inactive, 32kHz output on, SQW output off, (Note 4)	V_{CC} = 3.3V			110	µA
			V_{CC} = 5.5V			170	
Temperature Conversion Current	$I_{CCSCONV}$	I²C bus inactive, 32kHz output on, SQW output off	V_{CC} = 3.3V			575	µA
			V_{CC} = 5.5V			650	
Power-Fail Voltage	V_{PF}			2.45	2.575	2.70	V
Logic 0 Output (32kHz, $\overline{INT}$/SQW, SDA)	V_{OL}	I_{OL} = 3mA				0.4	V
Logic 0 Output ($\overline{RST}$)	V_{OL}	I_{OL} = 1mA				0.4	V
Output Leakage (32kHz, $\overline{INT}$/SQW, SDA)	I_{LO}	Output high impedance		-1	0	+1	µA

(V_{CC} or V_{BAT} = +2.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Leakage (SCL)	I_{LI}			-1		+1	µA
$\overline{RST}$ I/O Leakage	I_{OL}	$\overline{RST}$ high impedance (Note 5)		-200		+10	µA
V_{BAT} Leakage Current (V_{CC} active)	I_{BATLKG}	V_{BAT} = 3.0V			25	100	nA
BATTERY (V_{CC} = 0V, V_{BAT} = 2.3V to 5.5V, T_A = -40°C to +85°C, UNLESS OTHERWISE NOTED) (Note 1)							
Active Battery Current	I_{BATA}	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = 400kHz (Note 4)	V_{BAT} = 3V			70	µA
			V_{BAT} = 5.5V			150	
Timekeeping Battery Current	I_{BATT}	$\overline{EOSC}$ = 0, BBSQW = 0, EN32kHz = 0, SCL = SDA = 0V or V_{BAT} (Note 4)	V_{BAT} = 3V		660	3000	nA
			V_{BAT} = 5.5V		820	3500	
Temperature Conversion Current	I_{BATTC}	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = SDA = 0V or V_{BAT}	V_{BAT} = 3V			575	µA
			V_{BAT} = 5.5V			650	
Data Retention Current (Oscillator Stopped and I²C Inactive)	I_{BATTDR}	$\overline{EOSC}$ = 0, SCL = SDA = 0V, T_A = +25°C				100	nA
AC CHARACTERISTICS							
POWER SWITCH (Figure 2)							
Minimum V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}				300		µs
Minimum V_{CC} Rise Time; $V_{PF(Min)}$ to $V_{PF(MAX)}$	t_{VCCR}				0		µs
Recovery at Power-Up	t_{REC}	(Note 12)			250	300	ms
GENERAL (V_{CC} = 2.3V to 5.5V or V_{BAT} = 2.3V to 5.5V, V_{BAT} > V_{CC}, T_A = -40°C to +85°C, UNLESS OTHERWISE NOTED) (Note 2)							
SCL Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}			1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 6)		0.6			µs
Low Period of SCL	t_{LOW}			1.3			µs
High Period of SCL	t_{HIGH}			0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 7) (Note 8)		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 9)		100			ns
START Setup Time	$t_{SU:STA}$			0.6			µs
Minimum Rise Time of Both SDA and SCL	t_{RMIN}	(Note 10)			$20 + 0.1C_B$		ns
Maximum Rise Time of Both SDA and SCL	t_{RMAX}				300		ns
Minimum Fall Time for Both SDA and SCL	t_{FMIN}	(Note 11)			$20 + 0.1C_B$		ns
Maximum Fall Time for Both SDA and SCL	t_{FMAX}				300		ns

(V_{CC} or V_{BAT} = +2.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Maximum Capacitive Load for Each Bus Line	C_B	(Note 10)		400		pF
Capacitance for SDA, SCL	$C_{I/O}$			10		pF
SCL Spike Suppression	t_{SP}			30		ns
Pushbutton Debounce	PB_{DB}			250		ms
Reset Active Time	t_{RST}			250		ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 11)		100		ms
Temperature Conversion Time	t_{CONV}			125	200	ms

Note 1: Limits at -40°C are guaranteed by design and not production tested.

Note 2: All voltages are referenced to ground.

Note 3: I_{CCA} - SCL clocking at max frequency = 400kHz.

Note 4: Current is the averaged input current, which includes the temperature conversion current.

Note 5: The $\overline{RST}$ pin has an internal 50kΩ pullup resistor to V_{CC}.

Note 6: After this period, the first clock pulse is generated.

Note 7: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of the SCL.

Note 8: The maximum $t_{HD:DAT}$ needs only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

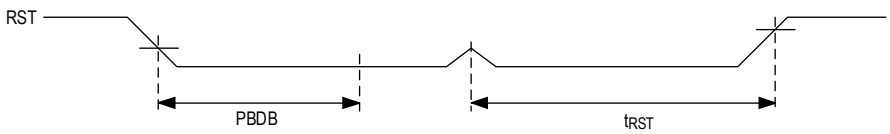
Note 9: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.

Note 10: C_B: Total capacitance of one bus line in pF.

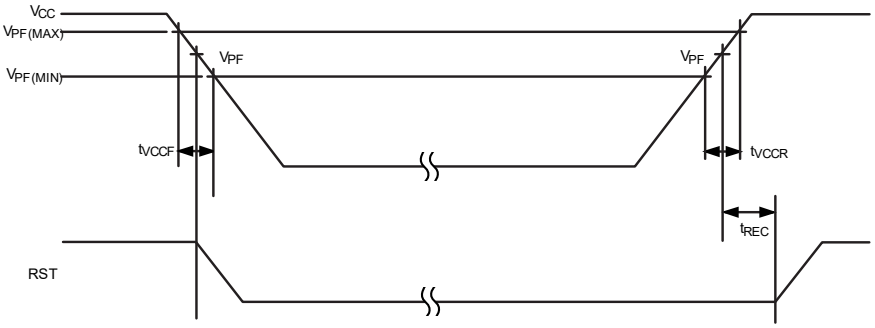
Note 11: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $0V \leq V_{CC} \leq V_{CC(MAX)}$ and $2.3V \leq V_{BAT} \leq 3.4V$.

Note 12: This delay applies only if the oscillator is enabled and running. If the $\overline{EOSC}$ bit is 1, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. The state of $\overline{RST}$ does not affect the I²C interface, RTC, or TCXO.

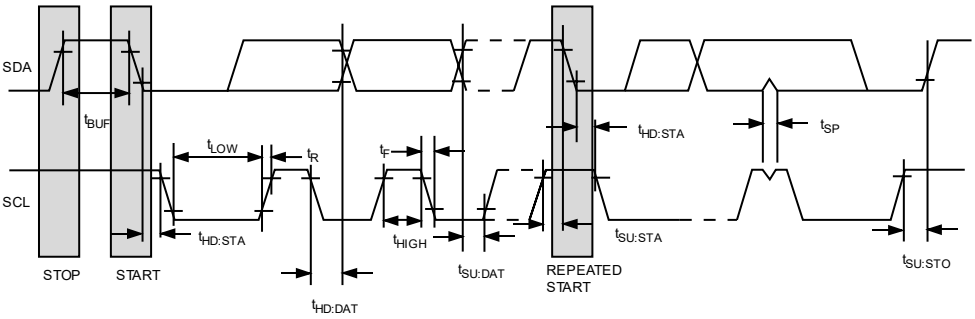
Pushbutton Reset Timing



Power-Switch Timing



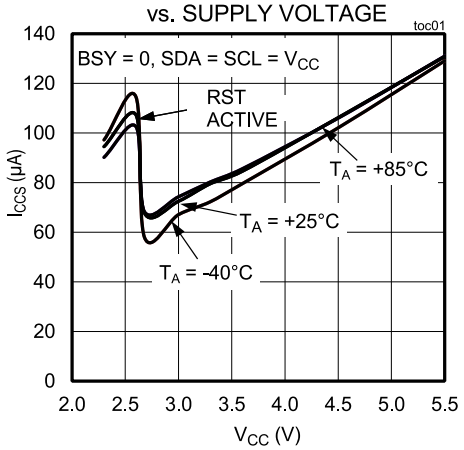
Data Transfer on I²C Serial Bus



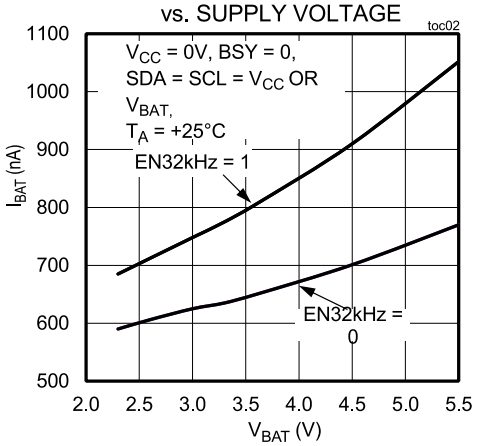
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = 3.3V, V_{BAT} = 3.0V, unless otherwise noted.)

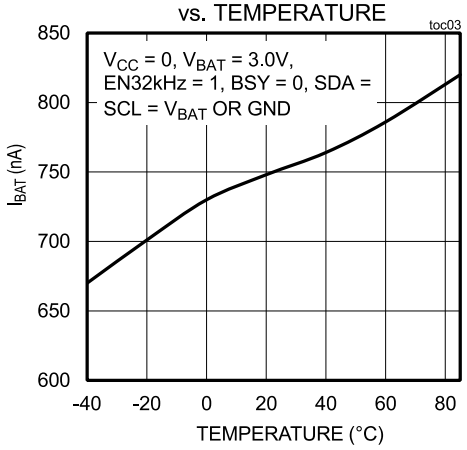
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



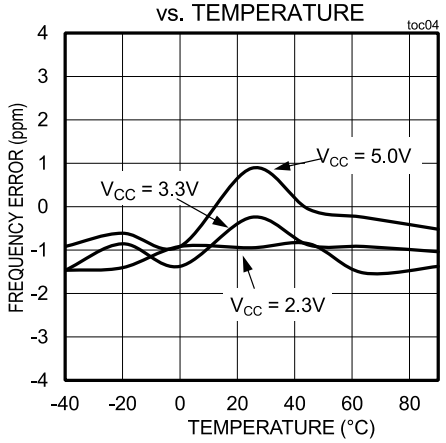
SUPPLY CURRENT vs. SUPPLY VOLTAGE



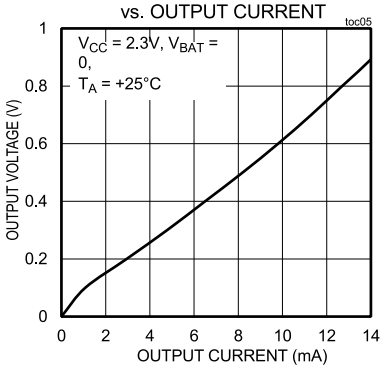
SUPPLY CURRENT vs. TEMPERATURE



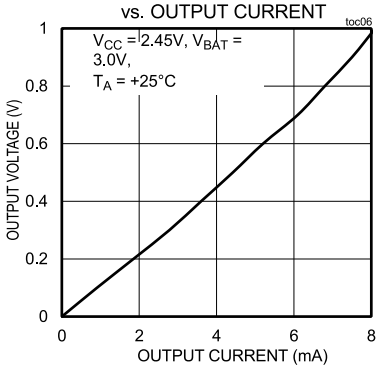
FREQUENCY ERROR vs. TEMPERATURE



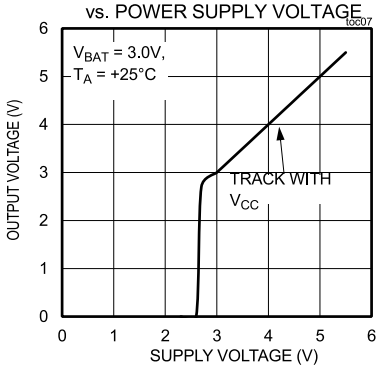
INT/SQW OUTPUT VOLTAGE vs. OUTPUT CURRENT



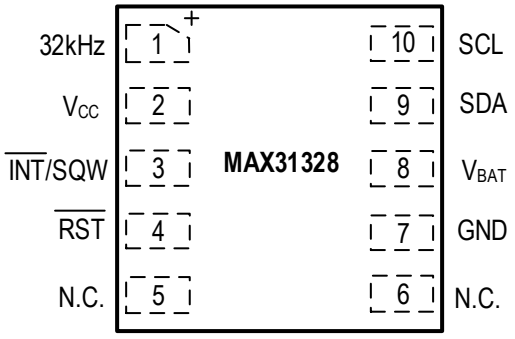
RST OUTPUT VOLTAGE vs. OUTPUT CURRENT



RST OUTPUT VOLTAGE vs. POWER SUPPLY VOLTAGE



Pin Configurations



PIN	NAME	FUNCTION
1	32kHz	32kHz Output. This open-drain pin requires an external pullup resistor. When enabled, the output operates on either power supply. It may be left open if not used.
2	V_{CC}	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1µF to 1.0µF capacitor. If not used, connect to ground.
3	$\overline{INT}$/SQW	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor connected to a supply at 5.5V or less. This multifunction pin is determined by the state of the INTCN bit in the Control Register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by RS2 and RS1 bits. When INTCN is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$ /SQW pin (if the alarm is enabled). It is because the INTCN bit is set to logic 1 when power is first applied, that the pin defaults to an interrupt output with alarms disabled. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}. If not used, this pin can be left unconnected.
4	$\overline{RST}$	Active-Low Reset. This pin is an open-drain input/output. It indicates the status of V_{CC} relative to the V_{PF} specification. As V_{CC} falls below V_{PF}, the $\overline{RST}$ pin is driven low. When V_{CC} exceeds V_{PF}, for t_{RST}, the $\overline{RST}$ pin is pulled high by the internal pullup resistor. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50kΩ nominal value pullup resistor to V_{CC}. No external pullup resistors should be connected. If the oscillator is disabled, t_{REC} is bypassed and $\overline{RST}$ immediately goes high.
5, 6	N.C.	No Connection. Must be connected to ground.
7	GND	Ground
8	V_{BAT}	Backup Power-Supply Input. When using the device with the V_{BAT} input as the primary power source, this pin should be decoupled using a 0.1µF to 1.0µF low-leakage capacitor. When using the device with the V_{BAT} input as the backup power source, the capacitor is not required. If V_{BAT} is not used, connect to ground.
9	SDA	Serial Data Input/Output. This pin is the data input/output for the I²C serial interface. This open-drain pin requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}.
10	SCL	Serial Clock Input. This pin is the clock input for the I²C serial interface and is used to synchronize data movement on the serial interface. Up to 5.5V can be used for this pin, regardless of the voltage on V_{CC}.

Detailed Description

The MAX31328 is a serial RTC driven by a temperature-compensated 32kHz crystal oscillator (TCXO). The TCXO provides a stable and accurate reference clock, and maintains the RTC to within ±2 minutes per year accuracy from -40°C to +85°C. The TCXO frequency output is available at the 32kHz pin. The RTC is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. The $\overline{INT}$/SQW provides either an interrupt signal due to alarm conditions or a square-wave output. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The internal registers are accessible through an I²C bus interface. A temperature-compensated voltage reference and comparator circuit monitors the level of V_{CC} to detect power failures and to automatically switch to the backup supply when necessary. The $\overline{RST}$ pin provides an external pushbutton function and acts as an indicator of a power-fail event.

The block diagram shows the main elements of MAX31328. The eight blocks can be grouped into four functional groups: TCXO, power control, pushbutton reset function, and RTC. Their operations are described separately in the following sections.

32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction, and then sets the internal capacitance selection registers. New values, including changes to the aging correction, are loaded only when a change in the temperature value occurs or when a user-initiated temperature conversion is completed. Temperature conversion occurs on initial application of V_{CC} and once every 64 seconds afterwards.

Power Control

This function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. When V_{CC} is greater than V_{PF}, the part is powered by V_{CC}. When V_{CC} is less than V_{PF} but greater than V_{BAT}, the MA31328 is powered by V_{CC}. If V_{CC} is less than V_{PF} and is less than V_{BAT}, the device is powered by V_{BAT}. See Table 1.

Table 1. Power Control

SUPPLY CONDITION	ACTIVE SUPPLY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	V_{BAT}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}

To preserve the battery, the first time V_{BAT} is applied to the device, the oscillator does not start up until V_{CC} exceeds V_{PF}, or until a valid I²C address is written to the part. Typical oscillator startup time is less than one second. Approximately 2 seconds after V_{CC} is applied, or a valid I²C address is written, the device makes a temperature measurement and applies the calculated correction to the oscillator. Once the oscillator is running, it continues to run as long as a valid power source is available (V_{CC} or V_{BAT}), and the device continues to measure the temperature and correct the oscillator frequency every 64 seconds. On the first application of power (V_{CC}) or when a valid I²C address is written to the part (V_{BAT}), the time and date registers are reset to 01/01/00 01 00:00:00 (DD/MM/YY DOW HH:MM:SS).

V_{BAT} Operation

There are several modes of operation that affect the amount of V_{BAT} current that is drawn. While the device is powered by V_{BAT} and the serial interface is active, active battery current, I_{BATA}, is drawn. When the serial interface is inactive, timekeeping current (I_{BATT}), which includes the averaged temperature conversion current, I_{BATTC}, is used (refer to *Application Note 3644: Power Considerations for Accurate Real-Time Clocks* for details). Temperature conversion current, I_{BATTC}, is specified since the system must be able to support the periodic higher current pulse and still maintain a

valid voltage level. Data retention current, I_{BATTDR}, is the current drawn by the part when the oscillator is stopped ($\overline{EOSC}$ = 1). This mode can be used to minimize battery requirements for times when maintaining time and date information is not necessary, e.g., while the end system is waiting to be shipped to a customer.

Pushbutton Reset Function

The MAX31328 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the MAX31328 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a falling edge. If an edge transition is detected, the MAX31328 debounces the switch by pulling the $\overline{RST}$ low. After the internal timer has expired (PB_{DB}), the MAX31328 continues to monitor the $\overline{RST}$ line. If the line is still low, the MAX31328 continuously monitors the line looking for a rising edge. Upon detecting release, the MAX31328 forces the $\overline{RST}$ pin low and holds it low for t_{RST}. The $\overline{RST}$ is also used to indicate a power-fail condition. When V_{CC} is lower than V_{PF}, an internal power-fail signal is generated, which forces the $\overline{RST}$ pin low. When V_{CC} returns to a level above V_{PF}, the $\overline{RST}$ pin is held low for approximately 250ms (t_{REC}) to allow the power supply to stabilize. If the oscillator is not running (see the *Power Control* section) when V_{CC} is applied, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. Assertion of the $\overline{RST}$ output, whether by pushbutton or power-fail detection, does not affect the internal operation of the MAX31328.

Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The clock provides two programmable time-of-day alarms and a programmable square-wave output. The $\overline{INT}$/SQW pin either generates an interrupt due to an alarm condition or outputs a square-wave signal, and the selection is controlled by the bit INTCN.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. The register map illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The MAX31328 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic-high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20–23 hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the MAX31328. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Alarms

The MAX31328 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the Alarm Enable and INTCN bits of the Control Register) to activate the $\overline{INT}$/SQW output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the $\overline{INT}$/SQW signal. The match is tested on the once-per-second update of the time and date registers.

Table 2. Alarm Mask Bits

DY/$\overline{DT}$	ALARM REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

I²C Interface

The I²C interface is accessible whenever either V_{CC} or V_{BAT} is at a valid level. If a microcontroller connected to the MAX31328 resets because of a loss of V_{CC} or other event, it is possible that the microcontroller and MAX31328 I²C communications could become unsynchronized, e.g., the microcontroller resets while reading data from the MAX31328. When the microcontroller resets, the MAX31328 I²C interface may be placed into a known state by toggling serial clock (SCL) until SDA is observed to be at a high level. At that point, the microcontroller should pull SDA low while SCL is high, generating a START condition.

I²C Serial Data Bus

The MAX31328 supports a bidirectional I²C bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data is defined as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the SCL, controls the bus access, and generates the START and STOP conditions. The MAX31328 operates as a slave on the I²C bus. Connections to the bus are made through the SCL input and open-drain SDA I/O lines. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The MAX31328 works in both modes.

The following bus protocol has been defined (Figure 1):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

START data transfer: A change in the state of the data line from HIGH to LOW, while the clock line is HIGH, defines a START condition.

STOP data transfer: A change in the state of the data line from LOW to HIGH, while the clock line is HIGH, defines a STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figures 2 and 3 detail how data transfer is accomplished on the I²C bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

Data transfer from a slave transmitter to a master receiver. The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned.

The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The MAX31328 can operate in the following two modes:

- **Slave Receiver Mode (MAX31328 Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit MAX31328 address, which is 1101000, followed by the direction bit (R/W), which is 0 for a write. After receiving and decoding the slave address byte, the MAX31328 outputs an acknowledge on SDA. After the MAX31328 acknowledges the slave address + write bit, the master transmits a word address to the MAX31328. This sets the register pointer on the MAX31328, with the MAX31328 acknowledging the transfer. The master may then transmit zero or more bytes of data, with the MAX31328 acknowledging each byte received. The register pointer increments after each data byte is transferred. The master generates a STOP condition to terminate the data write.
- **Slave Transmitter Mode (MAX31328 Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the MAX31328 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit MAX31328

address, which is 1101000, followed by the direction bit (R/W), which is 1 for a read. After receiving and decoding the slave address byte, the MAX31328 outputs an acknowledge on the SDA. The MAX31328 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode, then the first address that is read is the last one stored in the register pointer. The MAX31328 must receive a “not acknowledge” to end a read.

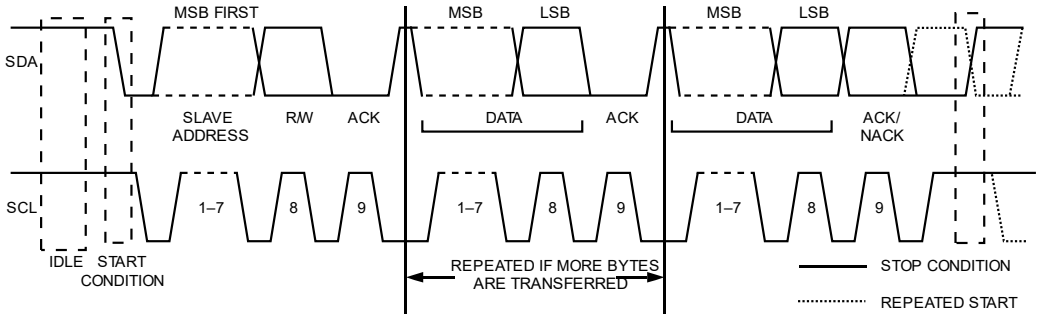


Figure 1. I²C Data Transfer Overview

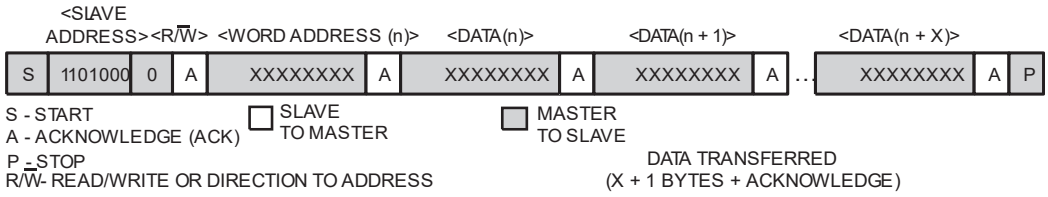


Figure 2. Data Write—Slave Receiver Mode

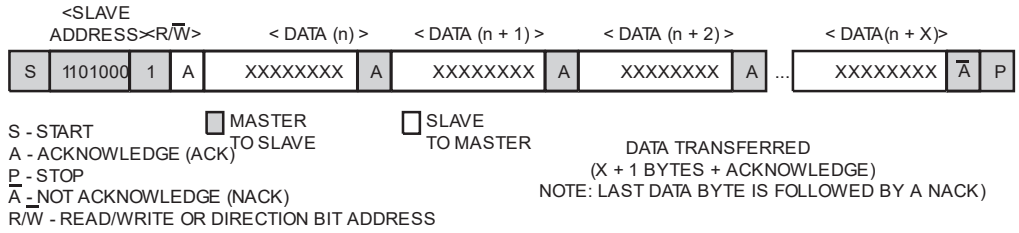


Figure 3. Data Read—Slave Transmitter Mode

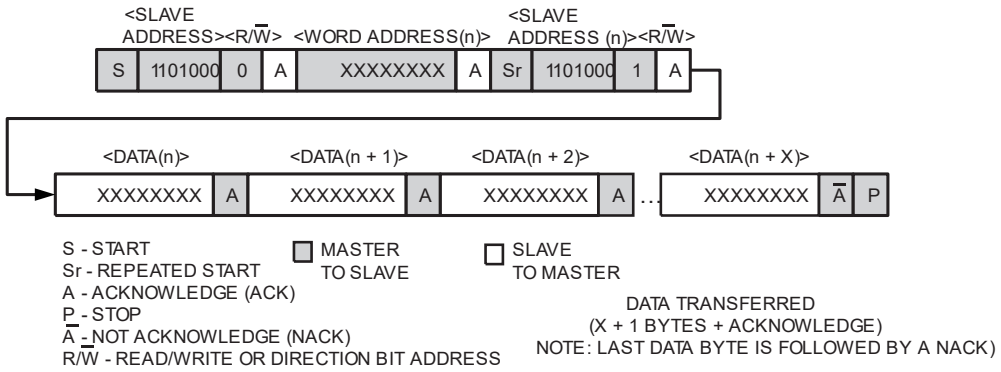


Figure 4. Data Write/Read (Write Pointer, Then Read)—Slave Receive and Transmit

Register Map

RC28 Register Map

ADDRESS	NAME	MSB							LSB
REGBLK									
0x00	Seconds[7:0]	–	sec_10[2:0]			seconds[3:0]			
0x01	Minutes[7:0]	–	min_10[2:0]			minutes[3:0]			
0x02	Hours[7:0]	–	f_24_12	hr20_AM_PM	hour_10	hour[3:0]			
0x03	Day[7:0]	–	–	–	–	–	day[2:0]		
0x04	Date[7:0]	–	–	date_10[1:0]		date[3:0]			
0x05	Month[7:0]	century	–	–	month_10	month[3:0]			
0x06	Year[7:0]	year_10[3:0]				year[3:0]			
0x07	Alm1_sec[7:0]	A1M1	sec_10[2:0]			seconds[3:0]			
0x08	Alm1_min[7:0]	A1M2	min_10[2:0]			minutes[3:0]			
0x09	Alm1_hrs[7:0]	A1M3	f_24_12	AM_PM_hr20	hr_10	hour[3:0]			
0x0A	Alm1day_date[7:0]	A1M4	DY_DT	date_10[1:0]		day_date[3:0]			
0x0B	Alm2_min[7:0]	A2M2	min_10[2:0]			minutes[3:0]			
0x0C	Alm2_hrs[7:0]	A2M3	f_24_12	AM_PM_hr20	hr_10	hour[3:0]			
0x0D	Alm2day_date[7:0]	A2M4	DY_DT	date_10[1:0]		day_date[3:0]			
0x0E	Control[7:0]	EOSC	BBSQW	CONV	RS[1:0]		INTCN	A2IE	A1IE
0x0F	Status[7:0]	OSF	–	–	–	EN32kHz	BSY	A2F	A1F
0x10	Aging Offset[7:0]	Sign	Data[6:0]						
0x11	Temp_MSB[7:0]	Sign	Data[6:0]						
0x12	Temp_LSB[7:0]	Data[1:0]		–	–	–	–	–	–

Register Details

Seconds (0x0)

BIT	7	6	5	4	3	2	1	0
Field	–	sec_10[2:0]			seconds[3:0]			
Reset	–							
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
sec_10	6:4	RTC seconds in multiples of 10
seconds	3:0	RTC seconds

Minutes (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	min_10[2:0]			minutes[3:0]			
Reset	–							
Access Type	–	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
min_10	6:4	RTC minutes in multiples of 10
minutes	3:0	RTC minutes

Hours (0x2)

BIT	7	6	5	4	3	2	1	0
Field	–	f_24_12	hr20_AM_PM	hour_10	hour[3:0]			
Reset	–							
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
f_24_12	6	Sets RTC in 12-hr or 24-hr format	0x0: 24-hr format 0x1: 12-hr format
hr20_AM_PM	5	In 12-hr format, this works as the AM/PM indicator. In 24-hr format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format 0x1: Indicates PM in 12-hr format
hour_10	4	RTC hours in multiples of 10	
hour	3:0	RTC hours	

Day (0x3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	day[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
day	2:0	RTC days

Date (0x4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	date_10[1:0]		date[3:0]			
Reset	–	–						
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION
date_10	5:4	RTC date in multiples of 10
date	3:0	RTC date

Month (0x5)

BIT	7	6	5	4	3	2	1	0

Field	century	–	–	month_10	month[3:0]
Reset		–	–		
Access Type	Write, Read	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
century	7	Century bit	0x0: Year is in current century 0x1: Year is in the next century
month_10	4	RTC month in multiples of 10	
month	3:0	RTC month	

Year (0x6)

BIT	7	6	5	4	3	2	1	0
Field	year_10[3:0]				year[3:0]			
Reset								
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
year_10	7:4	RTC years in multiples of 10
year	3:0	RTC years

Alm1_sec (0x7)

BIT	7	6	5	4	3	2	1	0
Field	A1M1	sec_10[2:0]			seconds[3:0]			
Reset								
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M1	7	Alarm1 mask bit for seconds
sec_10	6:4	Alarm 1 seconds in multiples of 10

BITFIELD	BITS	DESCRIPTION
seconds	3:0	Alarm 1 seconds

Alm1_min (0x8)

BIT	7	6	5	4	3	2	1	0
Field	A1M2	min_10[2:0]			minutes[3:0]			
Reset								
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M2	7	Alarm1 mask bit for minutes
min_10	6:4	Alarm 1 minutes in multiples of 10
minutes	3:0	Alarm 1 minutes

Alm1_hrs (0x9)

BIT	7	6	5	4	3	2	1	0
Field	A1M3	f_24_12	AM_PM_hr20	hr_10	hour[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M3	7	Alarm1 mask bit for hours	
f_24_12	6	Sets Alarm1 in 12-hr or 24-hr format	0x0: 24-hr format 0x1: 12-hr format
AM_PM_hr20	5	In 12-hr format, this works as the AM/PM indicator. In 24-hr format, it is the Alarm1 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format 0x1: Indicates PM in 12-hr format
hr_10	4	Alarm 1 hours in multiples of 10	
hour	3:0	Alarm 1 hours	

Alm1day_date (0xA)

BIT	7	6	5	4	3	2	1	0
Field	A1M4	DY_DT	date_10[1:0]		day_date[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M4	7	Alarm1 mask bit for day/date	
DY_DT	6		0x0: Alarm when date match 0x1: Alarm when day match
date_10	5:4	Alarm1 date in multiples of 10	
day_date	3:0	Alarm1 day/date	

Alm2_min (0xB)

BIT	7	6	5	4	3	2	1	0
Field	A2M2	min_10[2:0]			minutes[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A2M2	7	Alarm2 mask bit for minutes
min_10	6:4	Alarm2 minutes in multiples of 10
minutes	3:0	Alarm2 minutes

Alm2_hrs (0xC)

BIT	7	6	5	4	3	2	1	0
Field	A2M3	f_24_12	AM_PM_hr20	hr_10	hour[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M3	7	Alarm2 mask bit for hours	
f_24_12	6	Sets Alarm1 in 12-hr or 24-hr format	0x0: 24-hr format 0x1: 12-hr format
AM_PM_hr20	5	In 12-hr format, this works as the AM/PM indicator. In 24-hr format, it is the Alarm1 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format 0x1: Indicates PM in 12-hr format
hr_10	4	Alarm2 hours in multiples of 10	
hour	3:0	Alarm2 hours	

Alm2day_date (0xD)

BIT	7	6	5	4	3	2	1	0
Field	A2M4	DY_DT	date_10[1:0]		day_date[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M4	7	Alarm2 mask bit for day/date	
DY_DT	6	This bit selects alarm when day match or date match.	0x0: Alarm when date match 0x1: Alarm when day match
date_10	5:4	Alarm2 date in multiples of 10	
day_date	3:0	Alarm2 day/date	

Control (0xE)

Control Register

BIT	7	6	5	4	3	2	1	0
Field	EOSC	BBSQW	CONV	RS[1:0]		INTCN	A2IE	A1IE
Reset	0x0	0x0	0x0	0x3		0x1	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EOSC	7	Enable Oscillator Oscillator is always enabled when part is running on V_{CC}.	0x0: Oscillator enabled 0x1: Oscillator disabled (only on VBAT)
BBSQW	6	Battery-backed square-wave enable	0x0: INT/SQW pin goes high impedance when $V_{CC} < V_{PF}$ 0x1: Enables square wave on INT/SQW pin when INTCN = 0 and $V_{CC} < V_{PF}$
CONV	5	Temperature Conversion Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance array to the oscillator. This can only happen when a conversion is not already in progress. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second update cycle. A user-initiated temperature conversion does not affect the BSY bit for approximately 2ms. The CONV bit remains at a 1 from the time it is written until the conversion is finished, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion.	0x0 0x1: Convert temperature and execute TCXO algorithm
RS	4:3	SQW Frequency Select	0x0: 1Hz 0x1: 1.024kHz 0x2: 4.096kHz 0x3: 8.192kHz
INTCN	2	Interrupt Control	0x0: Square wave is output on the INT/SQW pin. 0x1: Alarm interrupts are output on the INT/SQW pin.
A2IE	1	Alarm 2 Interrupt Enable	0x0: Alarm 2 interrupt disabled 0x1: Alarm 2 interrupt enabled
A1IE	0	Alarm 1 interrupt enable	0x0: Alarm 1 interrupt disabled 0x1: Alarm 1 interrupt enabled

Status (0xF)

Status Register

BIT	7	6	5	4	3	2	1	0
Field	OSF	–	–	–	EN32kHz	BSY	A2F	A1F
Reset	0x1	–	–	–	0x1			
Access Type	Read Only	–	–	–	Write, Read	Read Only	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OSF	7	Oscillator Stop Flag A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set: 1) The first time when power is applied. 2) The voltages present on both V_{CC} and V_{BAT} are insufficient to support oscillation. 3) The EOSC bit is turned off in battery-backed mode. 4) External influences on the crystal (i.e., noise, leakage, etc.)	0x0 0x1: Indicates that the oscillator is stopped or was stopped for some period
EN32kHz	3	Enable 32kHz output	0x0: 32kHz pin goes to a high impedance state 0x1: 32.768kHz square wave is output on the 32kHz pin
BSY	2	Busy Flag This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the device is in the 1-minute idle state.	
A2F	1	Alarm 2 flag A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is logic 1 and the INTCN bit is set to logic 1, the INT/SQW pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.	
A1F	0	Alarm 1 flag A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is logic 1 and the INTCN bit is set to logic 1, the INT/SQW pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.	

Aging Offset (0x10)

The aging offset register takes a user-provided value to add to or subtract from the codes in the capacitance array registers. The code is encoded in two's complement, with bit 7 representing the sign bit. One LSB represents one small capacitor to be switched in or out of the capacitance array at the crystal pins. The aging offset register capacitance value is added or subtracted from the capacitance value that the device calculates for each temperature compensation. The offset register is added to the capacitance array during a normal temperature conversion, if the temperature changes from the previous conversion, or during a manual user conversion (setting the CONV bit). To see the effects of the aging register on the 32kHz output frequency immediately, a manual conversion should be started after each aging register change. Positive aging values add capacitance to the array, slowing the oscillator frequency. Negative values

remove capacitance from the array, increasing the oscillator frequency. The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is shifted by the values used in this register. At +25°C, one LSB typically provides about 0.1ppm change in frequency. Use of the aging register is not needed to achieve the accuracy as defined in the EC tables but could be used to help compensate for aging at a given temperature. See the *Typical Operating Characteristics* section for a graph showing the effect of the register on accuracy over temperature.

BIT	7	6	5	4	3	2	1	0
Field	Sign	Data[6:0]						
Reset								
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
Sign	7	
Data	6:0	

Temp_MSB (0x11)

Temperature is represented as a 10-bit code with a resolution of 0.25°C and is accessible at locations 11h and 12h. The temperature is encoded in two's complement format. The upper 8 bits, the integer portion, are at location 11h and the lower 2 bits, the fractional portion, are in the upper nibble at location 12h. For example, 00011001 01b = +25.25°C. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion. The temperature is read on initial application of V_{CC} or I²C access on V_{BAT} and once every 64 seconds afterwards. The temperature registers are updated after each user-initiated conversion and on every 64-second conversion. The temperature registers are read-only.

BIT	7	6	5	4	3	2	1	0
Field	Sign	Data[6:0]						
Reset								
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
Sign	7	
Data	6:0	

Temp_LSB (0x12)

BIT	7	6	5	4	3	2	1	0

Field	Data[1:0]	–	–	–	–	–	–
Reset		–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
Data	7:6	

Applications Information

Power-Supply Decoupling

To achieve the best results when using the device, decouple the V_{CC} and/or V_{BAT} power supplies with 0.1µF and/or 1.0µF capacitors. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize the lead inductance that improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

If communications during battery operation are not required, the V_{BAT} decoupling capacitor can be omitted.

Using Open-Drain Outputs

The $\overline{INT}$/SQW and 32kHz outputs are open-drain and, therefore, require external pullup resistors to realize logic-high output levels. The pullup resistor value is typically 10kΩ.

SDA and SCL Pullup Resistors

SDA is an open-drain output and requires an external pullup resistor to realize a logic-high level. It is because the device does not use clock cycle stretching, that a master using either an open-drain output with a pullup resistor or CMOS output driver (push-pull) could be used for SCL.

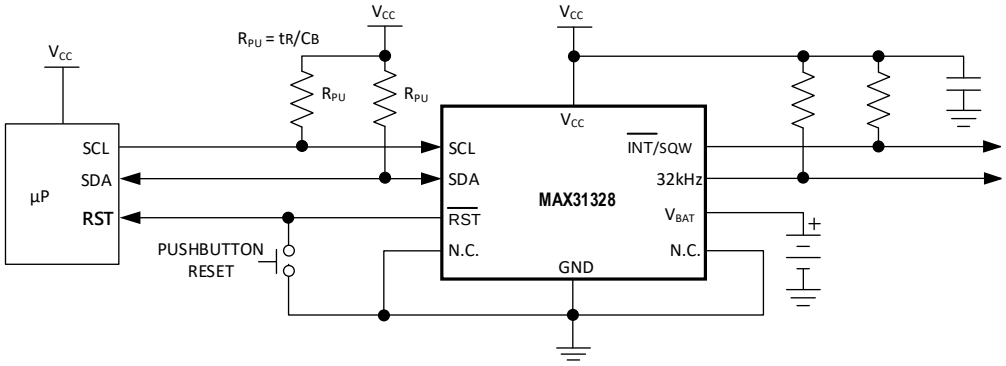
Handling, PCB Layout, and Assembly

The MAX31328 package contains a quartz tuning-fork crystal. Pick-and-place equipment can be used, but precautions should be taken to ensure that excessive shocks are avoided. Ultrasonic cleaning should be avoided to prevent damage to the crystal.

Avoid running signal traces under the package unless a ground plane is placed between the package and the signal line. All N.C. (no connection) pins must be connected to ground.

Moisture-sensitive packages are shipped from the factory dry packed. Handling instructions listed on the package label must be followed to prevent damage during reflow. Refer to the IPC/JEDEC J-STD-020 standard for moisture-sensitive device (MSD) classifications and reflow profiles. Exposure to reflow is limited to two times the maximum.

Typical Application Circuits



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX31328NELB+	-40°C to +85°C	10-LGA
MAX31328NELB+T	-40°C to +85°C	10-LGA

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

[LGA]

Package Code	L1055M+1
Outline Number	21-100481
Land Pattern Number	91-100169
Thermal Resistance, Multi-Layer Board:	
Junction-to-Ambient (θ_{JA})	145.45 °C/W
Junction-to-Case Thermal Resistance (θ_{JC})	66.67 °C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/21	Release for Market Intro	—

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