MAX31915

Industrial, Octal, Digital Input Translator

General Description

The MAX31915 translates and conditions the 24V digital output of sensors and switches used in industrial, process, and building automation to 5V CMOS-compatible signals required by microcontrollers. It provides the front-end interface circuit of a programmable logic controller (PLC) digital input module.

The signal voltage translation is performed in conjunction with input current limiting and lowpass filtering. Input current-limiting allows a significant reduction in power consumed from the field-supply voltage, as compared to traditional discrete resistor-divider implementations.

Selectable on-chip lowpass filters allow flexible debouncing and filtering of sensor inputs based on the application. When no filtering is selected, the IC is capable of detecting pulses as short as 0.75µs at its field inputs.

All 8 input channels are translated to CMOS logic levels and are presented in parallel on the eight output pins for direct or galvanically-isolated interface with a controller ASIC or micro.

The on-chip 5V voltage regulator can be used to power external optocouplers, digital isolators, or other external 5V circuitry.

For ultra-low-power applications and lowest possible heat dissipation, Maxim Integrated plans to offer a pin-compatible version of this device; the MAX31914. The MAX31914 uses patent-pending circuit techniques to achieve further reduction of power beyond what is possible by input current limiting alone. Contact the factory for availability.

Applications

- Digital Input Modules for Programmable Logic Controllers (PLCs)
- Industrial Automation, Building Automation
- Process Automation

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Flexible Supply Options Enables Usage in 24V, 12V, and 5V Supplied Systems
  - 7V to 36V Wide Operating Field Supply Range
  - Device Can Be Optionally Powered from the Logic-Side Using a 5V Supply
- Low Power and Low Heat Dissipation
  - Very Low Quiescent Current
  - Extremely Accurate and Stable Input Current Limiters
- Configurability Enables a Wide Range of Standard and Custom Applications
  - Configurable Inputs for IEC 61131-2 Input Types 1, 2, and 3 or for Standard CMOS Logic Levels
  - 0.5mA to 6mA Configurable Input Current Limiting
  - Selectable Input Filtering and Debounce: 0, 25µs, 0.75ms, and 3ms Settings
- High Integration Reduces BOM Count and Board Space
  - 8 High-Voltage Input Channels (36V Max)
  - 8 CMOS Logic Outputs for High-Speed Simultaneous Transfer of All Input States to the Controller
  - On-Chip 5V Regulator
  - On-Chip Overtemperature Indicator
  - On-Chip Field-Supply Voltage Monitor
  - High HBM ESD Immunity on all Field Input Pins (15kV HBM)

19-7472; Rev 1; 4/15

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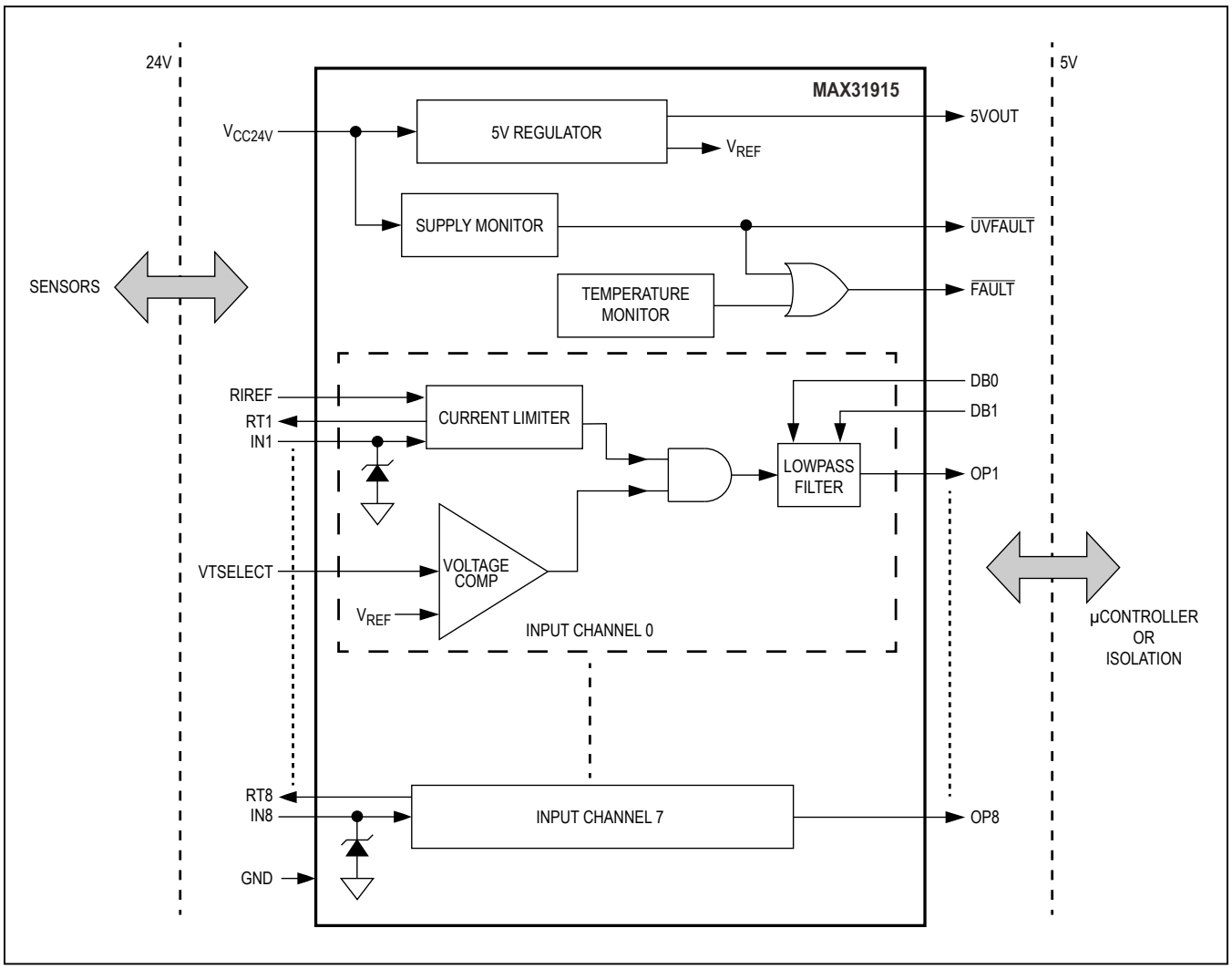
Block Diagram



Absolute Maximum Ratings

Voltage on V_{CC24V} Relative to GND .....-0.3V to +45V
Voltage on IN1–IN8 Relative to GND
through 2.2kΩ Resistors.....-45V to +45V
Voltage on DB0/DB1,
VTSELECT Relative to GND.....-0.3V to 6V
Ambient Temperature Range ..... -40°C to +125°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range..... -55°C to +125°C
Continuous Power Dissipation (T_A = +70°C)
(derate 22.2mW above +70°C) 1773.8mW
Soldering Temperature, Lead(Pb)-Free (reflow) .....260°C
Lead Temperature (soldering, 10s) .....300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....45.10°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Field-Supply Voltage	V_{CC24V}	Note 2	7		36	V
Field Inputs Voltage	V_{Inn}	Note 3	-0.3		+36	V
Logic Inputs Voltage	V_{LOGIC}		-0.3		+5.5	V
Current-Limit Setting Resistor	R_{REF}	VTSELECT = logic 1		15		kΩ
		VTSELECT = logic 0		150		

DC Electrical Characteristics

(T_A = -40°C to +125°C, T_J ≤ +150°C, V_{CC24V} = 7V to 36V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Field-Supply Curent	I_{CC24V}	IN1–IN8 = 24V, 5VOUT = open, OP1–OP8 and all logic inputs = open		1.6	2.3	mA
Field-Supply Low Alarm Off-On	V_{ONUVLO}		7	8		V
Field-Supply Low Alarm On-Off	$V_{OFFUVLO}$			9	10	V
Field Input Threshold, High to Low	$VIN1-_{(INF)}$	2.2kΩ external series resistor, VTSELECT = logic 1, R_{REF} = 15kΩ	7	8.4		V
Field Input Threshold, Low to High	$VIN1+_{(INF)}$	2.2kΩ external series resistor, VTSELECT = logic 1, R_{REF} = 15kΩ		9.4	10.5	V
Field Input Hysterisis	$VHYS1_{(INF)}$	2.2kΩ external series resistor, VTSELECT = logic 1, R_{REF} = 15kΩ		1		V
Field Input Threshold, High to Low	$VIN0-_{(INF)}$	2.2kΩ external series resistor, VTSELECT = logic 0, R_{REF} = 150kΩ	1.5	1.7		V

DC Electrical Characteristics (continued)

(T_A = -40°C to +125°C, T_J ≤ +150°C, V_{CC24V} = 7V to 36V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Field Input Threshold, Low to High	$VIN0+_{(INF)}$	2.2kΩ external series resistor, VTSELECT = logic 0, R_{REF} = 150kΩ		2.2	3.5	V
Field Input Hysterisis	$VHYS0_{(INF)}$	2.2kΩ external series resistor, VTSELECT = logic 0, R_{REF} = 150kΩ		0.5		V
Input Threshold, High to Low (at IC Pin)	$VTH1-_{(INP)}$	VTSELECT = logic 1, R_{REF} = 15kΩ	3	3.4		V
Input Threshold, Low to High (at IC Pin)	$VTH1+_{(INP)}$	VTSELECT = logic 1, R_{REF} = 15kΩ		4.4	5	V
Input Threshold Hysteresis (at IC Pin)	$VHYS1_{(INP)}$	VTSELECT = logic 1, R_{REF} = 15kΩ		1		V
Input Threshold, High to Low (at IC Pin)	$VTH0-_{(INP)}$	VTSELECT = logic 0, R_{REF} = 150kΩ	1.5	1.7		V
Input Threshold, Low to High (at IC Pin)	$VTH0+_{(INP)}$	VTSELECT = logic 0, R_{REF} = 150kΩ		2.2	3.5	V
Input Threshold Hysteresis (at IC Pin)	$VHYS0_{(INP)}$	VTSELECT = logic 0, R_{REF} = 150kΩ		0.5		V
Field Pin Input Resistance	R_{INP}			0.8		kΩ
Field Input Curent Limit	I_{INLIM}	R_{REF} = 15 kΩ (Note 4), VTSELECT = logic 1	2.26	2.45	2.72	mA
Filter Time Constant	t_{FILTER}	DB1/DB0 = 0/0: no filtering		0		ms
		DB1/DB0 = 0/1	0.008	0.025	0.038	
		DB1/DB0 = 1/0	0.25	0.75	1.1	
		DB1/DB0 = 1/1	1.0	3	4.5	
Linear Regulator Output	V_{5VOUT}	Max I_{ILOAD} = 50mA	4.75	5.0	5.25	V
Regulator Line Regulation	$dVREG_{LINE}$	I_{LOAD} = 50mA		10		mV
Regulator Load Regulation	$dVREG_{LOAD}$	I_{LOAD} = 1mA to 50mA		20		mV
Logic-Low Output Voltage	V_{OL}	I_{OL} = 4mA		0.4	1.0	V
Logic-High Output Voltage	V_{OH}	I_{OH} = -4mA	4.0			V
Logic Input Leakage Curent	I_{IL}	All inputs have internal pullups	-50	-30	-15	µA
Overtemperature Alarm	T_{ALRM}	(Note 5)		135		°C
LED On-State Current		R_{REF} = 15kΩ		2.2		mA

AC Electrical Characteristics

(T_A = -40°C to +125°C, T_J ≤ +150°C, V_{CC24V} = 7V to 36V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Data Rate	f_{IN}	DB0, DB1 = 0, 0 (filters disabled)		0.5	1.3	Mbps
Input Pulse Width	PW_{IN}	DB0, DB1 = 0, 0 (filters disabled)	0.75			µs
Interchannel Propagation Delay Mismatch (Interchannel Jitter)	ϕint	(Note 6)			25	ns
Propagation Delay	t_{PROP}	12V input applied on the field-side through external 2.2kΩ resistors, R_{REF} set to 15k, VTSELECT = 1 (Notes 7, 8)		300	700	ns
Output Rise/Fall Times (on OPn Pins)	$t_{R/F}$	Internally slew limited (with C_{LOAD} = 0–50pF)		25		ns
ESD		HBM, all pins		±2		kV
		HBM, IN1–IN8 with respect to GND		±15		

Note 2: If a 24V supply is not available, the device can be powered through 5VOUT. In this mode of operation, the V_{CC24V} supply must be left unconnected. All other specifications remain identical. The field-supply alarms are asserted indicating the absence of the 24V supply in this mode of operation.

Note 3: When using suggested external 2.2kΩ series resistors, limits of -36V to +36V apply.

Note 4: External resistor R_{REF} can be adjusted to set any desired current limit between 0.5mA and 6mA.

Note 5: INn-to-OPn propagation delay difference between two channels on the same IC.

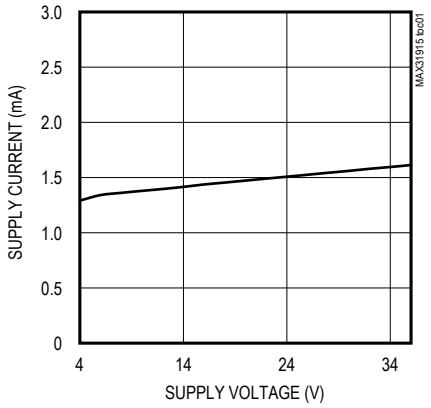
Note 6: Propagation delay from field input (INn) to CMOS output (OPn). Tested with a 6.5V pulse applied directly to the device INn pins. Propagation delay is measured between the 50% transitions of the rising and falling edges.

Note 7: The propagation delay limit is 1ms maximum when VTSEL = 0.

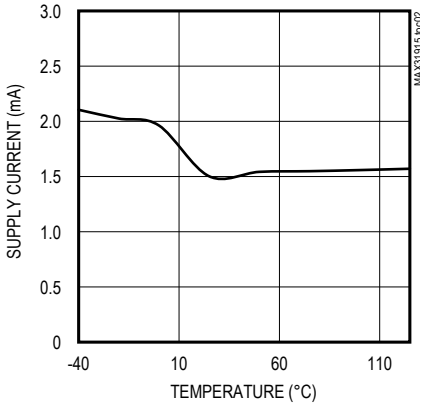
Typical Operating Characteristics

(T_A = +25°C, R_{REF} = 15kΩ, unless otherwise noted.)

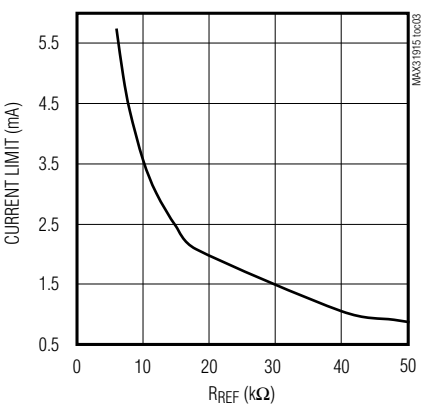
SUPPLY CURRENT vs. V_{CC24V} FIELD SUPPLY



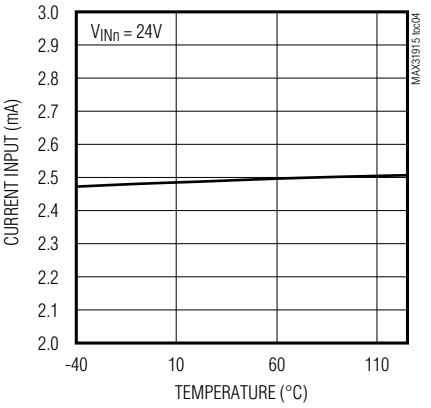
SUPPLY CURRENT vs. TEMPERATURE



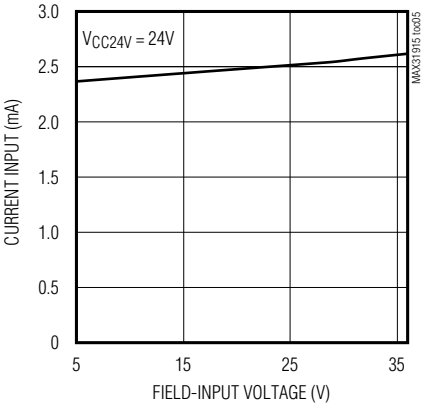
CURRENT LIMIT vs. R_{REF}



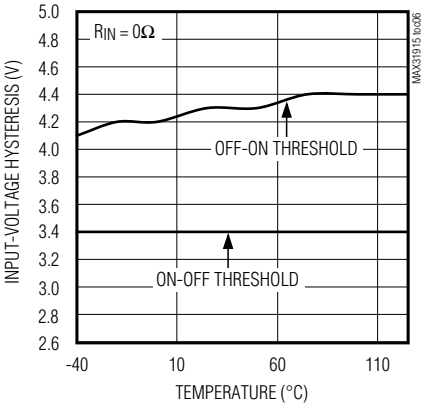
INPUT CURRENT LIMIT vs. TEMPERATURE



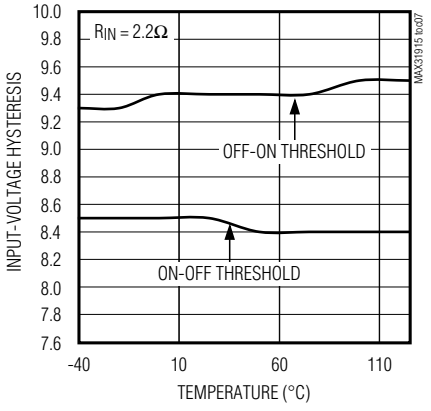
INPUT CURRENT LIMIT vs. FIELD-INPUT VOLTAGE



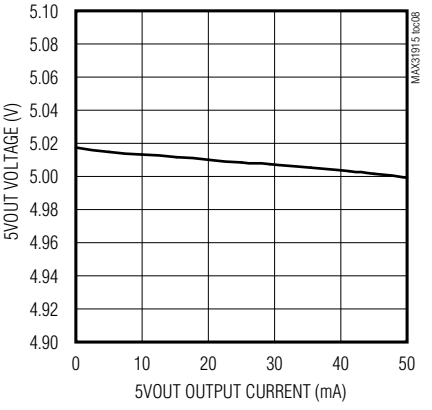
INPUT-VOLTAGE HYSTERESIS vs. TEMPERATURE



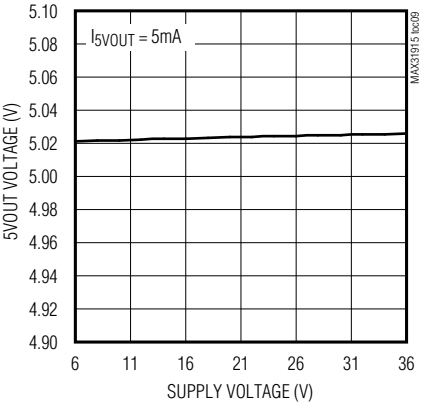
INPUT-VOLTAGE HYSTERESIS vs. TEMPERATURE



LDO LOAD REGULATION



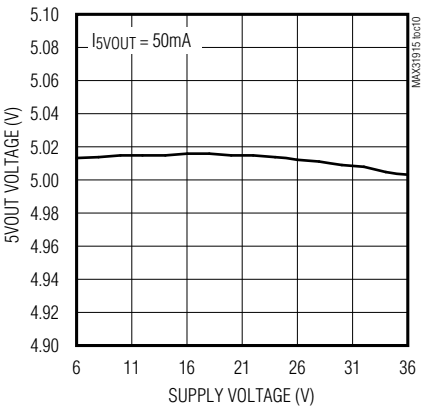
LDO LINE REGULATION



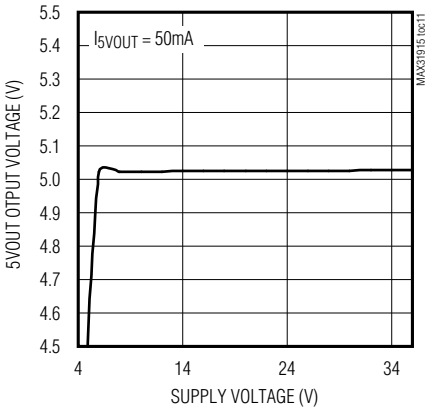
Typical Operating Characteristics (continued)

(T_A = +25°C, R_{REF} = 15kΩ, unless otherwise noted.)

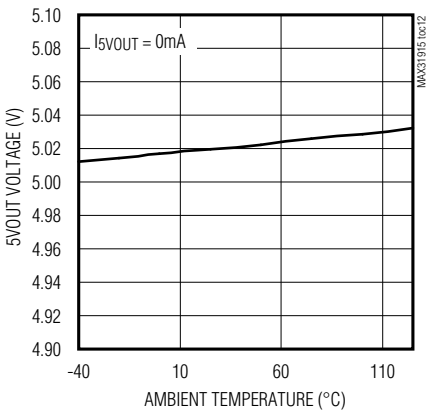
LDO LINE REGULATION



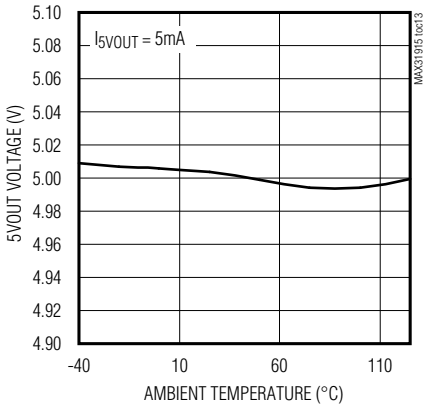
LDO OUTPUT vs. V_{CC24V} FIELD SUPPLY



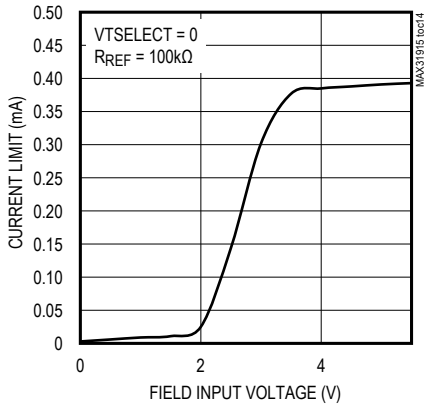
LDO OUTPUT VOLTAGE vs. TEMPERATURE



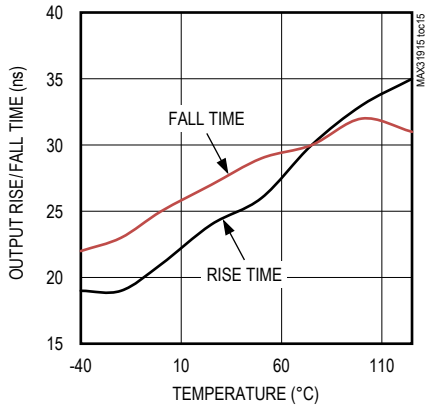
LDO OUTPUT VOLTAGE vs. TEMPERATURE



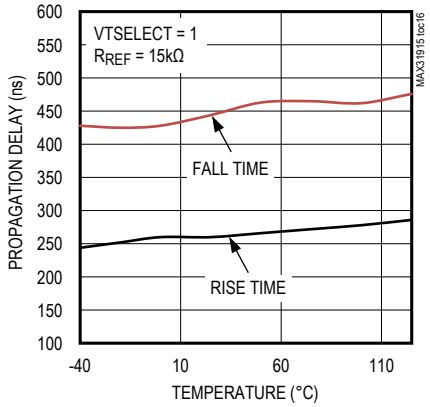
CURRENT LIMIT vs. FIELD INPUT VOLTAGE



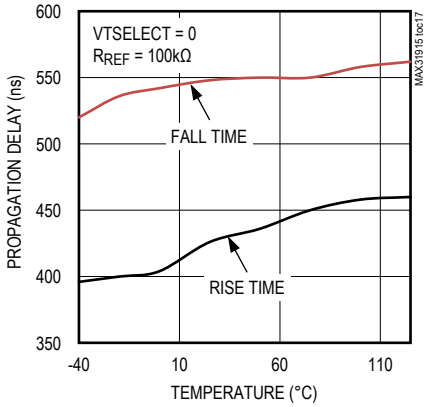
OUTPUT RISE/FALL TIME vs. TEMPERATURE



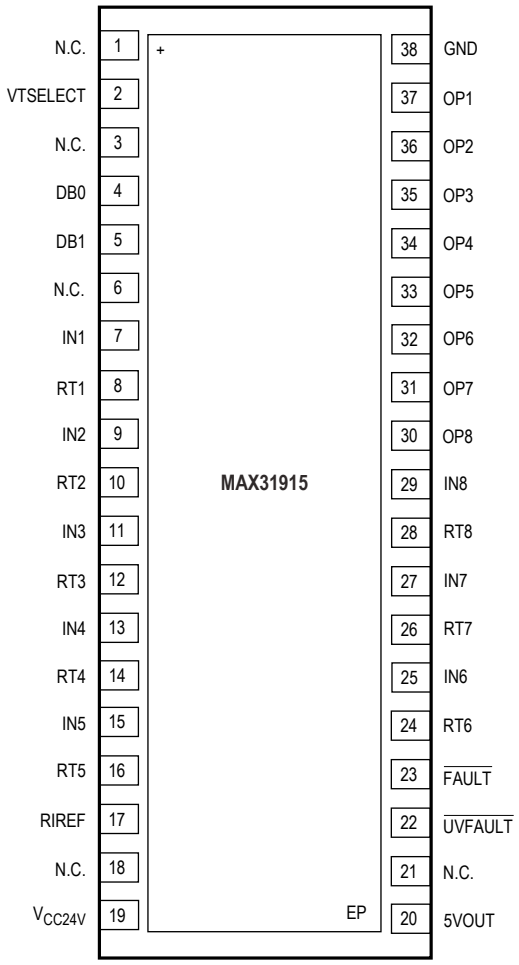
PROPAGATION DELAY vs. TEMPERATURE (FIELD INPUT VOLTAGE = 18V)



PROPAGATION DELAY vs. TEMPERATURE (FIELD INPUT VOLTAGE = 4.5V)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION		
1, 3, 6, 18, 21	N.C.	No Connection		
2	VTSELECT	Selects input trip points to be CMOS or IEC 61131-2 compliant. Logic 0 = CMOS compliant Logic 1 = IEC 61131-2 compliant		
4	DB0	Debounce (Filtering) Time Select Inputs		
5	DB1	**DB1**	**DB0**	**TIME CONSTANT OF FILTER APPLIED**
		0	0	0 (no filtering)
		0	1	0.025ms
		1	0	0.75ms
		1	1	3ms
7, 9, 11, 13, 15, 25, 27, 29	IN1–IN8	Field Input n. IN1 is pin 7 and IN8 is pin 29.		
8, 10, 12, 14, 16, 24, 26, 28	RT1–RT8	Energyless LED Driver Outputs. Connect to GND if LEDs are not required. RT1 is pin 8 and RT8 is pin 28.		
17	RIREF	Current-Limiter Reference Resistor		
19	VCC24V	Field-Supply Voltage		
20	5VOUT	5V Regulator Output		
22	$\overline{\text{UVFAULT}}$	Indicates Low Supply Voltage Alarm (Active Low)		
23	$\overline{\text{FAULT}}$	Indicates Hot Temperature Alarm. This is OR'ed with the $\overline{\text{UVFAULT}}$ indicator (active low).		
30–37	OP8–OP1	Logic Output n. OP1 is is 37. OP8 is pin 30.		
38	GND	Field Ground		
—	EP	Exposed Pad. Must connect EP to the PCB ground plane.		

Detailed Description

Principles of Operation

Input Current Clamp

The input pins (IN1–IN8) sense the state (on versus off) of field sensors by monitoring both the voltage and the current flowing through the sensor output. The current sinking through these input pins rises linearly with input voltage until the limit set by the current clamp is reached. Any voltage increase beyond this point does not increase the input current any further.

The value of the current clamp is adjustable through an external resistor connected between pin RIREF and ground. The voltage at the input pins (IN1–IN8) are compared against internally set references to determine if the sensor is on (logic 1) or off (logic 0). The trip points determining the on/off status of the sensor can be selected through pin VTSELECT as follows:

- VTSELECT = 1 selects trip points that satisfy the requirements of IEC 61131-2 type 1, type 2, and type 3 switches.
- VTSELECT = logic 0 selects trip points that are CMOS logic compatible and roughly centered approximately 2.5V.

Pins RT1–RT8 must be connected directly to GND to provide a return path for the input current if LEDs are not required for visual indication. If VTSELECT = logic 0, RT1–RT8 must be connected directly to GND. If visual indication is needed when VTSELECT = logic 0, then LEDs can be connected to pins OP1–OP8 through external current-limiting resistors.

Glitch Filter

A digital glitch filter provides debouncing and filtering of the noisy sensor signals. The time constant of this filter is selectable between 0 (i.e., no filtering), 25µs, 0.75ms, and 3ms. The selection is achieved through pins DB0 and DB1. The filtered outputs of the comparators are presented to the logic output pins, OP1–OP8.

To provide the digital glitch filter, the device checks that an input is stable for at least three clock cycles. The duration of a clock cycle is 1/3 of the selected debounce time. If the input is not stable for at least three clock cycles, the input change is not sent to the internal shift register.

Temperature Monitoring

The internal junction temperature of the IC is constantly monitored and an alarm is raised, by asserting the $\overline{FAULT}$ pin, if the temperature rises above T_{ALRM}.

Supply Voltage Monitoring

A primary supply voltage-monitor circuit constantly monitors the field-supply voltage. If this voltage falls below a threshold ($V_{OFFUVLO}$), an alarm is raised by asserting the $\overline{FAULT}$ and $\overline{UVFAULT}$ pins, indicating to the microcontroller that the part is experiencing a fault condition and the data is not to be trusted. Once the field-supply voltage has recovered and goes above V_{ONUVLO}, the $\overline{FAULT}$ and $\overline{UVFAULT}$ pins are released.

Powering the Device Through the 5VOUT Pin

The device can alternatively be powered using a 5V supply connected to the 5VOUT pin. In this case, a 24V supply is no longer needed and the VCC24V supply must be kept unconnected. (see Figure 1)

In this configuration, the device will always indicate a $\overline{UVFAULT}$ and the FAULT pin will always be active (pulled low). Faults due to the supply voltage monitoring and temperature monitoring will not be available.

This configuration has lower power consumption and heat dissipation since the on-chip 5V voltage regulator is disabled.

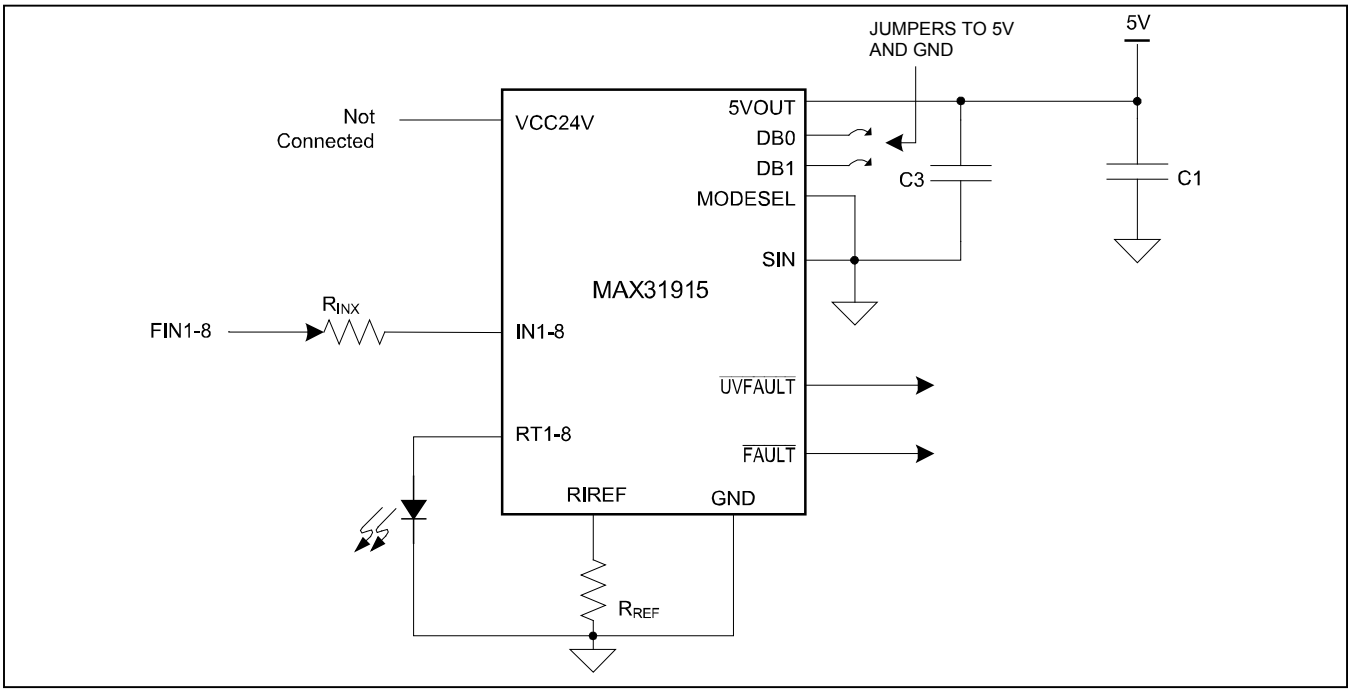
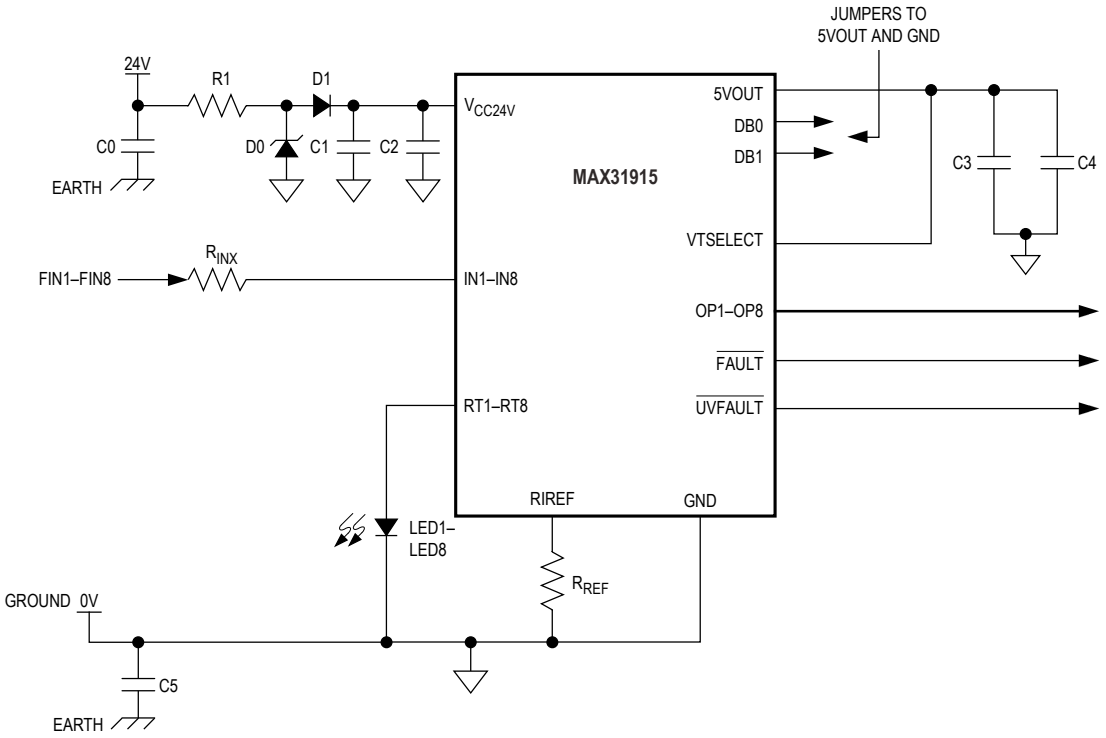


Figure 1: Basic Application Powered Through 5VOUT

Typical Application Circuit



NOTE: NOT ALL THE EXTERNAL COMPONENTS INDICATED ON THE DIAGRAM ARE REQUIRED FOR THE OPERATION OF THE IC.

Table 1. Recommended Components

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED/OPTIONAL
C0, C5	4.7nF, 2kV polypropylene capacitor	Recommended
C1	10µF, 60V ceramic capacitor	Required
C2	100nF, 60V ceramic capacitor	Required
C3	100nF, 10V ceramic capacitor	Recommended
C4	4.7µF, 10V low-ESR ceramic capacitor	Required
D0	36V fast zener diode (ZSMB36)	Recommended
D1	General-purpose rectifier (IN4007)	Optional: For reverse-polarity protection.
LED1–LED8	LEDs for visual input status indication	Optional
R1	150Ω, 1/3W MELF resistor	Required
R_{INX}	2.2kΩ, 1/4W MELF resistor	Required
R_{REF}	15kΩ, 1/8W resistor	Required

Note: *For higher EFT performance, a minimum 1nF, 1000V capacitor can be added from nodes FIN1–FIN8 to earth or ground. For alternative methods to improve EFT robustness, please check the Maxim website regularly for upcoming application notes currently being developed.*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	CARRIER
MAX31915AUI+	-40°C to +125°C	38 TSSOP-EP*	Bulk
MAX31915AUI+T	-40°C to +125°C	38 TSSOP-EP*	Tape and reel

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

- For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
38 TSSOP-EP	U38E+3	21-0714	90-0435

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/14	Initial release	—
1	4/15	Fixed IEC diagram and added 5VOUT description	11-12

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