19-3275; Rev 3; 10/07

USB On-the-Go Transceivers and Charge Pumps

General Description

The MAX3301E/MAX3302E fully integrated USB On-the-Go (OTG) transceivers and charge pumps allow mobile devices such as PDAs, cellular phones, and digital cameras to interface directly with USB peripherals and each other without the need of a host PC. Use the MAX3301E/MAX3302E with an embedded USB host to directly connect to peripherals such as printers or external hard drives.

The MAX3301E/MAX3302E integrate a USB OTG transceiver, a V_{BUS} charge pump, a linear regulator, and an I^2C-compatible, 2-wire serial interface. An internal level shifter allows the MAX3301E/MAX3302E to interface with +1.65V to +3.6V logic supply voltages. The MAX3301E/MAX3302E's OTG-compliant charge pump operates with +3V to +4.5V input supply voltages, and supplies an OTG-compatible output on V_{BUS} while sourcing more than 8mA of output current.

The MAX3301E/MAX3302E enable USB OTG communication from highly integrated digital devices that cannot supply or tolerate the +5V V_{BUS} levels that USB OTG requires. The device supports USB OTG session-request protocol (SRP) and host-negotiation protocol (HNP).

The MAX3301E/MAX3302E provide built-in ±15kV electrostatic-discharge (ESD) protection for the V_{BUS}, ID_IN, D+, and D- terminals. The MAX3301E/MAX3302E are available in 25-bump chip-scale (UCSP™), 25-bump WLP package, 28-pin TQFN, and 32-pin TQFN packages and operate over the extended -40°C to +85°C temperature range.

Selector Guide

PART	POWER-UP STATE†	I²C ADDRESSES FOR SPECIAL-FUNCTION REGISTER 2
MAX3301E	Shutdown (sdwn = 1, bit 0 of special-function register 2)	16h, 17h
MAX3302E	Operating ($\overline{sdwn}$ = 1, bit 0 of special-function register 2)	10h, 11h, and 16h, 17h

†The MAX3301E powers up in its lowest power state and the MAX3302E powers up in the operational, VP/VM USB mode.

Applications

Mobile Phones
PDAs
Digital Cameras
MP3 Players

Features

- **USB 2.0-Compliant Full-/Low-Speed OTG Transceivers**
- **Ideal for USB On-the-Go, Embedded Host, or Peripheral Devices**
- **±15kV ESD Protection on ID_IN, V_{BUS}, D+, and D- Terminals**
- **Charge Pump for V_{BUS} Signaling and Operation Down to 3V**
- **Internal V_{BUS} and ID Comparators**
- **Internal Switchable Pullup and Pulldown Resistors for Host/Peripheral Functionality**
- **I^2C Bus Interface with Command and Status Registers**
- **Linear Regulator Powers Internal Circuitry and D+/D- Pullup Resistors**
- **Support SRP and HNP**

Ordering Information

PART	PACKAGE SIZE (mm)	PIN-PACKAGE	PKG CODE
MAX3301EEBA-T	2.5 x 2.5	25 UCSP‡	B25-1
MAX3301EETJ	5 x 5	32 TQFN-EP**	T3255-4
MAX3302EEBA-T*	2.5 x 2.5	25 UCSP‡	B25-1
MAX3302EETI	4 x 4	28 TQFN-EP**	T2844-1
MAX3302EEWA+T	2.54 x 2.54	25 WLP	W252A2-1

Note: *All devices specified over the -40°C to +85°C operating range.*
‡UCSP bumps are in a 5 x 5 array. The UCSP package size is 2.5mm x 2.5mm x 0.62mm. Requires solder temperature profile described in the Absolute Maximum Ratings section. UCSP reliability is integrally linked to the user's assembly methods, circuit board material and environment. See the UCSP Applications Information section of this data sheet for more information.
**Future product—contact factory for availability.*
***EP = Exposed paddle.*
T = Tape and reel.
+Denotes a lead-free package.

Pin Configurations appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

All voltages are referenced to GND.
V_{CC}, V_L .....-0.3V to +6V
TRM (regulator off or supplied by V_{BUS}) ..-0.3V to (V_{BUS} + 0.3V)
TRM (regulator supplied by V_{CC}).....-0.3V to (V_{CC} + 0.3V)
D+, D- (transmitter tri-stated) .....-0.3V to +6V
D+, D- (transmitter functional).....-0.3V to (V_{CC} + 0.3V)
V_{BUS} .....-0.3V to +6V
ID_IN, SCL, SDA.....-0.3V to +6V
$\overline{INT}$, SPD, $\overline{RESET}$, ADD, $\overline{OE}/\overline{INT}$, RCV, VP, VM, SUS, DAT_VP, SE0_VM .....-0.3V to (V_L + 0.3V)
C+.....-0.3V to (V_{BUS} + 0.3V)
C-.....-0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, V_{BUS} to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
25-Bump WLP (derate 12.2mW/°C above +70°C).....976mW
25-Bump UCSP (derate 12.2mW/°C above +70°C) 976mW
32-Pin TQFN (5mm x 5mm x 0.8mm) (derate 21.3mW/°C above +70°C).....1702mW
28-Pin TQFN (4mm x 4mm x 0.8mm) (derate 20.8mW/°C above +70°C).....1666mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Reflow Temperature (Note 1)
Infrared (15s) .....+200°C
Vapor Phase (20s) .....+215°C

Note 1: The UCSP package is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +4.5V, V_L = +1.65V to +3.6V, C_{FLYING} = 100nF, C_{VBUS} = 1µF, ESR_{CVBUS} = 0.1Ω (max), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.7V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0		4.5	V
TRM Output Voltage	V_{TRM}		3.0		3.6	V
Logic Supply Voltage	V_L		1.65		3.60	V
V_L Supply Current	I_{VL}	I²C interface in steady state			5	µA
V_{CC} Operating Supply Current	I_{CC}	USB normal mode, C_L = 50pF, device switching at full speed			10	mA
V_{CC} Supply Current During Full-Speed Idle		V_{VBUS_DRV} = 1, I_{VBUS} = 0		1.4	2	mA
		V_{VBUS_DRV} = 0, D+ = high, D- = low		0.5	0.8	
V_{CC} Shutdown Supply Current	$I_{CC(SHDN)}$			3.5	10	µA
V_{CC} Interrupt Shutdown Supply Current	$I_{CC(ISHDN)}$	ID_IN unconnected or high		20	30	µA
V_{CC} Suspend Supply Current		USB suspend mode, ID_IN unconnected or high		170	500	µA
LOGIC I/O						
RCV, DAT_VP, SE0_VM, $\overline{INT}$, $\overline{OE}/\overline{INT}$, VP, VM Output High Voltage	V_{OH}	I_{OUT} = 1mA (sourcing)	V_L - 0.4			V
RCV, DAT_VP, SE0_VM, $\overline{INT}$, $\overline{OE}/\overline{INT}$, VP, VM Output Low Voltage	V_{OL}	I_{OUT} = 1mA (sinking)			0.4	V
$\overline{OE}/\overline{INT}$, SPD, SUS, $\overline{RESET}$, DAT_VP, SE0_VM Input High Voltage	V_{IH}		2/3 x V_L			V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +4.5V, V_L = +1.65V to +3.6V, C_{FLYING} = 100nF, C_{VBUS} = 1µF, ESR_{CVBUS} = 0.1Ω (max), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.7V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{OE}$/$\overline{INT}$, SPD, SUS, $\overline{RESET}$ DAT_VP, SE0_VM Input Low Voltage	V_{IL}					0.4	V
ADD Input High Voltage	V_{IHA}			2/3 x V_L			V
ADD Input Low Voltage	V_{ILA}					1/3 x V_L	V
Input Leakage Current					±1		µA
TRANSCEIVER SPECIFICATIONS							
Differential Receiver Input Sensitivity		$\lvert V_{D+} - V_{D-} \rvert$		0.2			V
Differential Receiver Common-Mode Voltage				0.8		2.5	V
Single-Ended Receiver Input Low Voltage	V_{ILD}	D+, D-				0.8	V
Single-Ended Receiver Input High Voltage	V_{IHD}	D+, D-		2.0			V
Single-Ended Receiver Hysteresis					0.2		V
Single-Ended Output Low Voltage	V_{OLD}	D+, D-, R_L = 1.5kΩ from D+ or D- to 3.6V				0.3	V
Single-Ended Output High Voltage	V_{OHD}	D+, D-, R_L = 15kΩ from D+ or D- to GND		2.8		3.6	V
Off-State Leakage Current		D+, D-				±1	µA
Driver Output Impedance		D+, D-, not including R_{EXT}	Low steady-state drive	2		13	Ω
			High steady-state drive	2		13	
ESD PROTECTION (V_{BUS}, ID_IN, D+, D-)							
Human Body Model					±15		kV
IEC 61000-4-2 Air-Gap Discharge					±10		kV
IEC 61000-4-2 Contact Discharge					±6		kV
THERMAL SHUTDOWN							
Thermal Shutdown Low-to-High					+160		°C
Thermal Shutdown High-to-Low					+150		°C
CHARGE-PUMP SPECIFICATIONS (vbus_drv = 1)							
V_{BUS} Output Voltage	V_{BUS}	3V < V_{CC} < 4.5V, C_{VBUS} = 10µF, I_{VBUS} = 8mA		4.80		5.25	V
V_{BUS} Output Current	I_{VBUS}			8			mA
V_{BUS} Output Ripple		I_{VBUS} = 8mA, C_{VBUS} = 10µF			100		mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +4.5V, V_L = +1.65V to +3.6V, C_{FLYING} = 100nF, C_{VBUS} = 1µF, ESR_{CVBUS} = 0.1Ω (max), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.7V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	f_{SW}			390		kHz
V_{BUS} Leakage Voltage		V_{VBUS_DRV} = 0			0.2	V
V_{BUS} Rise Time		C_{VBUS} = 10µF, I_{VBUS} = 8mA, measured from 0 to +4.4V			100	ms
V_{BUS} Pulldown Resistance		$V_{VBUS\_DISCHRG}$ = 1, V_{VBUS_DRV} = 0, V_{VBUS_CHRG} = 0	3.8	5	6.5	kΩ
V_{BUS} Pullup Resistance		V_{VBUS_CHRG} = 1, V_{VBUS_DRV} = 0, $V_{VBUS\_DISCHRG}$ = 0	650	930	1250	Ω
V_{BUS} Input Impedance	Z_{INVBUS}	$V_{VBUS\_DISCHRG}$ = 0, V_{VBUS_DRV} = 0, V_{VBUS_CHRG} = 0	40	70	100	kΩ
COMPARATOR SPECIFICATIONS						
V_{BUS} Valid Comparator Threshold	$V_{TH-VBUS}$		4.4	4.6	4.8	V
V_{BUS} Valid Comparator Hysteresis	$V_{HYS-VBUS}$			50		mV
Session-Valid Comparator Threshold	$V_{TH-SESS\_VLD}$		0.8	1.4	2.0	V
Session-End Comparator Threshold	$V_{TH-SESS\_END}$		0.2	0.5	0.8	V
dp_hi Comparator Threshold			0.8	1.3	2.0	V
dm_hi Comparator Threshold			0.8	1.3	2.0	V
cr_int Pulse Width				750		ns
cr_int Comparator Threshold			0.4	0.5	0.6	V
ID_IN SPECIFICATIONS						
ID_IN Input Voltage for Car Kit			0.2 x V_{CC}		0.8 x V_{CC}	V
ID_IN Input Voltage for A Device					0.1 x V_{CC}	V
ID_IN Input Voltage for B Device			0.9 x V_{CC}			V
ID_IN Input Impedance	Z_{ID_IN}		70	100	130	kΩ
ID_IN Input Leakage Current		ID_IN = V_{CC}	-1		+1	µA
ID_IN Pulldown Resistance		id_pulldown = 1		150	300	Ω
TERMINATING RESISTOR SPECIFICATIONS (D+, D-)						
D+ Pulldown Resistor		dp_pulldown = 1	14.25	15	15.75	kΩ
D- Pulldown Resistor		dm_pulldown = 1	14.25	15	15.75	kΩ
D+ Pullup Resistor		dp_pullup = 1	1.425	1.5	1.575	kΩ
D- Pullup Resistor		dm_pullup = 1	1.425	1.5	1.575	kΩ

TIMING CHARACTERISTICS

(V_{CC} = +3V to +4.5V, V_L = +1.65V to +3.6V, C_{FLYING} = 100nF, C_{VBUS} = 1µF, ESR_{CVBUS} = 0.1Ω (max), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.7V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER CHARACTERISTICS (FULL-SPEED MODE)						
D+, D- Rise Time	t_R	Figures 2 and 5	4		20	ns
D+, D- Fall Time	t_F	Figures 2 and 5	4		20	ns
Rise-/Fall-Time Matching		Figures 2 and 5 (Note 3)	90		110	%
Output-Signal Crossover Voltage	V_{CRS_F}	Figures 2, 6, and 7 (Note 3)	1.3		2.0	V
TRANSMITTER CHARACTERISTICS (LOW-SPEED MODE)						
D+, D- Rise Time	t_R	Figures 2 and 5	75		300	ns
D+, D- Fall Time	t_F	Figures 2 and 5	75		300	ns
Rise-/Fall-Time Matching		Figures 2 and 5	80		125	%
Output-Signal Crossover Voltage	V_{CRS_L}	Figures 2, 6, and 7	1.3		2.0	V
TRANSMITTER TIMING (FULL-SPEED MODE)						
Driver Propagation Delay (DAT_VP, SE0_VM to D+, D-)	t_{PLH}	Low-to-high, Figures 2 and 6			25	ns
	t_{PHL}	High-to-low, Figures 2 and 6			25	
Driver Disable Delay	t_{PDZ}	Figures 1 and 8			25	ns
Driver Enable Delay	t_{PZD}	Figures 2 and 8			25	ns
TRANSMITTER TIMING (LOW-SPEED MODE) (Low-speed delay timing is dominated by the slow rise and fall times.)						
SPEED-INDEPENDENT TIMING CHARACTERISTICS						
Receiver Disable Delay	t_{PVZ}	Figure 4			30	ns
Receiver Enable Delay	t_{PZV}	Figure 4			30	ns
D+ Pullup Assertion Time		During HNP			3	µs
RCV Rise Time	t_R	Figures 3 and 5, C_L = 15pF		4		ns
RCV Fall Time	t_F	Figures 3 and 5, C_L = 15pF		4		ns
Differential-Receiver Propagation Delay	t_{PHL}, t_{PLH}	Figures 3 and 10, |D+ - D-| to DAT_VP			30	ns
		Figures 3 and 9, |D+ - D-| to RCV			30	
Single-Ended-Receiver Propagation Delay	t_{PHL}, t_{PLH}	Figures 3 and 9, D+, D- to DAT_VP, SE0_VM			30	ns
Interrupt Propagation Delay					100	µs
V_{BUS_CHRG} Propagation Delay		Dominated by the V_{BUS} rise time		0.2		µs
Time to Exit Shutdown					1	µs
Shutdown Delay					10	µs

I²C-/SMBus™-COMPATIBLE TIMING SPECIFICATIONS

(V_{CC} = +3V to +4.5V, V_L = +1.65V to +3.6V, C_{FLYING} = 100nF, C_{VBUS} = 1µF, ESR_{CVBUS} = 0.1Ω (max), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.7V, V_L = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus-Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Start-Condition Hold Time	t_{HD_STA}		0.6			µs
Stop-Condition Setup Time	t_{SU_STO}		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	t_{SU_DAT}		100			ns
Data Hold Time	t_{HD_DAT}	(Note 4)			0.9	µs
Rise Time of SDA and SCL	t_R	(Note 5)	20 + 0.1 x C_B		300	ns
Fall Time of SDA and SCL	t_F	Measured from 0.3 x V_L to 0.7 x V_L (Note 5)			300	ns
Capacitive Load for each Bus Line	C_B				400	pF
SDA AND SCL I/O STAGE CHARACTERISTICS						
Input-Voltage Low	V_{IL}				0.3 x V_L	V
Input-Voltage High	V_{IH}		0.7 x V_L			V
SDA Output-Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Pulse Width of Suppressed Spike	t_{SP}	(Note 6)		50		ns

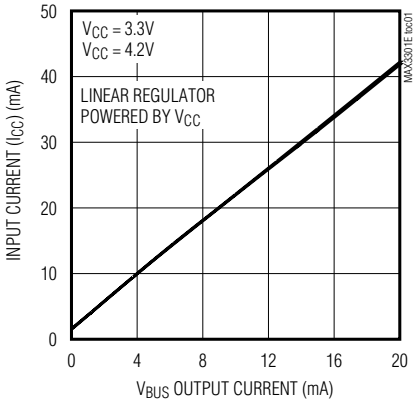
Note 2: Parameters are 100% production tested at +25°C. Limits over temperature are guaranteed by design.
Note 3: Guaranteed by bench characterization. Limits are not production tested.
Note 4: A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.
Note 5: C_B is the total capacitance of one bus line in pF, tested with C_B = 400pF.
Note 6: Input filters on SDA, SCL, and ADD suppress noise spikes of less than 50ns.

SMBus is a trademark of Intel Corporation.

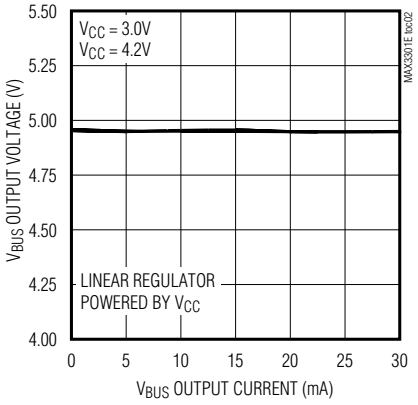
Typical Operating Characteristics

(Typical operating circuit, V_{CC} = +3.7V, V_L = +2.5V, C_{FLYING} = 100nF, T_A = +25°C, unless otherwise noted.)

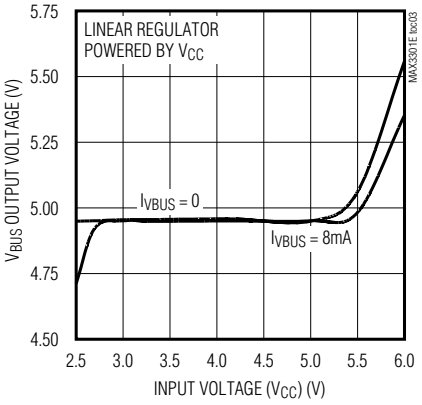
INPUT CURRENT (I_{CC}) vs. V_{BUS} OUTPUT CURRENT



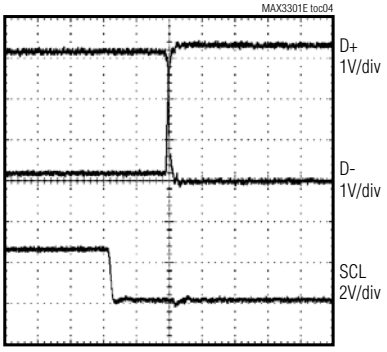
V_{BUS} OUTPUT VOLTAGE vs. V_{BUS} OUTPUT CURRENT



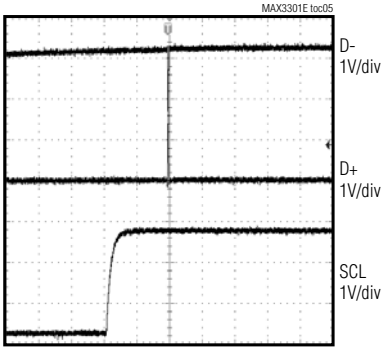
V_{BUS} OUTPUT VOLTAGE vs. INPUT VOLTAGE (V_{CC})



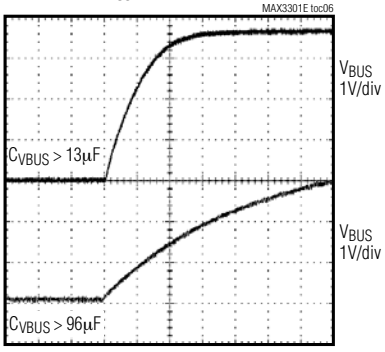
TIME TO ENTER SHUTDOWN



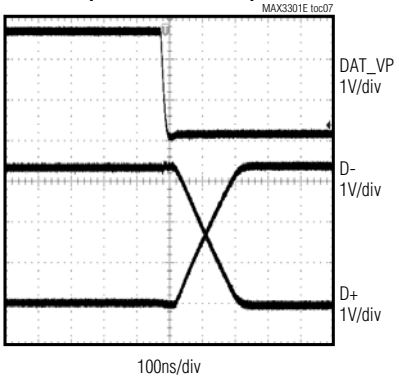
TIME TO EXIT SHUTDOWN



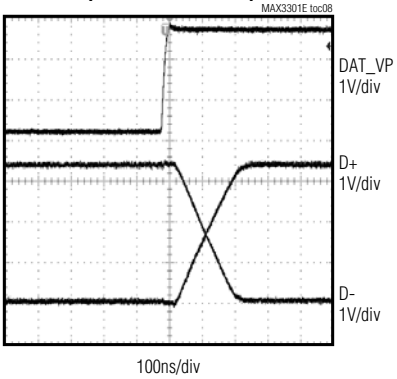
V_{BUS} DURING SRP



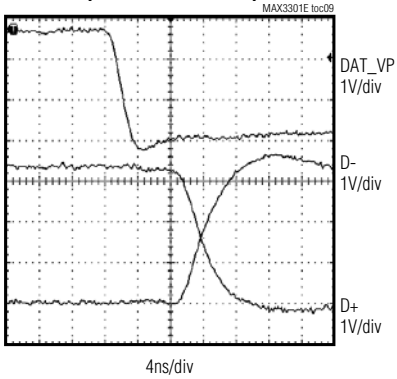
DRIVER PROPAGATION DELAY HIGH-TO-LOW (LOW-SPEED MODE)



DRIVER PROPAGATION DELAY LOW-TO-HIGH (LOW-SPEED MODE)



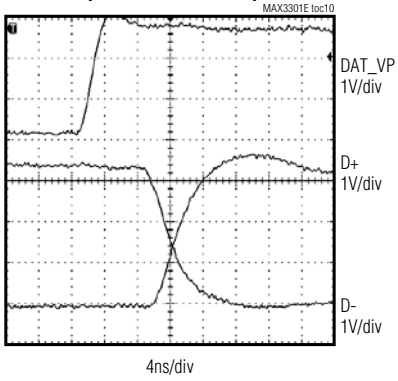
DRIVER PROPAGATION DELAY HIGH-TO-LOW (FULL-SPEED MODE)



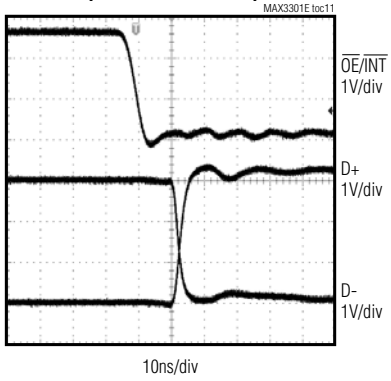
Typical Operating Characteristics (continued)

(Typical operating circuit, V_{CC} = +3.7V, V_L = +2.5V, C_{FLYING} = 100nF, T_A = +25°C, unless otherwise noted.)

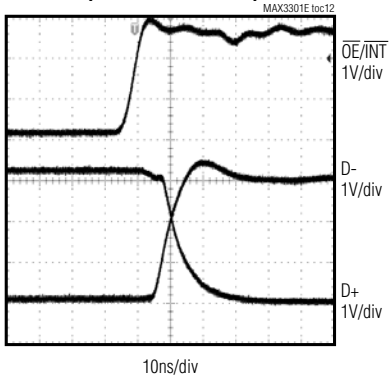
DRIVER PROPAGATION DELAY LOW-TO-HIGH (FULL-SPEED MODE)



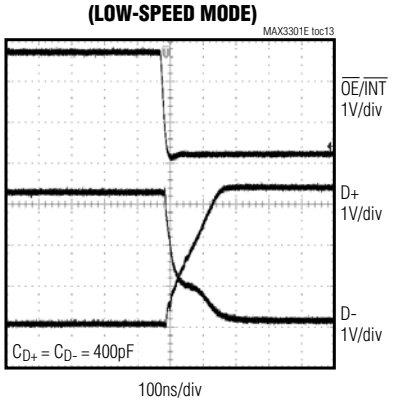
DRIVER ENABLE DELAY (FULL-SPEED MODE)



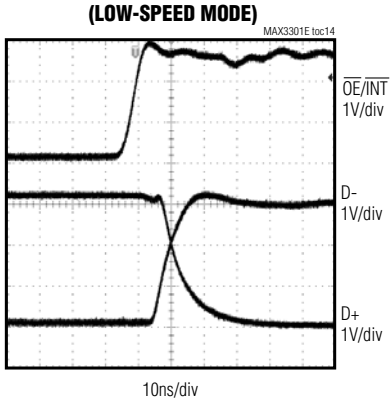
DRIVER DISABLE DELAY (FULL-SPEED MODE)



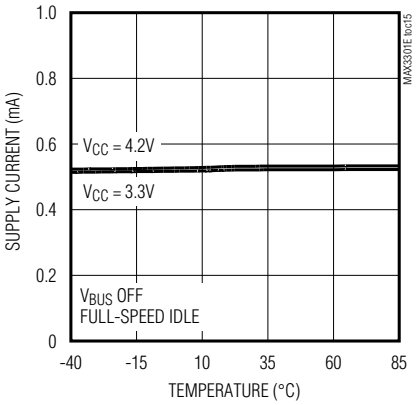
DRIVER ENABLE DELAY (LOW-SPEED MODE)



DRIVER DISABLE DELAY (LOW-SPEED MODE)



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX3302E 28-PIN TQFN	MAX3301E 32-PIN TQFN	UCSP/ WLP		
1	2	D2	DAT_VP	System-Side Data Input/Output. DAT_VP is an input if $\overline{OE}/\overline{INT}$ is logic 0. DAT_VP is an output if $\overline{OE}/\overline{INT}$ is logic 1. Program the function of DAT_VP with the dat_se0 bit (bit 2 of control register 1, see Table 7).
2, 25	3, 29	D1, E3	V_{CC}	Input Power Supply. Connect a +3V to +4.5V supply to V_{CC} and bypass to GND with a 1µF capacitor. The supply range enables direct powering from one Li+ battery.
3, 9, 23	1, 4, 9, 12, 17, 25, 28	—	N.C.	No Connection. Not internally connected.
4	5	C1	C-	Charge-Pump Flying-Capacitor Negative Terminal
5	6	C2	SE0_VM	System-Side Data Input/Output. SE0_VM is an input if $\overline{OE}/\overline{INT}$ is logic 0. SE0_VM is an output if $\overline{OE}/\overline{INT}$ is logic 1. Program the function of SE0_VM with the dat_se0 bit (bit 2 of control register 1, see Table 7).
6, 18	7, 21	B1, C5	GND	Ground
7	8	A1	SDA	I²C-Compatible Serial Data Interface. Open-drain data input/output.
8	10	B2	SCL	I²C-Compatible Serial Clock Input
10	11	A2	$\overline{OE}/\overline{INT}$	Output Enable. $\overline{OE}/\overline{INT}$ controls the input or output status of DAT_VP/SE0_VM and D+/D-. When $\overline{OE}/\overline{INT}$ is logic 0, the device is in transmit mode. When $\overline{OE}/\overline{INT}$ is logic 1, the device is in receive mode. When in suspend mode, $\overline{OE}/\overline{INT}$ can be programmed to function as an interrupt output that detects the same interrupts as $\overline{INT}$. The oe_int_en bit (bit 5 of control register 1, see Table 7) enables and disables the interrupt circuitry of $\overline{OE}/\overline{INT}$. The irq_mode bit (bit 1 of special-function register 2, see Table 15) programs the output configuration of $\overline{INT}$ and $\overline{OE}/\overline{INT}$ as open-drain or push-pull.
11	13	A3	RCV	D+ and D- Differential Receiver Output. In receive mode (see Table 4), when D+ is high and D- is low, RCV is high. In receive mode, when D+ is low and D- is high, RCV is low. RCV is low in suspend mode.
12	14	B3	SPD	Speed-Selector Input. Connect SPD to GND to select the low-speed data rate (1.5Mbps). Connect SPD to V_L to select the full-speed data rate (12Mbps). Disable the SPD input by writing a 1 to spd_susp_ctl (bit 1 in special-function register 1, see Table 14). The speed bit (bit 0 of control register 1, see Table 7) determines the maximum data rate of the MAX3301E/MAX3302E when the SPD input is disabled.
13	15	A4	V_L	System-Side Logic-Supply Input. Connect to the system's logic-level power supply, +1.65V to +3.6V. This sets the maximum output levels of the logic outputs and the input thresholds of the logic inputs. Bypass to GND with a 0.1µF capacitor.
14	16	A5	SUS	Active-High Suspend Input. Drive SUS low for normal USB operation. Drive SUS high to enable suspend mode. RCV asserts low in suspend mode. Disable the SUS input by writing a 1 to spd_susp_ctl (bit 1 in special-function register 1, see Table 14). The suspend bit (bit 1 of control register 1, see Table 7) determines the operating mode of the MAX3301E/MAX3302E when the SUS input is disabled.

USB On-the-Go Transceivers and Charge Pumps

Pin Description (continued)

PIN			NAME	FUNCTION
MAX3302E 28-PIN TQFN	MAX3301E 32-PIN TQFN	UCSP/ WLP		
15	18	B4	$\overline{INT}$	Active-Low Interrupt Source. Program the $\overline{INT}$ output as push-pull or open-drain with the irq_mode bit (bit 1 of special-function register 2, see Tables 15 and 16).
16	19	B5	$\overline{RESET}$	Active-Low Reset Input. Drive $\overline{RESET}$ low to asynchronously reset the MAX3301E/MAX3302E.
17	20	C3	ADD	I²C-Interface Address Selection Input. (See Table 5.)
19	22	C4	ID_IN	ID Input. ID_IN is internally pulled up to V_{CC}. The state of ID_IN determines ID bits 3 and 5 of the interrupt source register (see Table 10).
20	23	D5	D-	USB Differential Data Input/Output. Connect D- to the D- terminal of the USB connector through a 27.4Ω ±1% series resistor.
21	24	E5	D+	USB Differential Data Input/Output. Connect D+ to the D+ terminal of the USB connector through a 27.4Ω ±1% series resistor.
22	26	D4	VM	Single-Ended Receiver Output. VM functions as a receiver output in all operating modes. VM duplicates D-.
24	27	E4	TRM	USB Transceiver Regulated Output Voltage. TRM provides a regulated 3.3V output. Bypass TRM to GND with a 1µF ceramic capacitor installed as close to the device as possible. TRM normally derives power from V_{CC}. TRM provides power to internal circuitry and provides the pullup voltage for the internal USB pullup resistor. Do not use TRM to power external circuitry. The reg_sel bit (bit 3 of special-function register 2, see Table 15 and Table 16) controls the TRM power source with software.
26	30	D3	VP	Single-Ended Receiver Output. VP functions as a receiver output in all operating modes. VP duplicates D+.
27	31	E2	V_{BUS}	USB Bus Power. Use V_{BUS} as an output to power the USB bus, or as an input to power the internal linear regulator. Bits 5 to 7 of control register 2 (see Table 8) control the charging and discharging functions of V_{BUS}.
28	32	E1	C+	Charge-Pump Flying-Capacitor Positive Terminal
EP	EP	—	EP	Exposed Paddle. Connect EP to GND or leave unconnected.

Test Circuits and Timing Diagrams

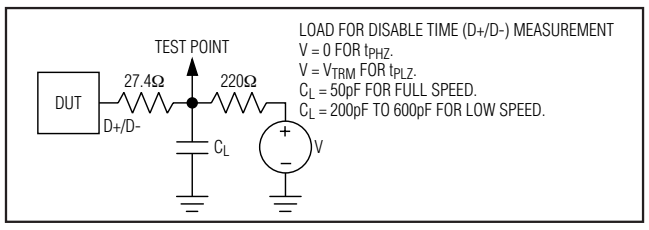


Figure 1. Load for Disable Time Measurement

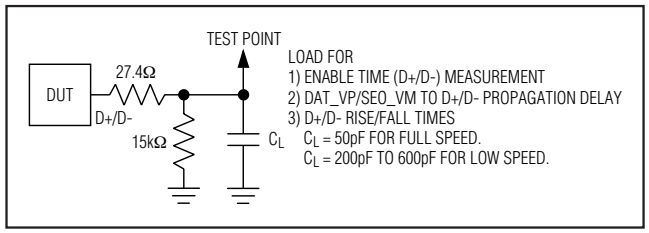


Figure 2. Load for Enable Time, Transmitter Propagation Delay, and Transmitter Rise/Fall Times

Test Circuits and Timing Diagrams (continued)

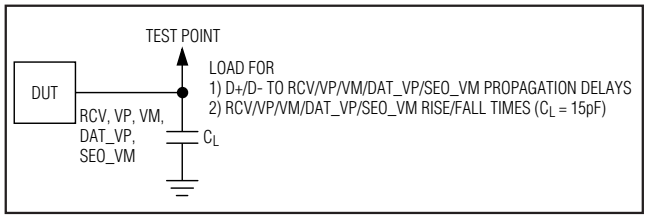


Figure 3. Load for Receiver Propagation Delay and Receiver Rise/Fall Times

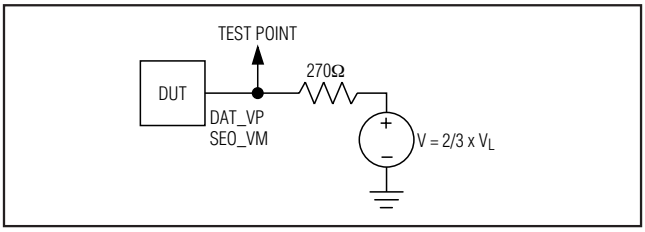


Figure 4. Load for DAT_VP, SE0_VM Enable/Disable Time Measurements

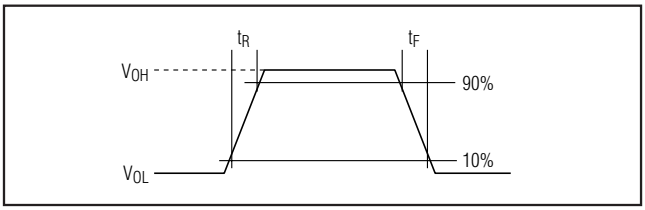


Figure 5. Rise and Fall Times

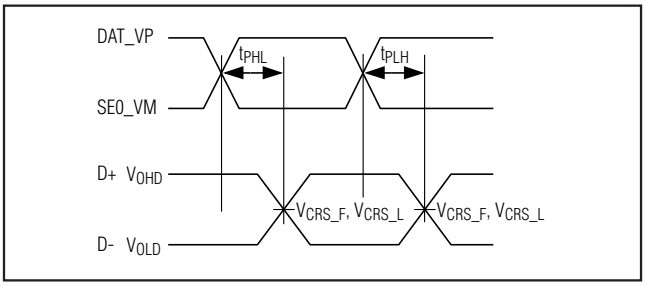


Figure 6. Timing of DAT_VP, SE0_VM to D+, D- in VP_VM Mode (dat_se0 = 0)

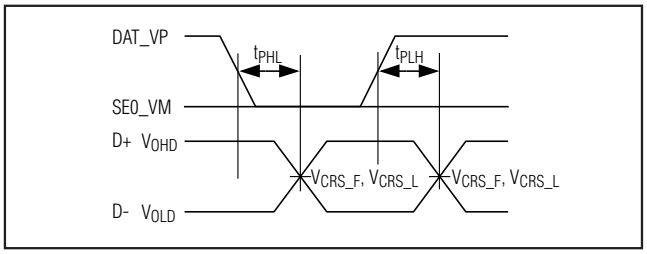


Figure 7. Timing of DAT_VP, SE0_VM to D+/D- in DAT_SE0 Mode (dat_se0 = 1)

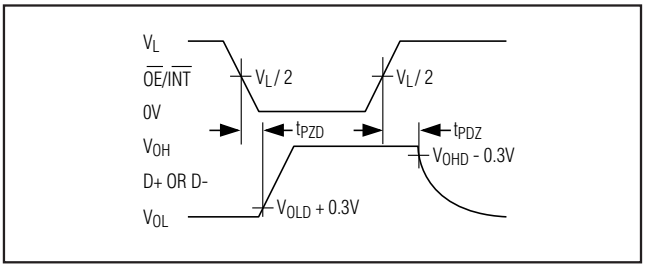


Figure 8. Enable and Disable Timing

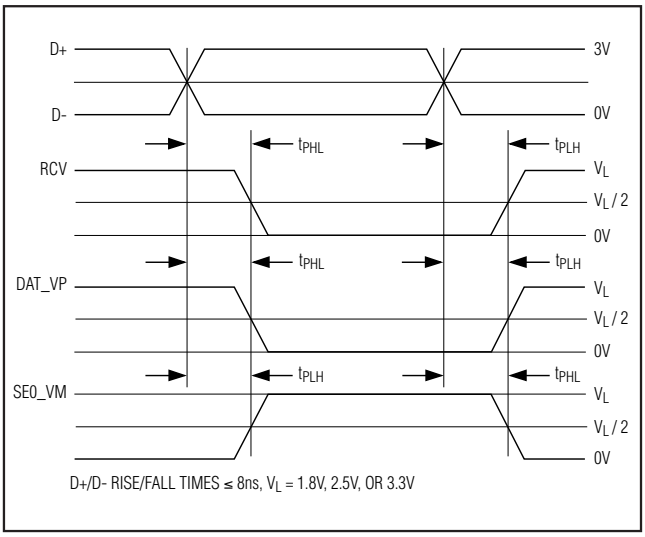


Figure 9. D+/D- to RCV, DAT_VP, SE0_VM Propagation Delays (VP_VM Mode)

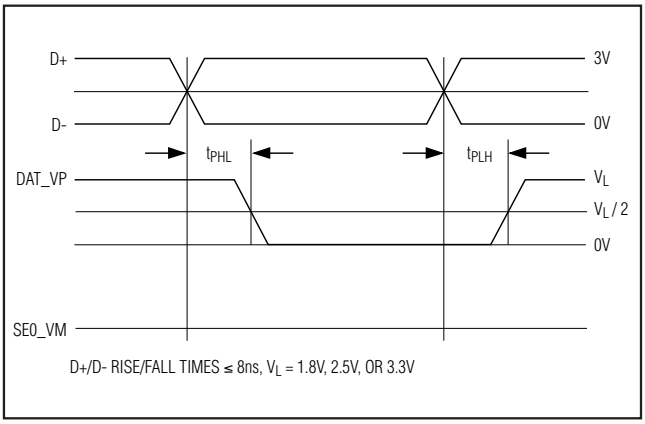


Figure 10. D+/D- to DAT_VP, SE0_VM Propagation Delays (DAT_SE0 Mode)

Block Diagram

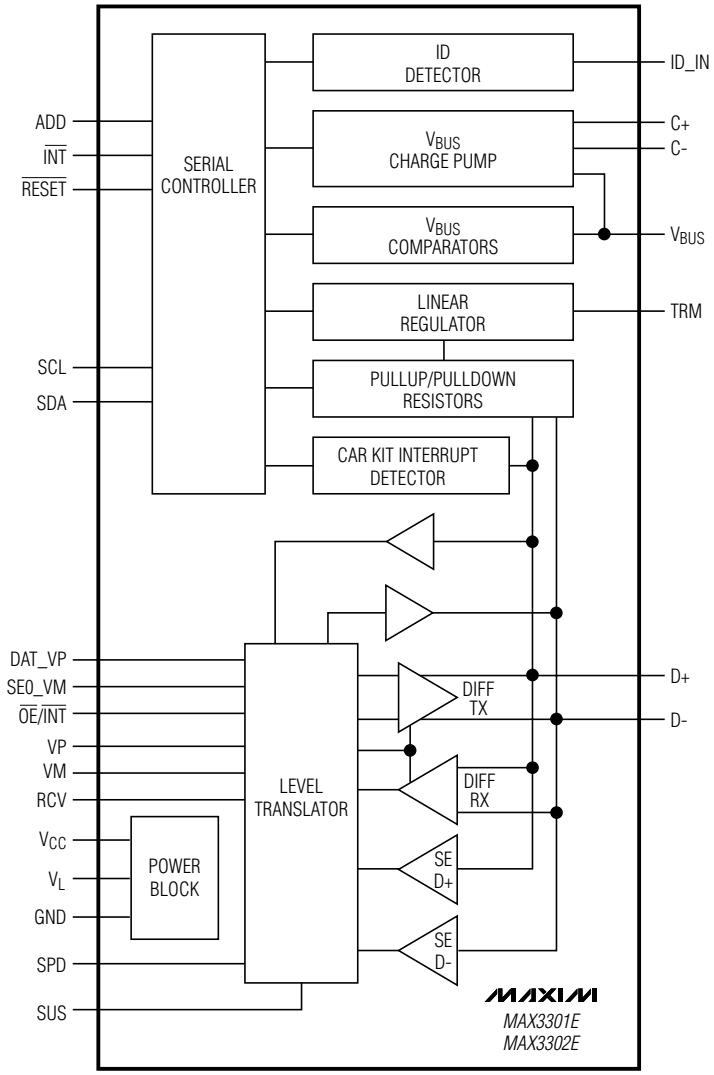


Figure 11. Block Diagram

Detailed Description

The USB OTG specification defines a dual-role USB device that acts either as an A device or as a B device. The A device supplies power on V_{BUS} and initially serves as the USB host. The B device serves as the initial peripheral and requires circuitry to monitor and pulse V_{BUS}. These initial roles can be reversed using HNP.

The MAX3301E/MAX3302E combine a low- and full-speed USB transceiver with additional circuitry required by a dual-role device. The MAX3301E/MAX3302E employ flexible switching circuitry to enable the device to act as a dedicated host or peripheral USB transceiver. For example, the charge pump can be turned off and the internal regulator can be powered from V_{BUS} for bus-powered peripheral applications.

The *Selector Guide* shows the differences between the MAX3301E and MAX3302E. The MAX3301E powers up in its lowest power state and must be turned on by setting the sdwn bit to 0. The MAX3302E powers up in the operational, VP/VM USB mode. This allows a microprocessor (µP) to use the USB port for power-on boot-up, without having to access I²C. To put the MAX3302E into low-power shutdown, set the sdwn bit to 0. In the MAX3302E, special-function register 2 can be addressed at I²C register location 10h, 11h (as well as locations 16h, 17h) to support USB OTG serial-interface engine (SIE) implementations that are limited to I²C register addresses between 0h and 15h.

Transceiver

The MAX3301E/MAX3302E transceiver complies with the USB version 2.0 specification, and operates at full-speed (12Mbps) and low-speed (1.5Mbps) data rates. Set the data rate with the SPD input. Set the direction of data transfer with the $\overline{OE}$/$\overline{INT}$ input. Alternatively, control transceiver operation with control register 1 (Table 7) and special-function registers 1 and 2 (see Tables 14, 15, and 16).

Level Shifters

Internal level shifters allow the system-side interface to run at logic-supply voltages as low as +1.65V. Interface logic signals are referenced to the voltage applied to the logic-supply voltage, V_L.

Charge Pump

The MAX3301E/MAX3302E's OTG-compliant charge pump operates with +3V to +4.5V input supply voltages (V_{CC}) and supplies a +4.8V to +5.25V OTG-compatible output on V_{BUS} while sourcing the 8mA or greater output current that an A device is required to supply. Connect a 0.1µF flying capacitor between C+ and C-. Bypass V_{BUS} to GND with a 1µF to 6.5µF capacitor, in accordance with USB OTG specifications. The charge pump can be turned off to conserve power when not used. Control of the charge pump is set through the vbus_drv bit (bit 5) of control register 2 (see Table 8).

Linear Regulator (TRM)

An internal 3.3V linear regulator powers the transceiver and the internal 1.5kΩ D+/D- pullup resistor. Under the control of internal register bits, the linear regulator can be powered from V_{CC} or V_{BUS}. The regulator power-supply settings are controlled by the reg_sel bit (bit 3) in special-function register 2 (Tables 15 and 16). This flexibility allows the system designer to configure the MAX3301E/MAX3302E for virtually any USB power situation.

The output of the TRM is not a power supply. Do not use as a power source for any external circuitry. Connect a 1.0µF (or greater) ceramic or plastic capacitor from TRM to GND, as close to the device as possible.

V_{BUS} Level-Detection Comparators

Comparators drive interrupt source register bits 0, 1, and 7 (Table 10) to indicate important USB OTG V_{BUS} voltage levels:

- V_{BUS} is valid (vbus_vld)
- USB session is valid (sess_vld)
- USB session has ended (sess_end)

The vbus_valid comparator sets vbus_vld to 1 if V_{BUS} is higher than the V_{BUS} valid comparator threshold. The V_{BUS} valid status bit (vbus_vld) is used by the A device to determine if the B device is sinking too much current (i.e., is not supported). The session_valid comparator sets sess_vld to 1 if V_{BUS} is higher than the session valid comparator threshold. This status bit indicates that a data transfer session is valid. The session_end comparator sets sess_end to 1 if V_{BUS} is higher than the

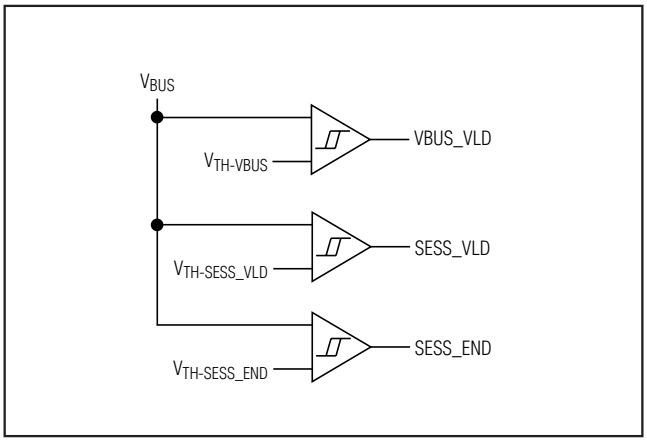


Figure 12. Comparator Network Diagram

session end comparator threshold. Figure 12 shows the level-detector comparators. The interrupt-enable registers (Tables 12 and 13) determine whether a falling or rising edge of V_{BUS} asserts these status bits.

ID_IN

The USB OTG specification defines an ID input that determines which dual-role device is the default host. An OTG cable connects ID to ground in the connector of one end and is left unconnected in the other end. Whichever dual-role device receives the grounded end becomes the A device. The MAX3301E/MAX3302E provide an internal pullup resistor on ID_IN. Internal comparators detect if ID_IN is grounded or left floating.

Interrupt Logic

When OTG events require action, the MAX3301E/MAX3302E provide an interrupt output signal on $\overline{INT}$. Alternatively, $\overline{OE}/\overline{INT}$ can be configured to act as an interrupt output while the device operates in USB suspend mode. Program $\overline{INT}$ and $\overline{OE}/\overline{INT}$ as open-drain or push-pull interrupts with irq_mode (bit 1 of special-function register 2, see Tables 15 and 16).

V_{BUS} Power Control

V_{BUS} is a dual-function port that powers the USB bus and/or provides a power source for the internal linear regulator. The V_{BUS} power-control block performs the various switching functions required by an OTG dual-role device. These actions are programmed by the system logic using bits 5 to 7 of control register 2 (see Table 8) to:

- Discharge V_{BUS} through a resistor
- Provide power-on or receive power from V_{BUS}
- Charge V_{BUS} through a resistor

The OTG supplement allows an A device to turn V_{BUS} off when the bus is not being used to conserve power. The B device can issue a request that a new session be started using SRP. The B device must discharge V_{BUS} to a level below the session-end threshold (0.8V) to ensure that no session is in progress before initiating SRP. Setting bit 6 of control register 2 to 1, discharges V_{BUS} to GND through a 5kΩ current-limiting resistor. When V_{BUS} has discharged, the resistor is removed from the circuit by resetting bit 6 of control register 2.

An OTG A device is required to supply power on V_{BUS}. The MAX3301E/MAX3302E provide power to V_{BUS} from V_{CC} or from the internal charge pump. Set bit 5 in control register 2 to 1 in both cases. Bit 5 in control register 2 controls a current-limited switch, preventing damage to the device in the event of a V_{BUS} short circuit.

An OTG B device (peripheral mode) can request a session using SRP. One of the steps in implementing SRP requires pulsing V_{BUS} high for a controlled time. A 930Ω resistor limits the current according to the OTG specification. Pulse V_{BUS} through the pullup resistor by asserting bit 7 of control register 2. Prior to pulsing V_{BUS} (bit 7), a B device first connects an internal pulldown resistor to discharge V_{BUS} below the session-end threshold. The discharge current is limited by the 5kΩ resistor and set by bit 6 of control register 2. An OTG A device must

Table 1. Functional Blocks Enabled During Specific Operating Modes

MODE	I²C	ID_IN	sess_end COMP	sess _vld COMP	vbus_ vld COMP	cr_int COMP	dp_hi COMP	dm_hi COMP	TRM	TX	DIFF RX	SE RX
Shutdown[1]	✓	X	X	X	X	X	X	X	X	X	X	X
Interrupt Shutdown[2]	✓	✓	X	✓	X	X	✓	✓	X	X	X	X
Suspend[3]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	X	✓
Normal Operating	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

✓ = Enabled.

X = Disabled.

1. *For the MAX3301E, enter shutdown mode by writing a 1 to sdwn (bit 0 of special-function register 2). For the MAX3302E, enter shutdown mode by writing a 0 to $\overline{sdwn}$ (bit 0 of special-function register 2).*
2. *Enter interrupt shutdown mode by writing a 1 to int_sdwn (bit 0 of special-function register 1).*
3. *Enter suspend mode by writing a 1 to spd_susp_ctl (bit 1 of special-function register 1) and suspend (bit 1 of control register 1), or by writing a 0 to spd_susp_ctl (bit 1 of special-function register 1) and driving SUS high.*

supply 5V power and at least 8mA on V_{BUS}. Setting bit 5 of control register 2 turns on the V_{BUS} charge pump.

Operating Modes

The MAX3301E/MAX3302E have four operating modes to optimize power consumption. Only the I²C interface remains active in shutdown mode, reducing supply current to 1µA. The I²C interface, the ID_IN port, and the session-valid comparator all remain active in interrupt shutdown mode. RCV asserts low in suspend mode; however, all other circuitry remains active. Table 1 lists the active blocks' power in each of the operating modes.

Applications Information

Data Transfer

Transmitting Data to the USB

The MAX3301E/MAX3302E transceiver features two modes of transmission: DAT_SE0 or VP_VM (see Table 3). Set the transmitting mode with dat_se0 (bit 2 in control register 1, see Table 7). In DAT_SE0 mode with $\overline{OE}/\overline{INT}$ low, DAT_VP specifies data for the differential transceiver, and SE0_VM forces D+/D- to the single-ended zero (SE0) state. In VP_VM mode with $\overline{OE}/\overline{INT}$ low, DAT_VP drives D+, and SE0_VM drives D-. The differential receiver determines the state of RCV.

Receiving Data from the USB

The MAX3301E/MAX3302E transceiver features two modes of receiving data: DAT_SE0 or VP_VM (see Table 4). Set the receiving mode with dat_se0 (bit 2 in control register 1, see Table 7). In DAT_SE0 mode with $\overline{OE}/\overline{INT}$ high, DAT_VP is the output of the differential receiver and SE0_VM indicates that D+ and D- are both logic-low. In VP_VM mode with $\overline{OE}/\overline{INT}$ high, DAT_VP provides the input logic level of D+ and SE0_VM provides the input logic level of D-. The differential receiver determines the state of RCV. VP and VM echo D+ and D-, respectively.

$\overline{OE}/\overline{INT}$

$\overline{OE}/\overline{INT}$ controls the direction of communication. $\overline{OE}/\overline{INT}$ can also be programmed to act as an interrupt output when in suspend mode. The output-enable portion controls the input or output status of DAT_VP/SE0_VM and D+/D-. When $\overline{OE}/\overline{INT}$ is a logic 0, DAT_VP and SE0_VM function as inputs to the D+ and D- outputs in a method depending on the status of dat_se0 (bit 2 in control register 1). When $\overline{OE}/\overline{INT}$ is a logic 1, DAT_VP and SE0_VM indicate the activity of D+ and D-.

$\overline{OE}/\overline{INT}$ functions as an interrupt output when the MAX3301E/MAX3302E is in suspend mode and oe_int_en = 1 (bit 5 in control register 1, see Table 7). In this mode, $\overline{OE}/\overline{INT}$ detects the same interrupts as $\overline{INT}$. Set irq_mode (bit 1 in special-function register 2, see Tables 15 and 16) to 0 to program $\overline{OE}/\overline{INT}$ as an open-drain interrupt output. Set irq_mode to 1 to configure $\overline{OE}/\overline{INT}$ as a push-pull interrupt output.

RCV

RCV monitors D+ and D- when receiving data. RCV is a logic 1 for D+ high and D- low. RCV is a logic 0 for D+ low and D- high. RCV retains its last valid state when D+ and D- are both low (single-ended zero, or SE0). RCV asserts low in suspend mode. Table 4 shows the state of RCV.

SPD

Use hardware or software to control the slew rate of the D+ and D- terminals. The SPD input sets the slew rate of the MAX3301E/MAX3302E when spd_susp_ctl (bit 1 in special-function register 1, see Table 14) is 0. Drive SPD low to select low-speed mode (1.5Mbps). Drive SPD high to select full-speed mode (12Mbps). Alternatively, when spd_susp_ctl (bit 1 of special-function register 1) is 1, software controls the slew rate. The SPD input is ignored when using software to control the data rate. The speed bit (bit 0 of control register 1, see Table 7) sets the slew rate when spd_susp_ctl = 1.

SUS

Use hardware or software to control the suspend mode of the MAX3301E/MAX3302E. Set spd_susp_ctl (bit 1 of special-function register 1, see Table 14) to 0 to allow the SUS input to enable and disable the suspend mode of the MAX3301E/MAX3302E. Drive SUS low for normal operation. Drive SUS high to enable suspend mode. RCV asserts low in suspend mode while all other circuitry remains active.

Alternatively, when the spd_susp_ctl bit (bit 1 of special-function register 1) is set to 1, software controls the suspend mode. Set the suspend bit (bit 1 of control register 1, see Table 7) to 1 to enable suspend mode. Set the suspend bit to 0 to resume normal operation. The SUS input is ignored when using software to control suspend mode. The MAX3301E/MAX3302E must be in full-speed mode (SPD = high or speed = 1) to issue a remote wake-up from the device when in suspend mode.

$\overline{RESET}$

The active-low $\overline{RESET}$ input allows the MAX3301E/MAX3302E to be asynchronously reset without cycling the power supply. Drive $\overline{RESET}$ low to reset the internal registers (see Tables 7–16 for the default power-up states). Drive $\overline{RESET}$ high for normal operation.

2-Wire I²C-Compatible Serial Interface

A register file controls the various internal switches and operating modes of the MAX3301E/MAX3302E through a simple 2-wire interface operating at clock rates up to 400kHz. This interface supports data bursting, where multiple data phases can follow a single address phase.

UART Mode

Set uart_en (bit 6 in control register 1) to 1 to place the MAX3301E/MAX3302E in UART mode. D+ transfers data to DAT_VP and SE0_VM transfers data to D- in UART mode.

General-Purpose Buffer Mode

Set gp_en (bit 7 in special-function register 1) and dat_se0 (bit 2 in control register 1) to 1, set uart_en (bit 6 in control register 1) to 0, and drive $\overline{OE}/\overline{INT}$ low to place the MAX3301E/MAX3302E in general-purpose buffer mode. Control the direction of data transfer with dminus_dir and dplus_dir (bits 3 and 4 of special-function register 1, see Tables 2 and 14).

Serial Addressing

The MAX3301E/MAX3302E operate as a slave device that sends and receives control and status signals through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX3301E/MAX3302E and generates the SCL clock that synchronizes the data transfer (Figure 13).

The MAX3301E/MAX3302E SDA line operates as both an input and as an open-drain output. SDA requires a pullup resistor, typically 4.7kΩ. The MAX3301E/MAX3302E SCL line only operates as an input. SCL requires a pullup resistor if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a start condition (see Figure 14) sent by a master device, the MAX3301E/MAX3302E 7-bit slave address (determined by the state of ADD), plus an $R/\overline{W}$ bit (see Figure 15), a register address byte, one or more data bytes, and a stop condition (see Figure 14).

Table 2. Setting the Direction of Data Transfer in General-Purpose Buffer Mode

dplus_dir	dminus_ dir	DIRECTION OF DATA TRANSFER
0	0	DAT_VP → D+ SE0_VM → D-
0	1	DAT_VP → D+ SE0_VM ← D-
1	0	DAT_VP ← D+ SE0_VM → D-
1	1	DAT_VP ← D+ SE0_VM ← D-

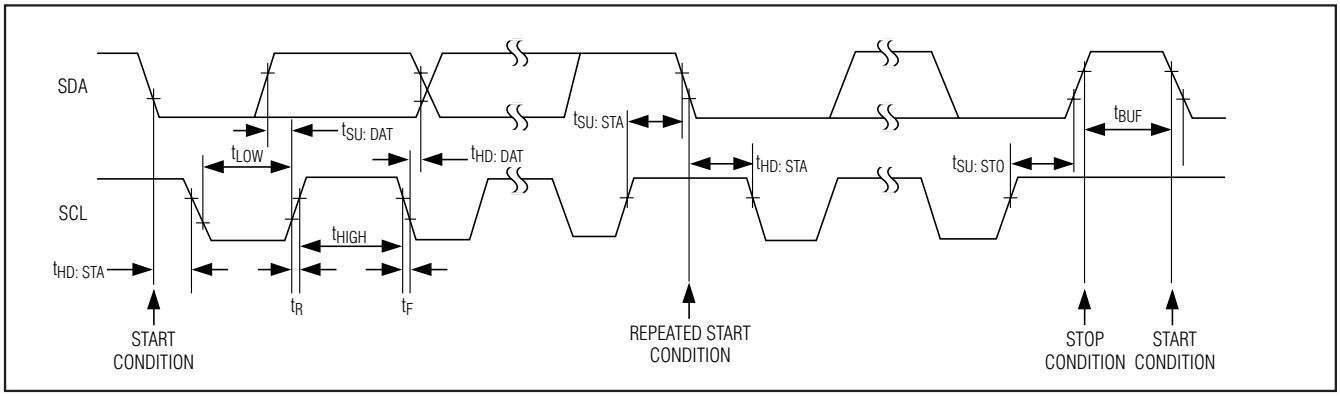


Figure 13. 2-Wire Serial-Interface Timing Details

Table 3. Transmit Mode

MODE	CONTROL PIN/BIT				INPUT		OUTPUT		DESCRIPTION
	SUS	GP_EN	$\overline{OE/INT}$	DAT_SE0	DAT_VP	SE0_VM	D+	D-	
Functional DAT_SE0	0	0	0	1	0	0	0	1	USB functional mode transceiver and I2C interface are fully functional
	0	0	0	1	1	0	1	0	
	0	0	0	1	0	1	0	0	
	0	0	0	1	1	1	0	0	
Functional VP_VM	0	0	0	0	0	0	0	0	
	0	0	0	0	1	0	1	0	
	0	0	0	0	0	1	0	1	
	0	0	0	0	1	1	1	1	
Suspend	1	0	0	1	0	0	0	1	USB suspend mode
	1	0	0	1	1	0	1	0	
	1	0	0	1	0	1	0	0	
	1	0	0	1	1	1	0	0	
	1	0	0	0	0	0	0	0	
	1	0	0	0	1	0	1	0	
	1	0	0	0	0	1	0	1	
	1	0	0	0	1	1	1	1	
	1	0	1	X	X	X	Driver is Hi-Z	Driver is Hi-Z	
Receiving	0	0	1	X	X	X	Driver is Hi-Z	Driver is Hi-Z	See Table 4
General-purpose buffer	X	1	0	1	See Table 2				General-purpose buffer mode

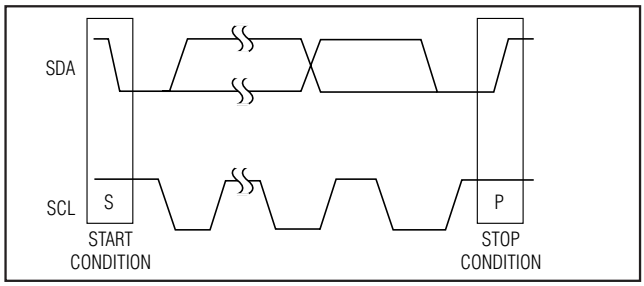


Figure 14. Start and Stop Conditions

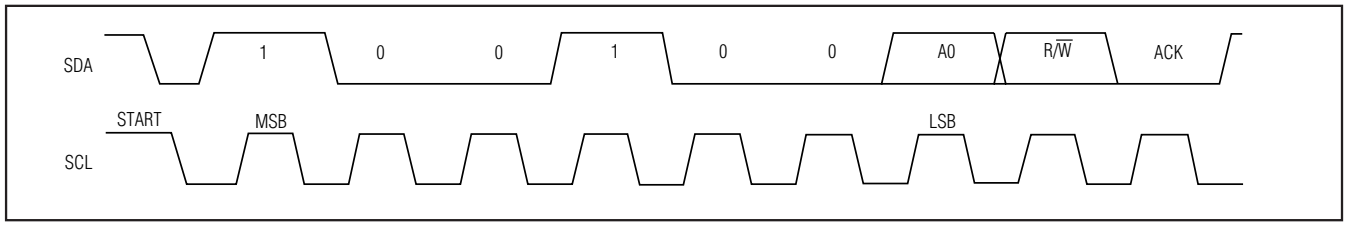


Figure 15. Slave Address

Table 4. Receive Mode

MODE	CONTROL PIN/BIT					INPUTS		OUTPUTS				
	SUS (NOTE 7)	GP_EN	OE/INT	DAT_SE0	BI_DI	D+	D-	DAT_VP	SE0_VM	RCV	VP	VM
Functional DAT_SE0	0	0	1	1	1	0	0	Last value of DAT_VP	1	Last value of RCV	Echo D+	Echo D-
	0	0	1	1	1	1	0	1	0	1		
	0	0	1	1	1	0	1	0	0	0		
	0	0	1	1	1	1	1	Undefined	0	Undefined		
	1	0	1	1	1	0	0	0	1	0		
	1	0	1	1	1	1	0	1	0	0		
	1	0	1	1	1	0	1	0	0	0		
	1	0	1	1	1	1	1	1	0	0		
Functional VP_VM	0	0	1	0	1	0	0	0	0	Last value of RCV		
	0	0	1	0	1	1	0	1	0	1		
	0	0	1	0	1	0	1	0	1	0		
	0	0	1	0	1	1	1	1	1	Undefined		
	1	0	1	0	1	0	0	0	0	0		
	1	0	1	0	1	1	0	1	0	0		
	1	0	1	0	1	0	1	0	1	0		
	1	0	1	0	1	1	1	1	1	0		
General-purpose buffer	X	1	X	X	X	See Table 2				0		
Transmitting (see Table 3)	X	X	0	X	X	—				0		
Unidirectional (transmitter only)	X	X	X	X	0	—				0		

Note 7: Enter suspend mode by driving SUS high or by writing a 1 to suspend (bit 1 in control register 1), depending on the status of spd_susp_ctl in special-function register 1.

X = Don't care.

Start and Stop Conditions

Both SCL and SDA assert high when the interface is not busy. A master device signals the beginning of a transmission with a start (S) condition by transitioning SDA from high to low while SCL is high. The master issues a stop (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (see Figure 14).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (see Figure 16).

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. ACK is always generated by the receiving device. The MAX3301E/MAX3302E generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. When transmitting data, the MAX3301E/MAX3302E wait for the receiving device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

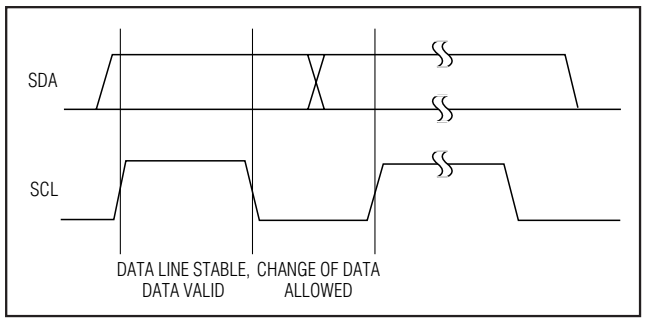


Figure 16. Bit Transfer

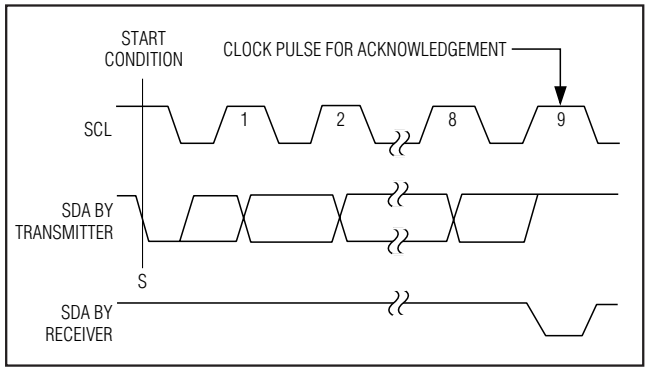


Figure 17. Acknowledge

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address (see Figure 15). When idle, the MAX3301E/MAX3302E wait for a START condition followed by its slave address. The LSB of the address word is the read/$\overline{\text{write}}$ (R/$\overline{W}$) bit. R/$\overline{W}$ indicates whether the master is writing to or reading from the MAX3301E/MAX3302E (R/$\overline{W}$ = 0 selects the write condition, R/$\overline{W}$ = 1 selects the read condition). After receiving the proper address, the MAX3301E/MAX3302E issue an ACK.

The MAX3301E/MAX3302E have two possible addresses (see Table 5). Address bits A6 through A1 are preset, while a reset condition or an I²C general call address loads the value of A0 from ADD. Connect ADD to GND to set A0 to 0. Connect ADD to V_L to set A0 to 1. This allows up to two MAX3301E's or two MAX3302E's to share the same bus.

Write Byte Format

Writing data to the MAX3301E/MAX3302E requires the transmission of at least 3 bytes. The first byte consists of the MAX3301E/MAX3302E's 7-bit slave address, followed by a 0 (R/$\overline{W}$ bit). The second byte determines which register is to be written to. The third byte is the new data for the selected register. Subsequent bytes are data for sequential registers. Figure 18 shows the typical write byte format.

Read Byte Format

Reading data from the MAX3301E/MAX3302E requires the transmission of at least 3 bytes. The first byte consists of the MAX3301E/MAX3302E's slave address, followed by a 0 (R/$\overline{W}$ bit). The second byte selects the register from which data is read. The third byte consists

S	SLAVE ADDRESS (7 BITS)							R/$\overline{W}$	A	REGISTER ADDRESS (8 BITS)								A	DATA (8 BITS)								A	P
	A6	A5	A4	A3	A2	A1	A0	0		MSB							LSB		MSB							LSB			

Figure 18. Write Byte Format

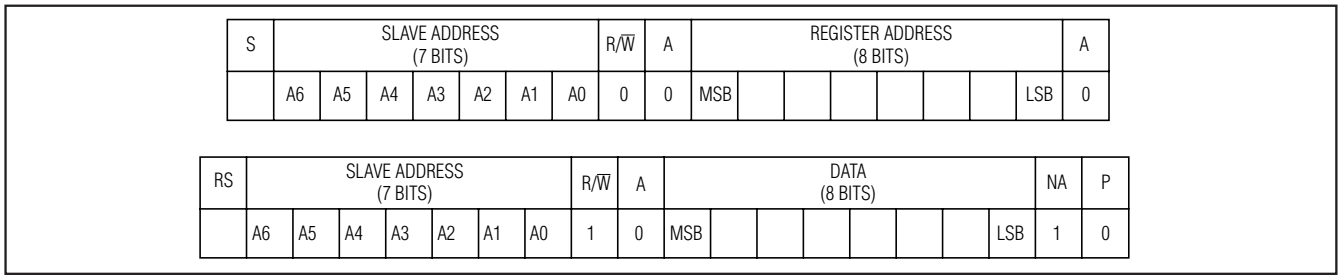


Figure 19. Read Byte Format

R/$\overline{W}$: Read/write (R/$\overline{W}$ = 1: read; R/$\overline{W}$ = 0: write)

S: Start condition

RS: Repeated start condition

P: Stop condition

A: Acknowledge bit from the slave

NA: Not-acknowledged bit from the master

Blank: Master transmission

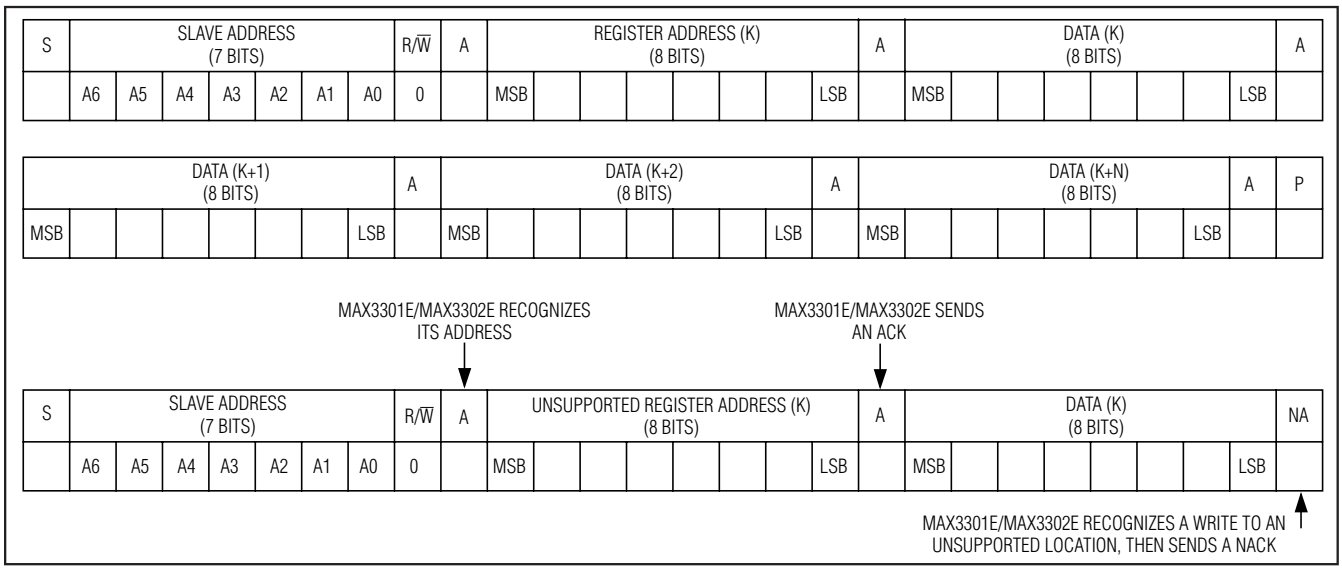


Figure 20. Burst-Mode Write Byte Format

of the MAX3301E/MAX3302E's slave address, followed by a 1 (R/$\overline{W}$ bit). The master then reads one or more bytes of data. Figure 19 shows the typical read byte format.

Burst-Mode Write Byte Format

The MAX3301E/MAX3302E allow a master device to write to sequential registers without repeatedly sending the slave address and register address each time. The master first sends the slave address, followed by a 0 to write data to the MAX3301E/MAX3302E. The MAX3301E/MAX3302E send an acknowledge bit back to the master. The master sends the 8-bit register address and the MAX3301E/MAX3302E return an acknowledge bit. The master writes a data byte to the selected register and receives an acknowledge bit if a supported register address has been chosen. The register address increments and is ready for the master to send the next data byte. The MAX3301E/MAX3302E send an acknowledge bit after each data byte. If an unsupported register is selected, the MAX3301E/MAX3302E send a NACK to the master and the register index does not increment (see Figure 20).

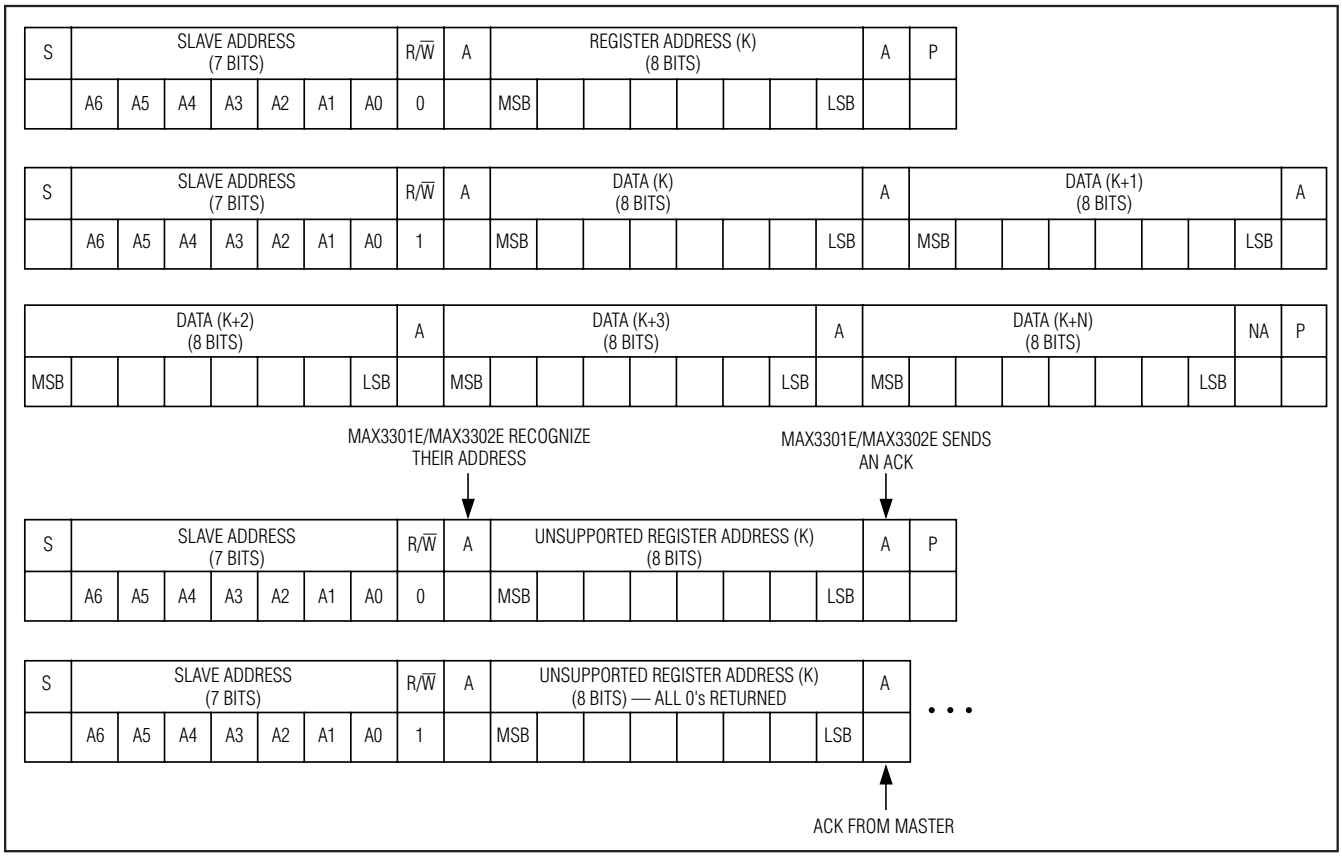


Figure 21. Burst-Mode Read Byte Format

Table 5. I²C Slave Address Map

ADD INPUT	ADDRESS BITS						
	A_6	A_5	A_4	A_3	A_2	A_1	A_0
GND (0)	0	1	0	1	1	0	0
V_L (1)	0	1	0	1	1	0	1

Table 6. Register Map

REGISTER	MEMORY ADDRESS	DESCRIPTION
Vendor ID	00h, 01h	Read only. The contents of registers 00h and 01h are 6Ah and 0Bh, respectively.
Product ID	02h, 03h	Read only. The contents of registers 02h and 03h are 01h and 33h, respectively.
Control 1	04h (set) 05h (clear)	Sets operating modes, maximum data rate, and direction of data transfer.
Control 2	06h (set) 07h (clear)	Controls D+/D- pullup/pulldown resistor connections, ID_IN state, and V_{BUS} behavior.
Interrupt source	08h (read)	Read only.
Unused*	09h	Not used.
Interrupt latch	0Ah (set) 0Bh (clear)	Indicates which interrupts have occurred.
Interrupt-enable Falling edge	0Ch (set) 0Dh (clear)	Enables interrupts for high-to-low transitions.
Interrupt-enable Rising edge	0Eh (set) 0Fh (clear)	Enables interrupts for low-to-high transitions.
Unused*/Special Function 2	10h (set) 11h (clear)	MAX3301E: Not used. MAX3302E: Alternate register addresses for special-function register 2. This register is also accessible from 16h and 17h.
Special function 1	12h (set) 13h (clear)	Enables hardware/software control of the MAX3301E's behavior, interrupt activity, and operating modes.
Revision ID	14h, 15h	Read only. The contents of registers 14h and 15h are 77h and 41h, respectively.
Special function 2	16h (set) 17h (clear)	Sets operating modes, $\overline{INT}$ output configuration, D+/D- behavior in audio mode, and TRM source.
Unused*	18h–Fh	Not used.

**When writing to an unused register, the device generates a NACK and the register index does not increment.*

Burst-Mode Read Byte Format

The MAX3301E/MAX3302E allow a master device to read data from sequential registers with the burst-mode read byte protocol (see Figure 21). The master device first sends the slave address, followed by a 0. The MAX3301E/MAX3302E then sends an acknowledge bit. Next, the master sends the register address to the MAX3301E/MAX3302E, which then generates another acknowledge bit. The master then sends a stop condition to the MAX3301E/MAX3302E. Next, the master sends a start condition, followed by the MAX3301E/MAX3302E's slave address, and then a 1 to indicate a read command. The MAX3301E/MAX3302E then sends data to the master device, one byte at a time. The master sends an acknowledge bit to the MAX3301E/MAX3302E after each data byte, and the register address of the MAX3301E/MAX3302E increments after each byte. This continues until the master sends a stop condition. If an unsupported register address is encountered, the MAX3301E/MAX3302E send a byte of zeros.

Registers

Control Registers

There are two read/write control registers. Control register 1 (Table 7) sets operating modes, sets the data rate, and controls the direction of data transfer. Control register 2 (Table 8) connects the D+/D- pullup or pulldown resistors, sets the V_{BUS} charge/discharge conditions, and grounds ID_IN. The control registers have two addresses that implement write-one-set and write-one-clear features for each of these registers. Writing a 1 to the set address sets that bit to 1. Writing a 1 to the clear address resets that bit to 0. Writing a 0 to either address has no effect on the bits.

Table 7. Control Register 1 Description (Write to Address 04h to Set, Write to Address 05h to Clear)

BIT NUMBER	SYMBOL	OPERATION	VALUE AT POWER-UP
0	speed	Set to 0 for low-speed (1.5Mbps) mode. Set to 1 for full-speed (12Mbps) mode. This bit changes the data rate only if spd_susp_ctl = 1 in special-function register 1.	0
1	suspend	Set to 0 for normal operating mode. Set to 1 for suspend mode. This bit changes the operating mode only if spd_susp_ctl = 1 in special-function register 1.	0
2	dat_se0	Set to 0 for VP_VM USB mode. Set to 1 for DAT_SE0 USB mode.	0
3	—	Not used.	0
4	bdis_acon_en	Enables the transceiver (when configured as an A device) to connect its pullup resistor if the B device disconnect is detected during HNP. Set to 0 to disable this feature. Set to 1 to enable this feature.	0
5	oe_int_en	Set to 0 to disable the interrupt output circuitry of $\overline{OE}/\overline{INT}$. Set to 1 to enable the interrupt output circuitry of $\overline{OE}/\overline{INT}$.	0
6	uart_en	Set to 0 to disable UART mode. Set to 1 to enable UART mode. This bit overrides the settings of dminus_dir, dplus_dir, and gp_en bits.	0
7	—	Not used.	0

Table 8. Control Register 2 Description (Write to Address 06h to Set, Write to Address 07h to Clear)

BIT NUMBER	SYMBOL	OPERATION	VALUE AT POWER-UP
0	dp_pullup	Set to 0 to disconnect the pullup resistor to D+. Set to 1 to connect the pullup resistor to D+.	0
1	dm_pullup	Set to 0 to disconnect the pullup resistor to D-. Set to 1 to connect the pullup resistor to D-.	0
2	dp_pulldown	Set to 0 to disconnect the pulldown resistor to D+. Set to 1 to connect the pulldown resistor to D+.	1
3	dm_pulldown	Set to 0 to disconnect the pulldown resistor to D-. Set to 1 to connect the pulldown resistor to D-.	1
4	id_pulldown	Set to 0 to allow ID_IN to float. Set to 1 to connect ID_IN to GND.	0
5	vbus_drv	Set to 0 to turn V_{BUS} off. Set to 1 to drive V_{BUS} through a low impedance (see Note 8).	0
6	vbus_dischrg	Set to 0 to disconnect the V_{BUS} discharge resistor. Set to 1 to connect the V_{BUS} discharge resistor (see Note 8).	0
7	vbus_chrg	Set to 0 to disconnect the V_{BUS} charge resistor. Set to 1 to connect the V_{BUS} charge resistor (see Note 8).	0

Note 8: To prevent a high-current state where the transceiver is both sourcing current to V_{BUS} and sinking current from V_{BUS}, the following logic is used to set bits 5, 6, and 7 of control register 2:

- Setting vbus_drv clears vbus_dischrg and vbus_chrg
- Setting vbus_dischrg clears vbus_drv and vbus_chrg, unless vbus_drv is set with the same command, in which case vbus_drv clears the other bits
- Setting vbus_chrg clears vbus_drv and vbus_dischrg, unless either of these bits are set with the same command, as shown in Table 9

Table 9. V_{BUS} Control Logic

SET COMMAND (ADDRESS 06h)			BEHAVIOR OF MAX3301E/MAX3302E		
vbus_drv	vbus_dischrg	vbus_chrg	vbus_drv	vbus_dischrg	vbus_chrg
1	X	X	1	0	0
0	1	X	0	1	0
0	0	1	0	0	1
0	0	0	Not affected	Not affected	Not affected

X = Don't care.

Table 10. Interrupt Source Register (Address 08h is Read Only)

BIT NUMBER	SYMBOL	CONTENTS
0	vbus_vld	Logic 1 if V_{BUS} > V_{BUS} valid comparator threshold.
1	sess_vld	Logic 1 if V_{BUS} > session valid comparator threshold.
2	dp_hi	Logic 1 if V_{D+} > dp_hi comparator threshold (D+ assertion during data line pulsing through SRP method).
3	id_gnd	Logic 1 if V_{ID_IN} < 0.1 x V_{CC}.
4	dm_hi	Logic 1 if V_{D-} > dm_hi comparator threshold (D- assertion during data line pulsing through SRP method).
5	id_float	Logic 1 if V_{ID_IN} > 0.9 x V_{CC}.
6	bdis_acon	Logic 1 if bdis_acon_en = 1 and the MAX3301E/MAX3302E assert dp_pullup after detecting a B device disconnect during HNP.
7	cr_int_sess_end	Logic 1 if V_{BUS} < sess_end comparator threshold, or if V_{D+} > cr_int comparator threshold (0.4V to 0.6V), depending on the value of int_source (bit 5 of special-function register 1, see Table 14).

Interrupt Registers

Four registers control all interrupt behavior of the MAX3301E/MAX3302E. A source register (Table 10) indicates the current status of the various interrupt sources. An interrupt latch register (Table 11) indicates which interrupts have occurred. An interrupt-enable low and interrupt-enable high register enable interrupts on rising or falling (or both) transitions. Tables 10–13 provide the bit configurations for the various interrupt registers. The interrupt latch, interrupt-enable low, and interrupt-enable high registers have two addresses that implement write- one-set and write-one-clear features for each of these registers. Writing a 1 to the set address sets that bit to 1. Writing a 1 to the clear address resets that bit to 0. Writing a 0 to either address has no effect on the bits.

Special-Function Registers

Tables 14, 15, and 16 describe the special-function registers. The special-function registers have two addresses that implement write-one-set and write-one-clear features for each of these registers. Writing a 1 to the set address sets that bit to 1. Writing a 1 to the clear address resets that bit to 0. Writing a 0 to either address has no effect on the bits. Special-function register 1 determines whether hardware or software controls the maximum data rate and suspend behavior, sets the direction of data transfer, and toggles general-purpose buffer mode. Special-function register 2 enables shutdown mode, configures the interrupt output as open-drain or push-pull, sets the TRM power source, and controls the D+/D- connections for audio mode. Table 15 depicts the special-function register 2 for the MAX3301E and Table 16 depicts the special-function register 2 for the MAX3302E.

The MAX3301E powers up in its lowest power state and must be turned on by setting the sdwn bit to 0. The MAX3302E powers up in the operational, VP/VM USB mode. This allows a µP to use the USB port for power-on boot-up, without having to access I²C. To put the MAX3302E into low-power shutdown, set the sdwn bit to 0. The MAX3302E also has special-function register 2 mapped to two I²C register addresses. In the MAX3302E, special-function register 2 can be

Table 11. Interrupt Latch Register Description (Write to Address 0Ah to Set, Write to Address 0Bh to Clear)

BIT NUMBER	SYMBOL	CONTENTS	VALUE AT POWER-UP
0	vbus_vld	vbus_vld asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0
1	sess_vld	sess_vld asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0
2	dp_hi	dp_hi asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0
3	id_gnd	id_gnd asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0
4	dm_hi	dm_hi asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0
5	id_float	id_float asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0
6	bdis_acon	bdis_acon asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0
7	cr_int_sess_end	cr_int_sess_end asserts if a transition occurs on this condition and the appropriate interrupt-high or interrupt-low enable bit is set. See Tables 10, 12, and 13.	0

Table 12. Interrupt-Enable Low Register (Write to Address 0Ch to Set, Write to Address 0Dh to Clear)

BIT NUMBER	SYMBOL	CONTENTS	VALUE AT POWER-UP
0	vbus_vld	Set to 0 to disable the vbus_vld interrupt for a high-to-low transition. Set to 1 to enable the vbus_vld interrupt for a high-to-low transition. See Tables 10 and 11.	0
1	sess_vld	Set to 0 to disable the sess_vld interrupt for a high-to-low transition. Set to 1 to enable the sess_vld interrupt for a high-to-low transition. See Tables 10 and 11.	0
2	dp_hi	Set to 0 to disable the dp_hi interrupt for a high-to-low transition. Set to 1 to enable the dp_hi interrupt for a high-to-low transition. See Tables 10 and 11.	0
3	id_gnd	Set to 0 to disable the id_gnd interrupt for a high-to-low transition. Set to 1 to enable the id_gnd interrupt for a high-to-low transition. See Tables 10 and 11.	0
4	dm_hi	Set to 0 to disable the dm_hi interrupt for a high-to-low transition. Set to 1 to enable the dm_hi interrupt for a high-to-low transition. See Tables 10 and 11.	0
5	id_float	Set to 0 to disable the id_float interrupt for a high-to-low transition. Set to 1 to enable the id_float interrupt for a high-to-low transition. See Tables 10 and 11.	0
6	bdis_acon	Set to 0 to disable the bdis_acon interrupt for a high-to-low transition. Set to 1 to enable the bdis_acon interrupt for a high-to-low transition. See Tables 10 and 11.	0
7	cr_int_sess_end	Set to 0 to disable the cr_int_sess_end interrupt for a high-to-low transition. Set to 1 to enable the cr_int_sess_end interrupt for a high-to-low transition. See Tables 10 and 11.	0

Table 13. Interrupt-Enable High Register (Write to Address 0Eh to Set, Write to Address 0Fh to Clear)

BIT NUMBER	SYMBOL	CONTENTS	VALUE AT POWER-UP
0	vbus_vld	Set to 0 to disable the vbus_vld interrupt for a low-to-high transition. Set to 1 to enable the vbus_vld interrupt for a low-to-high transition. See Tables 10 and 11.	0
1	sess_vld	Set to 0 to disable the sess_vld interrupt for a low-to-high transition. Set to 1 to enable the sess_vld interrupt for a low-to-high transition. See Tables 10 and 11.	0
2	dp_hi	Set to 0 to disable the dp_hi interrupt for a low-to-high transition. Set to 1 to enable the dp_hi interrupt for a low-to-high transition. See Tables 10 and 11.	0
3	id_gnd	Set to 0 to disable the id_gnd interrupt for a low-to-high transition. Set to 1 to enable the id_gnd interrupt for a low-to-high transition. See Tables 10 and 11.	0
4	dm_hi	Set to 0 to disable the dm_hi interrupt for a low-to-high transition. Set to 1 to enable the dm_hi interrupt for a low-to-high transition. See Tables 10 and 11.	0
5	id_float	Set to 0 to disable the id_float interrupt for a low-to-high transition. Set to 1 to enable the id_float interrupt for a low-to-high transition. See Tables 10 and 11.	0
6	bdis_acon	Set to 0 to disable the bdis_acon interrupt for a low-to-high transition. Set to 1 to enable the bdis_acon interrupt for a low-to-high transition. See Tables 10 and 11.	0
7	cr_int_sess_end	Set to 0 to disable the cr_int_sess_end interrupt for a low-to-high transition. Set to 1 to enable the cr_int_sess_end interrupt for a low-to-high transition. See Tables 10 and 11.	0

addressed at I²C register location 10h, 11h (as well as locations 16h, 17h) to support USB OTG SIE implementations that are limited to I²C register addresses between 0h and 15h.

ID and Manufacturer Register Address Map

Table 17 provides the contents of the ID registers of the MAX3301E/MAX3302E. Addresses 00h and 01h comprise the vendor ID registers. Addresses 02h and 03h comprise the product ID registers. Addresses 14h and 15h comprise the revision ID registers.

Audio Car Kit

Many cell phones are required to interface to car kits. Depending upon the car kit, the interface to the phone may be required to support any or all of the following functions:

- Audio input
- Audio output
- Charging
- Control and status

D+ and D- of the MAX3301E/MAX3302E go to a high-impedance state when in shutdown mode, allowing external signals (including audio) to be multiplexed onto these lines.

External Components

External Resistors

Two external resistors (27.4Ω ±1%) are required for USB connection. Install one resistor in series between D+ of the MAX3301E/MAX3302E and D+ of the USB connector. Install the other resistor in series between D- of the MAX3301E/MAX3302E and D- of the USB connector (see the *Typical Operating Circuit*).

External Capacitors

Five external capacitors are recommended for proper operation. Install all capacitors as close to the device as possible. Decouple V_L to GND with a 0.1µF ceramic capacitor. Bypass V_{CC} to GND with a 1µF ceramic capacitor. Bypass TRM to GND with a 1µF (or greater) ceramic or plastic capacitor. Connect a 100nF flying capacitor between C+ and C- for the charge pump (see the *Typical Operating Circuit*). Bypass V_{BUS} to GND with a 1µF to 6.5µF ceramic capacitor in accordance with USB OTG specifications.

ESD Protection

To protect the MAX3301E/MAX3302E against ESD, D+, D-, ID_IN, and V_{BUS}, have extra protection against static electricity to protect the device up to ±15kV. The ESD structures withstand high ESD in all states; normal oper-

Table 14. Special-Function Register 1 (Write to Address 12h to Set, Write to Address 13h to Clear)

BIT NUMBER	SYMBOL	CONTENTS	VALUE AT POWER-UP
0	int_sdwn	Set to 0 for normal operation. Set to 1 to enter interrupt shutdown mode. The I²C interface and interrupt sources remain active, while all other circuitry is off.	0
1	spd_susp_ctl	Set to 0 to control the MAX3301E/MAX3302E behavior with SPD and SUS. Set to 1 to control the MAX3301E/MAX3302E behavior with the speed and suspend bits in control register 1 (see Table 7).	0
2	bi_di	Set to 0 to transfer data from DAT_VP and SE0_VM to D+ and D-, respectively. DAT_VP and SE0_VM are always inputs when this bit is 0. Set to 1 to control the direction of data transfer with $\overline{OE}/\overline{INT}$.	1
3	dminus_dir	Set to 0 to transfer data from SE0_VM to D-. Set to 1 to transfer data from D- to SE0_VM. Ensure that gp_en = 1, dat_se0 = 1, uart_en = 0, and $\overline{OE}/\overline{INT}$ = low to activate this function.	0
4	dplus_dir	Set to 0 to transfer data from DAT_VP to D+. Set to 1 to transfer data from D+ to DAT_VP. Ensure that gp_en = 1, dat_se0 = 1, uart_en = 0, and $\overline{OE}/\overline{INT}$ = low to activate this function.	0
5	int_source	Set to 0 to use cr_int as the interrupt source for bit 7 of the interrupt source register. Set to 1 to use sess_end as the interrupt source for bit 7 of the interrupt source register (see Table 10).	0
6	sess_end	Session end comparator status (read only). Sess_end = 0 when V_{BUS} > sess_end threshold. Sess_end = 1 when V_{BUS} < sess_end threshold.	—
7	gp_en	Set to 0 to disable general-purpose buffer mode. Set to 1 to enable general-purpose buffer mode.	0

Note: sess_end value at power-up is dependent on the voltage at V_{BUS}.

Table 15. MAX3301E Special-Function Register 2 (Write to Address 16h to Set, Write to Address 17h to Clear)

BIT NUMBER	SYMBOL	CONTENTS	VALUE AT POWER-UP
0	sdwn	Set to 0 for normal operation. Set to 1 to enable shutdown mode. Only the I²C interface remains active in shutdown.	1
1	irq_mode	Set to 0 to set $\overline{INT}$ and $\overline{OE}/\overline{INT}$ as open-drain outputs. Set to 1 to set $\overline{INT}$ and $\overline{OE}/\overline{INT}$ as push-pull outputs.	0
2	xcvr_input_disc	Set to 0 to leave the D+/D- single-ended receiver inputs connected. Set to 1 to disconnect the D+/D- receiver inputs to reduce power consumption in audio mode.	0
3	reg_sel	Set to 0 to power TRM from V_{CC}. Set to 1 to power TRM from V_{BUS}.	0
4–7	—	Reserved. Set to 0 for normal operation.	0000

ation, suspend mode, interrupt shutdown, and shutdown. For the ESD structures to work correctly, connect a 1µF or greater capacitor from TRM to GND and from V_{BUS} to GND. ESD protection can be tested in various ways; the D+, D-, ID_IN, and V_{BUS} inputs/outputs are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±6kV using the IEC 61000-4-2 Contact Discharge Method
- ±10kV using the IEC 61000-4-2 Air-Gap Discharge Method

Table 16. MAX3302E Special-Function Register 2 (Write to Address 10h or 16h to Set, Write to Address 11h or 17h to Clear)

BIT NUMBER	SYMBOL	CONTENTS	VALUE AT POWER-UP
0	$\overline{sdwn}$	Set to 0 to enable shutdown mode. Set to 1 for normal operation. Only the I²C interface remains active in shutdown.	1
1	irq_mode	Set to 0 to set $\overline{INT}$ and $\overline{OE}/\overline{INT}$ as open-drain outputs. Set to 1 to set $\overline{INT}$ and $\overline{OE}/\overline{INT}$ as push-pull outputs.	0
2	xcvr_input_disc	Set to 0 to leave the D+/D- single-ended receiver inputs connected. Set to 1 to disconnect the D+/D- receiver inputs to reduce power consumption in audio mode.	0
3	reg_sel	Set to 0 to power TRM from V_{CC}. Set to 1 to power TRM from V_{BUS}.	0
4–7	—	Reserved. Set to 0 for normal operation.	0000

Table 17. ID Registers

REGISTER	ADDRESS	CONTENTS
Vendor ID	00h	6Ah
	01h	0Bh
Product ID	02h	01h
	03h	33h
Revision ID	14h	77h
	15h	41h

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 22 shows the Human Body Model and Figure 23 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3301E/MAX3302E helps the user design equipment that meets level 3 of IEC 61000-4-2, without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2, due to the fact that series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD-withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 24 shows the IEC 61000-4-2 model. The Air-Gap Discharge test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized. Figure 25 shows the IEC 61000-4-2 current waveform.

Layout Considerations

The MAX3301E/MAX3302E high operating frequency makes proper layout important to ensure stability and maintain the output voltage under all loads. For best performance, minimize the distance between the bypass capacitors and the MAX3301E/MAX3302E. Use symmetric trace geometry from D+ and D- to the USB connector.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and the recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: *Understanding the Basics of the Wafer-Level Chip-Scale Package (WL-CSP)* available on Maxim's website at www.maxim-ic.com/ucsp.

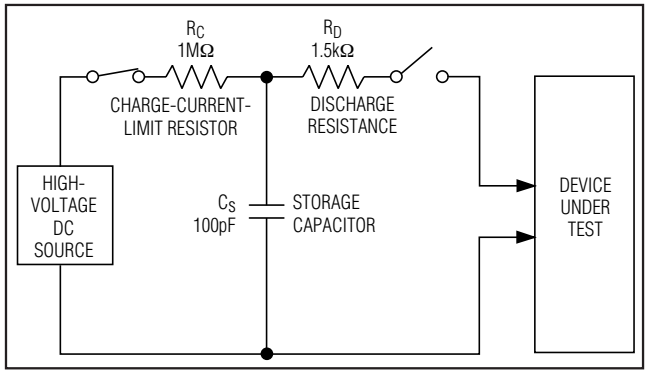


Figure 22. Human Body ESD Test Modes

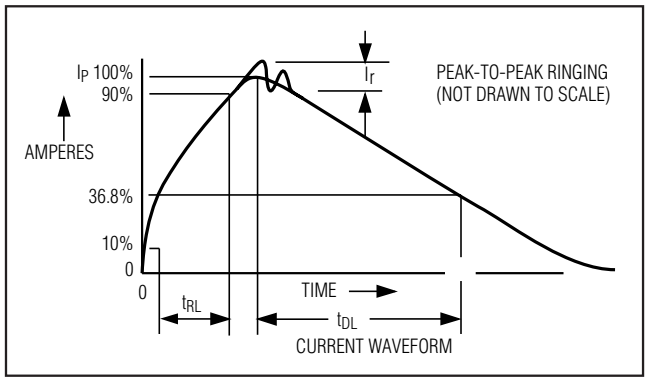


Figure 23. Human Body Model Current Waveform

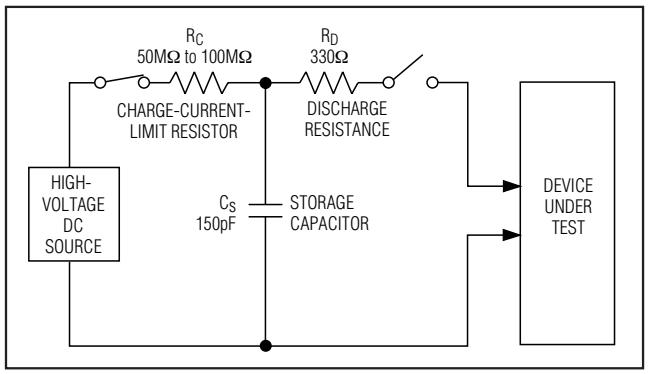


Figure 24. IEC 61000-4-2 ESD Test Model

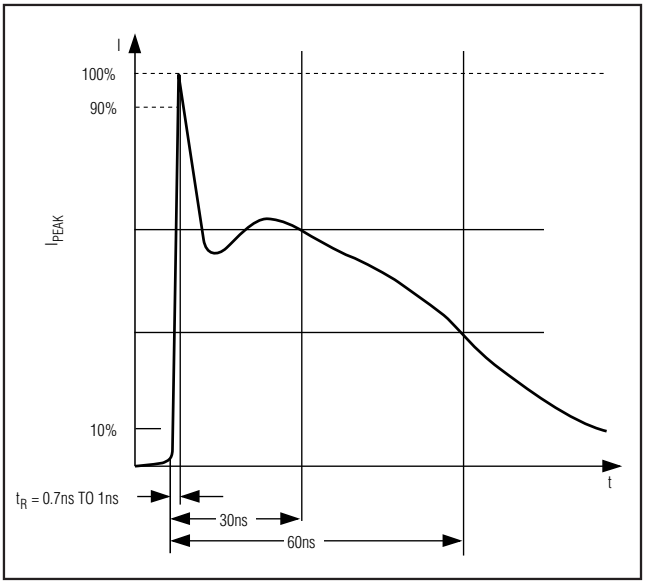
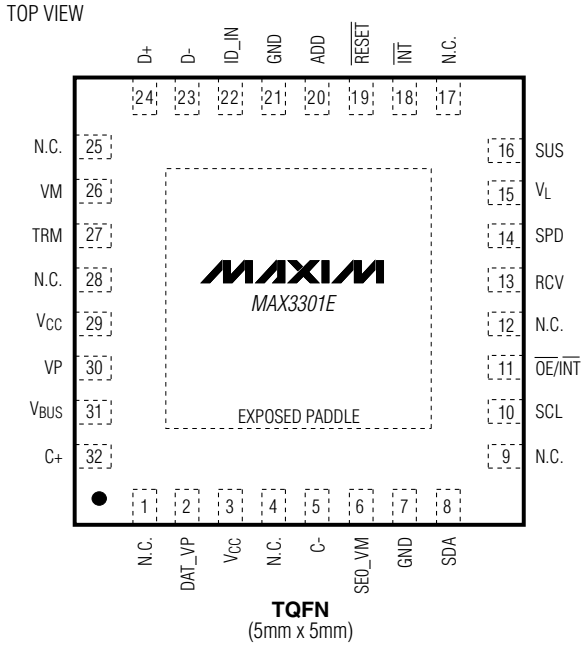


Figure 25. IEC 61000-4-2 Current Waveform

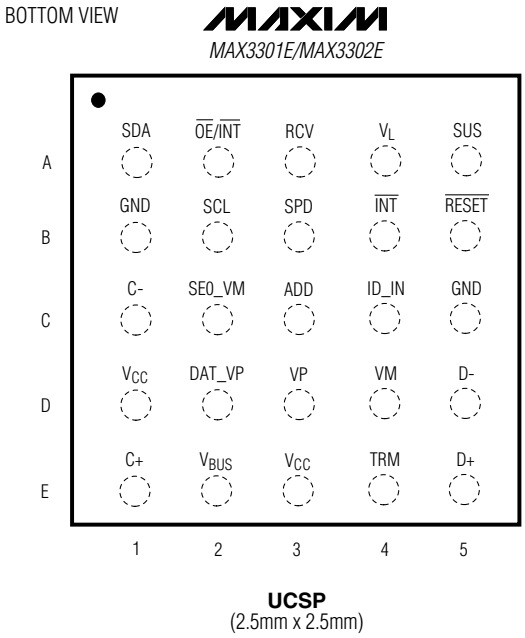
Chip Information

PROCESS: BiCMOS

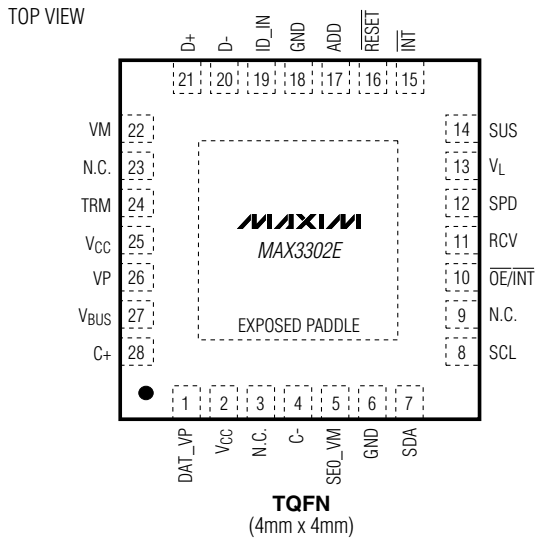
Pin Configurations



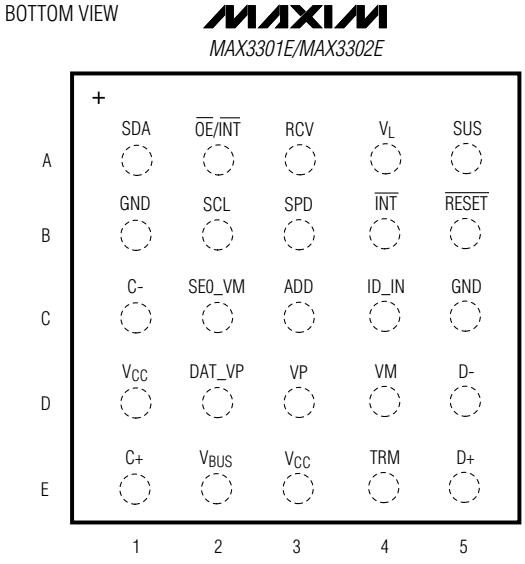
TQFN
(5mm x 5mm)



UCSP
(2.5mm x 2.5mm)

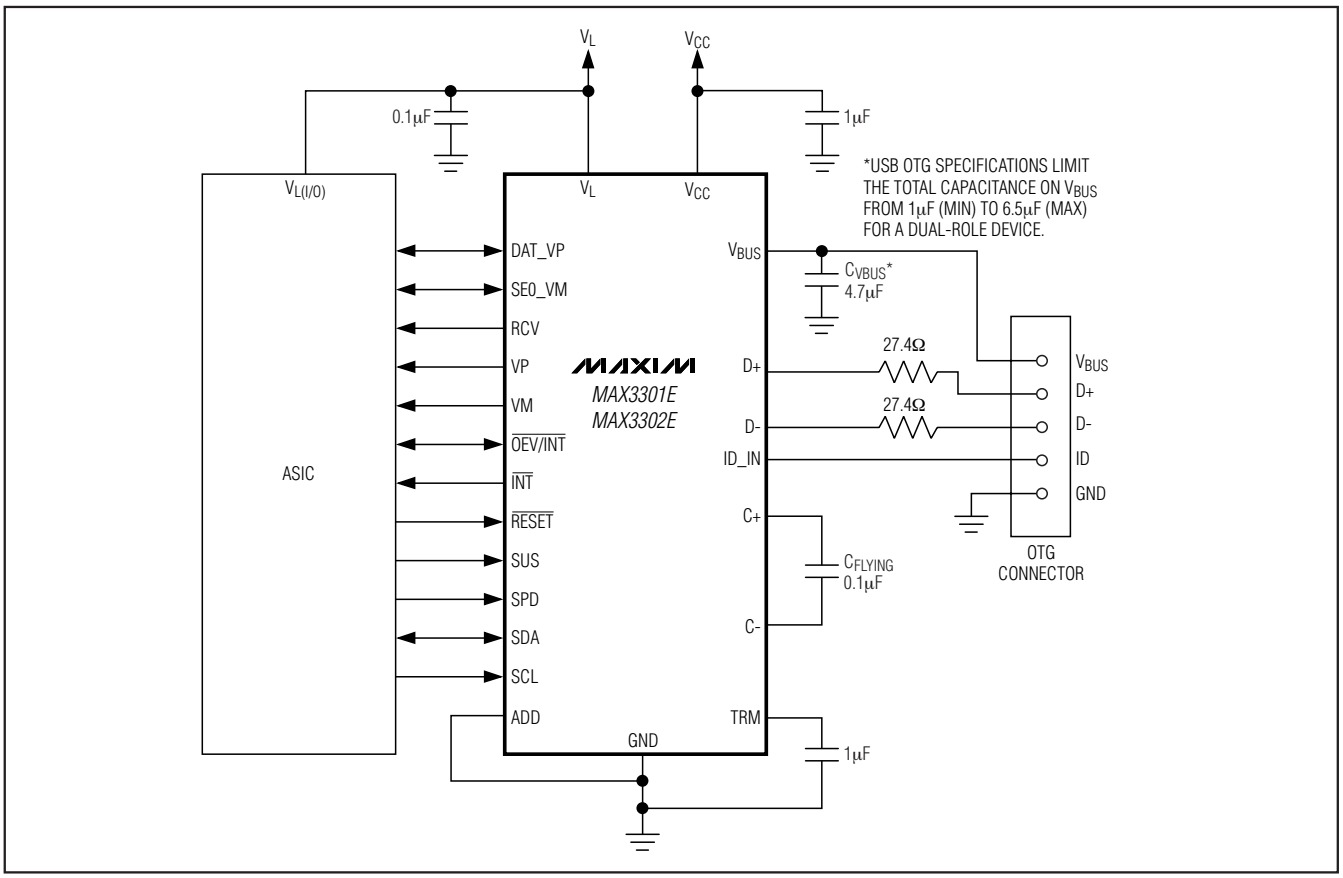


TQFN
(4mm x 4mm)



WLP PACKAGE
(2.54mm x 2.54mm)

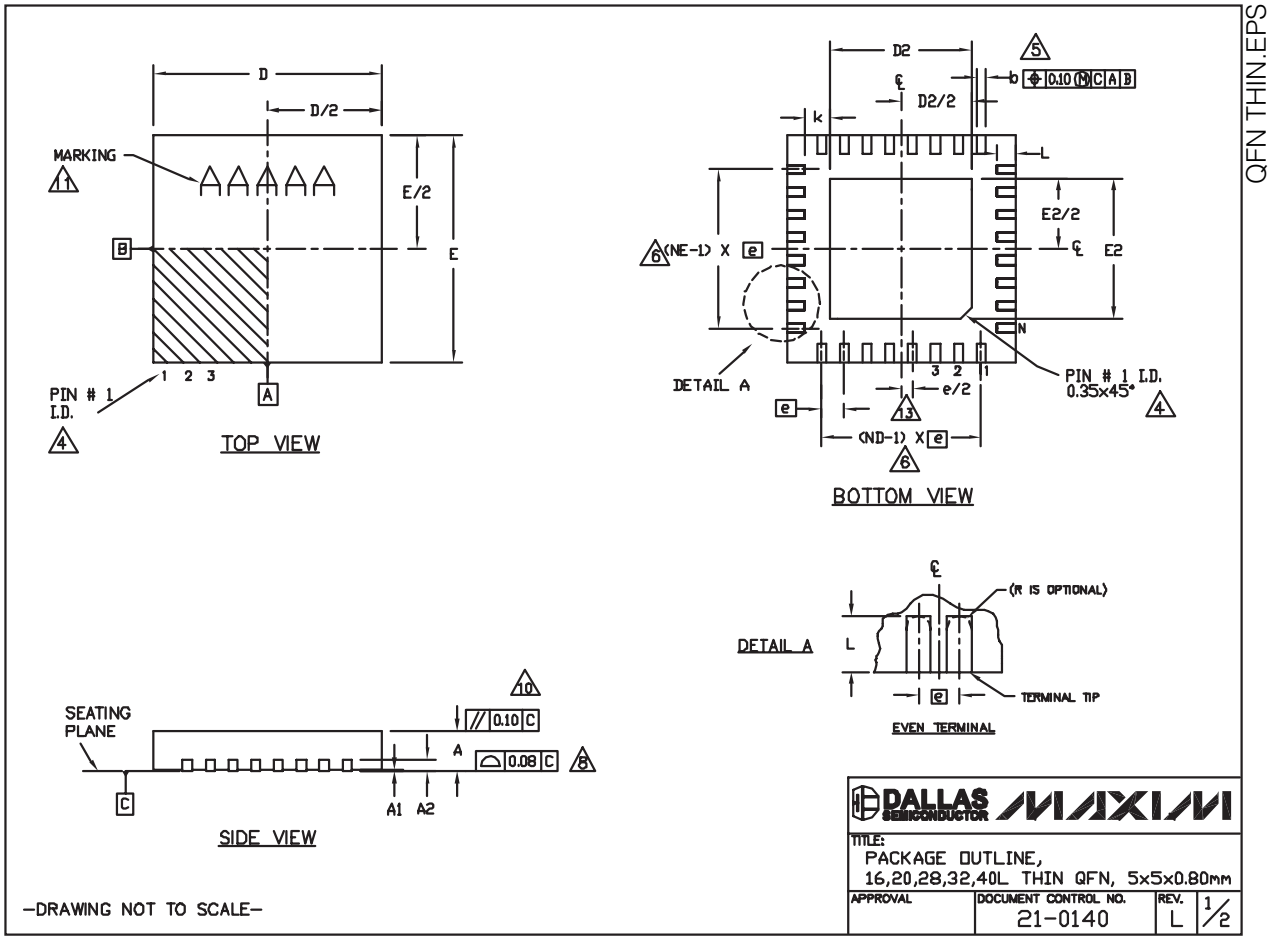
Typical Operating Circuit



USB On-the-Go Transceivers and Charge Pumps

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

—DRAWING NOT TO SCALE—

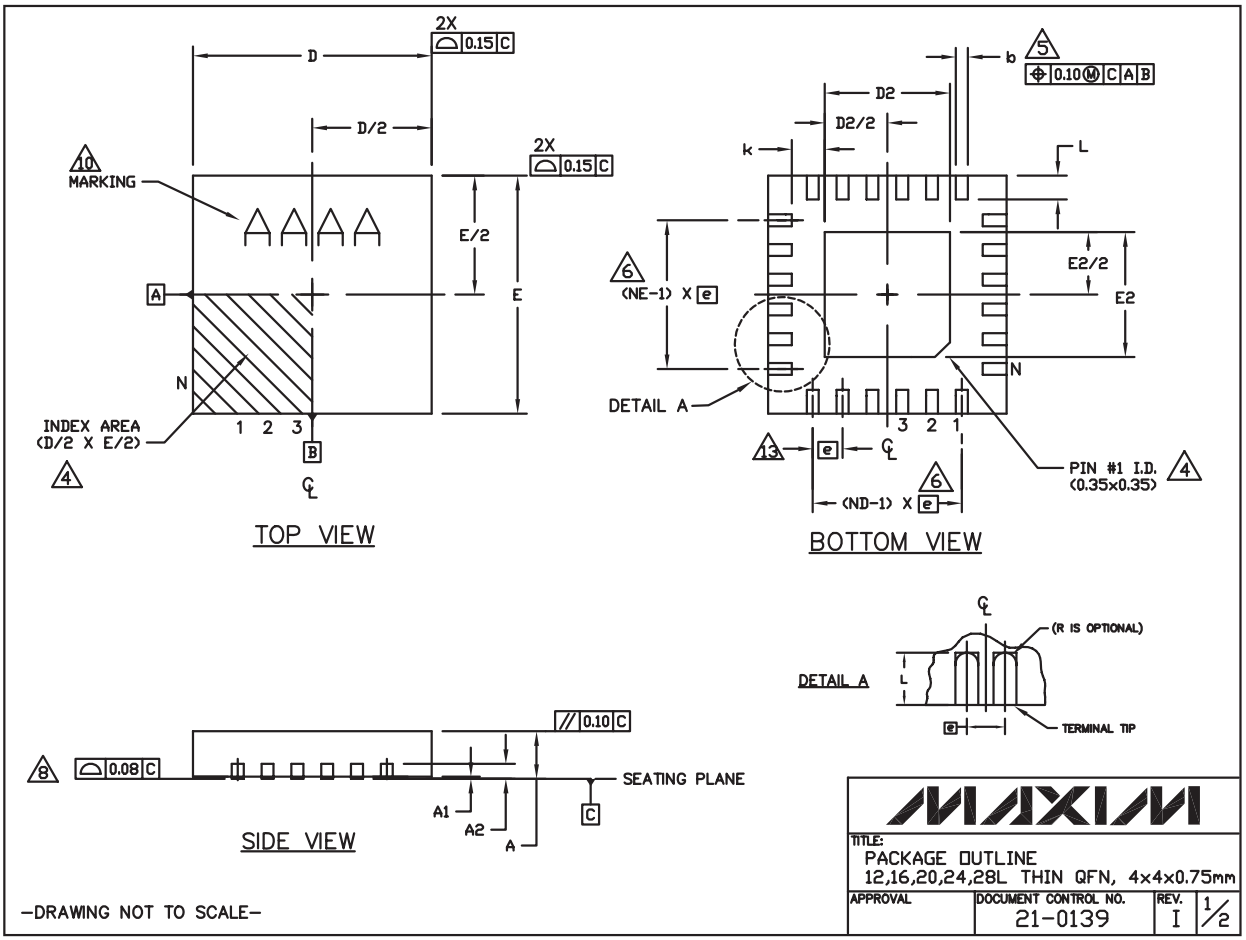
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	L	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

MAXIM

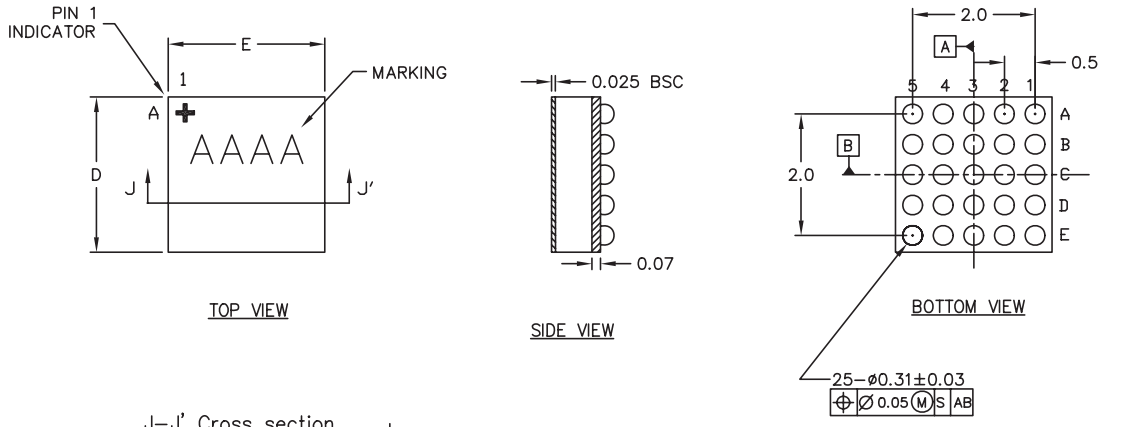
TITLE:
PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	I	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

25L WLP.EPS



PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W252A2+1	2.47	2.60	2.47	2.60	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.

-DRAWING NOT TO SCALE-

MAXIM

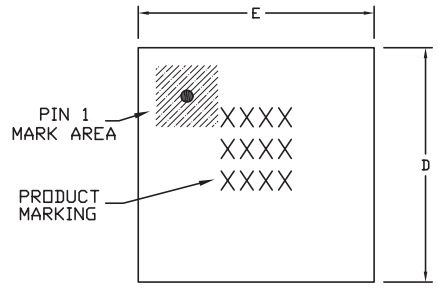
TITLE:
PACKAGE OUTLINE
25L WLP PKG. 0.5mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0191	A	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

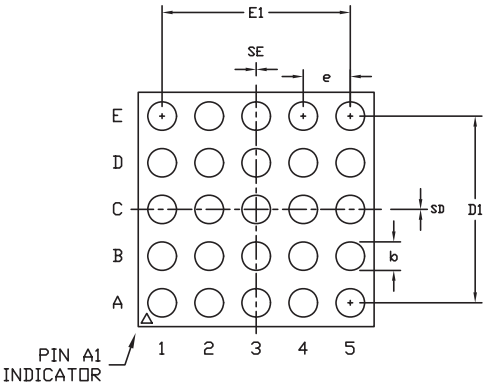
25L, UCSP.EPS



TOP VIEW

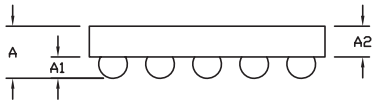
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D	2.54±0.08
D1	2.00 BASIC
E	2.54±0.08
E1	2.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	DEPOPULATED SOLDER BALLS
B25-1	NONE
B25-2	D2, D3, D4
B25-3	B2, B3, B4
B25-4	B3, C2, C3, C4, D3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 5x5 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0096	H	1/1

USB On-the-Go Transceivers and Charge Pumps

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	0	Initial release	—
1	10/04	Correction	—
2	1/06	Release of 3302E	—
3	10/07	Addition of new packaging	1, 2, 4, 9, 10, 30, 36, 37

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