19-1941; Rev 1; 3/06

±15kV ESD-Protected, Isolated, 3.3V RS-485/RS-422 Data Interfaces

General Description

The MAX3480EA/MAX3480EB are electrically isolated RS-485/RS-422 data-communications interfaces. The RS-485/RS-422 I/O pins are protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. Transceivers, optocouplers, and a transformer are all included in one low-cost, 28-pin PDIP package. A single +3.3V supply on the logic side powers both sides of the interface.

The MAX3480EB features reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 160kbps. The MAX3480EA's driver slew rate is not limited, allowing transmission rates up to 2.5Mbps.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX3480EA/MAX3480EB are guaranteed to withstand 1260V_{RMS} (1min) or 1520V_{RMS} (1s). Their isolated inputs and outputs meet RS-485/RS-422 specifications.

Applications

Isolated RS-485/RS-422 Data Interface
Transceivers for EMI-Sensitive Applications
Industrial-Control Local Area Networks
Automatic Test Equipment
HVAC/Building Control Networks
Telecom

Ordering Information

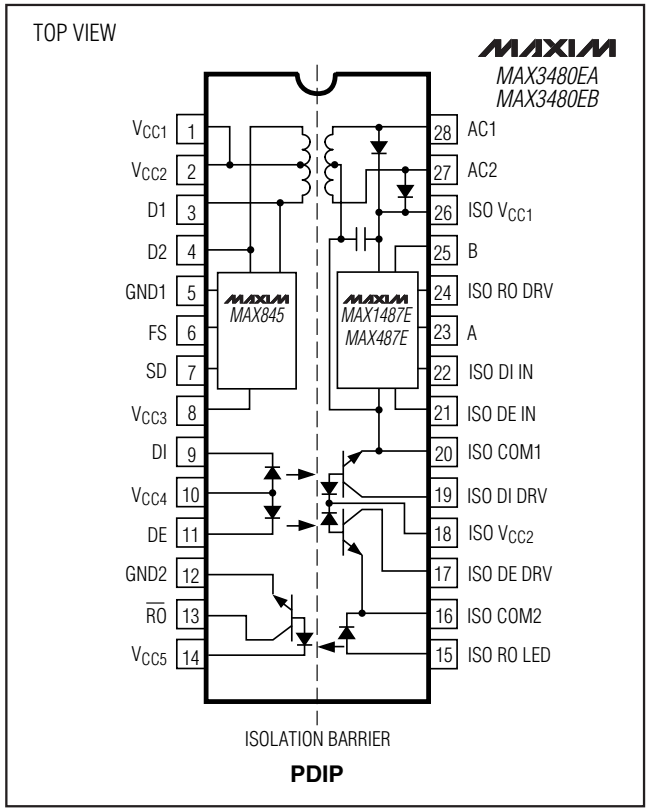
PART	TEMP RANGE	PIN-PACKAGE*	DATA RATE (kbps)	PKG CODE
MAX3480EACPI	0°C to +70°C	28 PDIP	2500	P28M-1
MAX3480EAEPI	-40°C to +85°C	28 PDIP	2500	P28M-1
MAX3480EBCPI	0°C to +70°C	28 PDIP	250	P28M-1
MAX3480EBEPI	-40°C to +85°C	28 PDIP	250	P28M-1

**See the Reliability section at end of data sheet.*

Features

- ♦ **Isolated Data Interface Guaranteed to 1260V_{RMS} (1min)**
- ♦ **±15kV ESD Protection for I/O Pins**
- ♦ **Slew-Rate-Limited Data Transmission (160kbps for MAX3480EB)**
- ♦ **High-Speed, Isolated, 2.5Mbps RS-485 Interface (MAX3480EA)**
- ♦ **Single +3.3V Supply**
- ♦ **Current Limiting and Thermal Shutdown for Driver Overload Protection**
- ♦ **Standard 28-Pin PDIP Package**
- ♦ **Allows Up to 128 Transceivers on the Bus**

Pin Configuration



PDIP

±15kV ESD-Protected, Isolated, 3.3V RS-485/RS-422 Data Interfaces

ABSOLUTE MAXIMUM RATINGS

With Respect to GND
- Supply Voltage (V_{CC1}, V_{CC2}, V_{CC4}, V_{CC5}) .....-0.3V to +3.8V
- Supply Voltage (V_{CC3}) .....-0.3V to +7V
- Control Input Voltage (SD, FS) .....-0.3V to (V_{CC3} + 0.3V)
- Receiver Output Voltage (RO).....-0.3V to (V_{CC5} + 0.3V)

With Respect to ISO COM
- Control Input Voltage (ISO DE _).....-0.3V to (ISO $V_{CC\_}$ + 0.3V)
- Driver Input Voltage (ISO DI _) .....-0.3V to (ISO $V_{CC\_}$ + 0.3V)
- Receiver Output Voltage (ISO RO _) ..-0.3V to (ISO $V_{CC\_}$ + 0.3V)
- Driver Output Voltage (A, B).....-8V to +12.5V
- Receiver Input Voltage (A, B).....-8V to +12.5V

LED Forward Current (DI, DE, ISO RO LED) 50mA
Continuous Power Dissipation (T_A = +70°C)
- 28-Pin PDIP (derate 9.09mW/°C above +70°C).....727mW

Operating Temperature Ranges
- MAX3480E_CPI.....0°C to +70°C
- MAX3480E_EPI.....-40°C to +85°C

Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = +3.0V to +3.6V, FS = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Switch Frequency	f_{SWL}	FS = 0			60		kHz
	f_{SWH}	FS = V_{CC} or open			900		
Operating Supply Current	I_{CC}	MAX3480EA, DE´ = V_{CC} or open	R_L = ∞		130	250	mA
			R_L = 54Ω		220		
		MAX3480EB, DE´ = V_{CC} or open	R_L = ∞		80	200	
			R_L = 54Ω		180		
Shutdown Supply Current (Note 3)	I_{SHDN}	SD = V_{CC3}			0.2		µA
FS Input Threshold	V_{FSH}	High		2.4			V
	V_{FSL}	Low				0.8	
FS Input Pullup Current	I_{FSL}	FS low				50	µA
FS Input Leakage Current	I_{FSM}	FS high			10		pA
Input High Voltage	V_{IH}	DE´, DI´, Figure 1		V_{CC} - 0.4			V
Input Low Voltage	V_{IL}	DE´, DI´, Figure 1				0.4	V
Isolation Voltage	V_{ISO}	T_A = +25°C, 1min (Note 4)		1260			V_{RMS}
Shutdown Input Threshold	V_{SDH}	High		2.4	1		V
	V_{SDL}	Low			1	0.8	
Isolation Resistance	R_{ISO}	T_A = +25°C, V_{ISO} = ±50VDC		100	10,000		MΩ
Isolation Capacitance	C_{ISO}	f = 1MHz			10		pF
ESD Protection	ESD	A, B, Y, and Z pins, tested at Human Body Model			±15		kV
Differential Driver Output (No Load)	V_{OD1}					8	V
Differential Driver Output	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 3		1.5		5.0	
Change in Magnitude of Driver Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 3	Differential			0.3	V
			Common mode			0.3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = +3.0V to +3.6V, FS = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Driver Common-Mode Output	V_{OC}	R = 27Ω or 50Ω, Figure 4					4	V
Input Current (A, B)	ISO I_{IN}	DE´ = 0, V_{CC} = 0 or +3.6V	MAX3480EA	V_{IN} = +12V			0.25	mA
				V_{IN} = -7V			-0.2	
			MAX3480EB	V_{IN} = +12V			0.25	
				V_{IN} = -7V			-0.2	
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V			48			kΩ
Receiver Differential Threshold	V_{TH}	-7V ≤ V_{CM} ≤ 12V			-0.2		+0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0				70		mV
Receiver Output Low Voltage	V_{OL}	DI´ = V_{CC}					0.4	V
Receiver Output High Current	I_{OH}	V_{OUT} = +3.6V, DI´ = 0					250	µA
Driver Short-Circuit Current	ISO I_{OSD}	-7V ≤ V_O ≤ 12V (Note 5)				100		mA

SWITCHING CHARACTERISTICS—MAX3480EA

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = +3.0V to +3.6V, FS = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output Propagation Delay	t_{PLH}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	275	ns
	t_{PHL}			100	275	
Driver Output Skew	t_{SKEW}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Note 5)		25	100	ns
Driver Rise or Fall Time	t_R, t_F	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		15	50	ns
Driver Enable to Output High	t_{ZH}	Figures 5, 7; C_L = 100pF, S2 closed		0.5	1.8	µs
Driver Enable to Output Low	t_{ZL}	Figures 5, 7; C_L = 100pF, S1 closed		0.5	1.8	µs
Driver Disable Time from High	t_{HZ}	Figures 5, 7; C_L = 15pF, S2 closed		0.6	1.8	µs
Driver Disable Time from Low	t_{LZ}	Figures 5, 7; C_L = 15pF, S1 closed		0.6	1.8	µs
Receiver Input to Output Propagation Delay	t_{PLH}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	225	ns
	t_{PHL}			120	225	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20	100	ns
Maximum Data Rate	f_{MAX}	t_{SKEW}, t_{SKD} ≤ 25% of data period	2.5			Mbps

SWITCHING CHARACTERISTICS—MAX3480EB

(V_{CC} = V_{CC1} = V_{CC2} = V_{CC4} = V_{CC5} = +3.0V to +3.6V, FS = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output Propagation Delay	t_{PLH}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.5	3.0	µs
	t_{PHL}			1.2	3.0	
Driver Output Skew	t_{SKEW}	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		300	1200	ns
Driver Rise or Fall Time	t_R, t_F	Figures 4, 6; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	µs
Driver Enable to Output High	t_{ZH}	Figures 5, 7; C_L = 100pF, S2 closed		1.2	4.5	µs
Driver Enable to Output Low	t_{ZL}	Figures 5, 7; C_L = 100pF, S1 closed		1.0	4.5	µs
Driver Disable Time from Low	t_{LZ}	Figures 5, 7; C_L = 15pF, S1 closed		1.5	4.5	µs
Driver Disable Time from High	t_{HZ}	Figures 5, 7; C_L = 15pF, S2 closed		2.0	4.5	µs
Receiver Input to Output Propagation Delay	t_{PLH}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		0.6	3.0	µs
	t_{PHL}			1.4	3.0	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 4, 8; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		750	1500	ns
Maximum Data Rate	f_{MAX}	t_{SKEW}, t_{SKD} ≤ 25% of data period	160			kbps

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to logic-side ground (GND1, GND2), unless otherwise specified.

Note 2: For DE´ and DI´ pin descriptions, see the *Block Diagram* and the *Typical Application Circuit* (Figure 1 for MAX3480EA/MAX3480EB).

Note 3: Shutdown supply current is the current at V_{CC1} when shutdown is enabled.

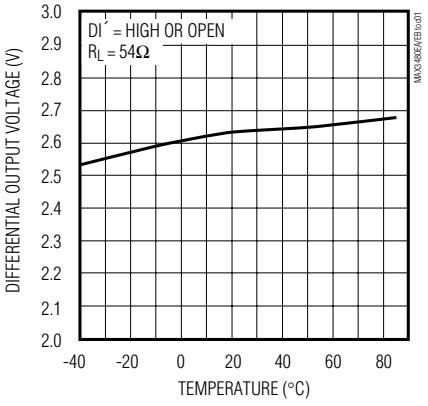
Note 4: Limit guaranteed by applying 1520V_{RMS} for 1s. Test voltage is applied between all pins on one side of the package to all pins on the other side of the package. For example, between pins 1 and 14, and 15 and 28.

Note 5: Applies to peak current. See the *Typical Operating Characteristics* and the *Applications Information* section.

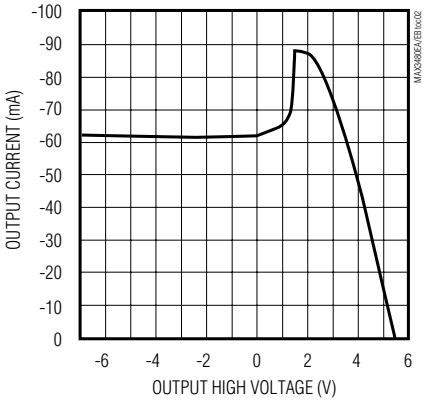
Typical Operating Characteristics

($V_{CC\_}$ = +3.3V, T_A = +25°C, Figure 1, unless otherwise noted.)

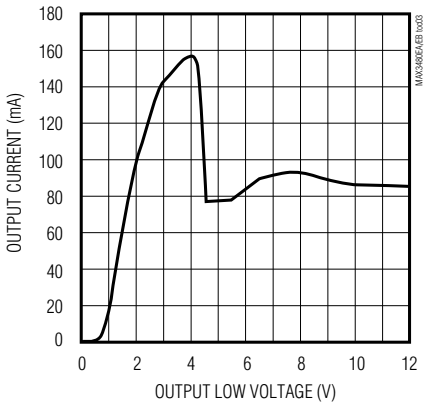
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



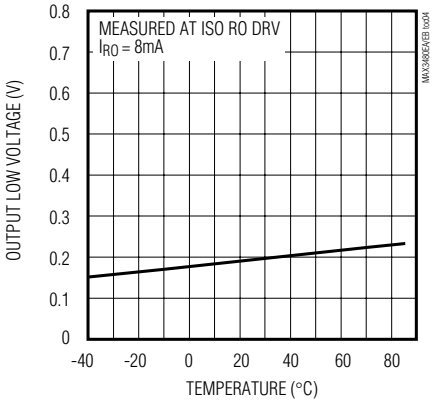
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



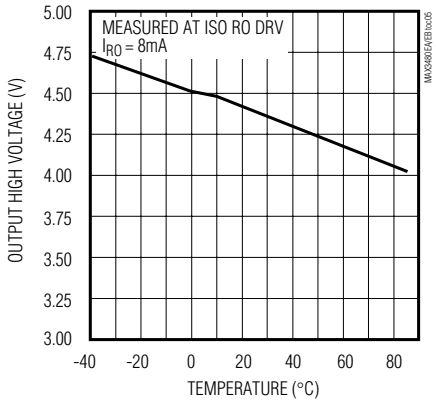
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



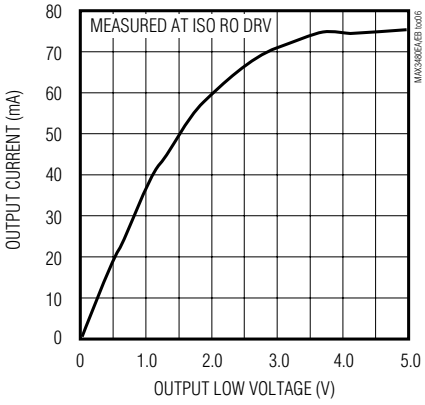
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



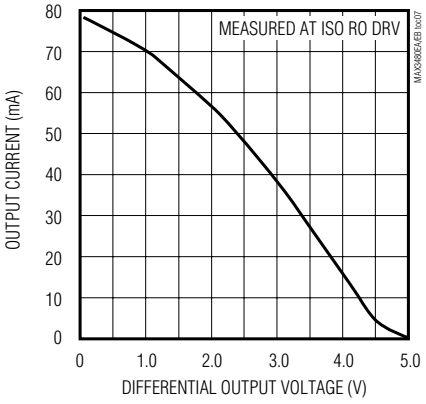
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE

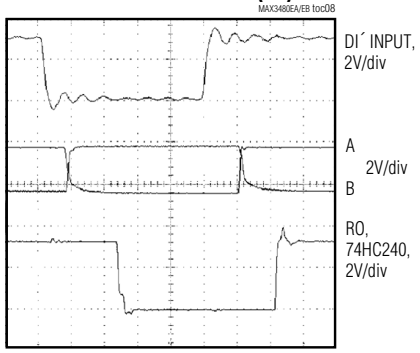


±15kV ESD-Protected, Isolated, 3.3V RS-485/RS-422 Data Interfaces

Typical Operating Characteristics (continued)

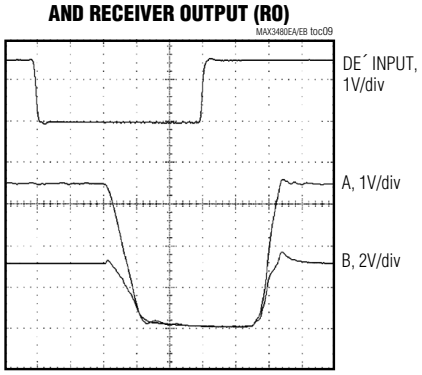
($V_{CC\_}$ = +3.3V, T_A = +25°C, Figure 1, unless otherwise noted.)

MAX3480EA DRIVER INPUT (AB) AND RECEIVER OUTPUT (RO)



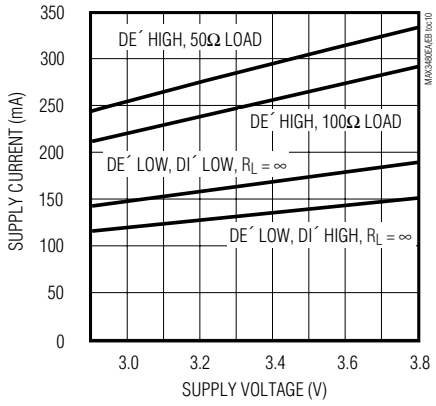
CIRCUIT OF FIGURE 2, TERMINATION: 100Ω

MAX3480EA DRIVER ENABLE (AB) AND RECEIVER OUTPUT (RO)

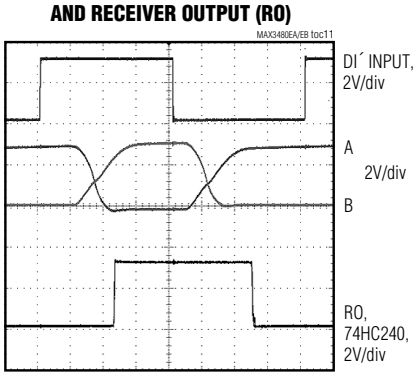


CIRCUIT OF FIGURE 2, TERMINATION: 100Ω

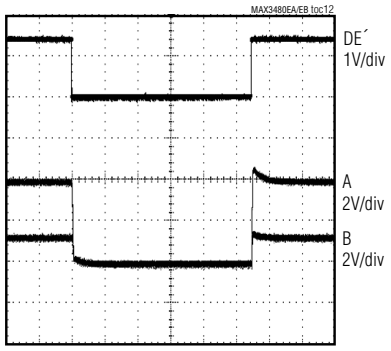
MAX3480EA SUPPLY CURRENT vs. SUPPLY VOLTAGE



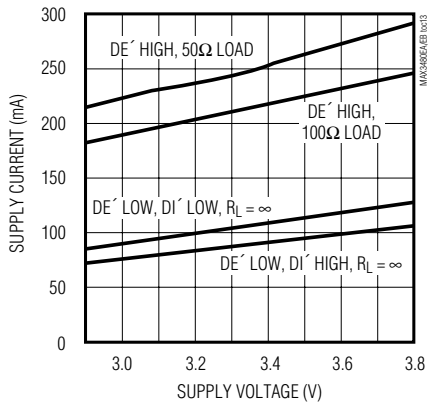
MAX3480EB DRIVER INPUT (AB) AND RECEIVER OUTPUT (RO)



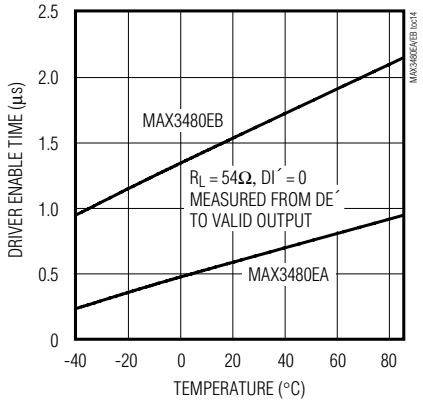
MAX3480EB DRIVER ENABLE (DE´) AND DRIVER OUTPUT (AB)



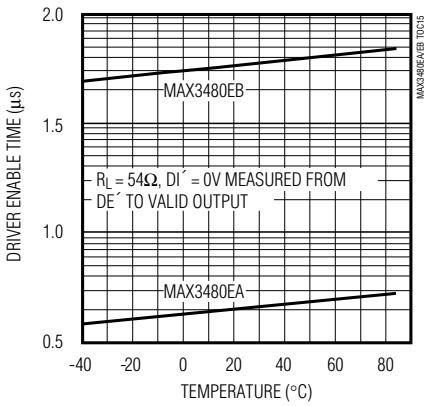
MAX3480EB SUPPLY CURRENT vs. SUPPLY VOLTAGE



DRIVER ENABLE TIME vs. TEMPERATURE



DRIVER ENABLE TIME vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
PINS ON THE NONISOLATED SIDE		
1	V_{CC1}	Logic-Side (Nonisolated Side) +3.3V Supply Voltage Input. Connect to pins 2, 10, and 14.
2	V_{CC2}	Logic-Side (Nonisolated Side) +3.3V Supply Voltage Input. Connect to pins 1, 10, and 14.
3, 4	D1, D2	Boost-Voltage Generator Outputs. See Figures 1 and 2.
5, 12	GND1, GND2	Logic-Side Ground Inputs. Must be connected; not internally connected.
6	FS	Frequency Switch Input. If $V_{FS} = V_{CC}$, switch frequency is high; if FS = 0, switch frequency is low (normal connection).
7	SD	Power-Supply Shutdown Input. Must be connected to logic ground.
8	V_{CC3}	Boosted V+ Voltage Input. Must be connected as shown in Figures 1 and 2.
9	DI	Driver Input. With DE´ high, a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Drives internal LED cathode through R1 (Table 1).
10	V_{CC4}	Logic-Side (Nonisolated Side) +3.3V Supply Voltage Input. Connect to pins 1, 2, and 14.
11	DE	Driver-Enable Input. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Drives internal LED cathode through R2 (Table 1).
13	$\overline{RO}$	Receiver Output. If A > B by 200mV, $\overline{RO}$ is low; if A < B by 200mV, $\overline{RO}$ is high. Open collector; must have pullup (R3) to V_{CC} (Table 1).
14	V_{CC5}	Logic-Side (Nonisolated Side) +3.3V Supply Voltage Input. Connect to pins 1, 2, and 10.

Pin Description (continued)

PIN	NAME	FUNCTION
PINS ON THE ISOLATED RS-485/RS-422 SIDE		
15	ISO RO LED	Isolated Receiver-Output LED Anode (Input). If A > B by 200mV, ISO RO LED is high; if A < B by 200mV, ISO RO LED is low.
16	ISO COM2	Isolated-Supply Common Input. Connect to ISO COM1.
17	ISO DE DRV	Isolated Driver-Enable Drive Input. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the device functions as a line driver. While the driver outputs are high impedance, the device functions as a line receiver. Open collector output; must have pullup (R4 in Figure 1) to ISO VCC and be connected to ISO DE IN for normal operation (Table 1).
18	ISO V_{CC2}	Isolated-Supply Positive Input Voltage. Connect to ISO V_{CC1}.
19	ISO DI DRV	Isolated Driver-Input Drive. With DE´ high, a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Open-collector output; must have pullup (R5 in Figure 1) to ISO VCC and be connected to ISO DI IN for normal operation (Table 1).
20	ISO COM1	Isolated-Supply Common Output. Connect to ISO COM2. If RS-485 wires have a shield, connect ISO COM1 to shield through 100Ω resistor.
21	ISO DE IN	Isolated Driver-Enable Input. Connect to ISO DE DRV for normal operation.
22	ISO DI IN	Isolated Driver Input. Connect to ISO DI DRV for normal operation.
23	A	Noninverting Driver Output and Noninverting Receiver Input
24	ISO RO DRV	Isolated Receiver-Output Drive. Connect to ISO RO LED through R6 (Table 1 and Figure 1).
25	B	Inverting Driver Output and Inverting Receiver Input
26	ISO V_{CC1}	Isolated Supply Positive Output Voltage. Connect to ISO V_{CC2}.
27, 28	AC2, AC1	Internal Connections. Leave these pins unconnected.

Note: *For DE´ and DI´ pin descriptions, see Detailed Block Diagram.*

Detailed Description

The MAX3480EA/MAX3480EB are electrically isolated, RS-485/RS-422 data-communications interface solutions. Transceivers, optocouplers, a power driver, and a transformer are in one standard 28-pin PDIP package. Signals and power are internally transported across the isolation barrier (Figure 1). Power is transferred from the logic side (nonisolated side) to the isolated side of the barrier through a center-tapped transformer. Signals cross the barrier through high-speed optocouplers. A single +3.3V supply on the logic side powers both sides of the interface.

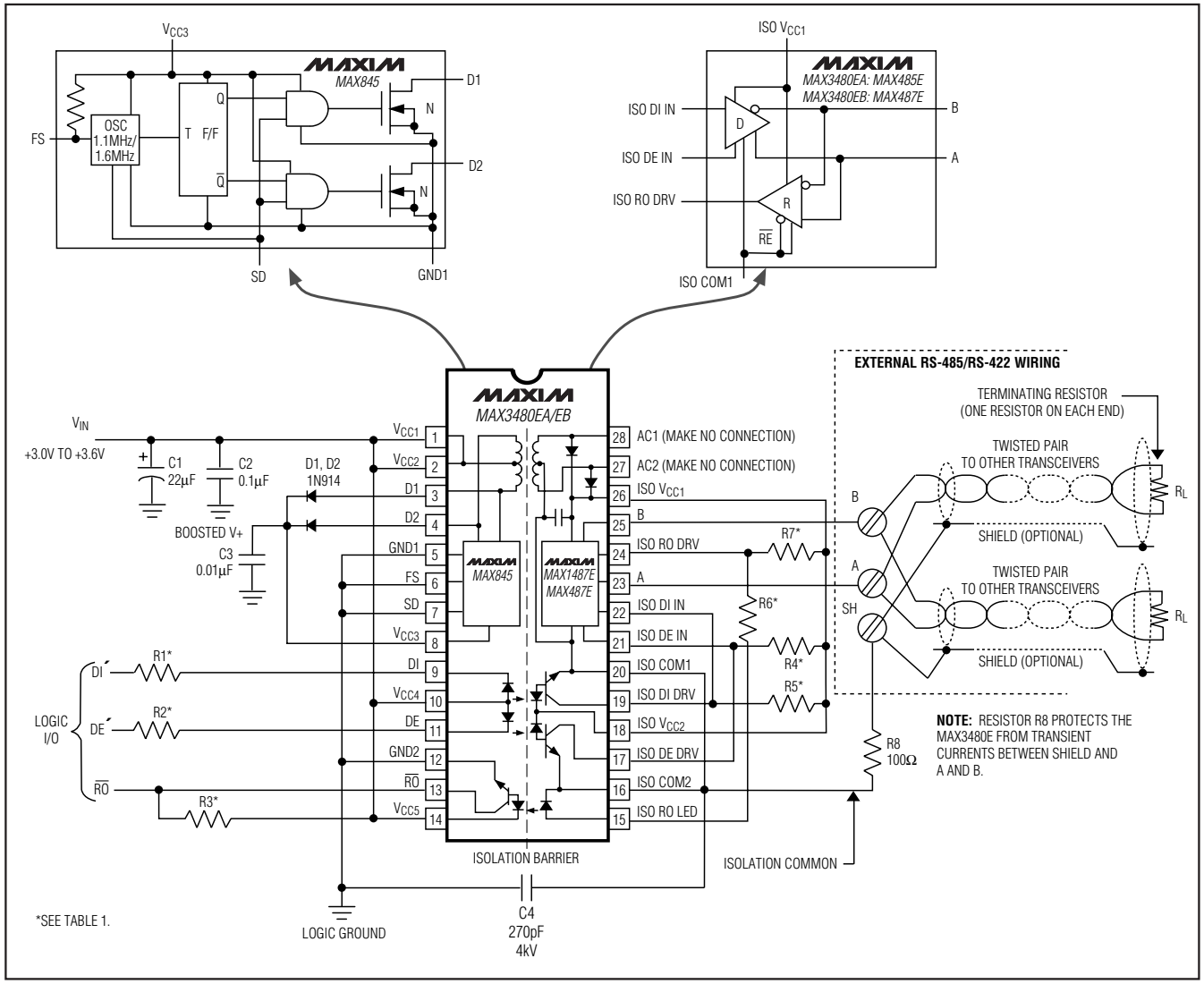


Figure 1. Block Diagram

Table 1. Pullup and LED Drive Resistors

PART	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)	R7 (Ω)
MAX3480EA	100	100	680	3600	1000	200	Open
MAX3480EB	100	100	2000	3600	3600	200	430

±15kV ESD-Protected, Isolated, 3.3V RS-485/RS-422 Data Interfaces

The MAX3480EB features reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission at data rates up to 160kbps. The MAX3480EA's driver slew rates are not limited, allowing transmission rates up to 2.5Mbps.

The frequency-select FS is connected to GND_ in normal operation, which selects a switching frequency of approximately 600kHz. Connect to high for a higher 900kHz switching frequency.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that puts the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The driver outputs are enabled by bringing DE´ high. Driver-enable times are typically 500ns for the MAX3480EA and 1µs for the MAX3480EB. Allow time for the devices to be enabled before sending data. When enabled, driver outputs function as line drivers. Driver outputs are high impedance when DE´ is low. While outputs are high impedance, they function as line receivers.

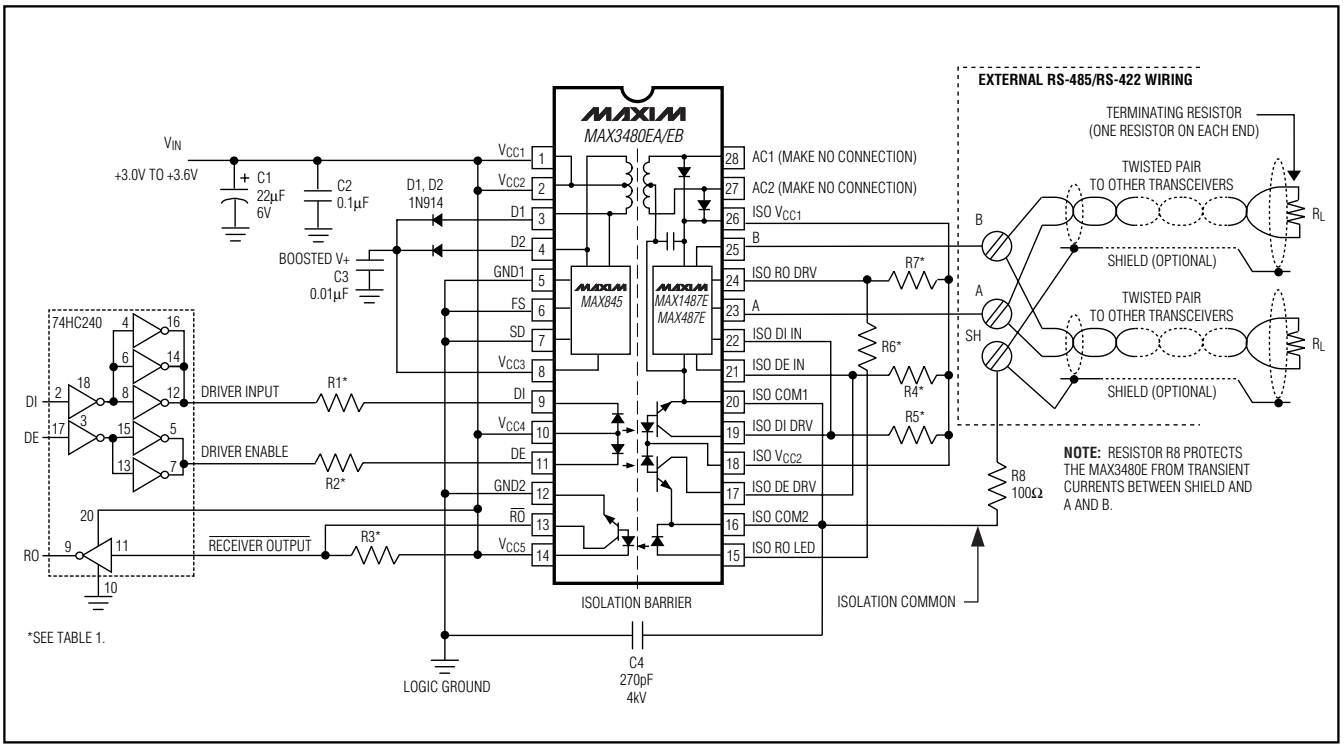


Figure 2. Typical Application Circuit

Test Circuits

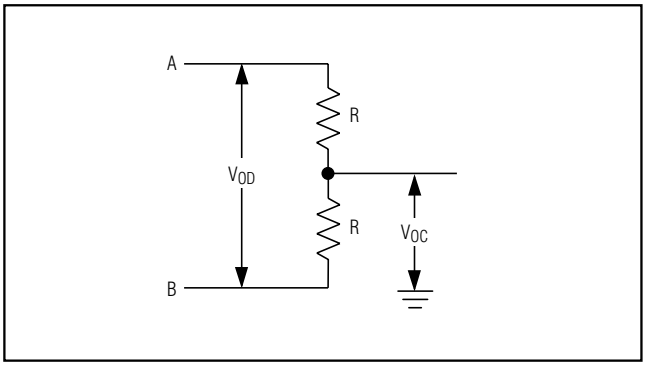


Figure 3. Driver DC Test Load

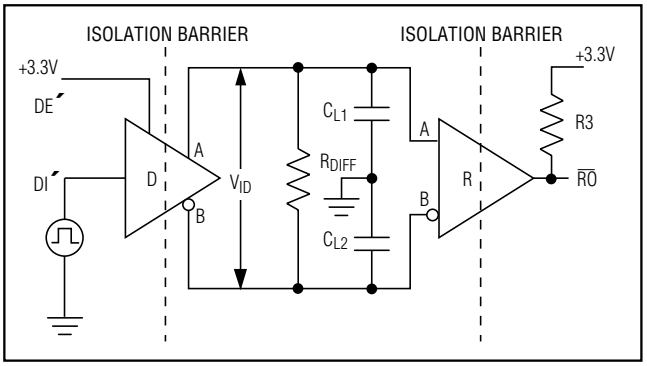


Figure 4. Driver/Receiver Timing Test Circuit

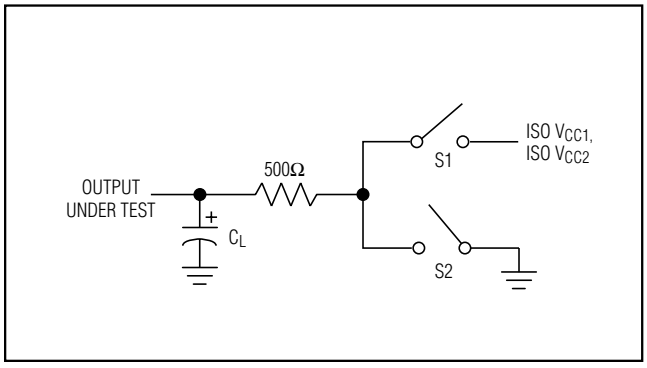


Figure 5. Driver Timing Test Load

Switching Waveforms

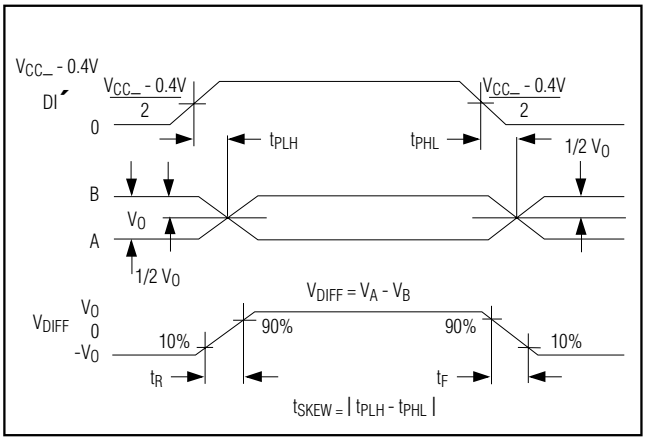


Figure 6. Driver Propagation Delays and Transition Times

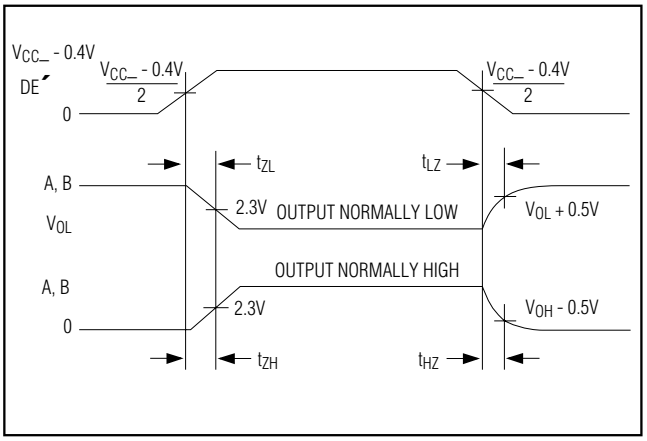


Figure 7. Driver Enable and Disable Times

±15kV ESD-Protected, Isolated, 3.3V RS-485/RS-422 Data Interfaces

Switching Waveforms (continued)

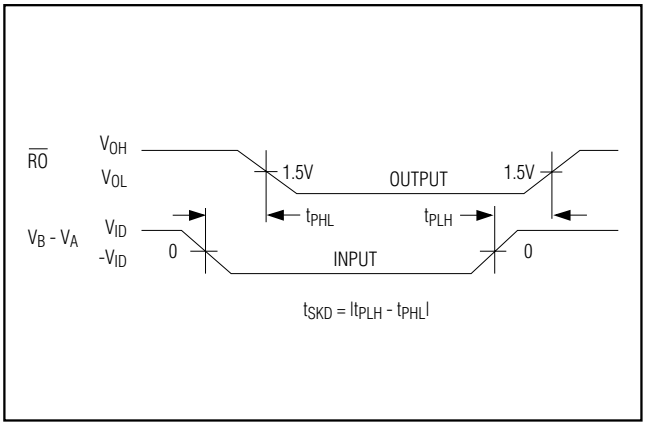


Figure 8. Receiver Propagation Delays

Function Tables

Table 2. Transmitting

INPUTS		OUTPUTS	
DE´	DI´	B	A
1	1	0	1
1	0	1	0
0	X	High Impedance	High Impedance

X = Don't care.

Table 3. Receiving

INPUTS		OUTPUT
DE´	A-B	$\overline{RO}$
0	≥ +0.2V	0
0	≤ -0.2V	1
0	Inputs open	0

The MAX3480EA/MAX3480EB withstand 1260V_{RMS} (1 min) or 1560V_{RMS} (1s). The isolated outputs of these devices meet all RS-485/RS-422 specifications.

Boost Voltage

The MAX3480EA/MAX3480EB require external diodes on the primary of the transformer to develop the boost voltage for the power oscillator. In normal operation, whenever one of the oscillator outputs (D1 and D2) goes low, the other goes to approximately double the supply voltage. Since the circuit is symmetrical, the two outputs can be combined with diodes, filtered, and used to power the oscillator itself.

The diodes on the primary side may be any fast-switching, small-signal diodes, such as the 1N914, 1N4148, or CMPD2838. The nominal value of the primary filter capacitor C3 is 0.01µF.

Driver Output Protection

There are two mechanisms to prevent excessive output current and power dissipation caused by faults or by bus contention. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Resistor R8 (Figures 1 and 2) provides additional protection by current limiting between the shield and the two signal wires. In the event that shielded cable is used and an external voltage or transient is inadvertently applied between the shield and the signal wires, the MAX3480EA/MAX3480EB can be damaged. Although unlikely, this condition can occur during installation.

The MAX3480EA/MAX3480EB provide electrical isolation between logic ground and signal paths; they do not provide isolation from external shields and the signal paths. When in doubt, do not connect the shield. The MAX3480EA/MAX3480EB can be damaged if resistor R8 is shorted out.

Applications Information

The MAX3480EA/MAX3480EB provide extra protection against ESD. The MAX3480EA/MAX3480EB are intended for harsh environments where high-speed communication is important. These devices eliminate the need for transient suppressor diodes or the use of discrete protection components. The standard (non-E) MAX3480A/MAX3480B are recommended for applications where cost is critical.

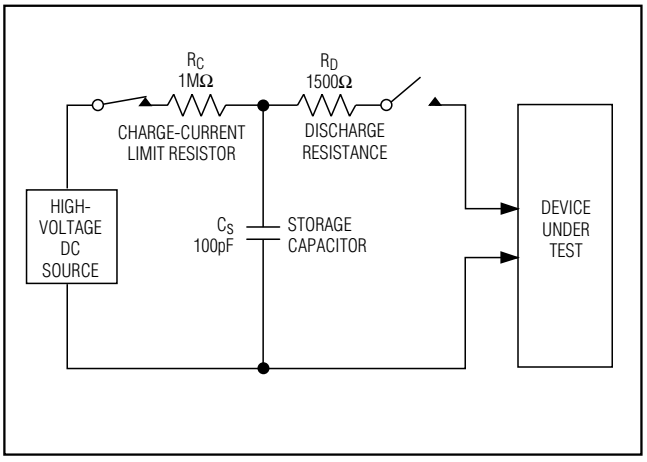


Figure 9. Human Body ESD Test Model

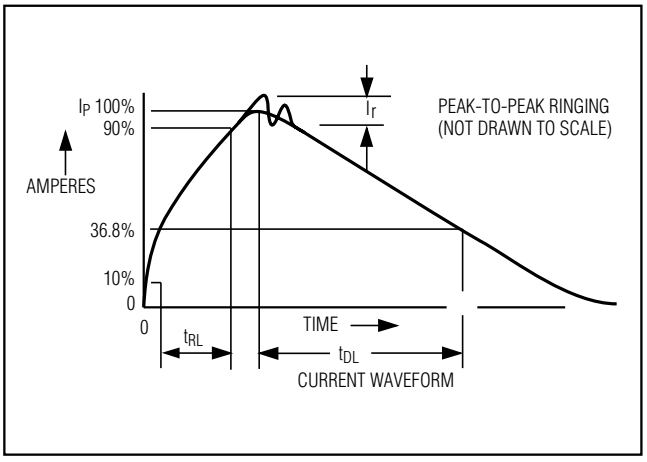


Figure 10. Human Body Model Current Waveform

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and power-down. After an ESD event, Maxim's MAX3480EA/MAX3480EB keep working without latchup. An isolation capacitor of 270pF 4kV should be placed between ISO COM and logic ground for optimal performance against an ESD pulse with respect to logic ground.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to ±15kV using the Human Body Model.

ESD Test Conditions

The +15kV ESD test specifications apply only to the A, B, Y, and Z I/O pins. The test surge may be referenced to either the ISO COM or to the nonisolated GND (this presupposes that a bypass capacitor is installed between V_{CC2} and the nonisolated GND).

Human Body Model

Figure 9 shows the Human Body Model, and Figure 10 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to simulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

The MAX3480EA/MAX3480EB are designed for bidirectional data communications on multipoint bus-transmission lines. Figure 11 shows a typical network application circuit. To minimize reflections, terminate the line at both ends with its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX3480EB is more tolerant of imperfect termination and stubs off the main line.

The MAX3480EA/MAX3480EB are specified and characterized using the resistor values shown in Table 1. Altering the recommended values can degrade performance.

The DI and DE inputs are the cathodes of LEDs whose anodes are connected to V_{CC}. These points are best driven by a +3.3V CMOS-logic gate with a series resistor to limit the current. The resistor values shown in Table 1 are recommended when the 74HC240 gate or equivalent is used. **DI and DE are intended to be**

driven through a series current-limiting resistor. Directly grounding these pins destroys the device.

Reliability

These products contain transformers, optocouplers, and capacitors, in addition to several monolithic ICs and diodes. As such, the reliability expectations more closely represent those of discrete optocouplers, rather than the more robust characteristics of monolithic silicon ICs. The reliability testing programs for these multicomponent devices may be viewed on the Maxim website (www.maxim-ic.com) under Technical Support, Technical Reference, Multichip Products.

Table 4. Maxim's ±15kV ESD-Protected Isolated RS-485 Product Family

PART	NO. OF Tx/Rx	GUARANTEED DATA RATE (Mbps)	FULL/HALF DUPLEX	SLEW-RATE LIMITED	NO. OF Tx/Rx ON BUS	SUPPLY VOLTAGE (V)
MAX1480EA	1/1	2.50	Half	No	128	5.0
MAX1480EC	1/1	0.25	Half	Yes	128	5.0
MAX1490EA	1/1	2.50	Full	No	32	5.0
MAX1490EB	1/1	0.25	Full	Yes	32	5.0
MAX3480EA	1/1	2.50	Half	No	128	3.3
MAX3480EB	1/1	0.25	Half	Yes	128	3.3

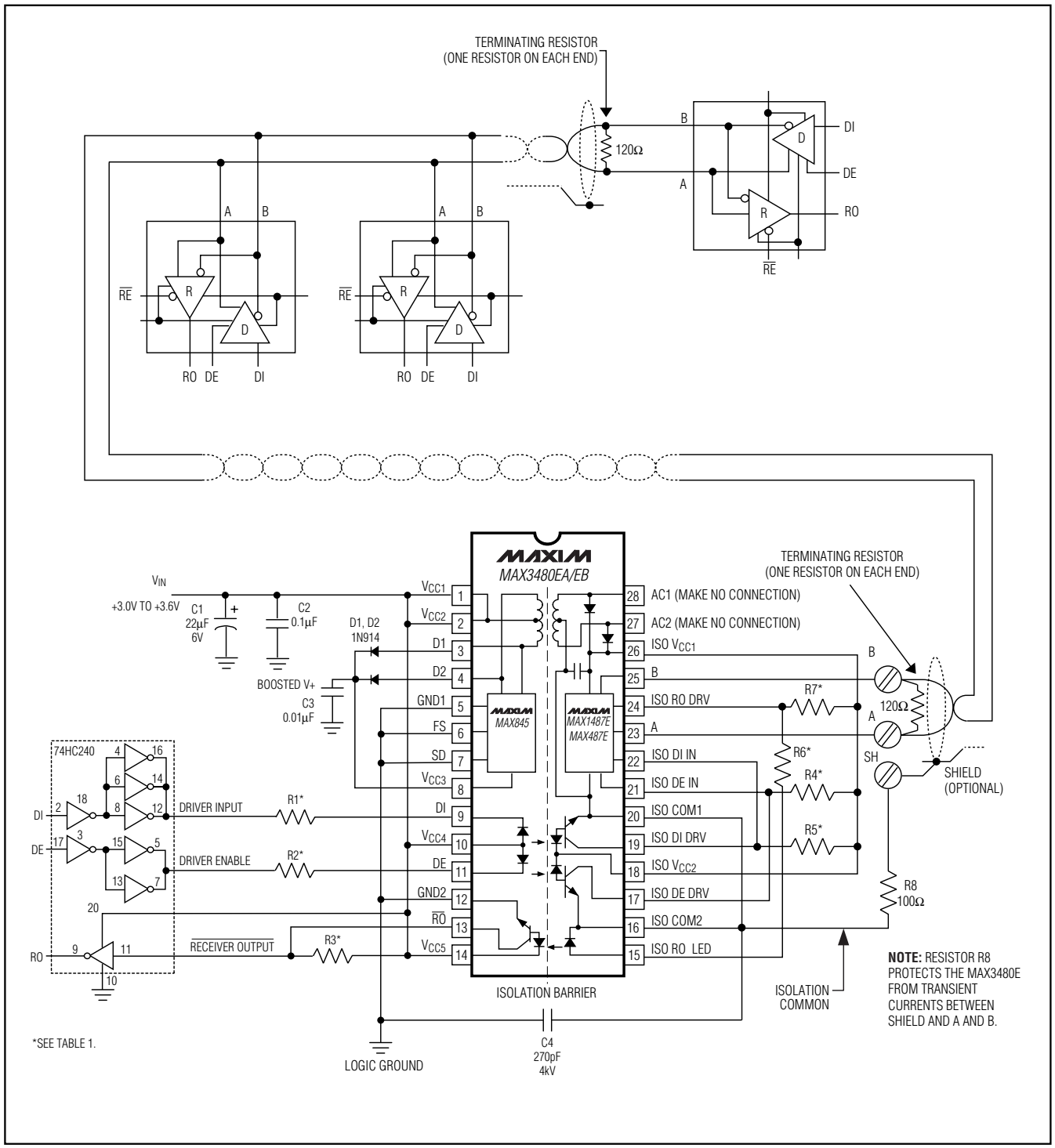


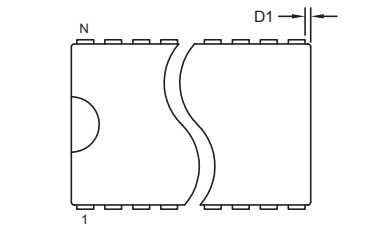
Figure 11. Typical RS-485/RS-422 Network

±15kV ESD-Protected, Isolated, 3.3V RS-485/RS-422 Data Interfaces

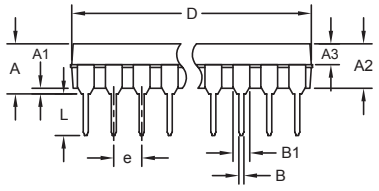
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

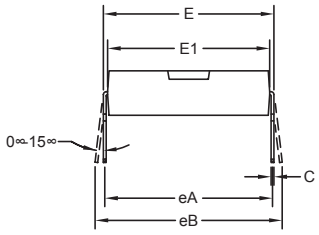
PDIPW.EPS



TOP VIEW



FRONT VIEW



SIDE VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.200	-	5.08
A1	0.015	-	0.39	-
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.21	0.30
D1	0.005	0.009	0.13	0.22
E	0.600	0.625	15.24	15.87
E1	0.525	0.575	13.34	14.61
e	0.100 BSC		2.54 BSC	
eA	0.600 BSC		15.24 BSC	
eB	-	0.700	-	17.78
L	0.120	0.150	3.05	3.81

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS011
D	1.230	1.270	31.24	32.26	24	AA
D	1.430	1.470	36.32	37.34	28	AB
D	2.025	2.075	51.44	52.71	40	AC

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MS011.
5. N = NUMBER OF PINS.

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PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .600" PDIP

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