19-4109; Rev 0; 7/08

EVALUATION KIT AVAILABLE

I²C 2-Wire Extender for DDC in DVI, HDMI, and VGA Interfaces

MAX3816A

General Description

The MAX3816A DDC*/I²C extender automatically compensates for excess load capacitance of long DVI™, HDMI™, and VGA cables. A single MAX3816A placed at the display side of the link restores signal integrity bidirectionally for both DDC clock and data over 0 to 60 meters of cable.

The MAX3816A features compensation for cable capacitance with a guaranteed range up to 3000pF, typically beyond 5000pF. The MAX3816A detects state-change assertion by the logical "AND" of the source side and display side. It asserts the new state with a rail-to-rail slew-rate-limited driver capable of meeting I²C rise- and fall-time requirements under the full load of the cable. After assertion of the new state, a holdoff period of 2.5µs prevents a subsequent state change while the cable channel settles.

Under full load at 100kbps, the MAX3816A consumes 25mW, excluding pullup resistors. It is available in a 16-pin TSSOP package and operates from 0°C to +70°C.

Applications

Front-Projector DVI/HDMI Inputs

High-Definition Televisions, Displays, and Computer Monitors

DVI/HDMI Cable-Extender Modules and Active Cable Assemblies

Features

- **DDC or I²C Cable Extension Up to 60 Meters at 100kbps for Both Clock and Data Channels**
- **Single-Sided Solution Requires Only One MAX3816A at the Display Side**
- **Compensates for Cable Capacitance, 0 to 3000pF Guaranteed (8x I²C Specification), or Beyond 5000pF Typical**
- **Parallel and Serial Operating Modes**
- **Prevents Ringing Due to Reflections by Terminating Transmission Line Impedance After Transitions**
- **Use with MAX3815 TMDS® Equalizer to Form a Complete Digital Video Extension Solution**
- **3.0V to 5.5V Power Supply**
- **Optional Voltage Translation Between 5V Cable DDC and 3.3V Display DDC Levels**

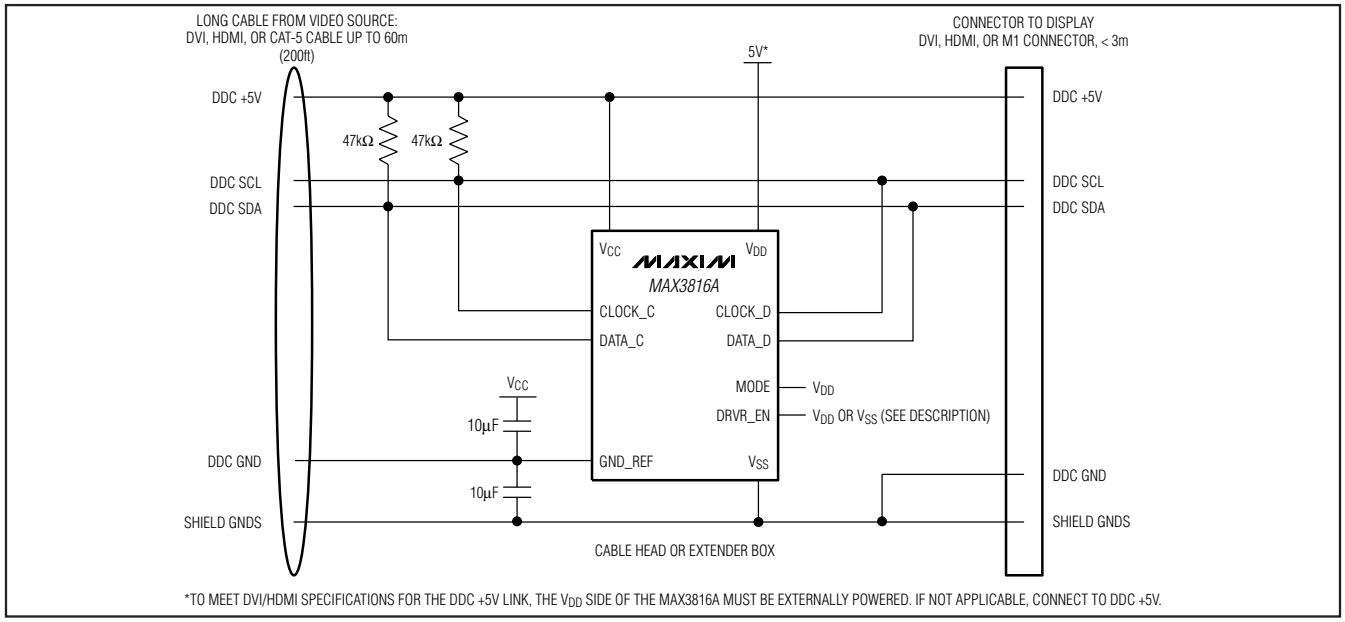
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3816ACUE+	0°C to +70°C	16 TSSOP

+Denotes a lead-free/RoHS-compliant package.

Pin Configuration appears at end of data sheet.

Typical Application Circuit (Parallel Mode)



**DDC (Display Data Channel) is part of the VESA Standard.*
TMDS is a registered trademark of Silicon Image, Inc.

DVI is a trademark of Digital Display Working Group.
HDMI is a trademark of HDMI Licensing, LLC.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range (relative to V_{SS}) at V_{DD}, V_{CC}, CLOCK_D, DATA_D, CLOCK_C, DATA_C, DRVR_EN, MODE .....-0.5V to +6.0V
Continuous Power Dissipation (T_A = +70°C) (derate 11.1mW/°C above +70°C).....889mW
Voltage Range (relative to V_{SS}) at GND_REF .....-0.5V to +0.5V
Operating Junction Temperature (T_J) Range....-55°C to +150°C
Storage Ambient Temperature (T_S) Range .....-40°C to +150°C
Electrostatic Discharge (ESD) Human Body Model.....> ±3kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, V_{DD} = +3.0V to +5.5V, T_A = 0°C to +70°C. Typical values are at T_A = +25°C, V_{CC} = +5.0V, V_{DD} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{CC} or V_{DD}	See the *Applications Information* section (Note 1)		3.0		5.5	V
Supply Current	I_{CC}	V_{CC} = 5.5V, V_{DD} = 5.5V, 100kbps, 60pF load on cable, 10pF load on display, current into V_{CC} pin			1.3	3.0	mA
	I_{DD}	V_{CC} = 5.5V, V_{DD} = 5.5V, 100kbps, 60pF load on cable, 10pF load on display, current into V_{DD} pin			4.3	7.0	
Supply Noise Tolerance		DC to 500kHz			100		mV_{P-P}
		DC to 60Hz (series mode)			700		
CLOCK_C, DATA_C, CLOCK_D, DATA_D (Notes 2, 3)							
Output-High Voltage	V_{OH}	Cable side (CLOCK_C, DATA_C)		V_{CC} - 0.1	V_{CC}		V
		Display side (CLOCK_D, DATA_D)		V_{DD} - 0.1	V_{DD}		
Output-Low Voltage	V_{OL}	V_{OL} achieved within 1µs of negative transition (see Figure 1a, State 2)			0.2	0.4	V
	V_{HOLD}	After V_{OL} is achieved, V_{HOLD} is the most positive level allowed if logic level is 0 and no other driver is asserting low on the same node (series mode)	Cable side		15		% of Supply
			Display side		20		
High-to-Low Threshold	V_{TRIGIH}	Threshold used to detect high-to-low transition relative to supply (V_{CC} for cable side, V_{DD} for display side)			75		% of Supply
Low-to-High Threshold	V_{TRIGIL}	Threshold used to detect low-to-high transition relative to supply (V_{CC} for cable side, V_{DD} for display side)	Cable side		12.5		% of Supply
			Display side		17.5		
Output-High-State Current Limit		Output in ramp-up mode for DATA_C		5.0		16.5	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +5.5V, V_{DD} = +3.0V to +5.5V, T_A = 0°C to +70°C. Typical values are at T_A = +25°C, V_{CC} = +5.0V, V_{DD} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time (Note 4)	t_R	3.0V to 3.6V supply		700	1000	ns
		4.5V to 5.5V supply		700		
Fall Time (Note 4)	t_F	3.0V to 3.6V supply		200	300	ns
		4.5V to 5.5V supply		300		
Driver On-Time		Driver asserting high or low		1750		ns
Driver Active Termination		Driver asserting high or low		60		Ω
TRANSITION SENSING						
Level-Sense Filter Delay		Time to transition decision and assert		300		ns
Holdoff Time	$t_{HOLDOFF}$	Data/clock sensing off during this period		2.5		µs
LVTTL/LVCMOS CONTROL INPUTS (DRVR_EN, MODE)						
Input-High Voltage	V_{IH}		2.0			V
Input-Low Voltage	V_{IL}				0.8	V
Input-High Current	I_{IH}	$V_{IH(MIN)} < V_{IN}$	-1		+1	µA
Input-Low Current	I_{IL}	$V_{IN} < V_{IL(MAX)}$	-1		+1	µA

Note 1: While the MAX3816A is operable over the continuous range of 3.0V to 5.5V, the DDC application requires V_{CC} connection to DDC +5V.

Note 2: All levels in the cable side clock and data I/O are referenced to GND_REF, unless otherwise noted.

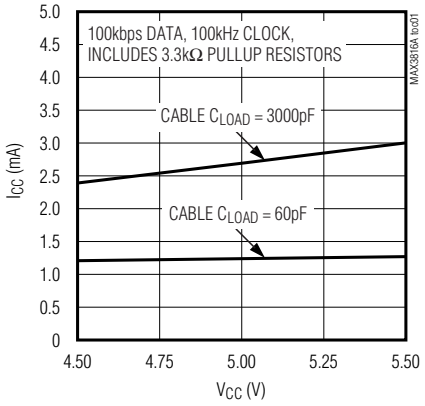
Note 3: All levels in the display side clock and data I/O are referenced to V_{SS}, unless otherwise noted.

Note 4: Rise time measured 30% to 70%; fall time measured 70% to 30%. Load range is 60pF to 3000pF on source side, and 10pF to 400pF on display side. Pullup resistors are chosen to supply I²C maximum of 3mA when asserting low state.

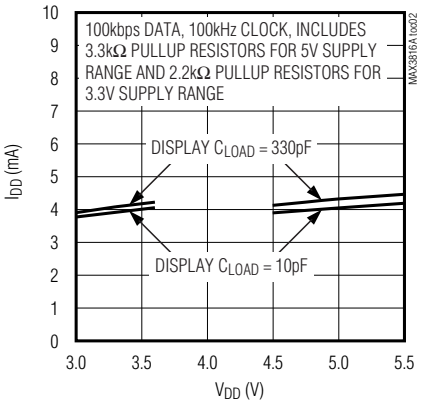
Typical Operating Characteristics

(V_{CC} = +5.0V, V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

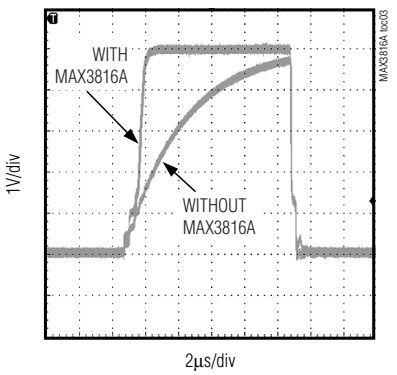
I_{CC} vs. V_{CC}



I_{DD} vs. V_{DD}



CLOCK_C TRANSIENT RESPONSE WITH AND WITHOUT MAX3816A, 30m CABLE LOAD (2350pF)



3.3kΩ PULLUP RESISTOR AT EACH END OF CABLE. PULLDOWN SOURCE: 25Ω CMOS SWITCH SIGNAL INITIATED AND MEASURED AT REMOTE SOURCE.

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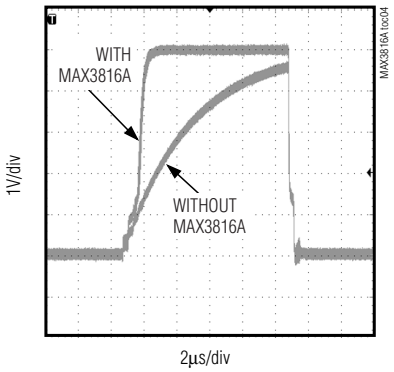
Typical Operating Characteristics (continued)

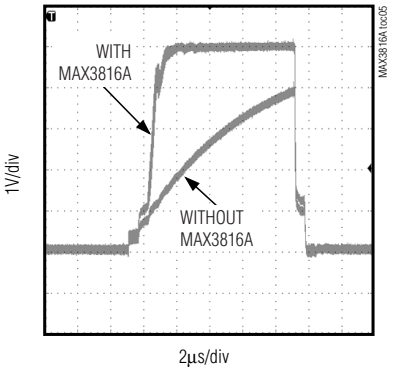
(V_{CC} = +5.0V, V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

CLOCK_C TRANSIENT RESPONSE WITH AND WITHOUT MAX3816A, 30m CABLE LOAD (3100pF)



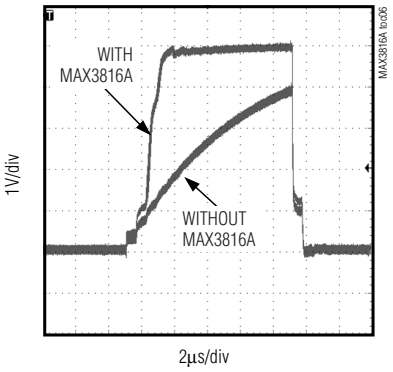
3.3kΩ PULLUP RESISTOR AT EACH END OF CABLE. PULLDOWN SOURCE: 25Ω CMOS SWITCH SIGNAL INITIATED AND MEASURED AT REMOTE SOURCE.

CLOCK_C TRANSIENT RESPONSE WITH AND WITHOUT MAX3816A, 60m CABLE LOAD (4700pF)



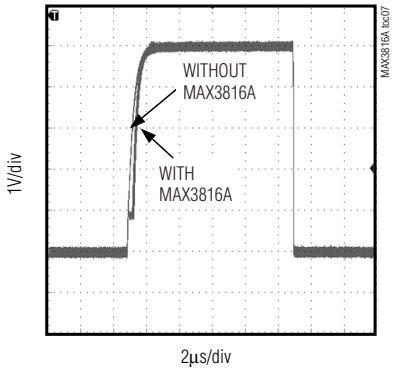
3.3kΩ PULLUP RESISTOR AT EACH END OF CABLE. PULLDOWN SOURCE: 25Ω CMOS SWITCH SIGNAL INITIATED AND MEASURED AT REMOTE SOURCE.

DATA_C TRANSIENT RESPONSE WITH AND WITHOUT MAX3816A, 60m CABLE LOAD (4700pF)



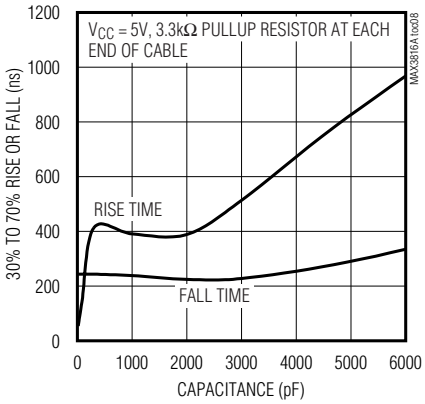
3.3kΩ PULLUP RESISTOR AT EACH END OF CABLE. PULLDOWN SOURCE: 25Ω CMOS SWITCH SIGNAL INITIATED AND MEASURED AT REMOTE SOURCE.

CLOCK_C TRANSIENT RESPONSE WITH AND WITHOUT MAX3816A, 62pF CABLE LOAD



PULLUP RESISTORS: TWO 3.3kΩ IN PARALLEL. PULLDOWN SOURCE: 25Ω CMOS SWITCH.

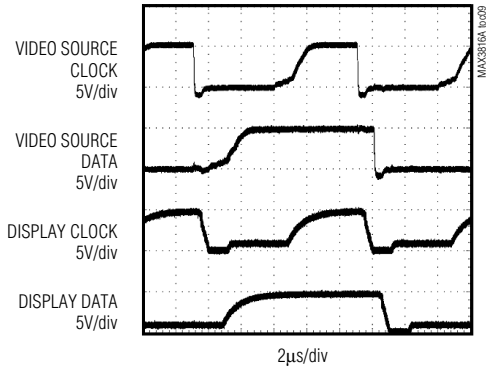
CABLE SIDE TRANSITION TIME vs. CABLE CAPACITANCE



Typical Operating Characteristics (continued)

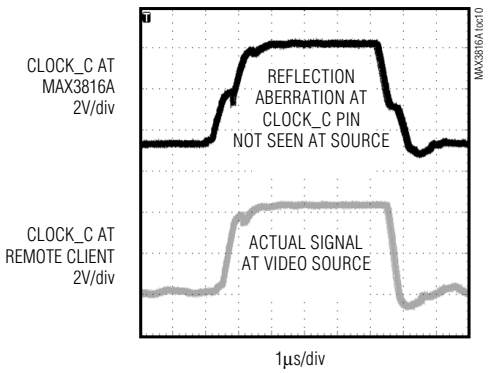
(V_{CC} = +5.0V, V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

SERIES MODE TRANSIENT RESPONSE (3000pF CABLE CAPACITANCE)



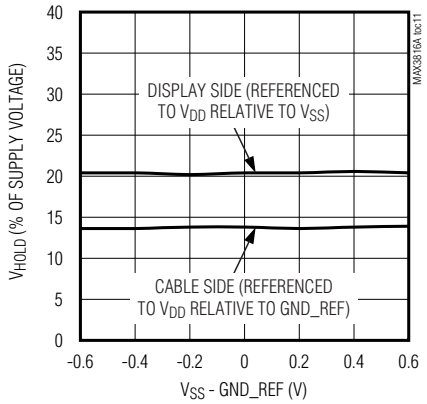
50m CABLE ON SOURCE SIDE, 330pF CAPACITANCE ON DISPLAY SIDE, V_{CC} = 5V, V_{DD} = 5V CLOCK AND DATA INITIATED AT VIDEO SOURCE AND MEASURED AT MAX3816A

REFLECTION ABSORBED BY MAX3816A

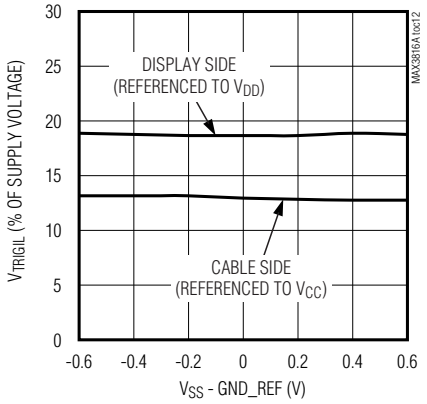


60m CABLE, SIGNAL INITIATED AT DISPLAY SIDE

V_{HOLD} vs. (V_{SS} - GND_REF)



V_{TRIGIL} vs. (V_{SS} - GND_REF)



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Pin Description

PIN	NAME	FUNCTION
1	DRVR_EN	Driver Enable Input, LVTTL/LVCMOS. Set high to enable all data and clock drivers for normal operation. Set low to disable drivers, permitting isolation of cable bus from display bus.
2	V_{CC}	Power Supply for Cable Side. In the DDC application, connect to DDC +5V. Connect 10µF or larger bypass capacitor as shown in Figure 6.
3	CLOCK_C	I²C Cable-Side Clock with Cable Driver, CMOS Input/Output. Connect a 47kΩ pullup resistor to V_{CC}.
4	GND_REF	Cable-Side Ground Return. Connect directly to cable DDC ground wire. The MAX3816A circuitry uses the video source DDC GND as a threshold reference. Also connect 10µF or larger bypass capacitors as shown in Figure 6.
5	DATA_C	I²C Cable-Side Data with Cable Driver, CMOS Input/Output. Connect a 47kΩ pullup resistor to V_{CC}.
6	GND_REF	Cable-Side Ground Return (Alternate). Connected internally to pin 4 above.
7	V_{CC}	Power Supply for Cable Side (Alternate). Connected internally to pin 2 above.
8, 9, 10	DNC	Do Not Connect
11	V_{DD}	Power Supply for Display Side and Core Circuitry. Connect bypass capacitor as shown in Figure 6.
12	DATA_D	I²C Display-Side Data, CMOS Input/Output. Connect a 2.2kΩ pullup resistor to V_{DD} for V_{DD} = 3.3V, or a 3.3kΩ pullup resistor to V_{DD} for V_{DD} = 5V.
13	V_{SS}	Ground for Display Side and Core Circuitry. Connect bypass capacitors as shown in Figure 6.
14	CLOCK_D	I²C Display-Side Clock, CMOS Input/Output. Connect a 2.2kΩ pullup resistor to V_{DD} for V_{DD} = 3.3V, or a 3.3kΩ pullup resistor to V_{DD} for V_{DD} = 5V.
15	V_{SS_T}	Must Be Connected to V_{SS} for Normal Operation
16	MODE	Mode Setting Input, LVTTL/LVCMOS. Force high for parallel mode (normal operation) and force low for serial operation.

Theory of Operation

The MAX3816A has parallel and series modes. The parallel mode is preferred for applications where high tolerance to noncompliant source and sink devices is desired (noncompliant V_{OL} from displays and noncompliant V_{IH} from sources are common). Further, the parallel mode can be operated with other speed-up devices on the same bus, either active (DRVR_EN = HI) or in bypass (DRVR_EN = LO).

Series mode is preferred for applications where high tolerance to ground offset or noise between and source and sink is needed. Series mode also isolates display circuits from transmission line reflections in very long cables, providing full isolation between cable and display buses. For in-display applications, series mode can provide level shifting between the 5V cable DDC and 3.3V display internal DDC.

A single MAX3816A is applied at the display side of the video link to compensate for excessive cable capacitance. The overall operation of the MAX3816A, for either the DATA or CLOCK signal, can be summarized as follows (Figures 1a and 1b).

1) **High state. Drivers off. Level sensing on.**

   If no client device is controlling the “wired-AND” bus from either the source or display side, all device drivers are off and the bus (including the MAX3816A) is waiting in the high state. The pullup resistors on each side are holding the bus up to V_{CC} on the source side and V_{DD} on the display side.

2) **High-to-low transition. Drivers assert low. Level sensing off (Holdoff).**

   A change of state is initiated by any device driver pulling low. Once the signal transitions below 75% of the power supply, the MAX3816A drives both the source and display sides toward ground with a low-impedance driver, level sensing is turned off, and the holdoff timer is started. The source side is pulled down to the level of the V_{SS}. This is accomplished using a low-impedance n-channel buffer that is designed to drive a 1 meter (60pF) to 60

meter (> 3000pF) cable with a controlled slew-rate. Similarly, the display side is pulled down to V_{SS} with a controlled slew rate, open-drain n-channel MOS device. These buffers stay on for 1.75µs.

3) **Low state. Level sensing off (Holdoff).**

   Level sensing remains off until the completion of the holdoff period, which is 2.5µs on both the clock and data channels.

   In series mode, drivers maintain low level (at or below V_{HOLD}). Either the client pulldowns sustain the level below V_{OL}, or the MAX3816A sustains the level at V_{HOLD} if no other driver on the same node is pulling down. This action is in support of the "wired-AND" function across source and display sides.

4) **Low state, drivers off. Level sensing on.**

   After the MAX3816A holdoff time completes, level sensing resumes.

   In series mode, the MAX3816A supports a "wired-AND" connection between source and display sides; returning to the high state is supported only when all client sources turn off. If either the source or display side releases the bus, but not both, a MAX3816A level-sensing buffer senses the transition at V_{TRIGIL}, supporting the existing low state by clamping the voltage to V_{HOLD} and waiting for the remaining side to release the bus.

5) **Low-to-high transition. Drivers on. Level sensing off (Holdoff).**

   A change of state is initiated when no device is holding the bus low on both source and display sides. When both sides exceed their respective V_{TRIGIL} levels, the source side turns on a slew-rate controlled open-drain p-channel device, pulling up to V_{CC} for 1.75µs. Simultaneously, the display side is released and the pullup resistors pull the display-side bus up to V_{DD}, as per normal I²C operation.

6) **High state. Drivers off. Level sensing off (Holdoff).**

   During holdoff, no transitions are sensed. The high state is maintained by external pullup resistors. Upon the end of holdoff, when the cable and display levels are above 85%, the state machine transitions to state (1); otherwise, it waits until levels raise above 85% to transition to state (1). Data, but not clock, has another exit from state (6) to (1) upon data source or data display levels dropping below 60%.

I²C continuous clock applications are not recommended for the MAX3816A. The MAX3816A is optimized for DDC applications with a noncontinuous clock.

Detailed Description

The MAX3816A DDC/I²C 2-wire extender consists of two controllers with level-shifters, cable drivers, display drivers, and level-sensing circuitry (Figure 2).

Controllers and Level Shifters

The MAX3816A functionality is governed by two controllers, one for CLOCK and one for DATA. Bidirectional signaling is fully supported on both CLOCK and DATA. The primary function of the controllers is to receive the state-change information from the source- and display-side level-sense circuitry and support the "wired-AND" function between the two. When the state changes, a holdoff period is timed during which the source and display drivers assert the next state, high or low, and all input sensing is ignored while I/O transients settle (Figure 3). The holdoff period is approximately 2.5µs. The cable transmission-line termination feature is active only during the first 1.75µs of holdoff, sufficiently long enough to absorb roundtrip reflections from a 60m cable.

In series mode, the CLOCK and DATA controllers isolate the source electronics from the display electronics. The cable side of the MAX3816A is referenced to V_{CC} and GND_REF, and the display side is referenced to V_{DD} and V_{SS}. This power scheme provides tolerance to offset and noise between the source and display devices.

Cable Drivers

The low-impedance cable drivers (Figure 10) can charge and discharge at least 3000pF of capacitive cable load within the I²C rise and fall time limits. The drivers each incorporate a slew-rate limiter to control the amount of high-frequency energy transmitted. The cable drivers also provide a back termination impedance of approximately 60Ω to absorb transmission-line reflections returning to the driver. The cable drivers each include a high-state current-limiting feature to clamp the output current to less than 16mA.

After 1.75µs of driver assertion, following a decision to transition, the low-impedance drivers are turned off. Subsequently, when another device asserts a new state, it does not have to work against the low impedance of the MAX3816A.

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Locally, connect a 47kΩ pullup resistor from CLOCK_C and DATA_C to V_{CC}. This assumes that a 1.65kΩ pullup resistor resides at the opposite end of each channel.

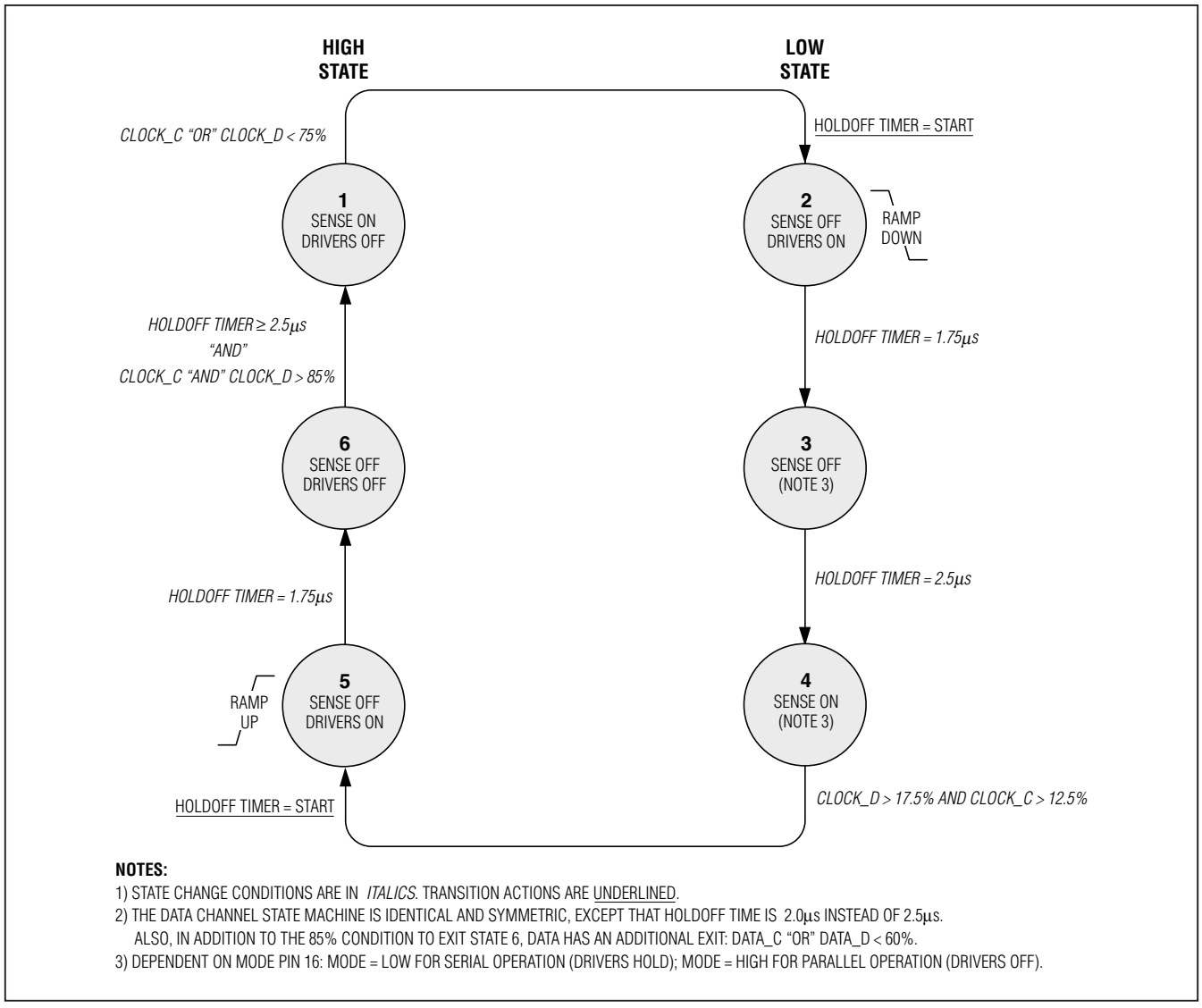
Display Drivers

The display drivers (Figure 11) are typical open-drain pulldown devices capable of discharging up to 400pF of capacitive load within the I²C fall-time limits.

Locally, connect a 2.2kΩ pullup resistor from CLOCK_D and DATA_D to V_{DD} for V_{DD} = 3.3V, or a 3.3kΩ pullup resistor to V_{DD} for V_{DD} = 5V.

Level Sense

The MAX3816A's level-sensing circuitry monitors the incoming data for state transitions. When the CLOCK or DATA signal is high and drops below V_{TRIGIH}, the controller ramps the outputs low. When the DATA and CLOCK are low and both rise above V_{TRIGIL}, referenced to GND_REF on the source side or V_{SS} on the display side, the output drives the level high.



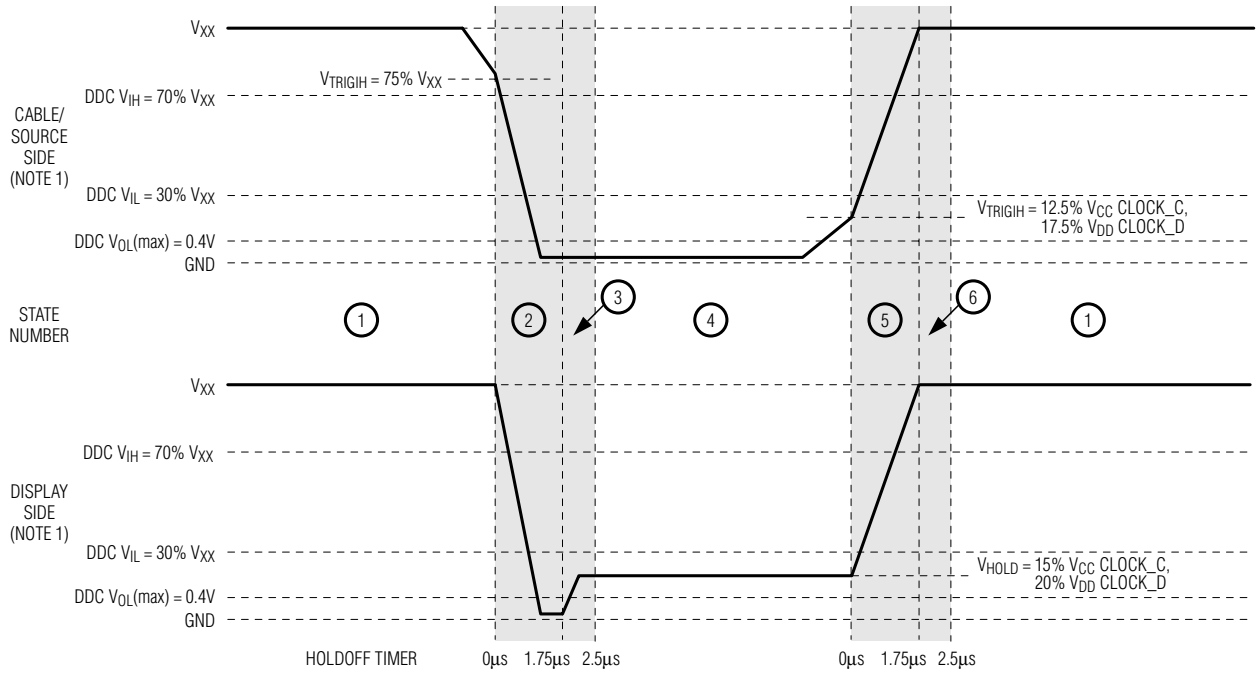
NOTES:

1) STATE CHANGE CONDITIONS ARE IN *ITALICS*. TRANSITION ACTIONS ARE UNDERLINED.

2) THE DATA CHANNEL STATE MACHINE IS IDENTICAL AND SYMMETRIC, EXCEPT THAT HOLDOFF TIME IS 2.0µs INSTEAD OF 2.5µs. ALSO, IN ADDITION TO THE 85% CONDITION TO EXIT STATE 6, DATA HAS AN ADDITIONAL EXIT: DATA_C "OR" DATA_D < 60%.

3) DEPENDENT ON MODE PIN 16: MODE = LOW FOR SERIAL OPERATION (DRIVERS HOLD); MODE = HIGH FOR PARALLEL OPERATION (DRIVERS OFF).

Figure 1a. Clock State Machine Diagram



NOTES:
1) THIS EXAMPLE APPLIES TO TRANSMISSION IN EITHER DIRECTION. SOURCE TO DISPLAY IS SHOWN.
2) V_{XX} IS USED GENERICALLY FOR THE VOLTAGE AT THE V_{CC} OR V_{DD} PINS.

Figure 1b. Signal Waveform Example Showing States

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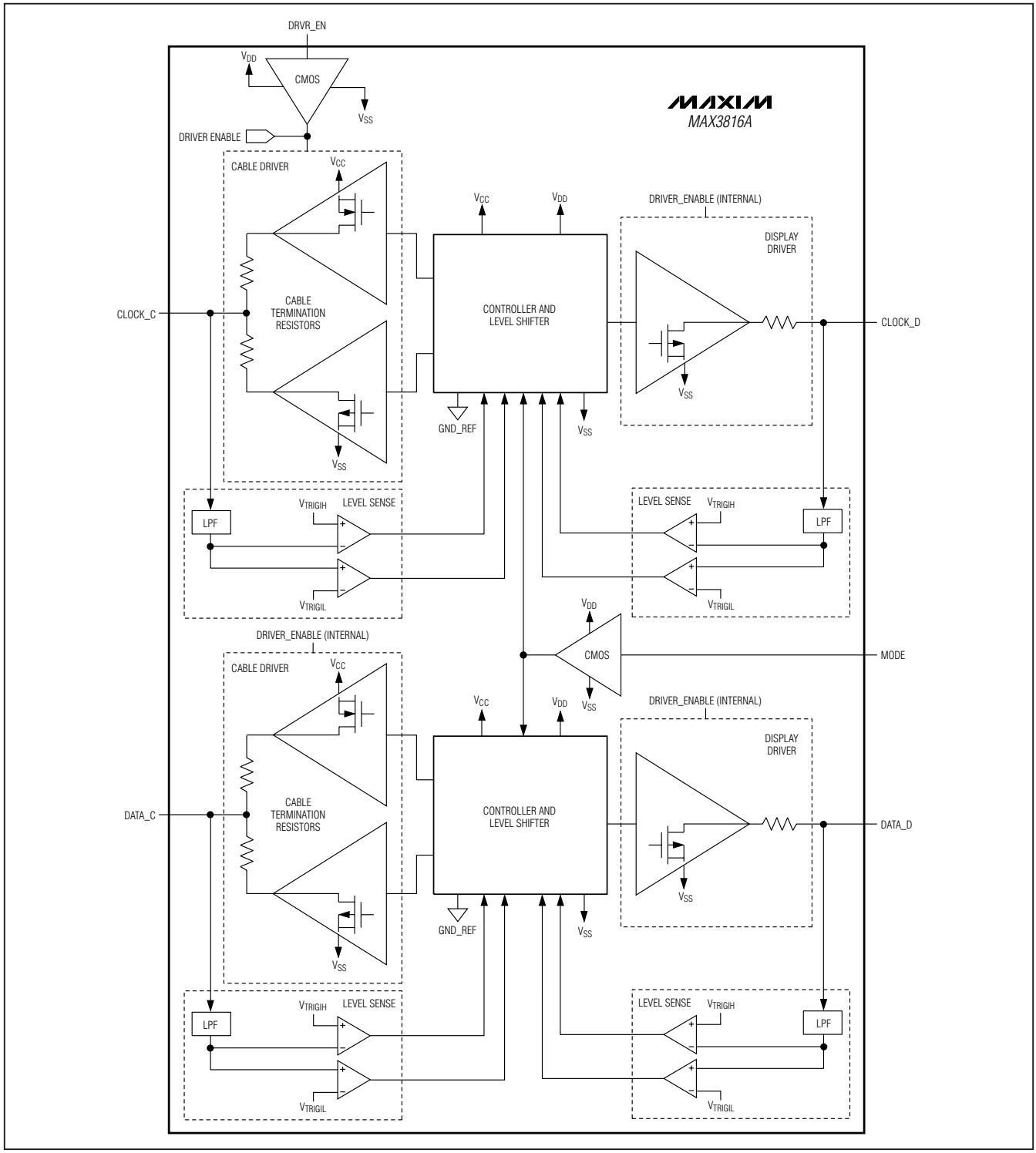


Figure 2. Functional Diagram

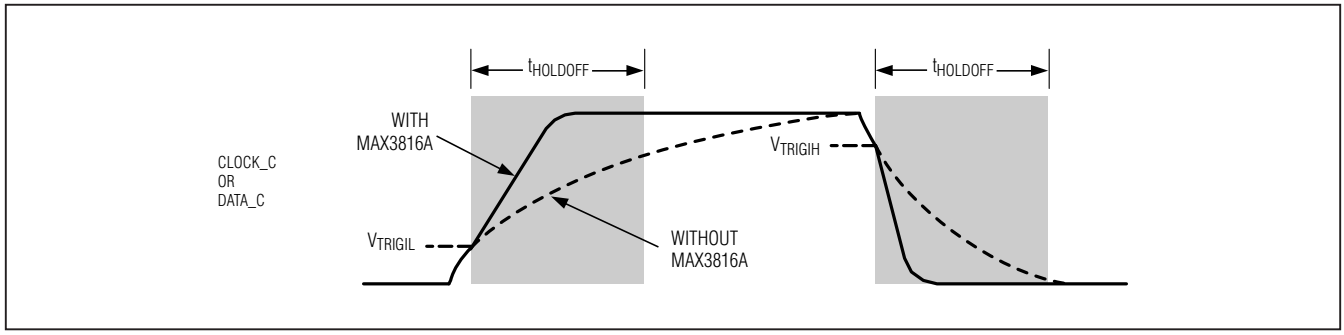


Figure 3. Holdoff Operation

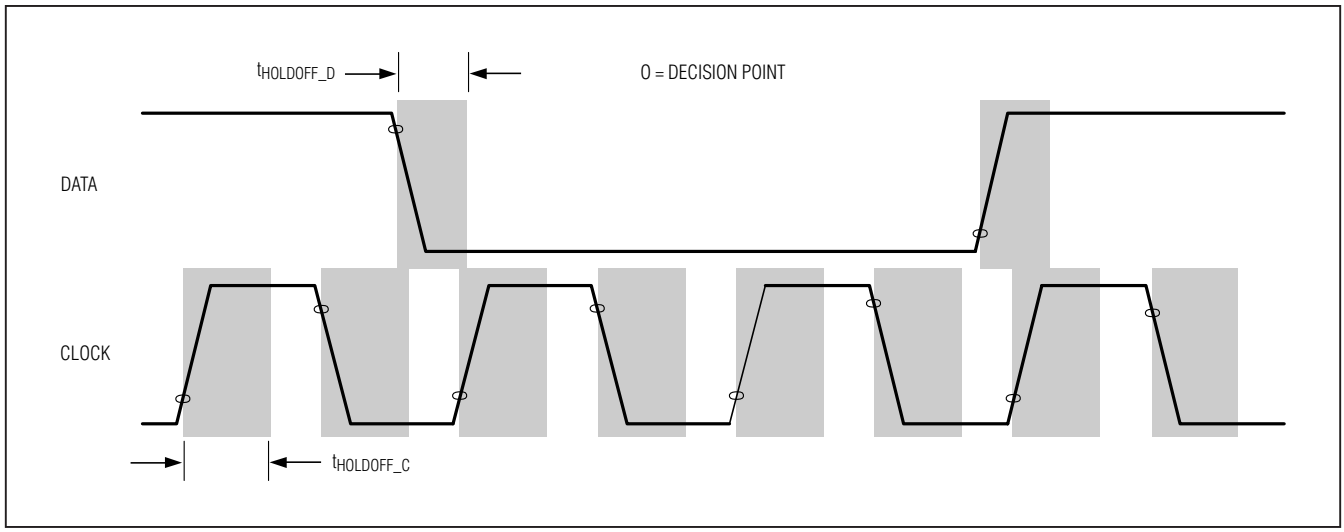


Figure 4. Holdoff with Decision Points Shown

I²C 2-Wire Extender for DDC in DVI, HDMI, and VGA Interfaces

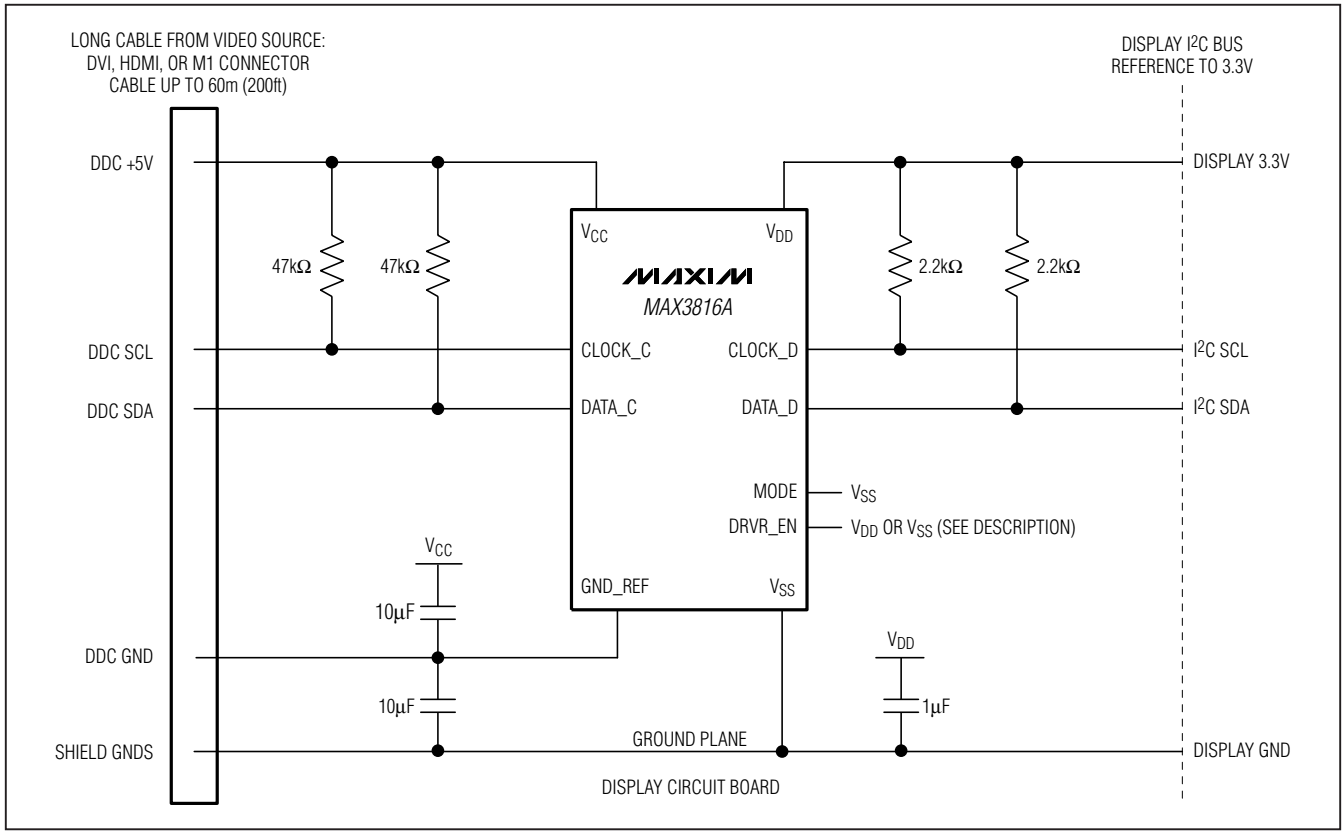


Figure 5. Typical In-Display Application Circuit

Applications Information

Use Single MAX3816A at Display Side

A single MAX3816A is designed to achieve full 100kbps operation over 60m (200ft) of cable.

In-Display Application, Series Mode

When inserted at the front-end of a display, the source side of the MAX3816A should be powered by the source V_{CC} (typically 5V) and ground (GND_REF). The display-side V_{DD} should be powered by the local display supply (typically 3.3V) to level-shift and diminish the effects of supply noise and offset between source and display (Figure 5). Supply decoupling capacitors of at least 10µF should be connected close to the MAX3816A between GND_REF and V_{SS}, as well as between GND_REF and V_{CC}.

MAX3816A In-Display, Series Mode Advantages (See Figure 5)

- Long cable reach.
- The MAX3816A acts as a buffer between source and display. Hence, source reflections are isolated to the source side of the MAX3816A, protecting display circuits from reflections (stair-step waveforms).
- The MAX3816A can be turned off (DRVR_EN asserted low) to isolate source and display buses. The display bus can then operate independently of source-cable loading or malfunctions.
- Multiple MAX3816As can be used in parallel as an input mux to display, with only one “on” at a time.

Consideration

When using the level-shifter feature, as shown, and assuming the display 3.3V supply is off when the display is off, the Display EDID Prom will not be able to communicate to source DDC. If required, the solution is to either place a 5V EDID Prom on the source side of the MAX3816A or derive the 3.3V V_{DD} from the DDC +5V supply.

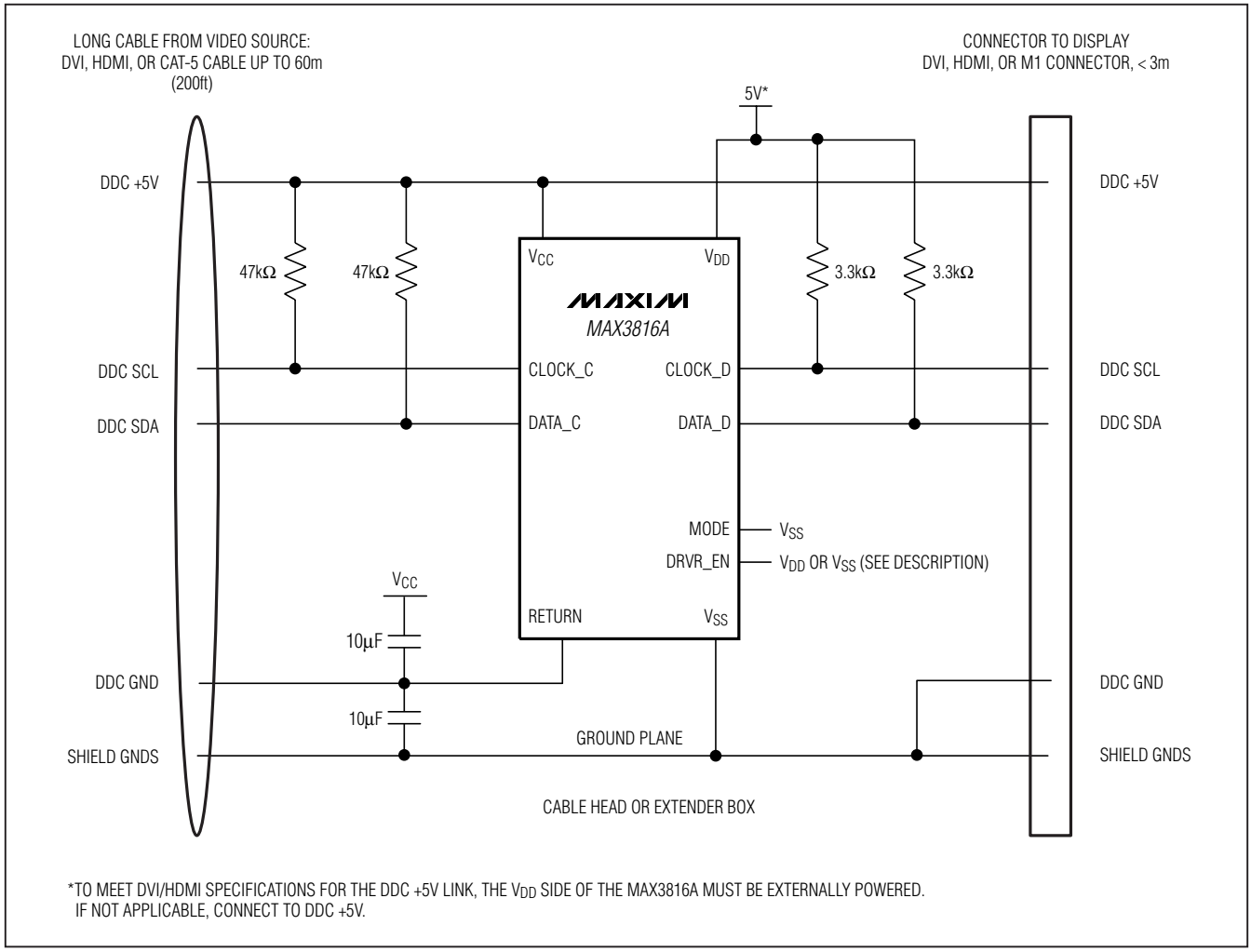


Figure 6. External to Display, In Series

External Box or Cable Assembly Applications

Three implementations external to the display such as external box products or cable assemblies are shown in Figures 6, 7, and 8.

MAX3816A External to Display, In Series Advantages (See Figure 6)

- Long cable reach.
- The MAX3816A acts as a buffer between the source and display. Hence, source reflections are isolated to the source side of the MAX3816A, protecting display circuits from possible double clocking due to stair-step waveforms caused by very long cables with reflections.
- The MAX3816A can be turned off (DRVR_EN asserted low) to isolate source and display buses. The display bus can then operate independently of source-cable loading or malfunctions. Also, multiple MAX3816As can be used in parallel as an input mux to display, with only one "on" at a time.

Consideration

Only one series-connected MAX3816A is allowed on a bus. Two or more series-connected MAX3816A ICs will not function. If multiple MAX3816A ICs are expected, use the parallel applications in Figures 7 and 8.

I²C 2-Wire Extender for DDC in DVI, HDMI, and VGA Interfaces

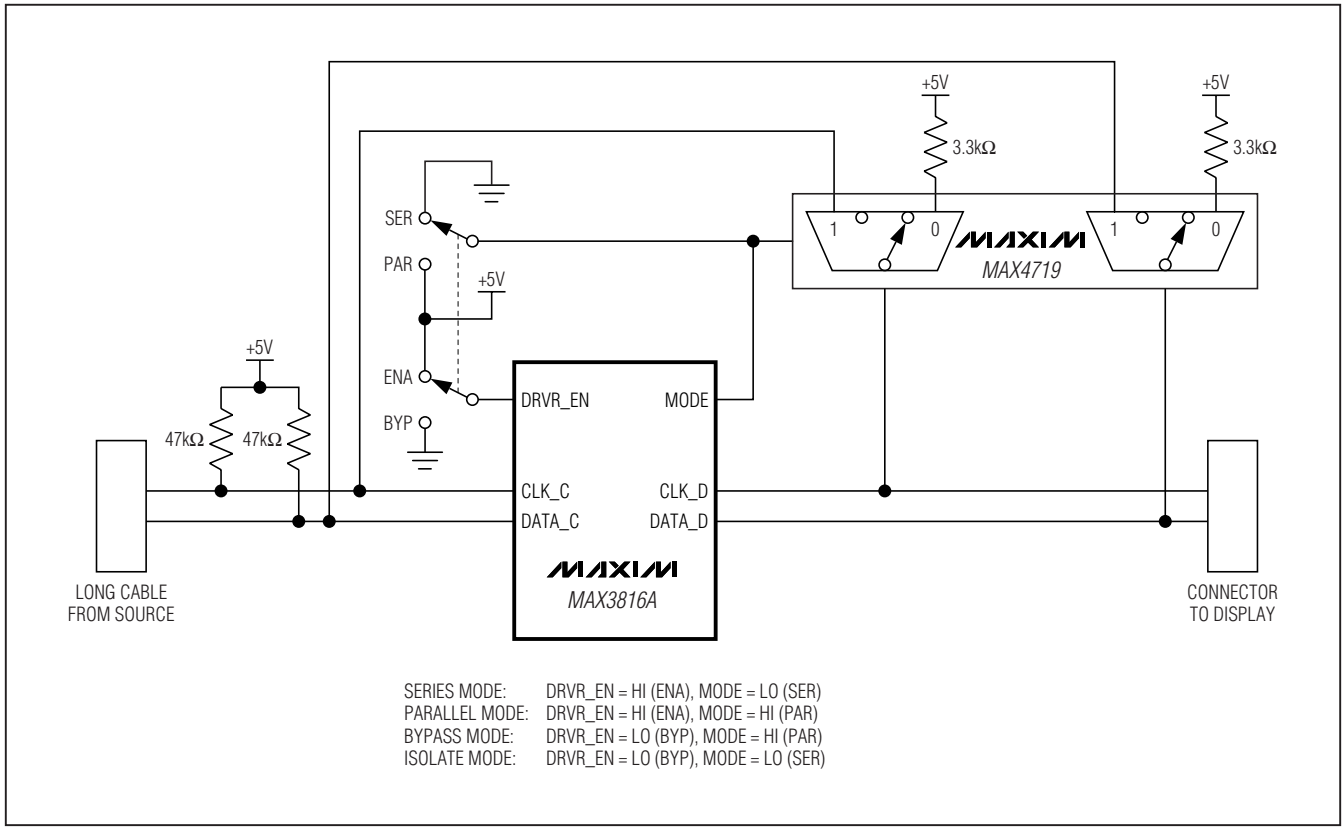


Figure 7. External to Display, Switchable Series and Parallel Mode

MAX3816A External to Display, Switchable Series and Parallel Mode Advantages (See Figure 7)

- Long cable reach.
- In parallel mode, the MAX3816A is very tolerant of noncompliant DDC sources and sinks.
- The MAX3816A can be turned off and bypassed if another MAX3816A or speed-up device is being used on the same DDC.
- In parallel mode, the MAX3816A can be used simultaneously with other I²C speed-up devices.
- The MAX3816A acts as a buffer between source and display. Hence, source reflections are isolated to the source side of the MAX3816A, protecting display circuits from possible double clocking due to stair-step waveforms caused by very long cables with reflections.
- In series mode, the MAX3816A can be turned off (DRVR_EN asserted low) to isolate between source and display buses. The display bus can then operate independently of source-cable loading or malfunctions.

Consideration

Use a good quality CMOS switch with low resistance (< 20Ω) and over/undervoltage tolerance.

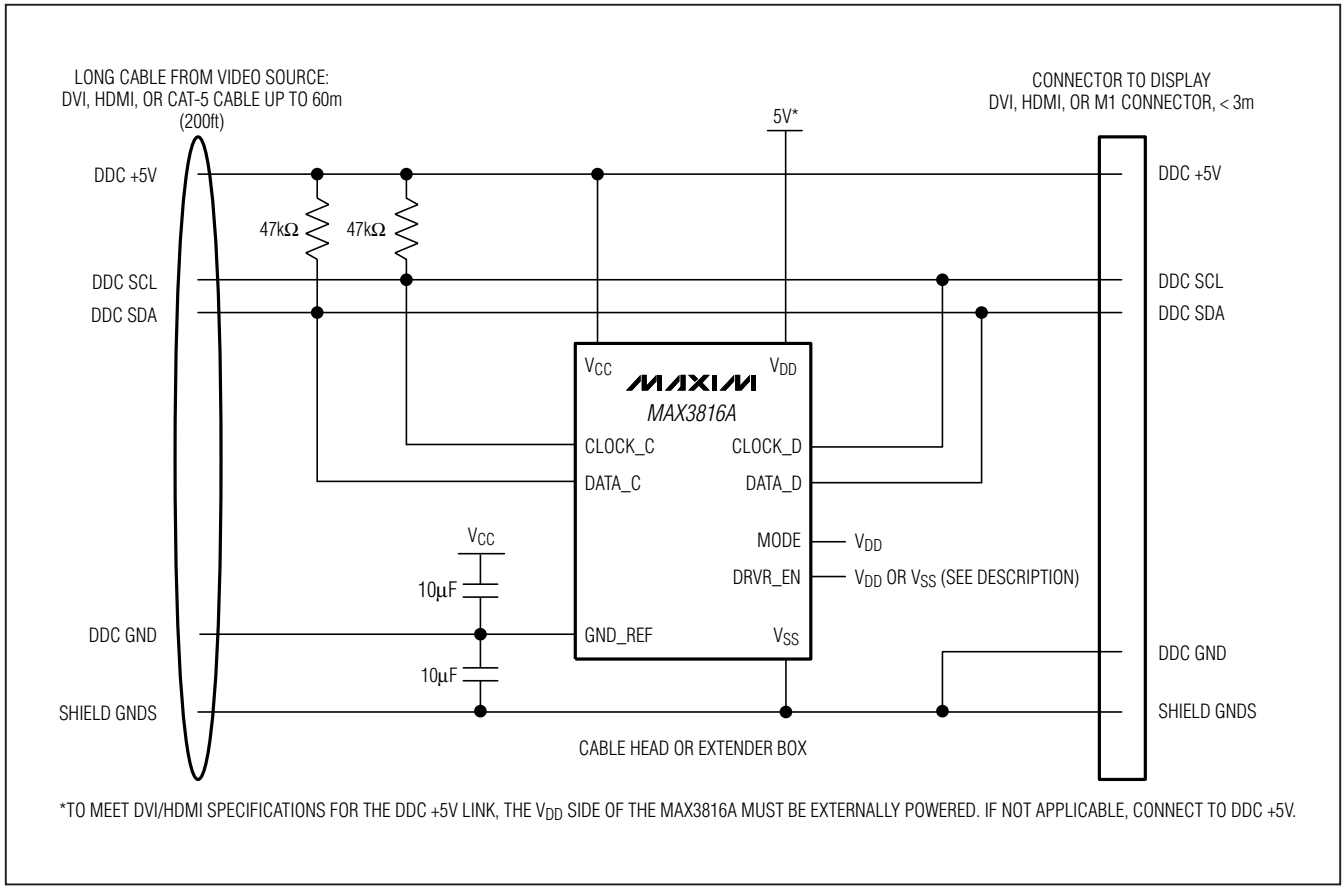


Figure 8. External to Display, In Parallel

MAX3816A External to Display, In Parallel Advantages (See Figure 8)

- Medium-long cable reach.
- In parallel mode, the MAX3816A is very tolerant of noncompliant DDC sources and sinks.
- The MAX3816A can be turned off if another MAX3816A or speed-up device is being used on the same DDC.
- The MAX3816A can be turned off without isolating the display from the source side, letting DDC operate straight through unassisted or assisted.

Consideration

Long cable reflections can reach display circuits since the MAX3816A is not used as a buffer between source and display. Hence, very long cables could cause double-clocking at display circuits due to stair-step rise/fall waveforms due to reflections.

I²C 2-Wire Extender for DDC in DVI, HDMI, and VGA Interfaces

Interface Schematics

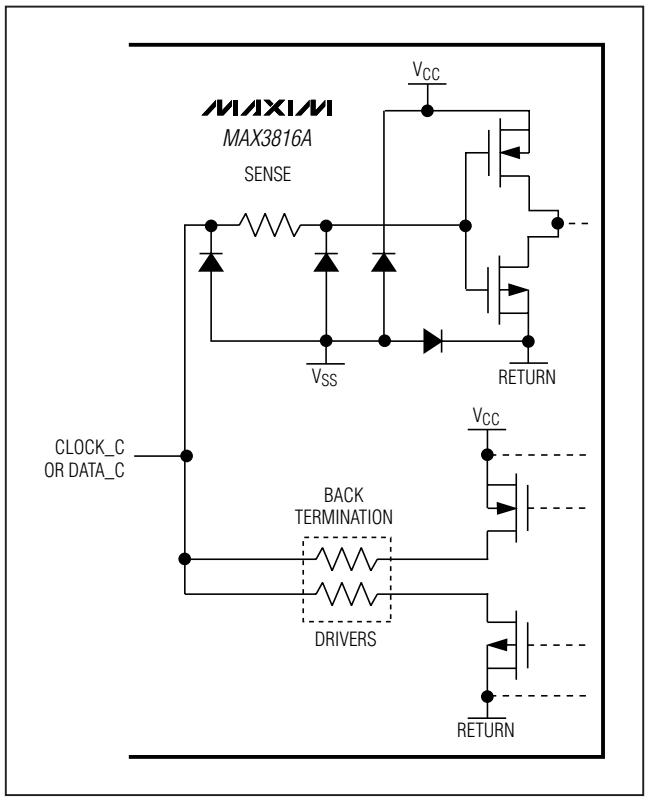


Figure 9. CLOCK_C/DATA_C Equivalent Interface Structure

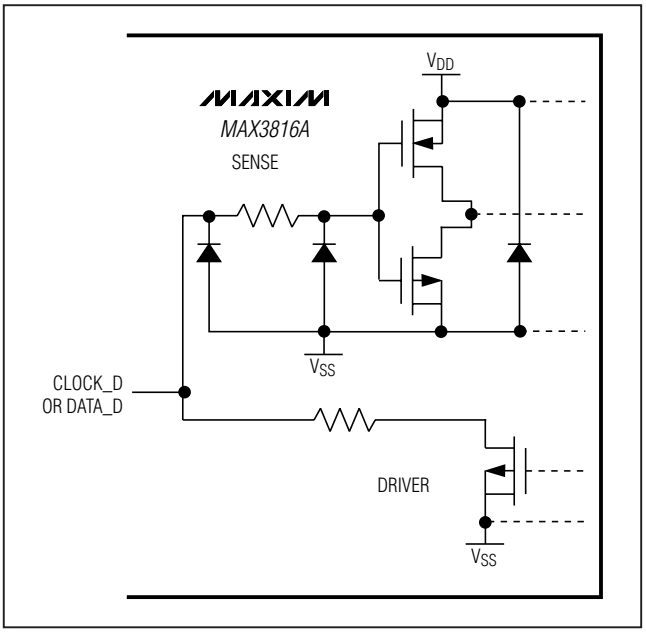


Figure 10. CLOCK_D/DATA_D Equivalent Interface Structure

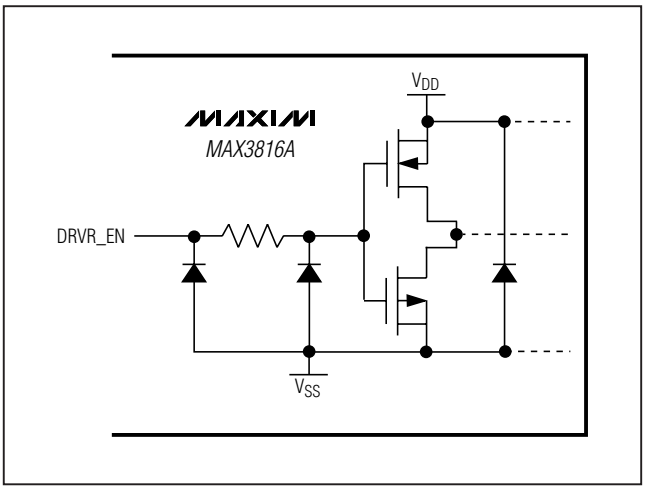
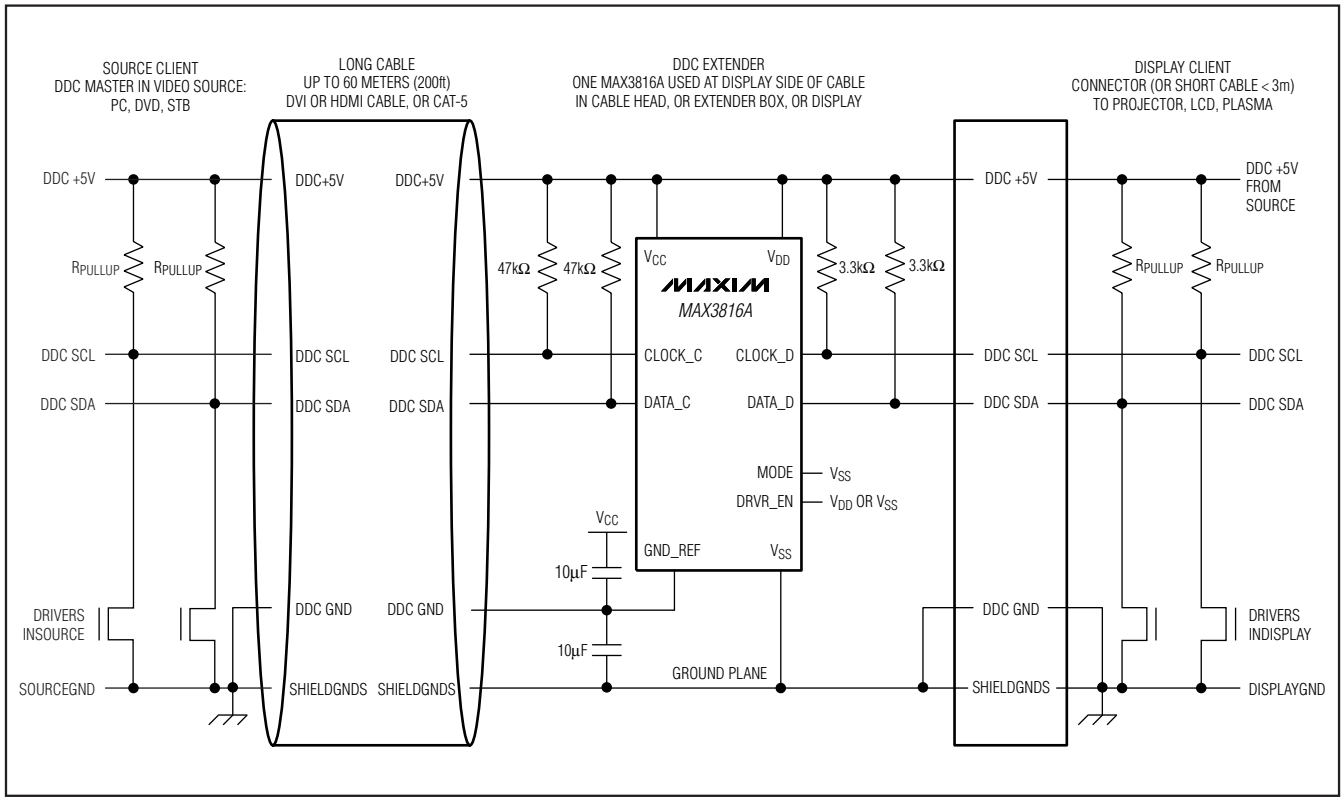
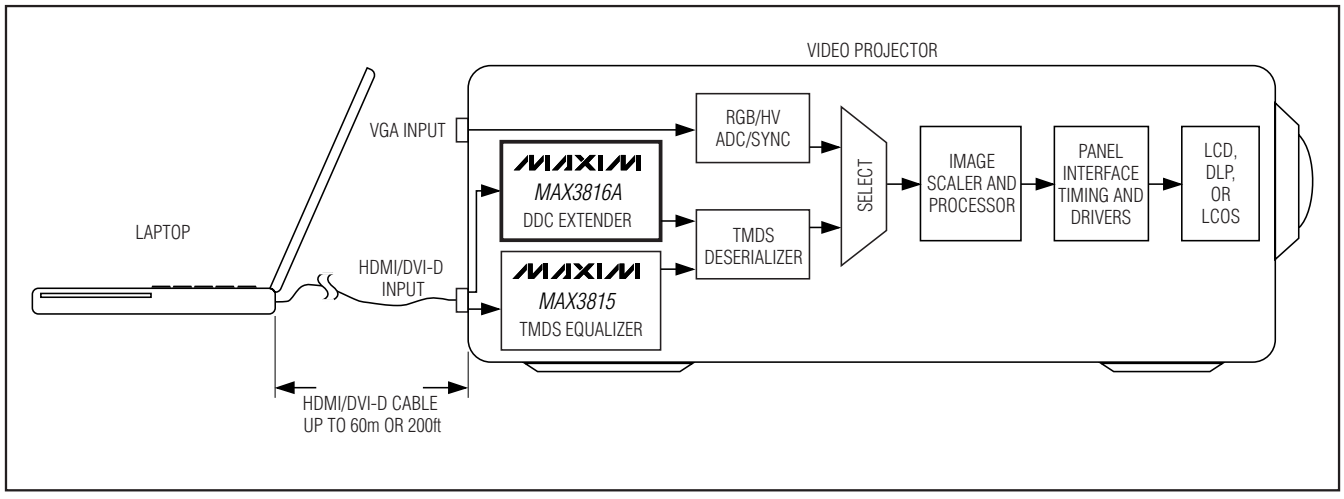


Figure 11. DRVR_EN Equivalent Interface Structure

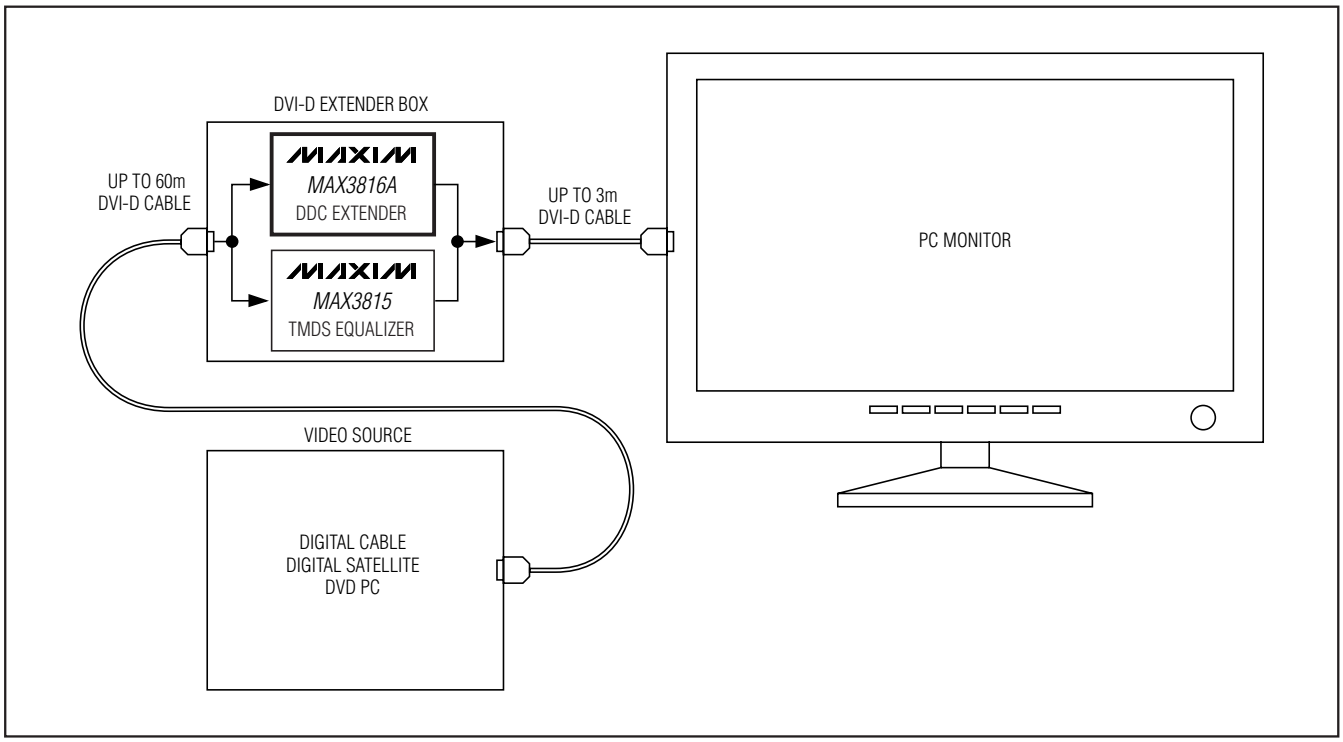
Typical In-Display Operating Circuits



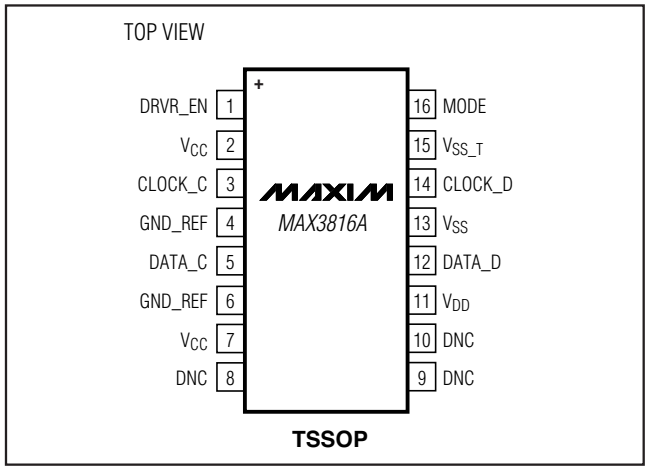


I²C 2-Wire Extender for DDC in DVI, HDMI, and VGA Interfaces

Typical In-Display Operating Circuits (continued)



Pin Configuration



Chip Information

TRANSISTOR COUNT: 5759

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 TSSOP	U16+2	21-0066

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