EVALUATION KIT AVAILABLE

MAX3948

11.3Gbps, Low-Power, DC-Coupled Laser Driver

General Description

The MAX3948 is a 3.3V, multirate, low-power laser diode driver designed for Ethernet, Fibre Channel, and SONET transmission systems at data rates up to 11.3Gbps. This device is optimized to drive a differential transmitter optical subassembly (TOSA) with a 25Ω flex circuit. The unique design of the output stage enables DC-coupling to unmatched TOSAs, thereby lowering transmitter power consumption by more than 100mW.

The MAX3948 receives differential AC-coupled signals with on-chip termination. It can deliver laser modulation currents of up to 85mA at an edge speed of 26ps (20% to 80%) into a 5Ω external differential load. The device is designed to have a high-bandwidth differential signal path with on-chip back termination resistors integrated into its outputs. An input equalization block can be activated to compensate for SFP+/QSFP+ host connector losses. The integrated DC circuit provides programmable laser DC currents up to 61mA. Both the laser DC current generator and the laser modulator can be disabled from a single pin.

The device offers one dedicated pin (VSEL) to program up to four channel addresses for multichannel applications.

The use of a 3-wire digital interface reduces the pin count while permitting adjustment of input equalization, polarity, output deemphasis, and modulation and DC currents without the need for external components. The MAX3948 is available in a 3mm x 3mm, 16-pin TQFN package, and is specified for the -40°C to +95°C extended temperature range.

Applications

40GBASE-LR4 QSFP+ Optical Transceivers

10GBASE-LR SFP+ Optical Transceivers

10GBASE-LRM SFP+ Optical Transceivers

OC192-SR SFP+ SDH/SONET Transceivers

Benefits and Features

- **Lowest Power Consumption**
  - **168mW Typical IC Power Dissipation at 3.3V (LD_{MOD} = 40mA, LD_{DC} = 20mA)**
  - **383mW Total Transmitter Power Dissipation at 3.3V Including LD_{MOD} = 40mA, LD_{DC} = 20mA**
  - **Enables < 1W Maximum Total SFP+ Module Power Dissipation**
  - **Enables < 2.5W Maximum Total QSFP+ Module Power Dissipation**
- **Saves Board Space**
  - **Small 3mm x 3mm Package**
  - **DC-Coupling to the Laser Reduces External Component Count**
- **Flexibility**
  - **Operate Up to Four MAX3948 ICs Over Single 3-Wire Digital Interface**
  - **Programmable Modulation Current Up to 85mA (5Ω Load)**
  - **Programmable DC Current Up to 61mA (Translates to Up to 100mA Laser Bias Current)**
  - **Programmable Input Equalization and Output Deemphasis**
- **Safety**
  - **Supports SFF-8431 SFP+ MSA and SFF-8472 Digital Diagnostic**
  - **Integrated Eye Safety Features with Maskable Faults**
  - **DC Current Monitor**

Ordering Information appears at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-5943; Rev 1; 6/12

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{CCT} ..... -0.3V to +4.0V
$|V_{CC} - V_{CCT}|$ ..... < 0.5V
Voltage Range at TIN+, TIN-, DISABLE,
SDA, SCL, CSEL, VSEL, FAULT, and BMON..... -0.3V to V_{CC}
Voltage Range at VOUT and TOUTC ..... 0.4V to (V_{CCT} - 0.4V)
Voltage Range at TOUTA..... (V_{CCT} - 1.3V) to (V_{CCT} + 1.3V)
Current Range into TIN+ and TIN-..... -20mA to +20mA
Current Range into VOUT ..... -2mA to +90mA
Current into TOUTC and TOUTA ..... +150mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 20.8mW/°C above +70°C)..... 1666.7mW
Storage Temperature Range ..... -55°C to +150°C
Die Attach Temperature ..... +400°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 10°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{CCT} = 2.95V to 3.63V, T_A = -40°C to +95°C; typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, LD_{DC} = 20mA, LD_{MOD} = 40mA, and 14Ω single-ended electrical output load, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Current	I_{CC}	Excludes output current through the external pullup inductors (Note 3)		51	62	mA
Power-Supply Voltage	V_{CCT}, V_{CC}		2.95		3.63	V
POWER-ON RESET						
V_{CC} for Enable High				2.55	2.75	V
V_{CC} for Enable Low			2.3	2.45		V
DATA INPUT SPECIFICATION						
Input Data Rate			1	10.3	11.3	Gbps
Differential Input Voltage	V_{IN}	Launch amplitude into FR4 transmission line ≤ 12in, SET_TXEQ[1:0] = 01b, SET_TXEQ[1:0] = 11b	0.2		0.8	V_{P-P}
		SET_TXEQ[1:0] = 01b, SET_TXEQ[1:0] = 11b, outside of optimized range	0.15		1.0	
		SET_TXEQ[1:0] = 00b	0.15		1.0	
Common-Mode Input Voltage	V_{CM}			2.15		V
Differential Input Resistance	R_{IN}		75	100	125	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CCT} = 2.95V to 3.63V, T_A = -40°C to +95°C; typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, LD_{DC} = 20mA, LD_{MOD} = 40mA, and 14Ω single-ended electrical output load, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input S-Parameters (Note 4)	SCD11	0.1GHz ≤ f ≤ 11.3GHz		-40		dB
	SDD11	f ≤ 4.1GHz		-19		
		4.1GHz ≤ f ≤ 11.3GHz		-16		
	SCC11	1GHz ≤ f ≤ 11.3GHz, Z_{CM_SOURCE} = 25Ω		-15		
DC CURRENT GENERATOR (Note 5, Figure 3)						
Maximum DC DAC Current	I_{DCMAX}	Current into VOUT pin	50	61		mA
Minimum DC DAC Current	I_{DCMIN}	Current into VOUT pin			2.5	mA
DC-Off Current	I_{DC-OFF}				0.1	mA
DC DAC LSB Size				116		µA
DC DAC Integral Nonlinearity	INL	2.5mA ≤ I_{DC} ≤ 50mA		±0.5		%FS
DC DAC Differential Nonlinearity	DNL	Guaranteed monotonic at 8-bit resolution, SET_IDC[8:1]		±0.5		LSB
DC Current DAC Stability		2.5mA ≤ I_{DC} ≤ 50mA, V_{VOUT} = V_{CCT} - 1.5V (Notes 6, 7)		1	4	%
DC Compliance Voltage at VOUT			V_{CCT} - 2	V_{CCT} - 1.5	V_{CCT} - 1	V
BMON Current Gain	G_{BMON}	G_{BMON} = I_{BMON}/I_{DC}, external resistor to GND defines voltage	15	16.7	20	mA/A
BMON Current Gain Stability		2.5mA ≤ I_{DC} ≤ 50mA, V_{VOUT} = V_{CCT} - 1.5V (Notes 6, 7)		1.5	5	%
Compliance Voltage at BMON			0		1.8	V
LASER MODULATOR (Note 8)						
Maximum Laser Modulation Current	LD_{MODMAX}	Current into TOUTC pin, 5Ω laser load, 6.25% deemphasis	85			mA_{P-P}
Minimum Laser Modulation Current	LD_{MODMIN}	Current into TOUTC pin, 5Ω laser load, 6.25% deemphasis			10	mA_{P-P}
Modulation-Off Laser Current	$LD_{MOD-OFF}$	Current into TOUTC pin			0.1	mA
Modulation DAC Full-Scale Current	I_{MOD-FS}		99.7	130		mA
Modulation DAC LSB Size				247		µA
Modulation DAC Integral Nonlinearity	INL			±1		%FS
Modulation DAC Differential Nonlinearity	DNL	Guaranteed monotonic at 8-bit resolution, SET_IMOD[8:1]		±0.5		LSB
TOUTA and TOUTC Instantaneous Output Compliance Voltage	V_{TOUTA}	With external inductive pullup to V_{CCT}	V_{CCT} - 1		V_{CCT} + 1	V
	V_{TOUTC}	With external inductive pullup to VOUT	0.6		V_{CCT} - 1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CCT} = 2.95V to 3.63V, T_A = -40°C to +95°C; typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, LD_{DC} = 20mA, LD_{MOD} = 40mA, and 14Ω single-ended electrical output load, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Modulation Output Termination	R_{OUT}		19	25	31	Ω
Modulation Current DAC Stability		10mA ≤ LD_{MOD} ≤ 85mA, V_{VOUT} = V_{CCT} - 1.5V (Notes 6, 7)		1.5	4	%
Modulation Current Rise/Fall Time	t_R, t_F	20% to 80%, 10mA ≤ LD_{MOD} ≤ 85mA (Note 6)		26	36	ps
Deterministic Jitter (Note 6)	DJ	10mA ≤ LD_{MOD} ≤ 85mA, 8.5Gbps with K28.5 pattern		4		ps_{P-P}
		10mA ≤ LD_{MOD} ≤ 85mA, 10.3125Gbps (Note 9)		6	12	ps_{P-P}
		10mA ≤ LD_{MOD} ≤ 85mA, 11.3Gbps (Note 9)		8	13	ps_{P-P}
Random Jitter	RJ	10mA ≤ LD_{MOD} ≤ 85mA (Note 6)		0.19	0.55	ps_{RMS}
Differential S-Parameters (Note 4)	SCC22	0.1GHz ≤ f ≤ 4.1GHz, Z_{CM_SOURCE} = 12.5Ω		-10		dB
		4.1GHz < f ≤ 11.3GHz, Z_{CM_SOURCE} = 12.5Ω		-6		dB
	SDD22	0.1GHz< f ≤ 11.3GHz, Z_{DIFF_SOURCE} = 50Ω		-13		dB
SAFETY FEATURES						
Threshold Voltage at VOUT		Fault never occurs for V_{VOUT} ≥ V_{CCT} - 2V, fault always occurs for V_{VOUT} < V_{CCT} - 2.8V, referenced to V_{CCT}	V_{CCT} - 2.8		V_{CCT} - 2	V
		Fault never occurs for V_{VOUT} ≥ 1.7V, fault always occurs for V_{VOUT} < 1.35V, referenced to GND, SET_IMOD[8:6] = 111b	1.35		1.7	V
		Fault never occurs for V_{VOUT} ≥ 0.57V, fault always occurs for V_{VOUT} < 0.43V, referenced to GND, SET_IMOD[8:6] = 000b	0.43		0.57	V
Threshold Voltage at TOUTC		Fault never occurs for V_{TOUTC} ≥ 0.48V, fault always occurs for V_{TOUTC} < 0.35V	0.35		0.48	V
Threshold Voltage at TOUTA		Fault never occurs for V_{TOUTA} ≥ V_{CCT} - 1.45V, fault always occurs for V_{TOUTA} < V_{CCT} - 1.88V	V_{CCT} - 1.88		V_{CCT} - 1.45	V
Threshold Voltage at V_{CCT}		Fault never occurs for V_{CCT} ≥ V_{CC} - 0.15V, fault always occurs for V_{CCT} < V_{CC} - 0.4V	V_{CC} - 0.4		V_{CC} - 0.15	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CCT} = 2.95V to 3.63V, T_A = -40°C to +95°C; typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, LD_{DC} = 20mA, LD_{MOD} = 40mA, and 14Ω single-ended electrical output load, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING REQUIREMENTS (Notes 5, 6, 8)						
Initialization Time	t_{INIT}	LD_{DC} = 25mA, LD_{MOD} = 65mA, DC and modulation DAC are both H0x00, time from TX_EN = high to LD_{DC} and LD_{MOD} at 90% of steady state		250		ns
DISABLE Assert Time	t_{OFF}	Time from rising edge of DISABLE input signal to LD_{DC} and LD_{MOD} at 10% of steady state (Note 6)		25	75	ns
DISABLE Negate Time	t_{ON}	Time from falling edge of DISABLE to LD_{DC} and LD_{MOD} at 90% of steady state (Note 6)		250	600	ns
FAULT Reset Time	$t_{RECOVER}$	Time from negation of latched fault using DISABLE to LD_{DC} and LD_{MOD} at 90% of steady state		250	600	ns
FAULT Assert Time	t_{FAULT}	Time from fault to FAULT = high, $C_{FAULT} \leq$ 20pF, R_{FAULT} = 4.7kΩ		0.7	3	µs
DISABLE to Reset Time		Time DISABLE must be held high to reset fault	4			µs
DIGITAL I/O SPECIFICATIONS (SDA, SCL, CSEL, FAULT, DISABLE)						
Input High Voltage	V_{IH}		1.8		V_{CC}	V
Input Low Voltage	V_{IL}		0		0.8	V
Input Hysteresis	V_{HYST}			80		mV
Input Capacitance	C_{IN}				5	pF
DISABLE Input Resistance	R_{PULL}	Internal pullup resistor	4.7	7.5	10	kΩ
Input Leakage Current (DISABLE)	I_{IH}	Input connected to V_{CC}			10	µA
	I_{IL}	Input connected to GND		440	775	
Input Leakage Current (SDA)	I_{IH}	Input connected to V_{CC}	-2		+2	µA
	I_{IL}	Input connected to GND; internal pullup is 75kΩ typical	35		75	
Input Leakage Current (SCL, CSEL)	I_{IH}	Input connected to V_{CC}; internal pulldown is 75kΩ typical	35		75	µA
	I_{IL}	Input connected to GND	-2		+2	
Output High Voltage (SDA, FAULT)	V_{OH}	External pullup is (4.7kΩ to 10kΩ) to V_{CC}	V_{CC} - 0.1			V
Output Low Voltage (SDA, FAULT)	V_{OL}	External pullup is (4.7kΩ to 10kΩ) to V_{CC}			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{CCT} = 2.95V to 3.63V, T_A = -40°C to +95°C; typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, LD_{DC} = 20mA, LD_{MOD} = 40mA, and 14Ω single-ended electrical output load, unless otherwise noted. See Figure 1 for electrical setup.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3-WIRE DIGITAL INTERFACE TIMING CHARACTERISTICS (Figure 5)						
SCL Clock Frequency	f_{SCL}			400	1000	kHz
SCL Pulse-Width High	t_{CH}		500			ns
SCL Pulse-Width Low	t_{CL}		500			ns
SDA Setup Time	t_{DS}			100		ns
SDA Hold Time	t_{DH}			100		ns
SCL Rise to SDA Propagation Time	t_D			5		ns
CSEL Pulse-Width Low	t_{CSW}		500			ns
CSEL Leading Time Before the First SCL Edge	t_L			500		ns
CSEL Trailing Time After the Last SCL Edge	t_T			500		ns
SDA, SCL Load	C_B	Total bus capacitance on one line with 4.7kΩ pullup to V_{CC}			20	pF
VSEL FOUR-LEVEL DIGITAL INPUT (Note 10, Table 2)						
Input Voltage High		3-wire address, ADDR[6:5] = 11b	$5/6V_{CC}$ + 0.2		V_{CC}	V
Input Voltage Mid-High		3-wire address, ADDR[6:5] = 10b	$3/6V_{CC}$ + 0.2	2/3 x V_{CC}	$5/6V_{CC}$ - 0.2	V
Input Voltage Mid-Low		3-wire address, ADDR[6:5] = 01b	$1/6V_{CC}$ + 0.2	1/3 x V_{CC}	$3/6V_{CC}$ - 0.2	V
Input Voltage Low		3-wire address, ADDR[6:5] = 00b	0		$1/6V_{CC}$ - 0.2	V

Note 2: Specifications at T_A = -40°C and +95°C are guaranteed by design and characterization.

Note 3: VOUT is connected to 1.9V. TOUTA is connected to V_{CCT} through pullup inductors, and TOUTC is connected to VOUT through pullup inductors.

Note 4: Measured with Agilent 8720ES + ATN-U112A and series RC (39Ω and 0.3pF) between TOUTC and TOUTA (Figure 1).

Note 5: LD_{DC} = I_{DC} + I_{MOD} x (DE + R x (1 - DE)/(50 + R)/2), where LD_{DC} is the effective laser DC current, I_{DC} is the DC DAC current, I_{MOD} is the modulation DAC current, DE is the deemphasis percentage, and R is the differential laser load resistance. Example: For R = 5Ω and DE = 6.25%, LD_{DC} = I_{DC} + 0.105 x I_{MOD}.

Note 6: Guaranteed by design and characterization.

Note 7: Stability is defined as [($I_{MEASURED}$) - ($I_{REFERENCE}$)]/($I_{REFERENCE}$) over the listed current/temperature range and V_{CCT} = V_{CC} = V_{CCREF} ±5%, V_{CCREF} = 3.3V. Reference current measured at V_{CCREF} and T_{REF} = +25°C.

Note 8: LD_{MOD} = I_{MOD} x (1 - DE) x 50/(50 + R), where LD_{MOD} is the effective laser modulation current, I_{MOD} is the modulation DAC current, DE is the deemphasis percentage, and R is the differential laser load resistance. Example: For RΩ = 5 and DE = 6.25%, LD_{MOD} = 0.852 x I_{MOD}.

Note 9: Equivalent 2^{23} - 1 PRBS pattern = 2^7 - 1 PRBS + 72 zeros + 2^7 - 1 PRBS + 72 ones.

Note 10: These limits are based on simulated values.

11.3Gbps, Low-Power, DC-Coupled Laser Driver

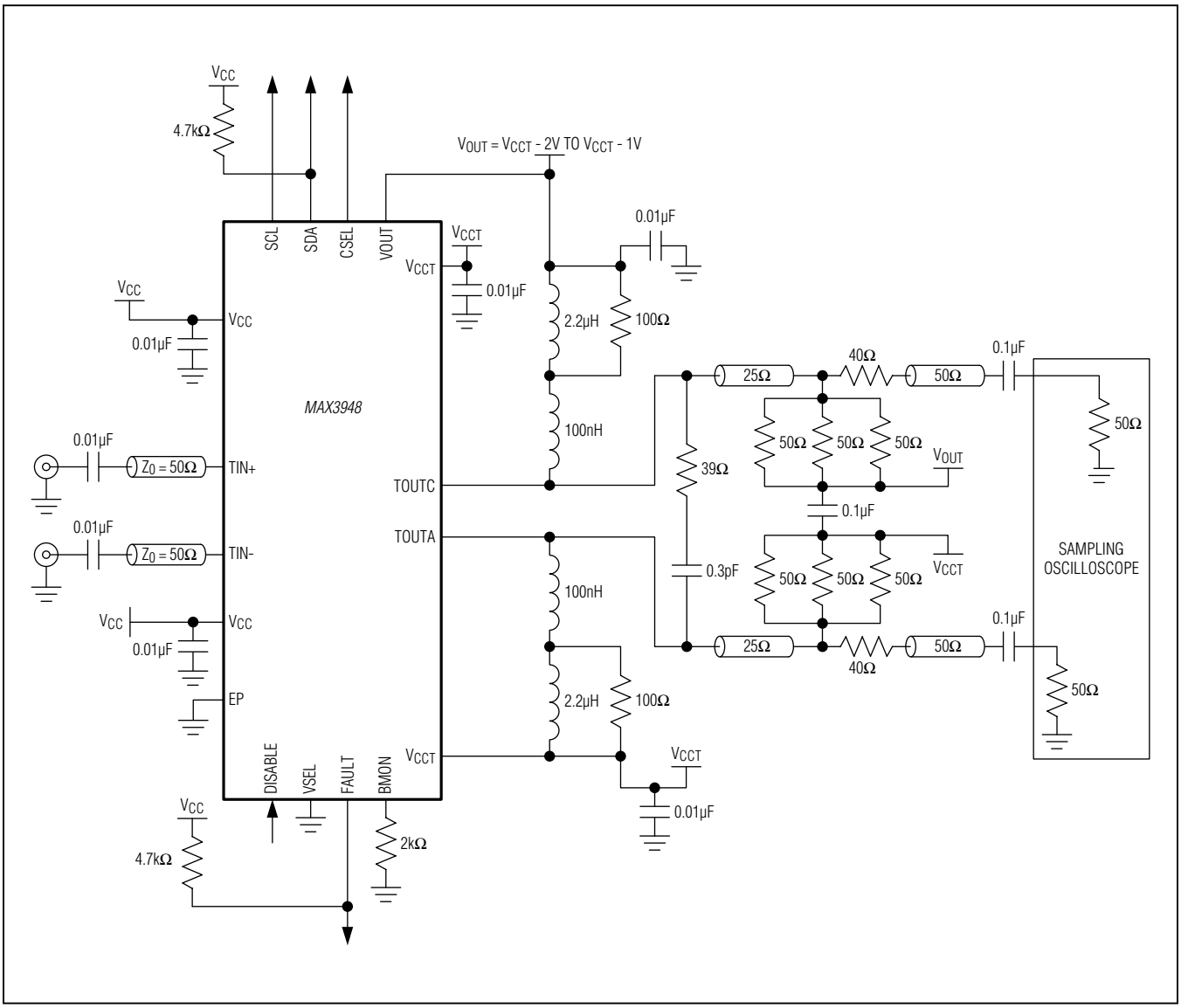


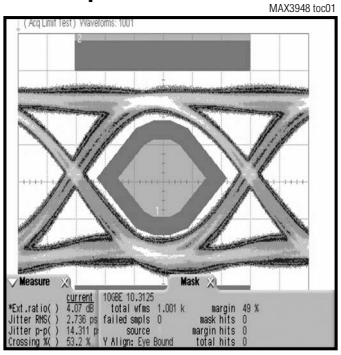
Figure 1. AC Test Setup

11.3Gbps, Low-Power, DC-Coupled Laser Driver

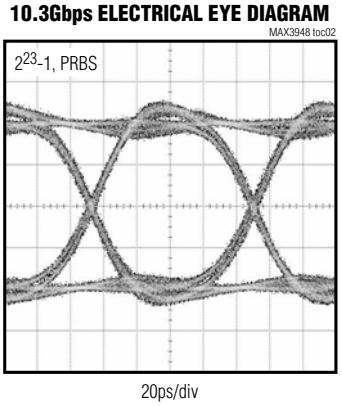
Typical Operating Characteristics

(Typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 72 zeros + 2^7 - 1 PRBS (inverted) + 72 ones, unless otherwise noted.)

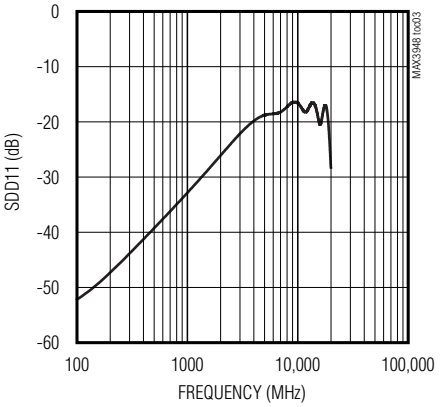
10.3Gbps OPTICAL EYE DIAGRAM



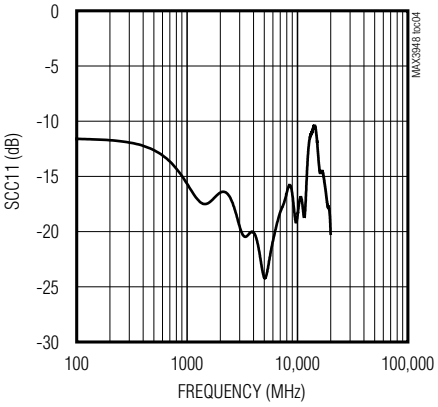
10.3Gbps ELECTRICAL EYE DIAGRAM



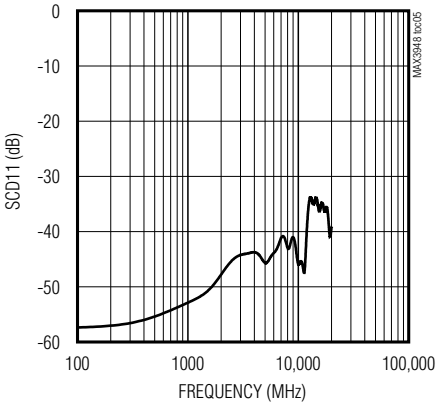
INPUT DIFFERENTIAL RETURN LOSS vs. FREQUENCY



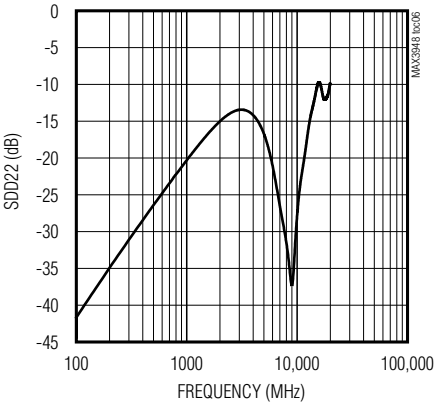
INPUT COMMON-MODE RETURN LOSS vs. FREQUENCY



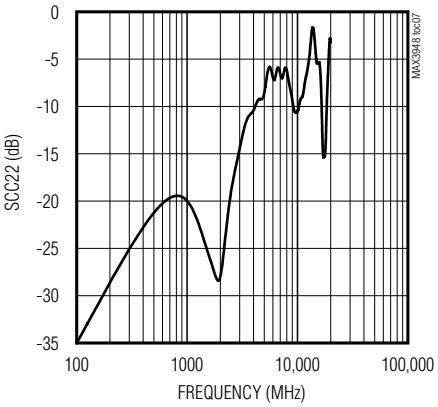
INPUT DIFFERENTIAL TO COMMON-MODE RETURN LOSS vs. FREQUENCY



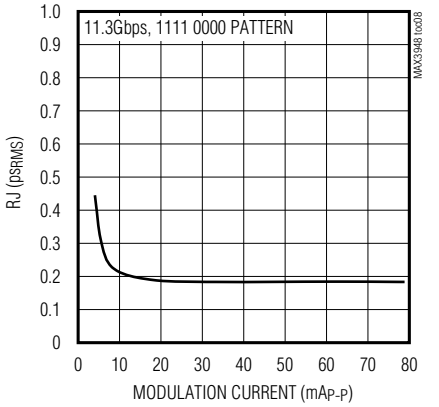
OUTPUT DIFFERENTIAL RETURN LOSS vs. FREQUENCY



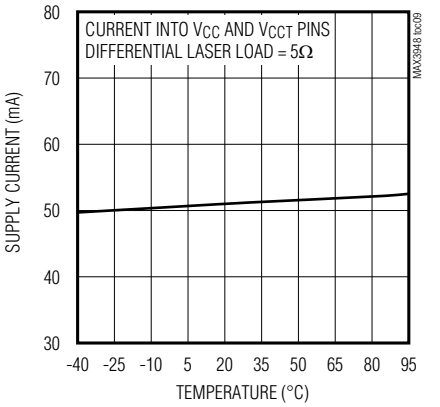
OUTPUT COMMMON-MODE RETURN LOSS vs. FREQUENCY



RANDOM JITTER vs. MODULATION CURRENT (AT LOAD)



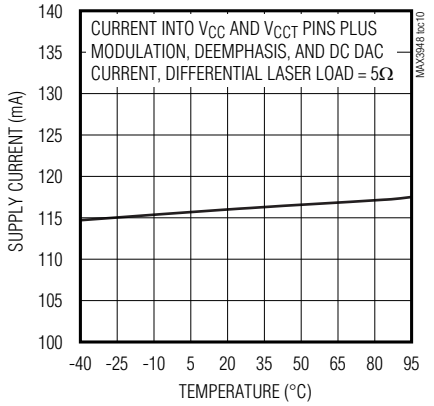
SUPPLY CURRENT vs. TEMPERATURE (LD_{MOD} = 40mA$_{P-P}$, LD_{DC} = 20mA)



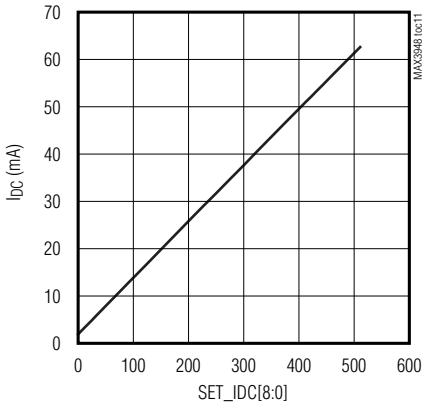
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 72 zeros + 2^7 - 1 PRBS (inverted) + 72 ones, unless otherwise noted.)

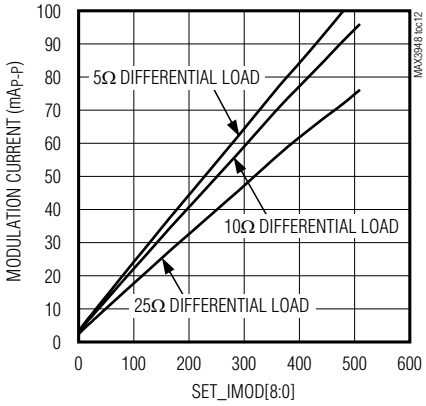
TOTAL CURRENT vs. TEMPERATURE (LD_{MOD} AT LOAD = 40mA_{P-P}, LD_{DC} = 20mA)



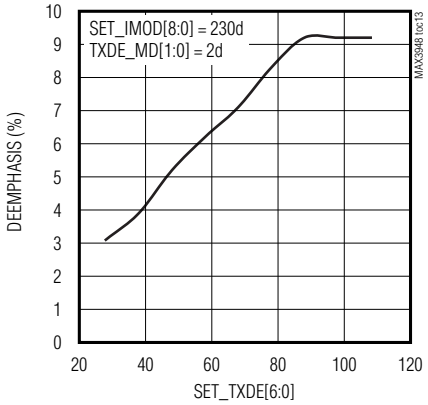
DC CURRENT vs. DAC SETTING



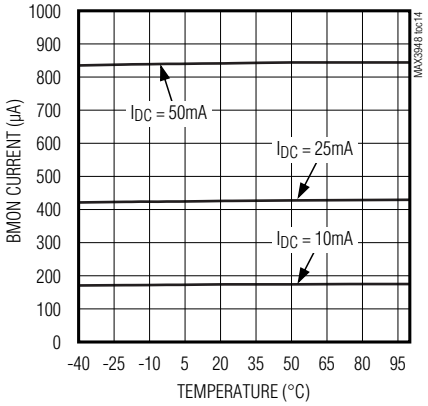
MODULATION CURRENT (AT LOAD) vs. DAC SETTING



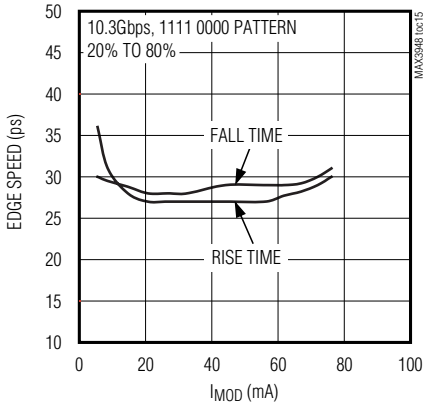
MODULATION CURRENT DEEMPHASIS vs. MANUAL DEEMPHASIS SETTING



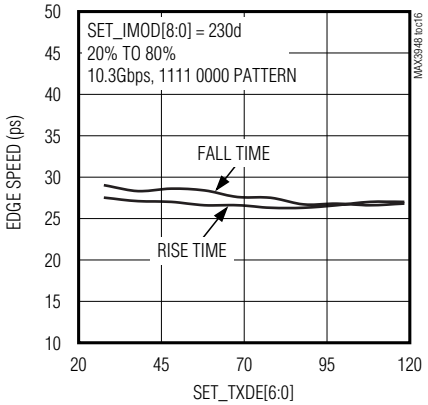
DC MONITOR CURRENT vs. TEMPERATURE



EDGE SPEED vs. MODULATION CURRENT



EDGE SPEED vs. DEEMPHASIS SETTING

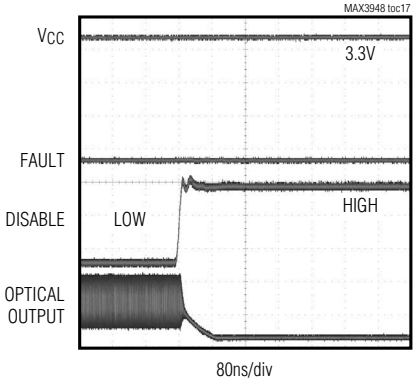


11.3Gbps, Low-Power, DC-Coupled Laser Driver

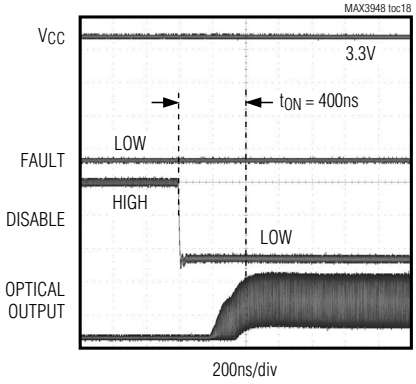
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = V_{CCT} = 3.3V, T_A = +25°C, data pattern = 2^7 - 1 PRBS + 72 zeros + 2^7 - 1 PRBS (inverted) + 72 ones, unless otherwise noted.)

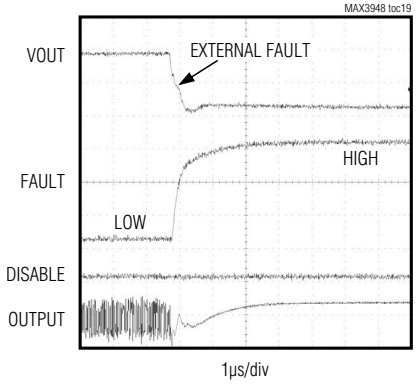
TRANSMITTER DISABLE



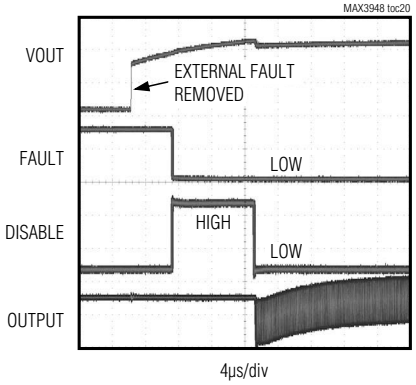
TRANSMITTER ENABLE



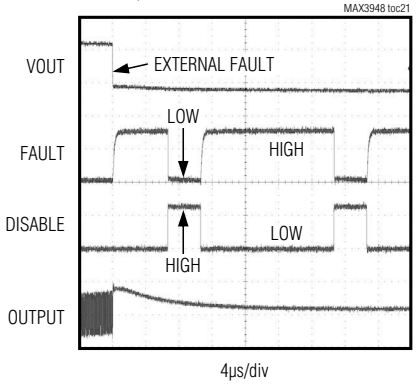
RESPONSE TO FAULT



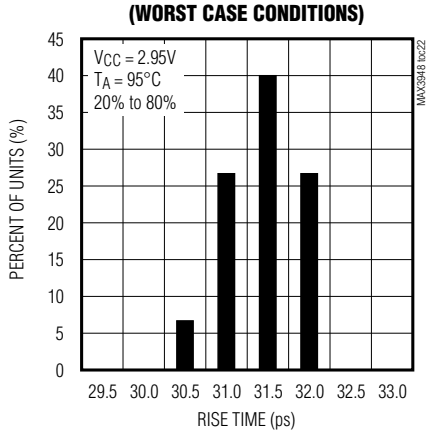
FAULT RECOVERY



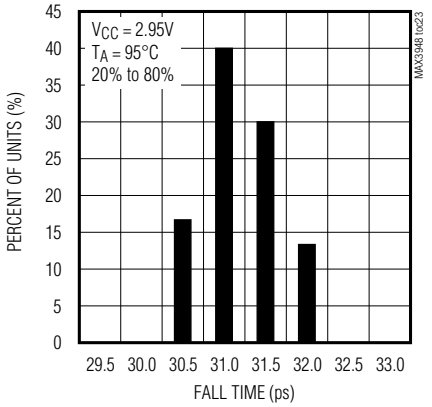
FREQUENT ASSERTION OF DISABLE



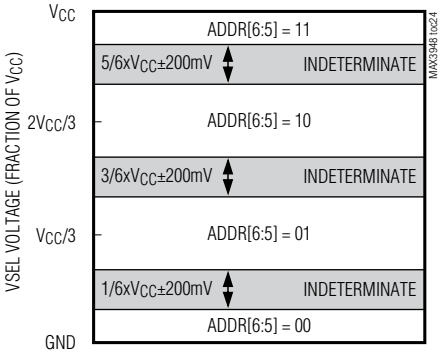
DISTRIBUTION OF RISE TIME (WORST CASE CONDITIONS)



DISTRIBUTION OF FALL TIME (WORST CASE CONDITIONS)

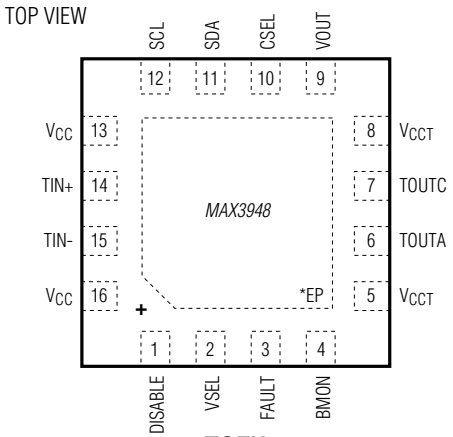


MAX3948 3-WIRE ADDRESS vs. VSEL VOLTAGE (DATA FROM SIMULATION)



11.3Gbps, Low-Power, DC-Coupled Laser Driver

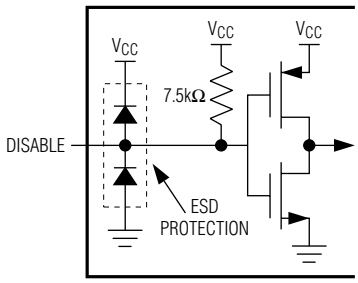
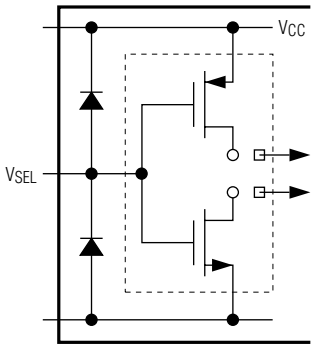
Pin Configuration



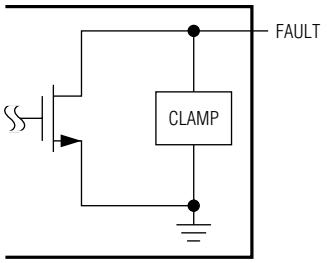
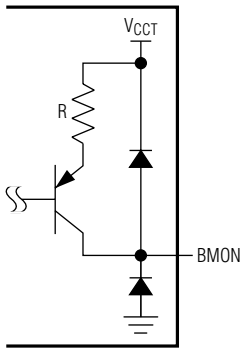
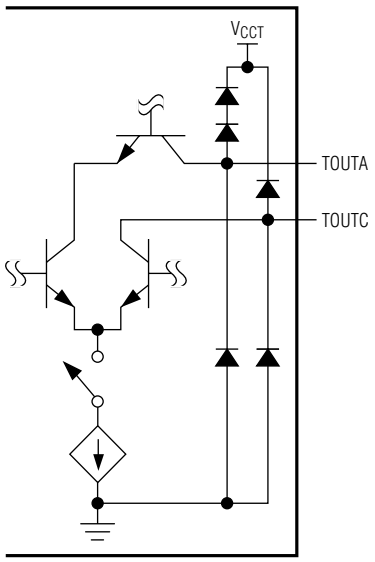
TQFN
(3mm x 3mm)

*EXPOSED PAD MUST BE CONNECTED TO GROUND.

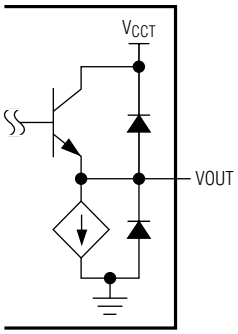
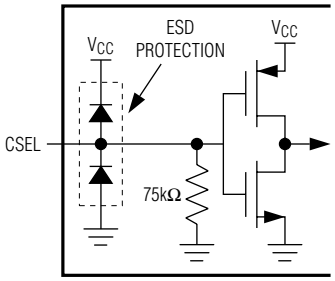
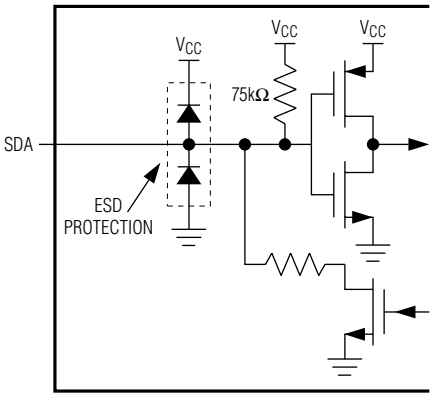
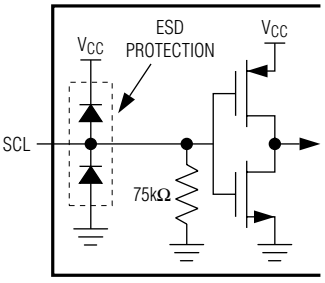
Pin Description

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	DISABLE	Disable Input, CMOS. Set to logic-low for normal operation. Logic-high or open disables both the modulation current and the DC current. Internally pulled up by a 7.5kΩ resistor to V_{CC}.	
2	VSEL	4-Level Input for SPI Device Address Detection. Connecting to V_{CC} sets ADDR[6:5] to 11b, connecting to V_{CC} x 2/3 sets ADDR[6:5] to 10b, connecting to V_{CC}/3 sets ADDR[6:5] to 01b, and connecting to GND sets ADDR[6:5] to 00b.	

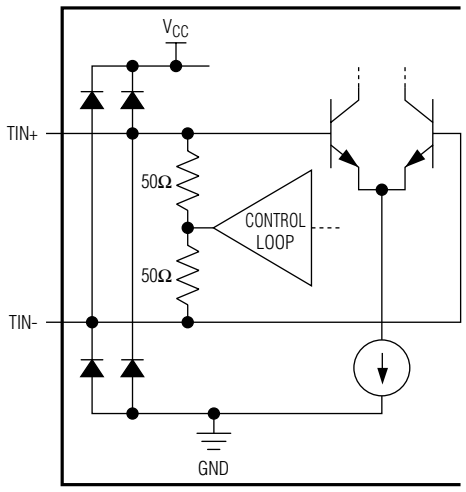
Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
3	FAULT	Fault Output, Open Drain. Logic-high indicates a fault condition has been detected. It remains high even after the fault condition has been removed. A logic-low occurs when the fault condition has been removed and the fault latch has been cleared by toggling DISABLE. FAULT should be pulled up to V_{CC} by a 4.7kΩ to 10kΩ resistor.	
4	BMON	Analog Laser DC Current Monitor Output. Current out of this pin develops a ground-referenced voltage across an external resistor that is proportional to the VOUT pin current. The current sourced by this pin is typically 1/60 the VOUT pin current.	
5,8	V_{CCT}	Power Supply. Provides supply voltage to the output block.	—
6	TOUTA	Inverting Laser Diode Modulation Current Output. Connect this pin to the anode of the laser diode.	
7	TOUTC	Noninverting Laser Diode Modulation Current Output. Connect this pin to the cathode of the laser diode.	

Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
9	VOUT	Combined Current Return Path and Laser DC Current Output	
10	CSEL	Chip-Select CMOS Input. Setting CSEL to logic-high starts a 3-wire command cycle. Setting CSEL to logic-low ends the cycle and resets the control state machine. Internally pulled down to GND by a 75kΩ resistor.	
11	SDA	Serial Data Bidirectional CMOS Input. Also an open-drain output. This pin has a 75kΩ internal pullup, but requires an external 4.7kΩ to 10kΩ pullup resistor to V_{CC} for proper operation.	
12	SCL	Serial-Clock CMOS Input. This pin has an internal 75kΩ pulldown resistor to GND.	

Pin Description (continued)

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
13, 16	V_{CC}	Power Supply. Provides supply voltage to core analog and digital circuitry.	—
14	TIN+	Noninverting Data Input. Input with internal 50Ω termination.	
15	TIN-	Inverting Data Input. Input with internal 50Ω termination.	
—	EP	Exposed Pad (Ground). This is the only electrical connection to ground on the MAX3948 and must be soldered to the circuit board ground for proper thermal and electrical performance (see the *Exposed-Pad Package* section).	—

11.3Gbps, Low-Power, DC-Coupled Laser Driver

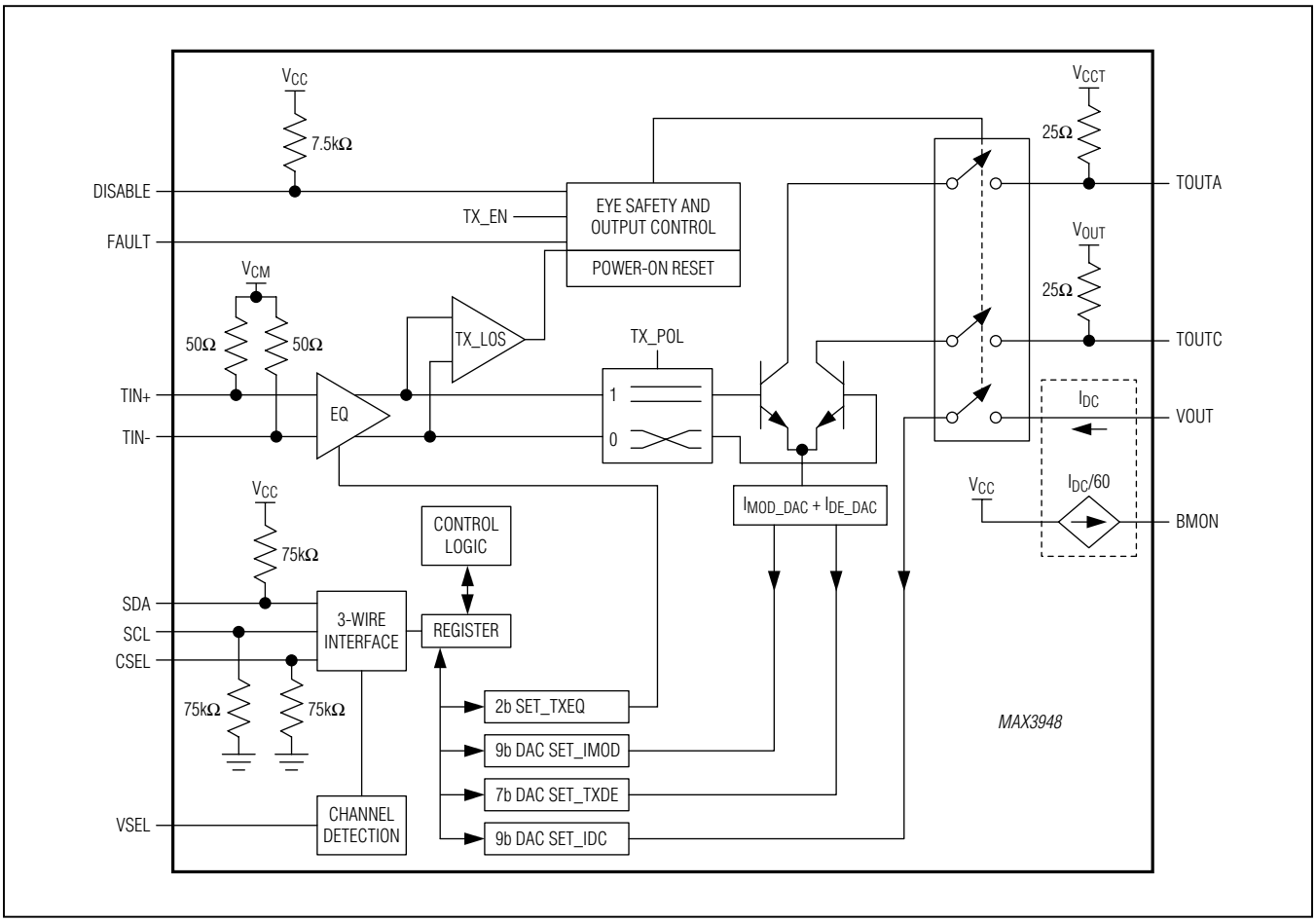


Figure 2. Functional Diagram

Detailed Description

The MAX3948 SFP+/QSFP+ laser driver is designed to drive 5Ω to 10Ω TOSAs from 1Gbps to 11.3Gbps. It contains an input buffer with programmable equalization, DC and modulation current DACs, an output driver with adjustable deemphasis, power-on-reset circuitry, DC current monitor, programmable 3-wire address, and eye safety circuitry with maskable fault monitors. A 3-wire digital interface is used to control these functions.

Input Buffer with Programmable Equalization

The input is internally biased and terminated with 50Ω to a common-mode voltage. The first amplifier stage features a programmable equalizer for high-frequency losses including a SFP+/QSFP+ host connector. Equalization is controlled by the SET_TXEQ register (Table 1). The TX_POL bit in the TXCTRL register controls the polarity of TOUTA and TOUTC vs. TIN+ and TIN-. A status indicator bit (TXSTAT1 bit 5) monitors the presence of an AC input signal.

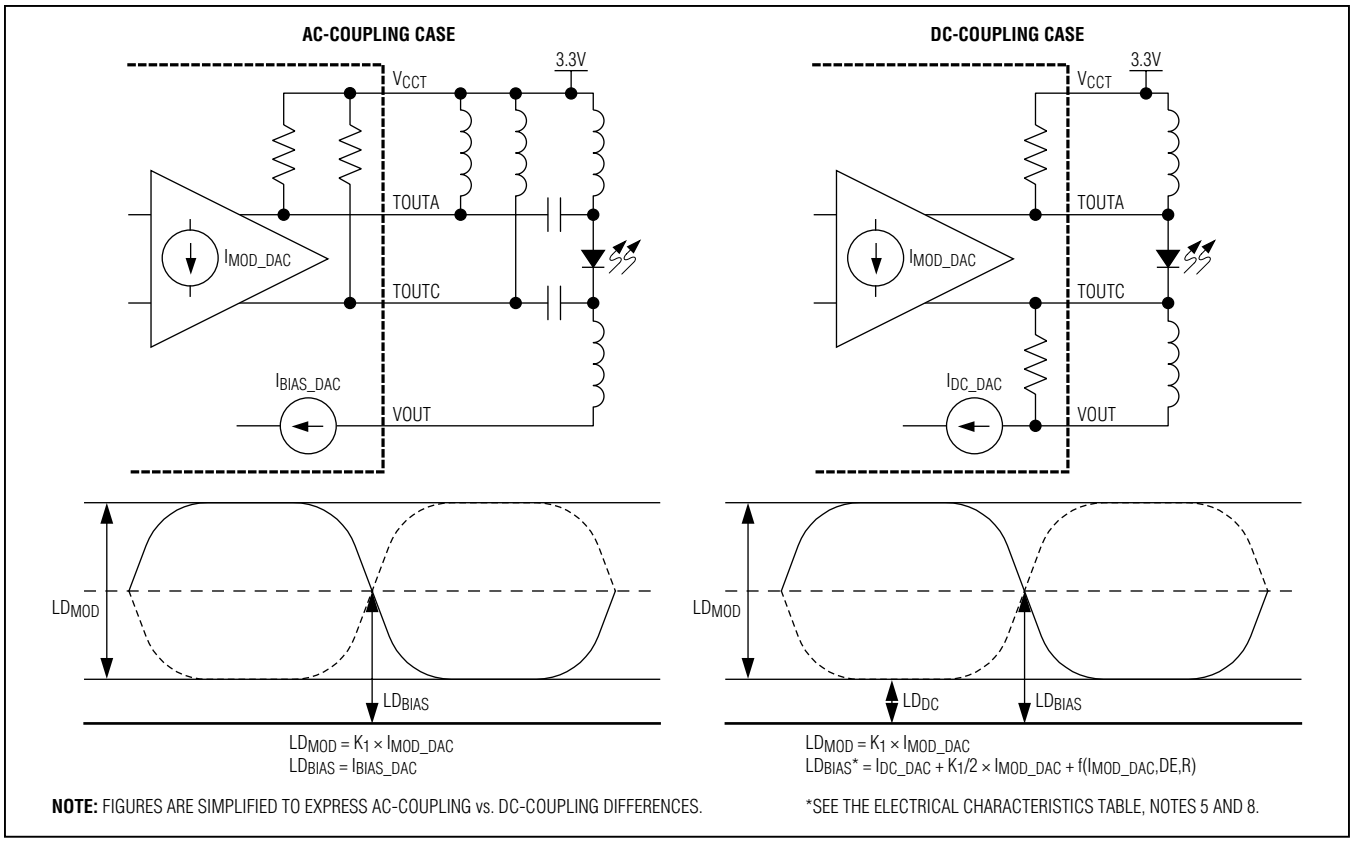
Table 1. Input Equalization Control Register Settings

SET_TXEQ[1:0]		BOOST AT 5.16GHz (dB)
0	0	1
0	1	3
1	1	5.5

DC Current DAC

The DC current from the device is optimized to provide up to 61mA of DC current into a laser diode with 116µA resolution (Figure 3). The DC DAC current is controlled through the 3-wire digital interface using the SET_IDC[8:0], IDCMAX[7:0], and DCINC[4:0] bits.

For laser operation, the laser DC current can be set using the 9-bit SET_IDC DAC register. The upper 8 bits are set by the SET_IDC[8:1] register, commonly used during the initialization procedure after power-on reset (POR). The LSB (bit 0) of SET_IDC (DCINC[7]) is initialized to zero after POR and can be updated using the DCINC register.



NOTE: FIGURES ARE SIMPLIFIED TO EXPRESS AC-COUPLING vs. DC-COUPLING DIFFERENCES.

*SEE THE ELECTRICAL CHARACTERISTICS TABLE, NOTES 5 AND 8.

Figure 3. AC-/DC-Coupling Cases

The IDCMAX register limits the maximum SET_IDC[8:1] DAC code.

After initialization the value of the SET_IDC DAC register should be updated using the DCINC register to optimize cycle time and enhance laser safety. The DCINC register is an 8-bit register. The first 5 bits of DCINC contain the increment information in two's complement format. Increment values range from -16 to +15 LSBs. If the updated value of SET_IDC[8:1] exceeds IDCMAX[7:0], the IDCERR warning flag is set and SET_IDC[8:1] is set to IDCMAX[7:0].

Modulation Current DAC

The modulation current from the MAX3948 is optimized to provide up to 85mA of modulation current into a 5Ω laser load with 210µA resolution. The modulation current is controlled through the 3-wire digital interface using the SET_IMOD[8:1], IMODMAX[7:0], MODINC[7:0], and SET_TXDE registers.

For laser operation, the laser modulation current can be set using the 9-bit SET_IMOD DAC. The upper 8 bits are programmed through the SET_IMOD[8:1] register, commonly used during the initialization procedure after POR. The LSB (bit 0) of SET_IMOD (MODINC[7])is initialized to zero after POR and can be updated using the MODINC register. The IMODMAX register limits the maximum SET_IMOD[8:1] DAC code.

After initialization the value of the SET_IMOD DAC register should be updated using the MODINC[4:0] bits to optimize cycle time and enhance laser safety. The MODINC register is an 8-bit register. The first 5 bits of MODINC contain the increment information in two's complement format. Increment values range from -16 to +15 LSBs. If the updated value of SET_IMOD[8:1] exceeds IMODMAX[7:0], the IMODERR warning flag is set and SET_IMOD[8:1] is set to IMODMAX[7:0].

Effective modulation current seen by the laser is actually the combination of the DAC current generated by the SET_IMOD[8:0] register (I_{MOD}), deemphasis setting (DE), and differential laser load (R). It is calculated by the following formula:

$$LD_{MOD} = I_{MOD} \times 50 \times (1 - DE)/(50 + R)$$

Output Driver

This device is optimized to drive a differential TOSA with a 25Ω flex circuit. The unique design of the output stage enables DC-coupling to unmatched TOSAs with laser diode impedances ranging from 5Ω to 10Ω. The output stage also features programmable deemphasis that can be set as a percentage of the modulation current. The deemphasis function is controlled by the TXCTRL[4:3] and the SET_TXDE registers.

Power-On Reset (POR)

Power-on reset ensures that the laser is off until the supply voltage has reached a specified threshold (2.75V). After power-on reset, TX_EN is 0 and DC current and modulation current DACs default to small codes. In the case of a POR, all registers are reset to their default values.

BMON Function

The current out of the BMON pin is typically 1/60th the value of the current into the VOUT pin. The total resistance to ground at BMON sets the voltage.

VSEL Function

The VSEL pin is an analog input that sets the 3-wire address for the MAX3948. The pin can be set to either V_{CC}, V_{CC} x 2/3, V_{CC}/3, or to GND (Table 2). This allows up to four MAX3948s to be operated on a single 3-wire bus, each with their own address.

Table 2. 3-Wire Address Selection

VSEL	ADDR[6:5]
V_{CC}	11b
V_{CC} x 2/3	10b
V_{CC}/3	01b
GND	00b

Eye Safety and Output Control Circuitry

The safety and output control circuitry includes the disable pin (DISABLE) and enable bit (TX_EN), along with a FAULT indicator and fault detectors (Figure 4). A fault condition triggers the FAULT pin to go high and a corresponding bit is set in the TXSTAT1 register. The MAX3948 has two types of faults: hard faults and soft faults. Hard faults are maskable, trigger the FAULT pin (transitions high), disable the outputs and are stored in the TXSTAT1 register. Soft faults serve as warnings, do not disable the outputs, and are stored in the TXSTAT2 register.

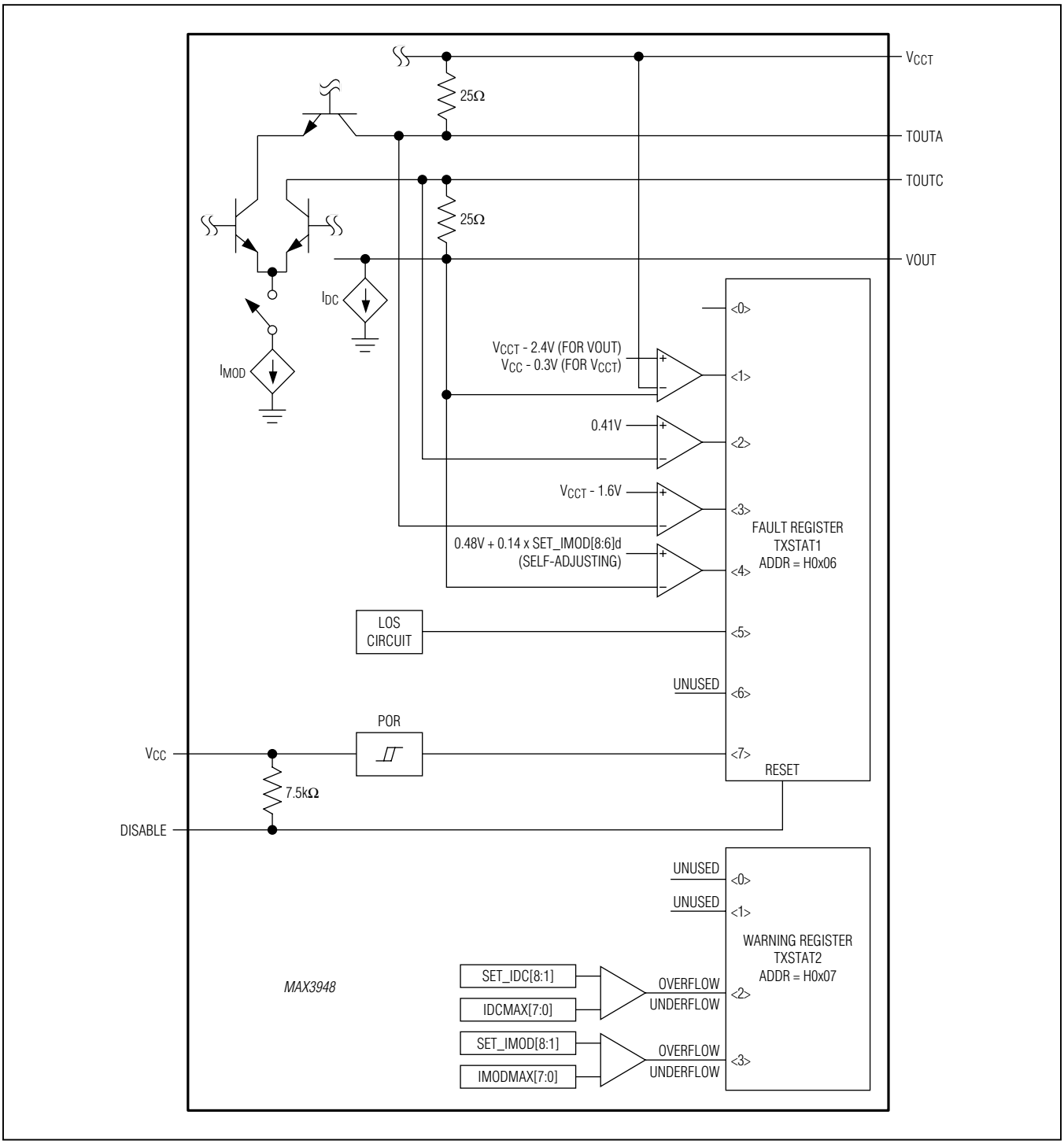


Figure 4. Eye Safety Circuitry

The FAULT pin is a latched output that can be cleared by toggling the DISABLE pin. Toggling the DISABLE pin also clears the TXSTAT1 and TXSTAT2 registers. A single-point failure can be a short to V_{CC} or GND. Table 3 shows the circuit response to various single-point failures.

Table 3. Circuit Response to Single-Point Failure

PIN	NAME	SHORT TO V_{CC}	SHORT TO GND	OPEN
1	DISABLE	Disabled	Normal (Note 1). Can only be disabled by other means.	Disabled
2	VSEL	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
3	FAULT	Normal (Note 2)	Normal (Note 1)	Normal (Note 2)
4	BMON	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
5, 8	V_{CCT}	Normal	Disabled—Fault (external supply shorted) (Note 3)	Redundant path (Note 4)
6	TOUTA	Laser modulation current is reduced	Disabled (hard fault)	Laser modulation current is reduced or disabled (hard fault)
7	TOUTC	Laser modulation current is reduced or off	Disabled (hard fault)	Laser modulation current is reduced or disabled (hard fault)
9	VOUT	IDC is on, but not delivered to the laser; no fault	Disabled (hard fault)	Disabled (hard fault)
10	CSEL	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
11	SDA	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
12	SCL	Normal (Note 2)	Normal (Note 2)	Normal (Note 2)
13, 16	V_{CC}	Normal	Disabled—Hard fault (external supply shorted) (Note 3)	Redundant path (Note 4)
14	TIN+	Disabled (hard fault)	Disabled (hard fault)	Normal (Note 2) or disabled (hard fault)
15	TIN-	Disabled (hard fault)	Disabled (hard fault)	Normal (Note 2) or disabled (hard fault)

Note 1: Normal operation—Does not affect the laser power.
Note 2: Pin functionality might be affected, which could affect laser power/performance.
Note 3: Supply-shorted current is assumed to be primarily on the circuit board (outside this device) and the main supply is collapsed by the short.
Note 4: Normal in functionality, but performance could be affected.
Warning: Shorted to V_{CC} or shorted to ground on some pins can violate the *Absolute Maximum Ratings*.

3-Wire Interface

The MAX3948 implements a proprietary 3-wire digital interface. An external controller generates the clock. The 3-wire interface consists of an SDA bidirectional data line, a SCL clock signal input, and a CSEL chip-select input (active high). The external master initiates a data transfer by asserting the CSEL pin. The master starts to generate a clock signal after the CSEL pin has been set to a logic-high. All data transfers are most significant bit (MSB) first.

Protocol

Each operation consists of 16-bit transfers (15-bit address/data, 1-bit RWN). The bus master generates 16 clock cycles to SCL. All operations transfer 8 bits to the MAX3948. The RWN bit determines if the cycle is read or write (Table 5).

Register Addresses

The MAX3948 contains 13 registers available for programming. Table 6 shows the registers and addresses.

Write Mode (RWN = 0)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 16 bits (MSB first) to the SDA line at the falling edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 5 shows the interface timing.

Read Mode (RWN = 1)

The master generates 16 clock cycles at SCL in total. The master outputs a total of 8 bits (MSB first) to the SDA line at the falling edge of the clock. The SDA line is released after the RWN bit has been transmitted. The slave outputs 8 bits of data (MSB first) at the rising edge of the clock. The master closes the transmission by setting CSEL to 0. Figure 5 shows the interface timing.

Mode Control

Normal mode allows read-only instruction for all registers. Only the MODINC and DCINC registers can be updated during normal mode. Doing so speeds up the laser control update through the 3-wire interface by a factor of two. The normal mode is the default mode.

Setup mode allows the master to write unrestricted data into any register except the status (TXSTAT1, TXSTAT2) registers. To enter the setup mode, the MODECTRL register (address = H0x0F) must be set to 12h. After the MODECTRL register has been set to 12h, the next operation is unrestricted. The setup mode is automatically exited after the operation is finished. This sequence must be repeated if further unrestricted settings are necessary.

Broadcast mode allows for faster configuration of multiple MAX3948 ICs by causing the address selection bits (ADDR[6:5]) to be ignored so all MAX3948s on the bus can be written to simultaneously.

A block write in broadcast mode can start at any of the addresses in Table 4. The block write is achieved by holding the CSEL pin high to lengthen the SPI cycle. The register address increments automatically through the sequence listed in Table 4 and wraps from TXCTRL to FMSK. The block write ends once the CSEL pin is asserted low.

Table 4. Broadcast Mode Register Initialization Sequence

ADDRESS	NAME
H0x0F	FMSK
H0x10	SET_TXDE
H0x11	SET_TXEQ
H0x0A	IMODMAX
H0x0B	IDCMAX
H0x08	SET_IDC
H0x09	SET_IMOD
H0x05	TXCTRL

Table 5. Digital Communication Word Structure

BIT															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR[6:0]							RWN	DATA[7:0]							

Table 6. Register Descriptions and Addresses

ADDRESS	NAME	FUNCTION
H0x05	TXCTRL	Transmitter Control Register
H0x06	TXSTAT1	Transmitter Status Register 1
H0x07	TXSTAT2	Transmitter Status Register 2
H0x08	SET_IDC	DC Current Setting Register
H0x09	SET_IMOD	Modulation Current Setting Register
H0x0A	IMODMAX	Maximum Modulation Current Setting Register
H0x0B	IDCMAX	Maximum DC Current Setting Register
H0x0C	MODINC	Modulation Current Increment Setting Register
H0x0D	DCINC	DC Current Increment Setting Register
H0x0E	MODECTRL	Mode Control Register
H0x0F	FMSK	Fault Mask Register
H0x10	SET_TXDE	Transmitter Deemphasis Control Register
H0x11	SET_TXEQ	Transmitter Equalization Control Register

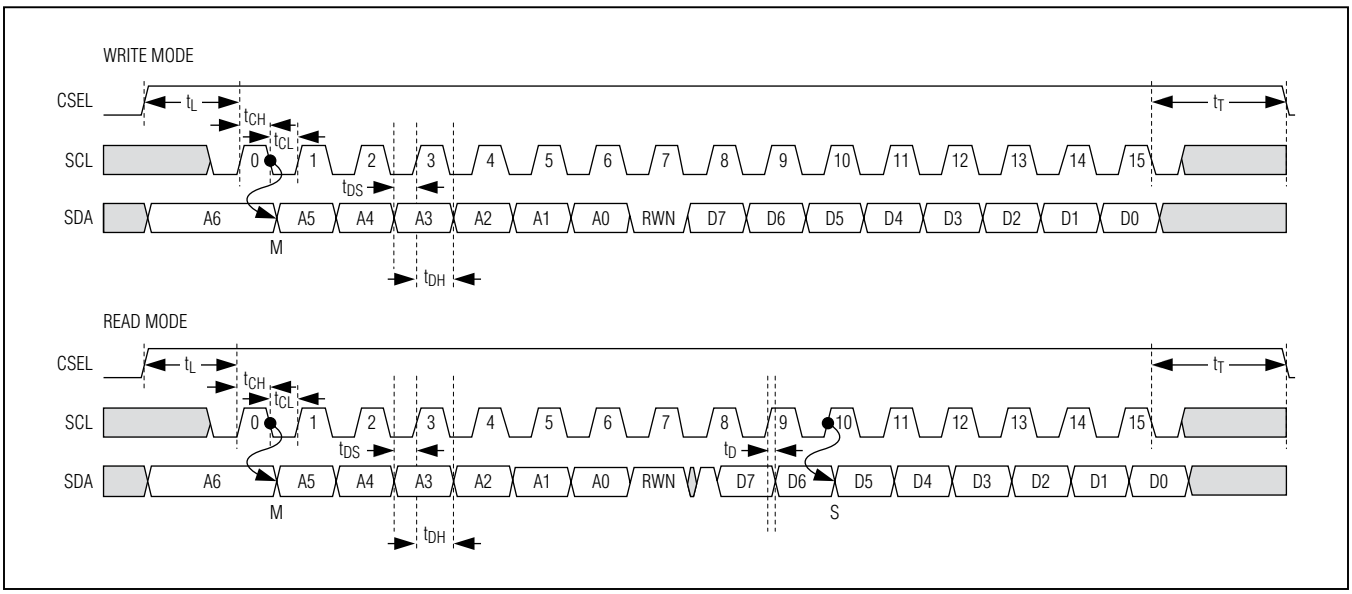


Figure 5. Timing for 3-Wire Digital Interface

Register Descriptions

Transmitter Control Register (TXCTRL), Address: H0x05

Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Name	RESERVED	RESERVED	RESERVED	TXDE_MD[1]	TXDE_MD[0]	SOFTRES	TX_POL	TX_EN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	1	0

The TXCTRL register sets the device's operation.

BIT	NAME	DESCRIPTION
D[7:5]	RESERVED	Reserved Bits. **The default state for these bits is 0 and they must be kept 0 when the register is accessed for a write operation.**
D[4:3]	TXDE_MD	Controls the mode of the transmit output deemphasis circuitry. 00 = Deemphasis is fixed at 6% of the modulation amplitude 01 = Deemphasis is fixed at 3% of the modulation amplitude 10 = Deemphasis is programmed by SET_TXDE register setting (3% to 9%) 11 = Deemphasis is at its maximum of ~9%
D2	SOFTRES	Resets all registers to their default values (TXCTRL[1:0] must be = 10b during the write to SOFTRES for the registers to be set to their default values). 0 = Normal operation 1 = Reset
D1	TX_POL	Controls the polarity of the transmit signal path. 0 = Inverse 1 = Normal operation
D0	TX_EN	Enables or disables the transmit circuitry. 0 = Disabled 1 = Enabled

Transmitter Status Register 1 (TXSTAT1), Address: H0x06

Bit	D7 (STICKY)	D6 (STICKY)	D5 (STICKY)	D4 (STICKY)	D3 (STICKY)	D2 (STICKY)	D1 (STICKY)	D0 (STICKY)
Bit Name	FST[7]	FST[6]	FST[5]	FST[4]	FST[3]	FST[2]	FST[1]	FST[0]
Read/Write	R	R	R	R	R	R	R	R
POR State	1	X	X	X	X	X	X	X
Reset Upon Read	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

The TXSTAT1 register is a device status register.

BIT	NAME	DESCRIPTION
D7	FST[7]	When the V_{CC} supply voltage is below 2.3V, the POR circuitry reports a FAULT and **communication to the SPI cannot be performed**. Once the V_{CC} supply voltage is above 2.75V, the POR resets all registers to their default values and the FAULT latch is cleared.
D6	FST[6]	Reserved.
D5	FST[5]	Indicates low or no AC signal at the inputs, a hard fault is reported unless masked.
D4	FST[4]	Indicates VOUT too low condition. Intended to be used as a warning/soft fault rather than a hard fault. In normal operation, FMSK[4] should be kept at logic 1 to convert this to a soft fault behavior. Self-adjustable threshold = 0.48V + 0.14V x SET_IMOD[8:6] (decimal value 0 to 7). A logic 1 can indicate marginal power-supply headroom.
D3	FST[3]	Indicates TOUTA open or shorted to GND condition, threshold = V_{CCT} - 1.6V, a hard fault is reported unless masked.
D2	FST[2]	Indicates TOUTC open or shorted to GND condition, threshold = 0.41V, a hard fault is reported unless masked.
D1	FST[1]	Indicates VOUT or V_{CCT} open or shorted to GND conditions, threshold (V_{CCT}) = V_{CC} - 0.3V, threshold (VOUT) = V_{CCT} - 2.4V, a hard fault is reported unless masked.
D0	FST[0]	Copy of a FAULT signal.

Transmitter Status Register 2 (TXSTAT2), Address: H0x07

Bit	D7	D6	D5	D4	D3 (STICKY)	D2 (STICKY)	D1	D0
Bit Name	X	X	X	X	IMODERR	IDCERR	X	X
Read/Write	X	X	X	X	R	R	X	X
POR State	X	X	X	X	0	0	X	X
Reset Upon Read	X	X	X	X	Yes	Yes	X	X

The TXSTAT2 register is a device status register.

BIT	NAME	DESCRIPTION
D3	IMODERR	Modulation current overflow (on increment) or underflow (on decrement) error. Overflow occurs if result > IMODMAX. In overflow condition, SET_IMOD[8:1] = IMODMAX[7:0]. Underflow occurs if result < 0. In underflow condition, SET_IMOD[8:0] = 0.
D2	IDCERR	DC current overflow (on increment) or underflow (on decrement) error. Overflow occurs if result > IDCMAX. In overflow condition, SET_IDC[8:1] = IDCMAX[7:0]. Underflow occurs if result < 0. In underflow condition, SET_IDC[8:0] = 0.

DC Current Setting Register (SET_IDC), Address: H0x08

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_IBIAS[8]	SET_IBIAS[7]	SET_IBIAS[6]	SET_IBIAS[5]	SET_IBIAS[4]	SET_IBIAS[3]	SET_IBIAS[2]	SET_IBIAS[1]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	1

The SET_BIAS register sets the laser bias current DAC.

BIT	NAME	DESCRIPTION
D[7:0]	SET_IBIAS[8:1]	The bias current DAC is controlled by a total of 9 bits. The SET_IBIAS[8:1] bits are used to set the bias current with even denominations from 0 to 510 bits. The LSB (SET_IBIAS[0]) bit is controlled by the BIASINC register and is used to set the odd denominations in the SET_IBIAS[8:0]. Any direct write to SET_IBIAS[8:1] resets the LSB.

Modulation Current Setting Register (SET_IMOD), Address: H0x09

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_IMOD[8]	SET_IMOD[7]	SET_IMOD[6]	SET_IMOD[5]	SET_IMOD[4]	SET_IMOD[3]	SET_IMOD[2]	SET_IMOD[1]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	1	0	0

The SET_IMOD register sets the laser modulation current DAC.

BIT	NAME	DESCRIPTION
D[7:0]	SET_IMOD[8:1]	The mod current DAC is controlled by a total of 9 bits. The SET_IMOD[8:1] bits are used to set the modulation current with even denominations from 0 to 510 bits. The LSB (SET_IMOD[0]) bit is controlled by the MODINC register and is used to set the odd denominations in the SET_IMOD[8:0]. Any direct write to SET_IMOD[8:1] resets the LSB.

Maximum Modulation Current Setting Register (IMODMAX), Address: H0x0A

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IMODMAX[7]	IMODMAX[6]	IMODMAX[5]	IMODMAX[4]	IMODMAX[3]	IMODMAX[2]	IMODMAX[1]	IMODMAX[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	1	0	0	0	0	0

The IMODMAX register sets the upper limit of modulation current.

BIT	NAME	DESCRIPTION
D[7:0]	IMODMAX[7:0]	The IMODMAX register is an 8-bit register that can be used to limit the maximum modulation current. IMODMAX[7:0] is continuously compared to SET_IMOD[8:1].

Maximum DC Current Setting Register (IDCMAX), Address: H0x0B

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	IBIASMAX[7]	IBIASMAX[6]	IBIASMAX[5]	IBIASMAX[4]	IBIASMAX[3]	IBIASMAX[2]	IBIASMAX[1]	IBIASMAX[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	1	0	0	0	0	0

The IBIASMAX register sets the upper limit of bias current.

BIT	NAME	DESCRIPTION
D[7:0]	IBIASMAX[7:0]	The IBIASMAX register is an 8-bit register that can be used to limit the maximum bias current. IBIASMAX[7:0] is continuously compared to SET_IBIAS[8:1].

Modulation Current Increment Setting Register (MODINC), Address: H0x0C

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_IMOD[0]	X	X	MODINC[4]	MODINC[3]	MODINC[2]	MODINC[1]	MODINC[0]
Read/Write	R	X	X	R/W	R/W	R/W	R/W	R/W
POR State	0	X	X	0	0	0	0	0

The MODINC register increments/decrements the SET_IMOD register.

BIT	NAME	DESCRIPTION
D7	SET_IMOD[0]	LSB of SET_IMOD register
D[4:0]	MODINC	This string of bits is used to increment or decrement the modulation current. When written to, the SET_IMOD[8:0] bits are updated. MODINC[4:0] are a two's complement string.

DC Current Increment Setting Register (DCINC), Address: H0x0D

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SET_IBIAS[0]	X	X	BIASINC[4]	BIASINC[3]	BIASINC[2]	BIASINC[1]	BIASINC[0]
Read/Write	R	X	X	R/W	R/W	R/W	R/W	R/W
POR State	0	X	X	0	0	0	0	0

The BIASINC register increments/decrements the SET_IBIAS register.

BIT	NAME	DESCRIPTION
D7	SET_IBIAS[0]	LSB of SET_IBIAS register.
D[4:0]	BIASINC	This string of bits is used to increment or decrement the modulation current. When written to, the SET_IBIAS[8:0] bits are updated. BIASINC[4:0] are a two's complement string.

Mode Control Register (MODECTRL), Address: H0x0E

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	MODECTRL[7]	MODECTRL[6]	MODECTRL[5]	MODECTRL[4]	MODECTRL[3]	MODECTRL[2]	MODECTRL[1]	MODECTRL[0]
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	Yes*	Yes*	Yes*	Yes*	Yes*	Yes*	Yes*	Yes*

**All three modes reset back to 0h on the next 3-wire access.*

The MODECTRL register set the operational mode of the 3-wire control for the MAX3948.

BIT	NAME	DESCRIPTION
D[7:0]	MODECTRL[7:0]	The MODECTRL register enables the user to switch between normal and setup modes. The setup mode is achieved by setting this register to 12h. MODECTRL must be updated before each write operation. Exceptions are MODINC and DCINC, which can be updated in normal mode. 00h: normal mode 12h: setup mode C9h: broadcast mode

Fault Mask Register (FMSK), Address: H0x0F

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	RESERVED	FMSK[5]	FMSK[4]	FMSK[3]	FMSK[2]	FMSK[1]	FMSK[0]
Read/Write	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	X	1	1	0	0	0	0	0
Reset Upon Read	X	No	No	No	No	No	No	No

The FMSK register sets masking for the fault circuitry.

BIT	NAME	DESCRIPTION
D6	RESERVED	Reserved. **This bit must be kept at logic 1 for all operations.**
D5	FMSK[5]	Input LOS FAULT condition mask. 0 = No mask 1 = Mask
D4	FMSK[4]	VOUT too low FAULT condition mask. This condition is intended to behave like a warning/soft fault in normal operation. In normal operation, FMSK[4] should be kept at logic 1. 0 = No mask 1 = Mask
D3	FMSK[3]	TOUTA open or shorted to GND FAULT condition mask. 0 = No mask 1 = Mask
D2	FMSK[2]	TOUTC open or shorted to GND FAULT condition mask. 0 = No mask 1 = Mask
D1	FMSK[1]	VOUT or V_{CCT} open or shorted to GND FAULT conditions mask. 0 = No mask 1 = Mask
D0	FMSK[0]	Masks the FAULT latch signal, which controls the output stage on/off behavior. 0 = No mask 1 = Mask When FMSK[0] = 1, output stage behavior becomes independent of FAULT conditions and is only controlled by DISABLE pin and TX_EN bit. Masking this bit has no impact on normal reporting of fault status bits and assertion of the FAULT pin.

Transmitter Deemphasis Control Register (SET_TXDE), Address: H0x10

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	SET_TXDE[6]	SET_TXDE[5]	SET_TXDE[4]	SET_TXDE[3]	SET_TXDE[2]	SET_TXDE[1]	SET_TXDE[0]
Read/Write	X	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	X	0	0	0	0	0	1	0

The SET_TXDE register sets the deemphasis amount for the transmitter when TXDE_MD[1:0] is 10b.

BIT	NAME	DESCRIPTION
D[6:0]	SET_TXDE[6:0]	This is a 7-bit register used to control the amount of deemphasis on the transmitter output. When calculating the total modulation current, the amount of deemphasis must be taken into account. Deemphasis is set as a percentage of modulation current.

Transmitter Equalization Control Register (SET_TXEQ), Address: H0x11

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	X	X	X	X	X	X	SET_TXEQ[1]	SET_TXEQ[0]
Read/Write	X	X	X	X	X	X	R/W	R/W
POR State	X	X	X	X	X	X	0	0

The SET_TXEQ register sets the equalization amount for the transmitter input.

BIT	NAME	DESCRIPTION
D[1:0]	SET_TXEQ	This is a 2-bit register used to control the amount of equalization on the transmitter input. See Table 1 for more information.

Design Procedure

Programming Modulation Current

1) IMODMAX[7:0] = Maximum_Modulation_Current_Value

2) SET_IMOD_n[8:0] = Present_Modulation_Current_Value

   Note: SET_IMOD[8:1] are the bits that can be manually written. SET_IMOD[0] can only be updated using the MODINC register.

   When implementing modulation current temperature compensation, it is recommended to use the MODINC register, which guarantees the fastest modulation current update.

3) $MODINC_n$[4:0] = New_Increment_Value

   The device performs the following operation when $MODINC_n$[4:0] is written to:

   If (SET_IMOD_n[8:1] ≤ IMODMAX[7:0]), then

   (SET_IMOD_n[8:0] = SET_IMOD_{n-1}[8:0] + $MODINC_n$[4:0])

   else (SET_IMOD_n[8:1] = IMODMAX[7:0])

   The modulation DAC current can be calculated using the following equation:

   $$\text{IMOD DAC Current} = I_{MOD} = (16 + \text{SET\_IMOD[8:0]}) \times 247\mu A$$

   The net modulation current (P-P) seen at the laser when driven differentially is calculated using the following equation:

   $$LD_{MOD} = I_{MOD} \times (1 - DE) \times 50/(50 + R)$$

   where R is the differential load impedance of the laser plus any added series resistance, and DE is the deemphasis factor controlled by the TX_DEMD[1:0] bits.

4) TXCTRL[4:3] = 00, DE = 0.0625 (~ 6% deemphasis case). In this mode, the device calculates and sets SET_TXDE[6:0] = SET_IMOD[8:2]. SET_TXDE is not accessible for external write.

5) TXCTRL[4:3] = 01, DE = 0.03125 (~ 3% deemphasis case). In this mode, the device calculates and sets SET_TXDE[6:0] = SET_IMOD[8:3]. SET_TXDE is not accessible for external write.

6) TXCTRL[4:3] = 10, SET_TXDE can be externally set to any value ≥ SET_IMOD[8:3]:

   $$I_{DE} = (2 + \text{SET\_TXDE[6:0]}) \times 61.8\mu A$$

   In this case $DE = I_{DE}/I_{MOD}$. The value of the DE factor starts close to 0.03 and can go up to 0.09 as the value of SET_TXDE[6:0] is increased. Once the DE ratio is close to 0.09, the I_{DE} saturates and a further increase in SET_TXDE[6:0] value does not change I_{DE} much.

7) TXCTRL[4:3] = 11, DE = 0.09 (~ 9% deemphasis case). In this mode, the device calculates and sets the SET_TXDE[6:0] = 127. SET_TXDE is not accessible for external write.

Programming DC Current

1) IDCMAX[7:0] = Maximum_DC_Current_Value

2) SET_IDC_n[8:0] = Present_ DC _Current_Value

   Note: SET_IDC[8:1] are the bits that can be manually written. SET_IDC[0] can only be updated using the DCINC register.

   When implementing laser bias current temperature compensation, it is recommended to use the DCINC register, which guarantees the fastest modulation current update.

3) $DCINC_n$[4:0] = New_Increment_Value

   The device performs the following operation when $DCINC_n$[4:0] is written to:

   If (SET_IDC_n[8:1] ≤ IDCMAX[7:0]), then

   (SET_IDC_n[8:0] = SET_IDC_{n-1}[8:0] + $DCINC_n$[4:0])

   else (SET_IDC_n[8:1] = IDCMAX[7:0])

   The DC DAC current can be calculated using the following equation:

   $$\text{DC DAC Current} = I_{DC} = (16 + \text{SET\_IDC[8:0]}) \times 116\mu A$$

   The net DC current seen at the laser when driven differentially is calculated using the following equation:

   $$LD_{DC} = I_{DC} + I_{MOD} \times (DE + R \times (1 - DE)/(50 + R)/2)$$

   where R is the differential load impedance of the laser plus any added series resistance, DE is the deemphasis factor controlled by the TX_DEMD[1:0] bits, and I_{MOD} is the modulation DAC current.

Applications Information

Laser Safety and IEC 825

Using the MAX3948 laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each user must determine the level of fault tolerance required by the application, recognizing that Maxim products are neither designed nor authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application in which the failure of a Maxim product could create a situation where personal injury or death could occur.

Table 7. Register Summary

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Transmitter Control Register **Address = H0x05**	TXCTRL	R	R/W	7	Reserved	0	Must be kept at 0
		R	R/W	6	Reserved	0	Must be kept at 0
		R	R/W	5	Reserved	0	Must be kept at 0
		R	R/W	4	TXDE_MD[1]	0	Tx deemphasis control
		R	R/W	3	TXDE_MD[0]	0	Tx deemphasis control
		R	R/W	2	SOFTRES	0	Global digital reset
		R	R/W	1	TX_POL	1	Tx polarity 0: inverse, 1: normal
		R	R/W	0	TX_EN	0	Tx control 0: disable, 1: enable
Transmitter Status Register 1 **Address = H0x06**	TXSTAT1	R	R	7 (sticky)	FST[7]	1	POR→V_{CC} low-limit violation
		R	R	6 (sticky)	FST[6]	X	Reserved
		R	R	5 (sticky)	FST[5]	X	Low or no AC signal at input
		R	R	4 (sticky)	FST[4]	X	VOUT too low
		R	R	3 (sticky)	FST[3]	X	TOUTA open or shorted to GND
		R	R	2 (sticky)	FST[2]	X	TOUTC open or shorted to GND
		R	R	1 (sticky)	FST[1]	X	VOUT/V_{CCT} open or shorted to GND
		R	R	0 (sticky)	FST[0]	X	Copy of FAULT signal

Table 7. Register Summary (continued)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Transmitter Status Register 2 **Address = H0x07**	TXSTAT2	R	R	3 (sticky)	IMODERR	0	Modulation current overflow (on increment) or underflow (on decrement) error. Overflow occurs if result > IMODMAX. Underflow occurs if result < 0.
		R	R	2 (sticky)	IDCERR	0	DC current overflow (on increment) or underflow (on decrement) error. Overflow occurs if result > IDCMAX. Underflow occurs if result < 0.
DC Current Setting Register **Address = H0x08**	SET_IDC	R	R/W	7	SET_IDC[8]	0	MSB DC DAC
		R	R/W	6	SET_IDC[7]	0	
		R	R/W	5	SET_IDC[6]	0	
		R	R/W	4	SET_IDC[5]	0	
		R	R/W	3	SET_IDC[4]	0	
		R	R/W	2	SET_IDC[3]	0	
		R	R/W	1	SET_IDC[2]	0	
		R	R/W	0	SET_IDC[1]	1	
Modulation Current Setting Register **Address = H0x09**	SET_IMOD	R	R/W	7	SET_IMOD[8]	0	MSB modulation DAC
		R	R/W	6	SET_IMOD[7]	0	
		R	R/W	5	SET_IMOD[6]	0	
		R	R/W	4	SET_IMOD[5]	0	
		R	R/W	3	SET_IMOD[4]	0	
		R	R/W	2	SET_IMOD[3]	1	
		R	R/W	1	SET_IMOD[2]	0	
		R	R/W	0	SET_IMOD[1]	0	
Maximum Modulation Current Setting Register **Address = H0x0A**	IMODMAX	R	R/W	7	IMODMAX[7]	0	MSB modulation limit
		R	R/W	6	IMODMAX[6]	0	
		R	R/W	5	IMODMAX[5]	1	
		R	R/W	4	IMODMAX[4]	0	
		R	R/W	3	IMODMAX[3]	0	
		R	R/W	2	IMODMAX[2]	0	
		R	R/W	1	IMODMAX[1]	0	
		R	R/W	0	IMODMAX[0]	0	LSB modulation limit

Table 7. Register Summary (continued)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Maximum DC DAC Current Setting Register **Address = H0x0B**	IDCMAX	R	R/W	7	IDCMAX[7]	0	MSB DC DAC limit
		R	R/W	6	IDCMAX[6]	0	
		R	R/W	5	IDCMAX[5]	1	
		R	R/W	4	IDCMAX[4]	0	
		R	R/W	3	IDCMAX[3]	0	
		R	R/W	2	IDCMAX[2]	0	
		R	R/W	1	IDCMAX[1]	0	
		R	R/W	0	IDCMAX[0]	0	LSB DC DAC limit
Modulation Current Increment Setting Register **Address = H0x0C**	MODINC	R	R	7	SET_IMOD[0]	0	LSB of SET_IMOD DAC register address = H0x09
		R/W	R/W	4	MODINC[4]	0	MSB MOD DAC two's complement
		R/W	R/W	3	MODINC[3]	0	
		R/W	R/W	2	MODINC[2]	0	
		R/W	R/W	1	MODINC[1]	0	
		R/W	R/W	0	MODINC[0]	0	LSB MOD DAC two's complement
DC Current Increment Setting Register **Address = H0x0D**	DCINC	R	R	7	SET_IDC[0]	0	LSB of SET_IDC DAC register address = H0x08
		R/W	R/W	4	DCINC[4]	0	MSB DC DAC two's complement increment/ decrement
		R/W	R/W	3	DCINC[3]	0	
		R/W	R/W	2	DCINC[2]	0	
		R/W	R/W	1	DCINC[1]	0	
		R/W	R/W	0	DCINC[0]	0	LSB DC DAC two's complement increment/ decrement
Mode Control Register **Address = H0x0E**	MODECTRL	R/W	R/W	7	MODECTRL[7]	0	MSB mode control
		R/W	R/W	6	MODECTRL[6]	0	
		R/W	R/W	5	MODECTRL[5]	0	
		R/W	R/W	4	MODECTRL[4]	0	
		R/W	R/W	3	MODECTRL[3]	0	
		R/W	R/W	2	MODECTRL[2]	0	
		R/W	R/W	1	MODECTRL[1]	0	
		R/W	R/W	0	MODECTRL[0]	0	LSB mode control

Table 7. Register Summary (continued)

REGISTER FUNCTION/ ADDRESS	REGISTER NAME	NORMAL MODE	SETUP MODE	BIT NUMBER/ TYPE	BIT NAME	DEFAULT VALUE	NOTES
Fault Mask Register **Address = H0x0F**	FMSK	R	R/W	6	RESERVED	1	Must be kept at logic 1
		R	R/W	5	FMSK[5]	1	MSB Tx fault mask
		R	R/W	4	FMSK[4]	0	
		R	R/W	3	FMSK[3]	0	
		R	R/W	2	FMSK[2]	0	
		R	R/W	1	FMSK[1]	0	
		R	R/W	0	FMSK[0]	0	LSB Tx fault mask
Transmitter Deemphasis Control Register **Address = H0x10**	SET_TXDE	R	R/W	6	SET_TXDE[6]	0	MSB Tx deemphasis
		R	R/W	5	SET_TXDE[5]	0	
		R	R/W	4	SET_TXDE[4]	0	
		R	R/W	3	SET_TXDE[3]	0	
		R	R/W	2	SET_TXDE[2]	0	
		R	R/W	1	SET_TXDE[1]	1	
		R	R/W	0	SET_TXDE[0]	0	LSB Tx deemphasis
Transmitter Equalization Control Register **Address = H0x11**	SET_TXEQ	R	R/W	1	SET_TXEQ[1]	0	Tx equalization control
		R	R/W	0	SET_TXEQ[0]	0	Tx equalization control

Layout Considerations

The data inputs and outputs are the most critical paths for the MAX3948 and great care should be taken to minimize discontinuities on these transmission lines. The following are some suggestions for maximizing the performance of the IC:

- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.
- The data inputs should be wired directly between the module connector and IC without stubs.
- Maintain 100Ω differential transmission line impedance into the IC.
- The data transmission lines to the laser should be kept as short as possible, and must be designed for 50Ω differential or 25Ω single-ended characteristic impedance.
- An uninterrupted ground plane should be positioned beneath the high-speed I/Os.
- Ground path vias should be placed close to the IC and the input/output interfaces to allow a return current path to the IC and the laser.

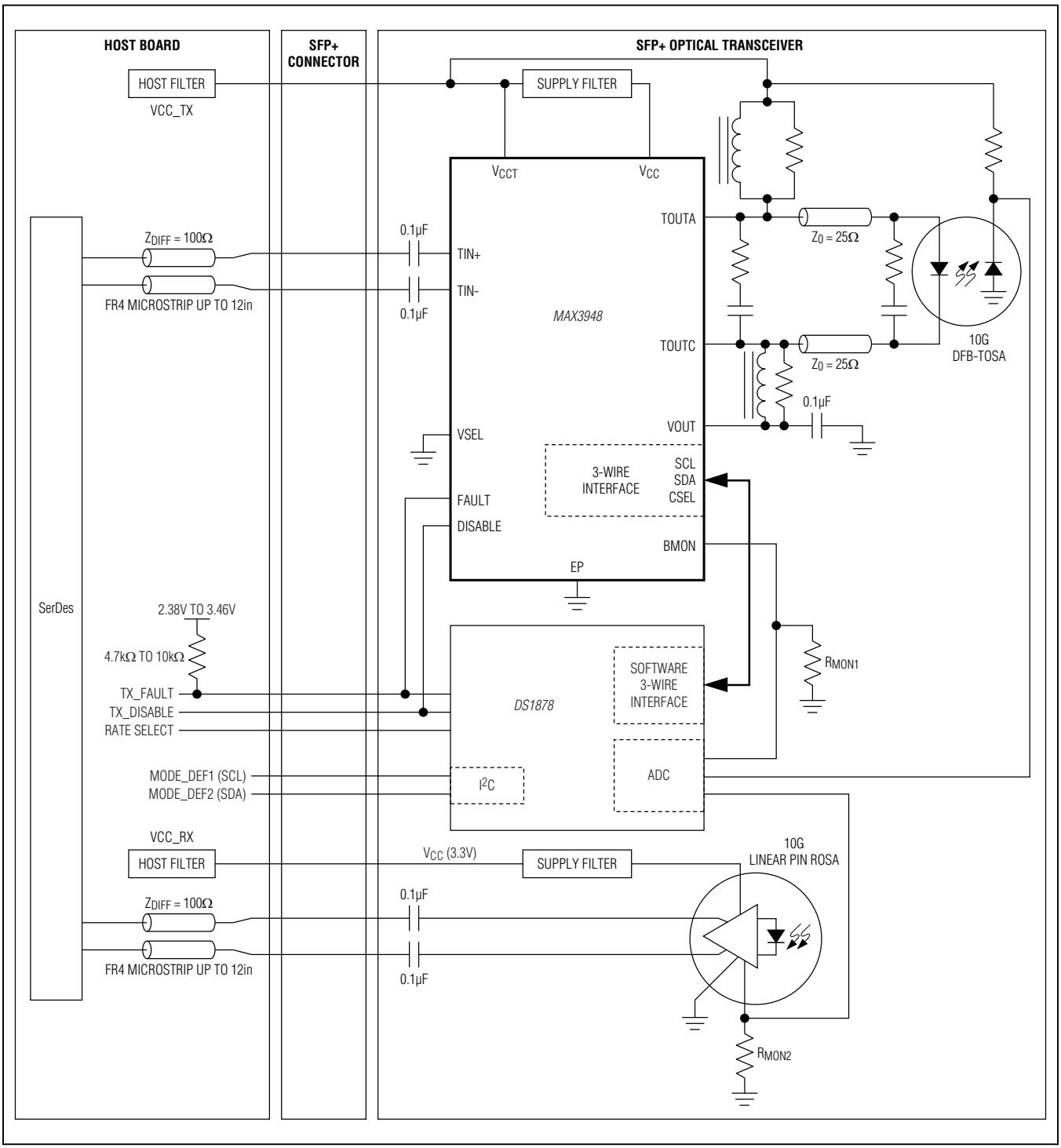
Refer to the schematic and board layers of MAX3948 Evaluation Kit for more information.

Exposed-Pad Package and Thermal Considerations

The exposed pad on the 16-pin TQFN package provides a very low-thermal resistance path for heat removal from the IC. The pad is the only electrical ground on the MAX3948 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations for QFN and Other Exposed-Paddle Packages* for additional information.

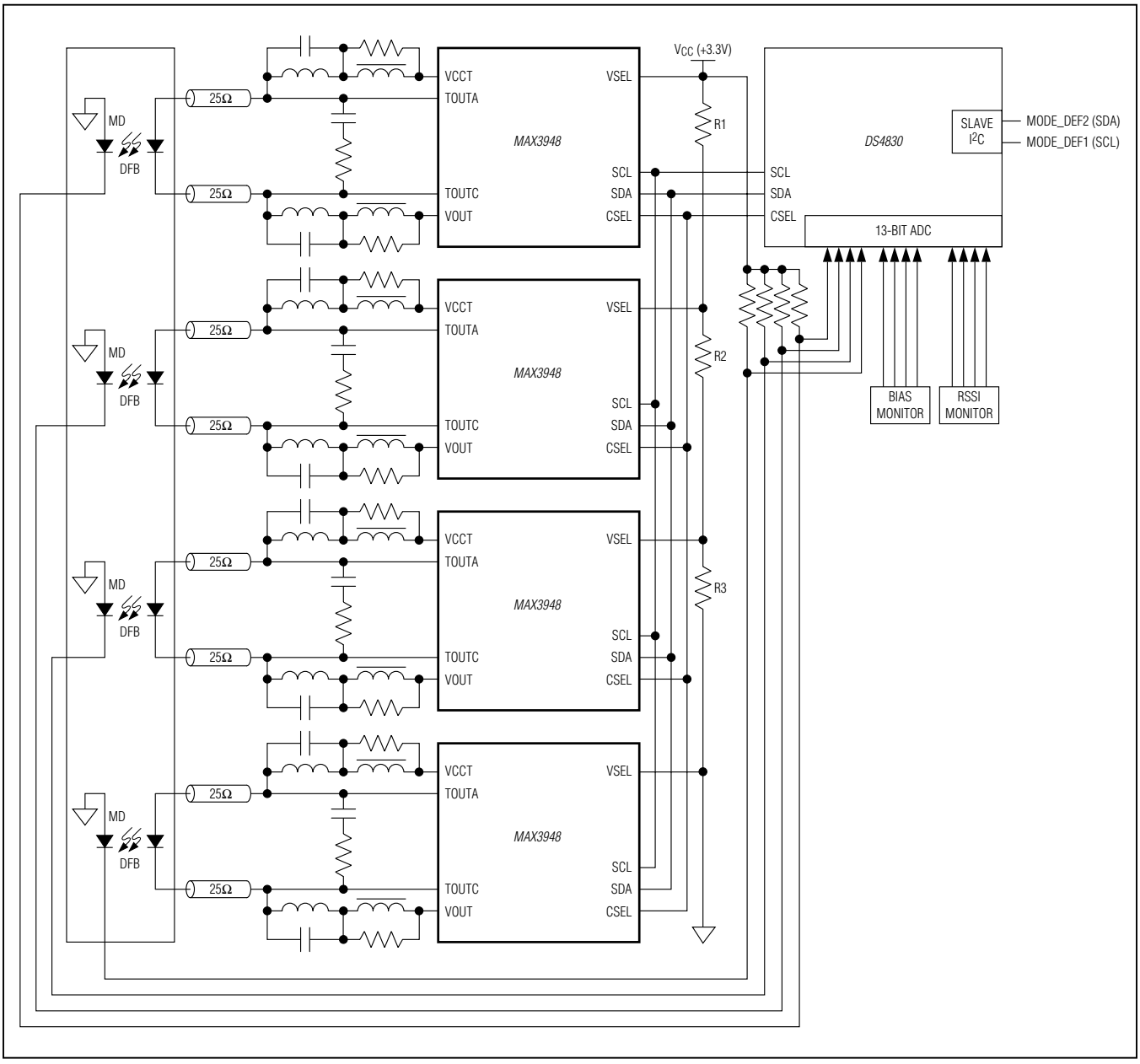
11.3Gbps, Low-Power, DC-Coupled Laser Driver

Typical Application Circuits



11.3Gbps, Low-Power, DC-Coupled Laser Driver

Typical Application Circuits (continued)



11.3Gbps, Low-Power, DC-Coupled Laser Driver

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3948ETE+	-40°C to +85°C	16 TQFN-EP*

Note: *Parts are guaranteed by design and characterization to operate over the -40°C to +95°C ambient temperature range (T_A) and are tested up to +85°C.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Exposed pad.*

Chip Information

PROCESS: SiGe BiPOLAR

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+5	21-0136	90-0032

11.3Gbps, Low-Power, DC-Coupled Laser Driver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	6/12	Updated step 5 in the *Programming Modulation Current* section; updated *Typical Application Circuit*	29, 34

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