19-1314; Rev 5; 8/06

EVALUATION KIT AVAILABLE

+3.0V to +5.5V, 125Mbps to 266Mbps Limiting Amplifiers with Loss-of-Signal Detector

General Description

The MAX3969 is a recommended upgrade for the MAX3964 and MAX3968. The MAX3964A limiting amplifier, with 2mV$_{P-P}$ input sensitivity and PECL data outputs, is ideal for low-cost ATM, FDDI, and Fast Ethernet fiber optic applications.

The MAX3964A features an integrated power detector that senses the input-signal power. It provides a received-signal-strength indicator (RSSI), which is an analog indication of the power level and complementary PECL loss-of-signal (LOS) outputs, which indicate when the power level drops below a programmable threshold. The threshold can be adjusted to detect signal amplitudes as low as 2.7mV$_{P-P}$. An optional squelch function disables switching of the data outputs by holding them at a known state during an LOS condition.

The MAX3968 provides the same functionality as the MAX3964A, but has data-output edge speed suitable for ESCON and 266Mbps fibre channel applications.

The MAX3964A/MAX3968 are available in die form, as tested wafers, and in 20-pin QSOP packages. The MAX3964AETP is available in a 20-pin thin QFN package.

Applications

125Mbps FDDI Receivers

155Mbps LAN ATM Receivers

Fast Ethernet Receivers

ESCON Receivers

155Mbps FTTx Receivers

Features

- **Single Supply: +3.0V to +5.5V**
- **2mV$_{P-P}$ Input Sensitivity**
- **1.2ns Output Edge Speed**
- **Loss-of-Signal Detector with Programmable Threshold**
- **Analog Received-Signal-Strength Indicator**
- **Output Squelch Function**
- **Compatible with 4B/5B Data Coding**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3964AETP	-40°C to +85°C	20 Thin QFN**
MAX3964AETP+	-40°C to +85°C	20 Thin QFN**
MAX3964AC/D	-40°C to +85°C	Dice*
MAX3968CEP	0°C to +70°C	20 QSOP
MAX3968C/D	0°C to +70°C	Dice*

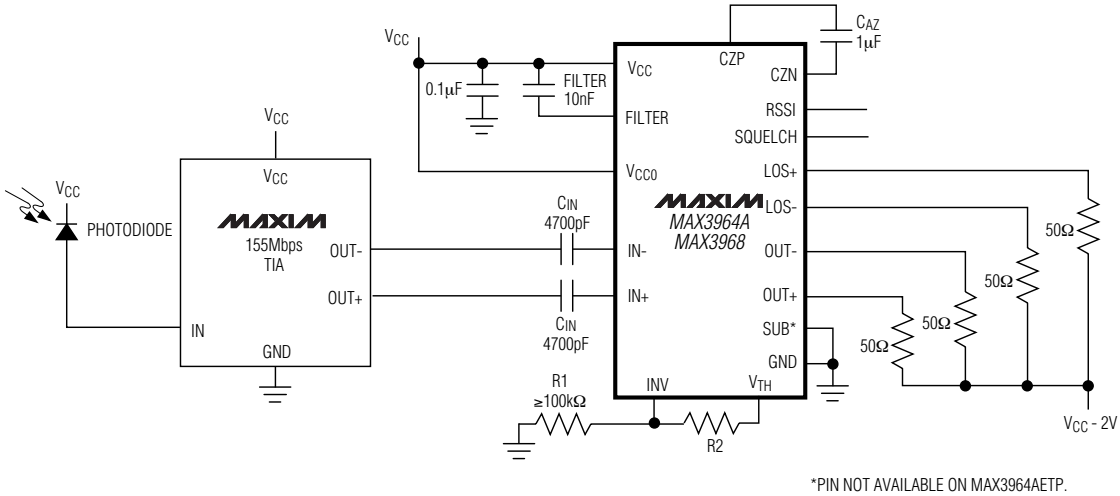
**Dice are designed to operate over a 0°C to +100°C junction temperature (Tj) range, but are tested and guaranteed only at T_A = +25°C.*

***Package Code: T2044-1*

+Denotes lead-free package.

Pin Configurations and Selector Guide appear at end of data sheet.

Typical Operating Circuit



+3.0V to +5.5V, 125Mbps to 266Mbps Limiting Amplifiers with Loss-of-Signal Detector

ABSOLUTE MAXIMUM RATINGS

(SUB, GND tied to ground)
V_{CC}, V_{CCO}.....-0.5V to +7.0V
FILTER, RSSI, IN+, IN-, CZP, CZN, SQUELCH,
LOS+, LOS-, INV, VTH, OUT+, OUT- .....-0.5V to (V_{CC} + 0.5V)
PECL Output Current (OUT+, OUT-, LOS+, LOS-) 50mA
Differential Voltage Between CZP and CZN.....-1.5V to +1.5V
Differential Voltage Between IN+ and IN- .....-1.5V to +1.5V

Continuous Power Dissipation (T_A = +70°C)
20-Lead Thin QFN
(derate 16.9mW/°C above +70°C).....1349mW
20-Pin QSOP (derate 6.7mW/°C above +70°C).....500mW
Operating Temperature Range .....-40°C to +85°C
Operating Junction Temperature Range (die).....-40°C to +150°C
Processing Temperature (die) .....+400°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX3964ACEP/MAX3968CEP

(V_{CC} = +3.0V to +5.5V, PECL outputs terminated with 50Ω to (V_{CC} - 2V), T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	PECL outputs open		22	40	mA
LOS Hysteresis		Input = 3.3mV_{P-P} to 90mV_{P-P} (Note 2)	3.8	5	8.0	dB
SQUELCH Input Current		$V_{SQUELCH}$ = V_{CC}, T_A = +25°C		27	100	µA
PECL Output Voltage High		(Note 3)	-1025		-880	mV
PECL Output Voltage Low		(Note 3)	-1810		-1620	mV
PECL LOS Output Voltage High		(Note 3)	-1035		-880	mV
PECL LOS Output Voltage Low		(Note 3)	-1810		-1620	mV
LOS Assert Accuracy		Input = 7mV_{P-P} or 90mV_{P-P}	-2.5		+2.5	dB
Minimum LOS Assert Input					2.7	mV_{P-P}
Maximum LOS Deassert Input			143			mV_{P-P}
Input Sensitivity				2.0	3.3	mV_{P-P}
Input Overload			1.5			V_{P-P}
Output Transition Time	t_r, t_f	20% to 80% transition time, MAX3964A	0.92	1.2	2.20	ns
		MAX3968	0.4	0.8	1.2	
Pulse-Width Distortion		(Note 4)		50	200	ps

ELECTRICAL CHARACTERISTICS—MAX3964AETP

(V_{CC} = +3.0V to +5.5V, PECL outputs terminated with 50Ω to (V_{CC} - 2V), T_A = -40°C to +85°C. Typical values measured at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

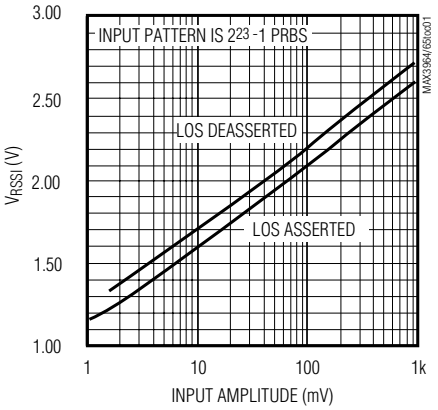
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	PECL outputs open		22	45	mA
LOS Hysteresis		Input = 4.0mV$_{P-P}$ (Note 2)	3.0	5	8.0	dB
SQUELCH Input Current				27	100	µA
PECL Output Voltage High		(Note 3)	-1.085		-0.880	V
PECL Output Voltage Low		(Note 3)	-1.830		-1.550	V
LOS Assert Accuracy		Input = 7mV$_{P-P}$ or 90mV$_{P-P}$, 0°C to +85°C	-3		+3	dB
		Input = 7mV$_{P-P}$ or 90mV$_{P-P}$, -40°C to 0°C	-3.6		+3.6	
Minimum LOS Assert Input					2.7	mV$_{P-P}$
Maximum LOS Deassert Input			143			mV$_{P-P}$
Input Sensitivity				2	4	mV$_{P-P}$
Input Overload			1.5			V$_{P-P}$
Output Transition Time	t_r, t_f	20% to 80%		1.6	2.4	ns
Pulse-Width Distortion		(Note 4)		50	250	ps$_{P-P}$

Note 1: Dice are tested and guaranteed at T_A = +25°C only.
Note 2: LOS hysteresis = 20log($V_{LOS-DEASSERT}$ / $V_{LOS-ASSERT}$).
Note 3: Voltage measurements are relative to supply voltage (V_{CC}).
Note 4: PWD = [(width of wider pulse) - (width of narrower pulse)] / 2, measured with 100Mbps 1-0 pattern.

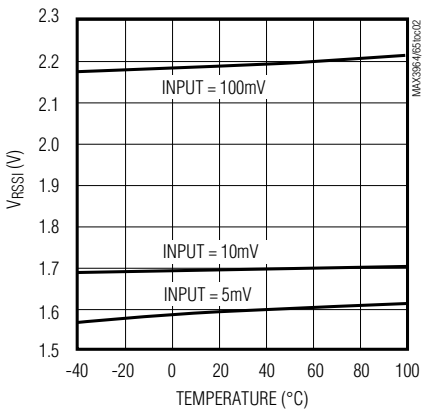
Typical Operating Characteristics

(MAX3964A EV kit, V_{CC} = +3.3V, decibels (dB) calculated as 20 log ΔV, PECL outputs terminated with 50Ω to (V_{CC} - 2V), T_A = +25°C, unless otherwise noted.)

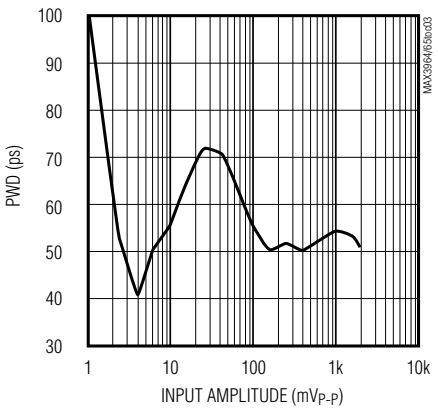
RSSI VOLTAGE vs. INPUT AMPLITUDE



RSSI VOLTAGE vs. TEMPERATURE



PULSE-WIDTH DISTORTION vs. INPUT AMPLITUDE

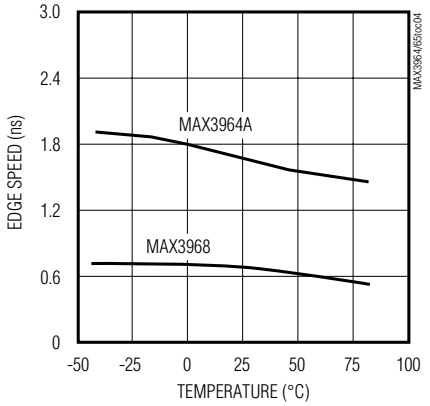


+3.0V to +5.5V, 125Mbps to 266Mbps Limiting Amplifiers with Loss-of-Signal Detector

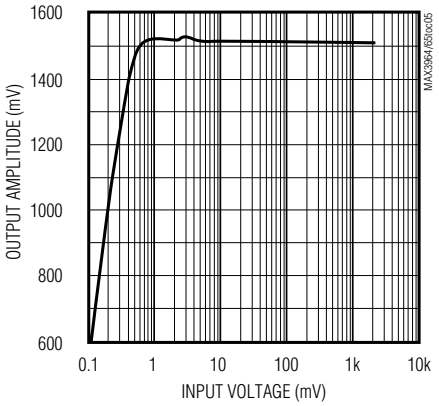
Typical Operating Characteristics (continued)

(MAX3964A EV kit, V_{CC} = +3.3V, decibels (dB) calculated as 20 log ΔV, PECL outputs terminated with 50Ω to (V_{CC} - 2V), T_A = +25°C, unless otherwise noted.)

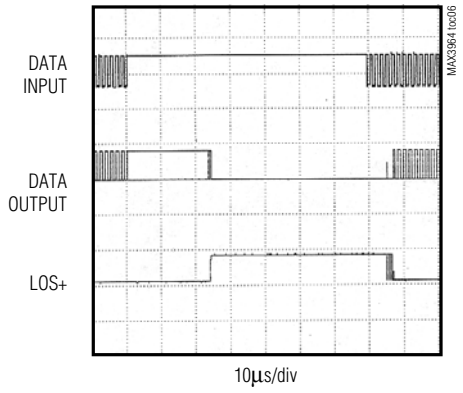
DATA OUTPUT EDGE SPEED (20% to 80%) vs. TEMPERATURE



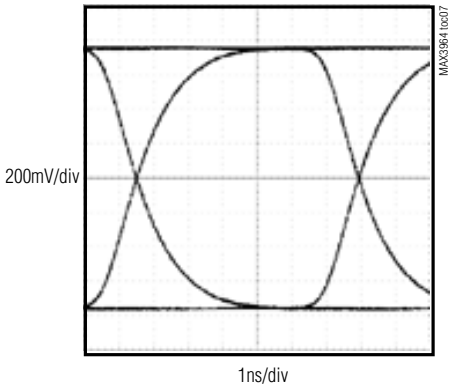
OUTPUT AMPLITUDE vs. INPUT VOLTAGE (DIFFERENTIAL SIGNAL LEVELS)



LOS OPERATION WITH SQUELCH



MAX3964A EYE DIAGRAM (INPUT = 3.3mV)



Pin Description

PIN		NAME	FUNCTION
QSOP	THIN QFN		
1	19	SQUELCH	Squelch Input. The squelch function disables the data outputs by forcing OUT- low and OUT+ high during a loss-of-signal condition. Connect to GND or leave unconnected to disable. Connect to V_{CC} to enable squelching.
2	20	V_{TH}	Output of Internal Op Amp that Sets Loss-of-Signal Threshold Voltage (Figure 1). Connect a resistor from V_{TH} to INV and from INV to ground (minimum resistance 100kΩ) to program the desired threshold voltage.
3	1	INV	Inverting Input of Internal Op Amp that Sets Loss-of-Signal Threshold Voltage (Figure 1). Connect a resistor from V_{TH} to INV and from INV to ground (minimum resistance 100kΩ) to program the desired threshold voltage.
4	2	FILTER	Filter Output of Full-Wave Logarithmic Detectors (FWDs). The FWD outputs are summed together at FILTER to generate the received-signal-strength indicator (RSSI). Connect a capacitor from FILTER to V_{CC} for proper operation.
5	3	RSSI	Received-Signal-Strength Indicator Output. The analog DC voltage at RSSI indicates the input signal power. The RSSI output is reduced approximately 120mV when LOS+ is asserted.
6	4	IN-	Inverting Data Input
7	5	IN+	Noninverting Data Input
8	—	SUB	Substrate. Connect to ground.
9, 10	6, 7, 8	GND	Ground
11	9	CZP	Auto-Zero Capacitor Input. Connect a capacitor between CZP and CZN to determine the offset-correction-loop bandwidth.
12	10	CZN	Auto-Zero Capacitor Input. Connect a capacitor between CZP and CZN to determine the offset-correction-loop bandwidth.
13	11	V_{CCO}	Output Buffer Supply Voltage. Connect to the same potential as V_{CC}, but filter V_{CCO} and V_{CC} separately.
14	12	OUT+	Noninverting PECL Data Output. Terminate with 50Ω to (V_{CC} - 2V).
15	13	OUT-	Inverting PECL Data Output. Terminate with 50Ω to (V_{CC} - 2V).
16	14	LOS-	Inverting Loss-of-Signal Output. LOS- is asserted low when input power drops below the LOS threshold. This pin is PECL compatible and should be terminated with 50Ω to (V_{CC} - 2V).
17	15	LOS+	Noninverting Loss-of-Signal Output. LOS+ is asserted high when input power drops below the LOS threshold. This pin is PECL compatible and should be terminated with 50Ω to (V_{CC} - 2V).
18	16	V_{CCO}	MAX3964A/MAX3968: This pin can be left open or connected to the positive supply.
19, 20	17, 18	V_{CC}	+3.0V to +5.5V Supply Voltage
—	EP	Exposed Pad	Connect the exposed pad to board ground for optional electrical and thermal performance.

+3.0V to +5.5V, 125Mbps to 266Mbps Limiting Amplifiers with Loss-of-Signal Detector

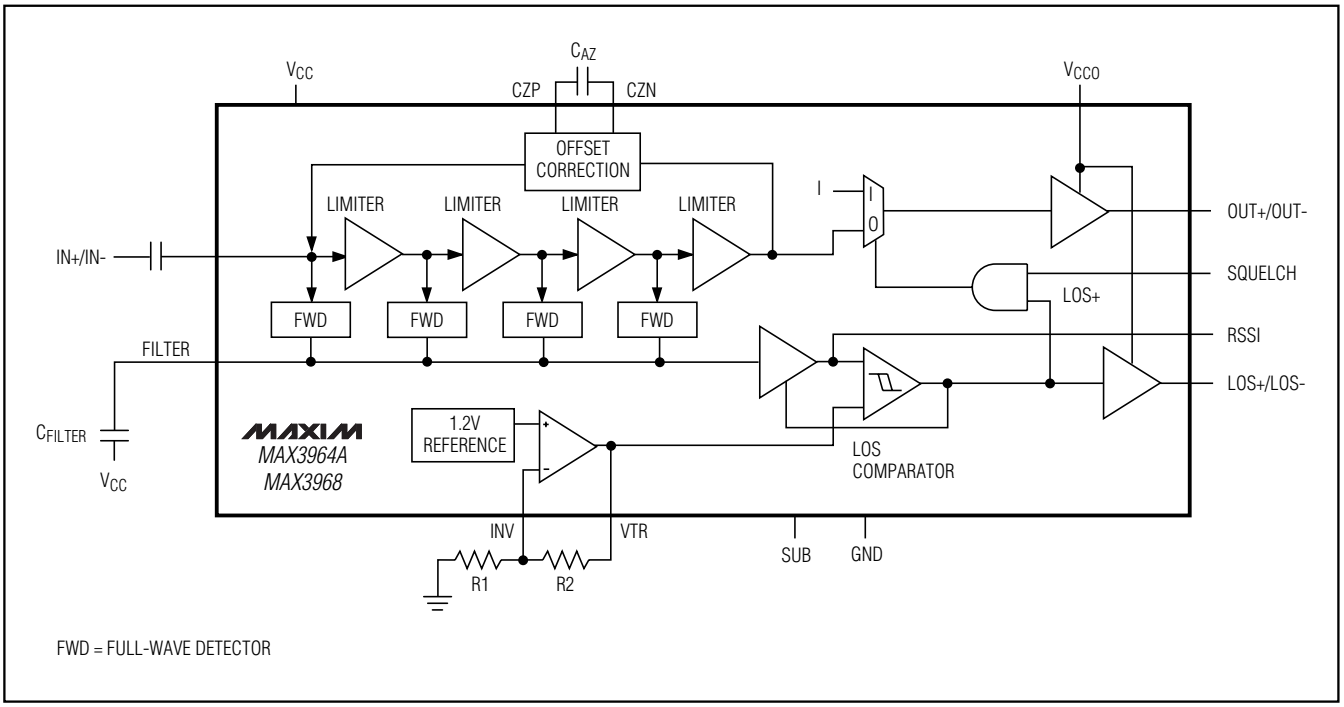


Figure 1. Functional Diagram

Detailed Description

The MAX3964A contains a series of limiting amplifiers and power detectors, offset correction, data-squelch circuitry, and PECL output buffers for data and loss-of-signal (LOS) outputs. The MAX3968 provides PECL LOS outputs with data outputs suitable for 266Mbps. Figure 1 shows a functional diagram of the MAX3964A/MAX3968.

Limiting Amplifiers

A series of four limiting amplifiers provides gain of approximately 65dB.

Power Detector

Each amplifier stage contains a full-wave logarithmic detector (FWD), which indicates the RMS input signal power. The FWD outputs are summed together at the FILTER pin where the signal is filtered by an external capacitor (CFILTER) connected between FILTER and V_{CC}. The FILTER signal generates the RSSI output voltage, which is proportional to the input power in decibels. When LOS+ is low, V_{RSSI} is approximated by the following equation:

$$V_{RSSI}\ (V) = 1.2V + 0.5\log\ (V_{IN})$$

where V_{IN} is measured in mV_{P-P}.

This relation translates to a 25mV increase in V_{RSSI} for every 1dB increase in V_{IN} (25mV/dB). The RSSI output is reduced approximately 120mV when LOS+ is asserted.

PECL Outputs

The data outputs (OUT+, OUT-) and the MAX3964A/MAX3968 loss-of-signal outputs (LOS+, LOS-) are supply-referenced PECL outputs. Standard PECL termination at each output of 50Ω to (V_{CC} - 2V) is recommended for best performance.

Input Offset Correction

A low-frequency feedback loop around the limiting amplifier improves receiver sensitivity and powerdetector accuracy. The offset-correction loop's bandwidth is determined by an external capacitor (CAZ) connected between the CZP and CZN pins.

The offset correction is optimized for data streams with a 50% duty cycle. A different average duty cycle results in increased pulse-width distortion and loss of sensitivity. The offset-correction circuitry is less sensitive to variations of input duty cycle (for example, the 40% to 60% duty cycle encountered in 4B/5B coding) when the input is less than $30mV_{P-P}$.

Loss-of-Signal Comparator

The LOS comparator indicates when the input signal power is below the programmed LOS threshold. To ensure supply and temperature independence, VTH is generated by a 1.2V bandgap reference. The op amp's external gain-setting resistors (R1 and R2) can be chosen to set V_{TH} between 1.2V and 2.4V. To ensure chatter-free operation, the LOS comparator is designed with approximately 5dB of hysteresis.

Squelch

The squelch function disables the data outputs by forcing OUT- low and OUT+ high during a LOS condition. This function ensures that when there is a loss of signal, the limiting amplifier (and all downstream devices) does not respond to input noise or corrupt data. Connect SQUELCH to GND or leave it unconnected to disable squelch. Connect SQUELCH to V_{CC} to enable data squelching.

Applications Information

Program the LOS Threshold

Figure 2 provides information for selecting the LOS threshold voltage (V_{TH}). If R1 is 100kΩ and if the responsivities of the photodiode and preamplifier are known, then the value of R2 can be selected from Figure 2 to provide LOS assert at the desired input power.

Select Capacitors

A typical MAX3964A/MAX3968 implementation requires four external capacitors (C_{AZ}, C_{FILTER}, and two input coupling capacitors). For all applications up to 266Mbps, Maxim recommends the following:

C_{AZ} = 1µF

C_{FILTER} = 10nF

C_{IN} = 4700pF

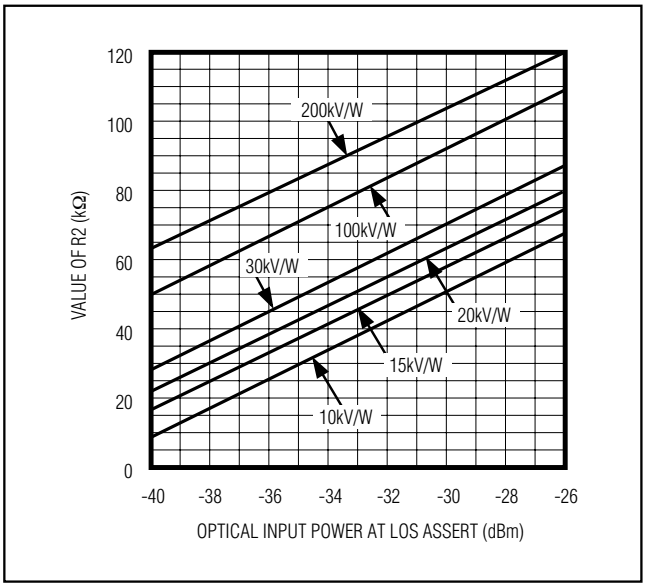


Figure 2. LOS Assert Programming Resistor vs. LOS Assert Power (for Various PIN-TIA Gains)

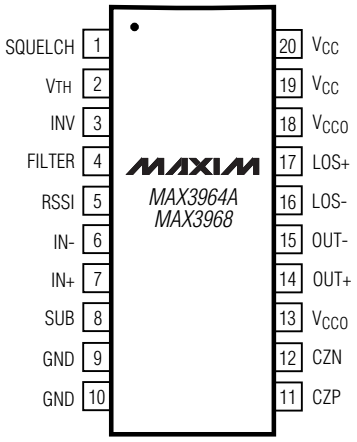
Wire Bonding

For high-current density and reliable operation, the MAX3964A series uses gold metalization. Diepad size is 4mils square with a 6mil pitch. Die thickness is 15mils.

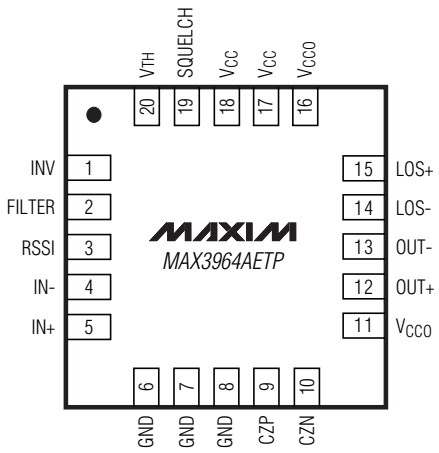
+3.0V to +5.5V, 125Mbps to 266Mbps Limiting Amplifiers with Loss-of-Signal Detector

Pin Configurations

TOP VIEW



QSOP



THIN QFN

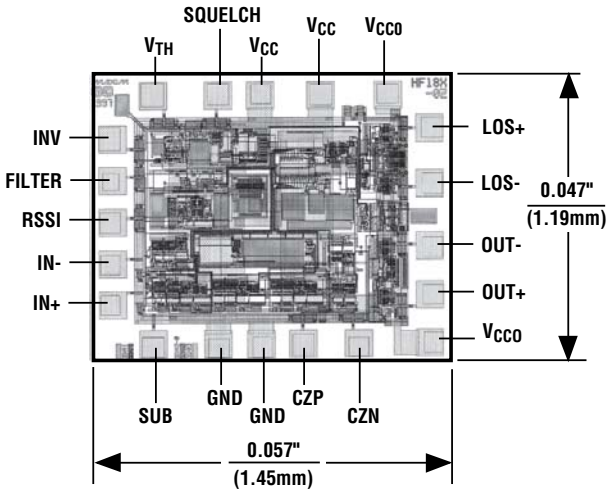
Selector Guide

PART	DATA RATE (Mbps)	LOS OUTPUTS
MAX3964A*	125 to 155	PECL
MAX3968	125 to 266	PECL

**The MAX3964A is functionally equivalent to MAX3964, but offers slightly improved ESD tolerance. The MAX3969 is a recommended upgrade for the MAX3964, MAX3964A, and MAX3968.*

Chip Topography

MAX3964A
MAX3968

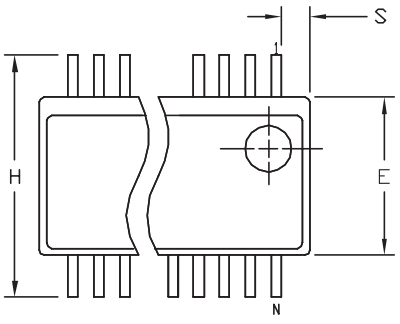


TRANSISTOR COUNT: 915
SUBSTRATE CONNECTED TO SUB
SUB CONNECTED TO GND ON MAX3964AETP

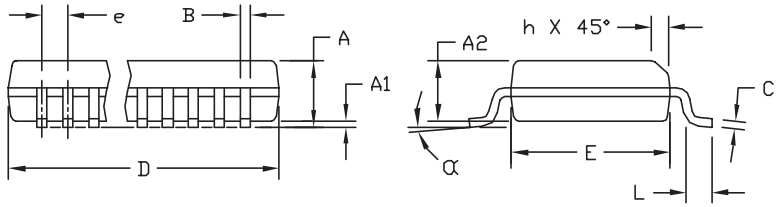
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

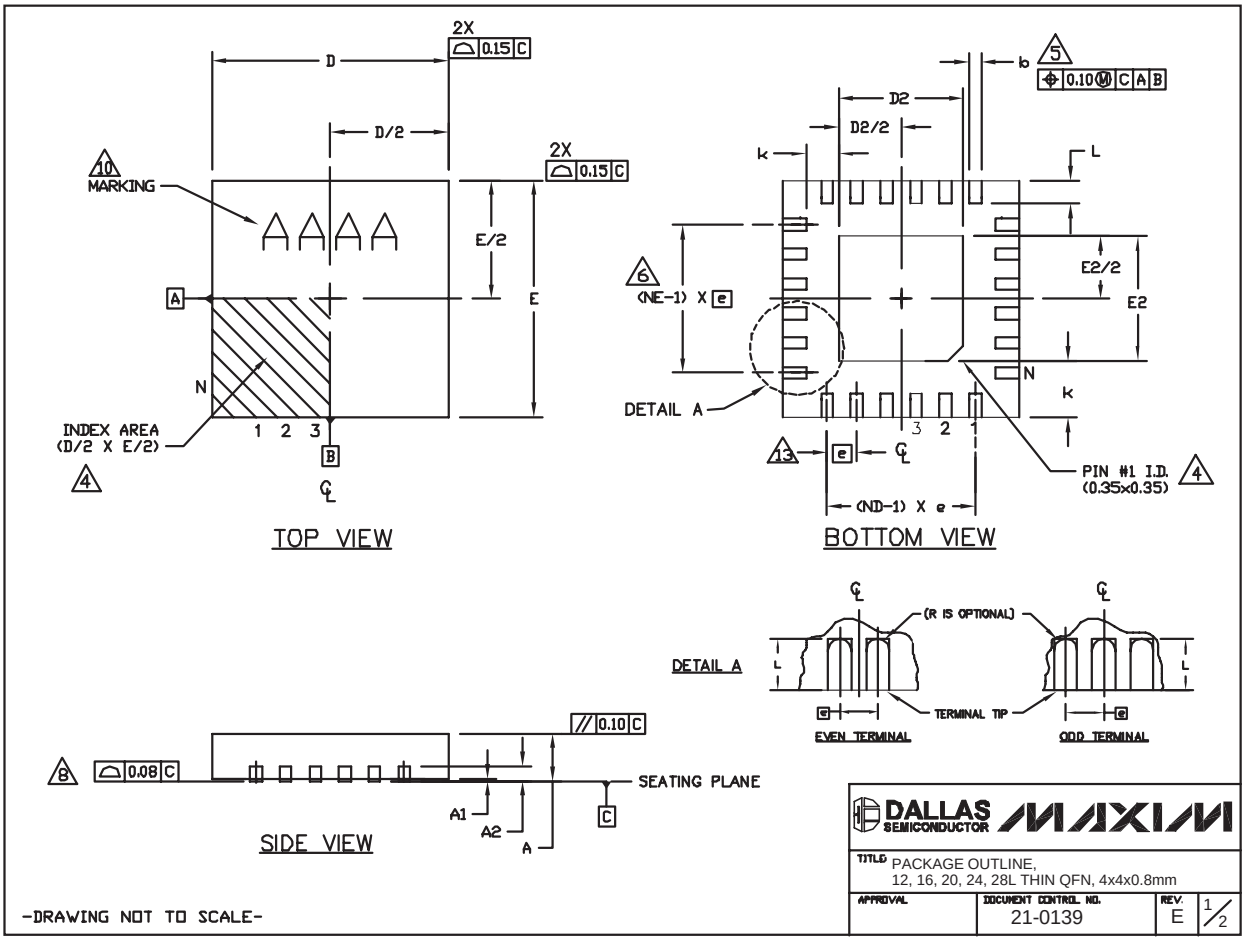
TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	F	1/1

+3.0V to +5.5V, 125Mbps to 266Mbps Limiting Amplifiers with Loss-of-Signal Detector

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2

Revision History

Rev 0;	10/98:	Initial data sheet release.
Rev 1;	10/02:	Added MAX3964ETP.
Rev 2;	5/03:	Added package code for TQFN (page 1); updated package drawing (pages 11, 12).
Rev 3;	9/04:	Added MAX3964A (pages 1 to 13).
Rev 4;	2/06:	Added lead-free package information to Ordering Information table (page 1).
Rev 5;	8/06:	Removed references to MAX3964 and MAX3965, TTL Loss of Signal, GNDO; updated CAZ value to 0.1µF and CIN from 10nF to 4700pF. Updated Typical Application Circuit.

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