

MAX40000/MAX40001

1.7V, nanoPower Comparators with Built-In Reference

General Description

The MAX40000/MAX40001 are tiny, single comparators with built-in voltage references that are ideal for a wide variety of portable electronics applications, such as cell phones, portable instruments, and notebooks that have extremely tight board space and power constraints. The MAX40000/MAX40001 are available in a 6-bump wafer-level package (WLP) with 1.11mm x 0.76mm footprint and a 6-pin SOT23 package. The MAX40000 has a push-pull output and the MAX40001 has an open-drain output.

The devices offer a supply voltage range from 1.7V to 5.5V and consume only 0.9µA of supply current. They also feature internal filtering to provide high RF immunity, important in many portable applications.

The devices have a high-precision integrated reference that is factory trimmed to an initial accuracy of 1% and better than 2.5% over the entire temperature range. Internal reference voltage options include 1.252V, 1.66V, 1.94V, and 2.22V. See [Ordering Information](#) for help with ordering a MAX40000/MAX40001 with a particular voltage reference value and package type. The reference output is stable for capacitive loads up to 100pF.

These devices are fully specified over -40°C to +125°C automotive temperature range.

Applications

- Cell Phones
- Tablets and Consumer Accessories
- Notebook Computers
- Electronic Toys
- Portable Medical Instruments/Wearables
- Level Detectors

Benefits and Features

- Micropower Operating Current (0.9µA typ, 1.7µA max) Preserves Battery Power
- Tiny 1.11mm x 0.76mm 6-Bump WLP and SOT23 Packages Save Board Space
- Internal Precision Reference Saves Space and Cost of an External Reference
 - < 1% at Room Temperature, < 2.5% Over Temp Reference
 - Multiple Reference Voltages (1.252V, 1.66V, 1.94V, and 2.22V)
- Input Voltage Range = -0.2V to 5.7V
- Supply Voltage Range (1.7V to 5.5V) Allows Operation from 1.8V, 2.5V, 3V, and 5V Supplies
- <10µs Propagation Delay
- Push-Pull (MAX40000) or Open-Drain (MAX40001) Outputs

[Ordering Information](#) appears at end of data sheet.

Simplified Block Diagram

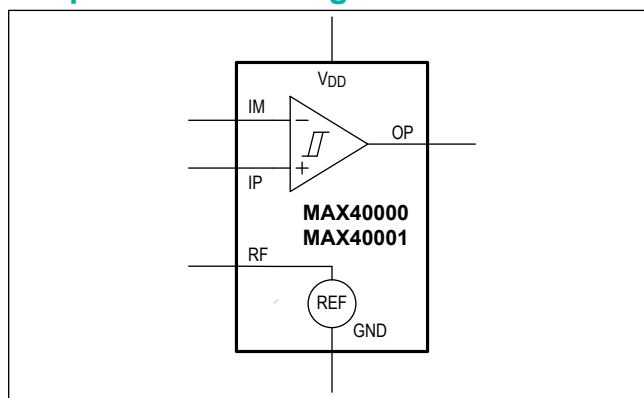


TABLE OF CONTENTS

General Description	1
Applications	1
Benefits and Features	1
Simplified Block Diagram	1
Absolute Maximum Ratings	5
Package Information	5
6 WLP	5
6 SOT23	6
Electrical Characteristics	8
Typical Operating Characteristics	12
Pin Configurations	15
BUMP (WLP)	15
PIN (SOT23)	16
Pin Description	16
Functional Diagram	16
Detailed Description	17
Input Stage Circuitry	17
Output Stage Structure	17
Voltage Reference	17
Applications Information	18
Battery-Powered Operation	18
Internal Hysteresis	18
Adding External Hysteresis	18
Output Considerations	19
Component Selection	19
Board Layout and Bypassing	19
Logic-Level Translator	19
Typical Application Circuit	20
Ordering Information	20
Revision History	21

LIST OF FIGURES

Figure 1. Hysteresis Band 18
Figure 2. External Hysteresis on MAX40000 19

MAX40000/MAX40001	1.7V, nanoPower Comparators with Built-In Reference
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LIST OF TABLES

Table 1. Battery Applications Using MAX40000 and MAX40001	19
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Absolute Maximum Ratings

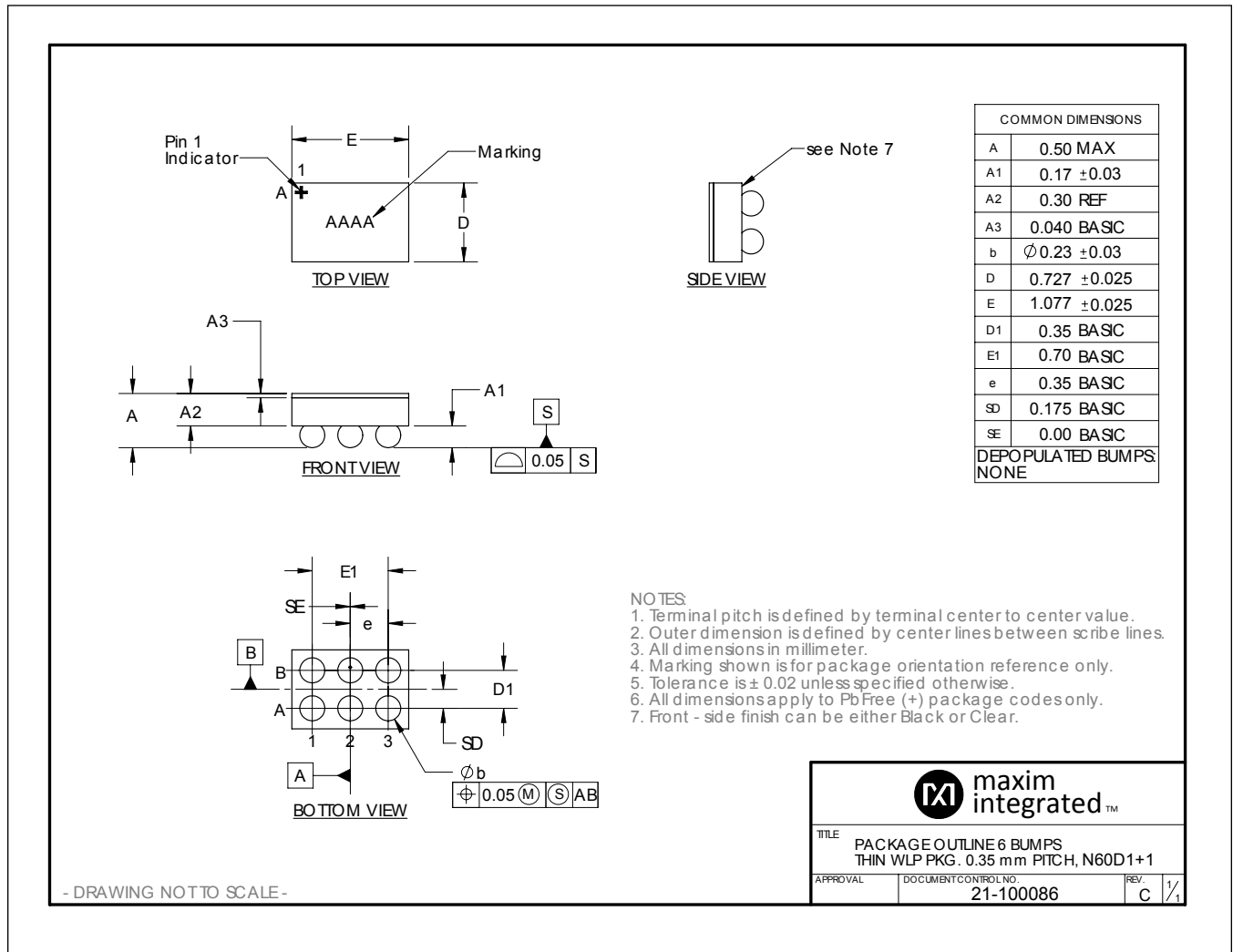
V _{DD} to GND.....	-0.3V to +6V	Continuous Power Dissipation (T _A = +70°C) Maximum Power
REF to GND	-0.3V to +6V	Dissipation (WLP, derate 10.2mW/°C above +70°C).....
IP, IM to GND	-0.3V to +6V	816mW
IP to IM	±6V	Maximum Power Dissipation (SOT23, derate 4.3mW/°C above
OUT (open-drain) to GND	-0.3V to +6V	+70°C).....
OUT (push-pull) to GND	-0.3V to V _{DD} + 0.3V	347.8mW
Output Short-Circuit Duration	10s	Operating Temperature Range
Continuous Current Into Any Input Pin	20mA	-40°C to +125°C
Continuous Current Into/Out of Any Output Pin	50mA	Junction Temperature (T _{JMAX}).....
		+150°C
		Storage Temperature Range
		-65°C to +150°C
		Lead Temperature (soldering, 10s).....
		+300°C
		Soldering Temperature (reflow)
		+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 WLP

Package Code	N60D1+1
Outline Number	21-100086
Land Pattern Number	Refer to Application Note 1891
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ _{JA})	98°C/W



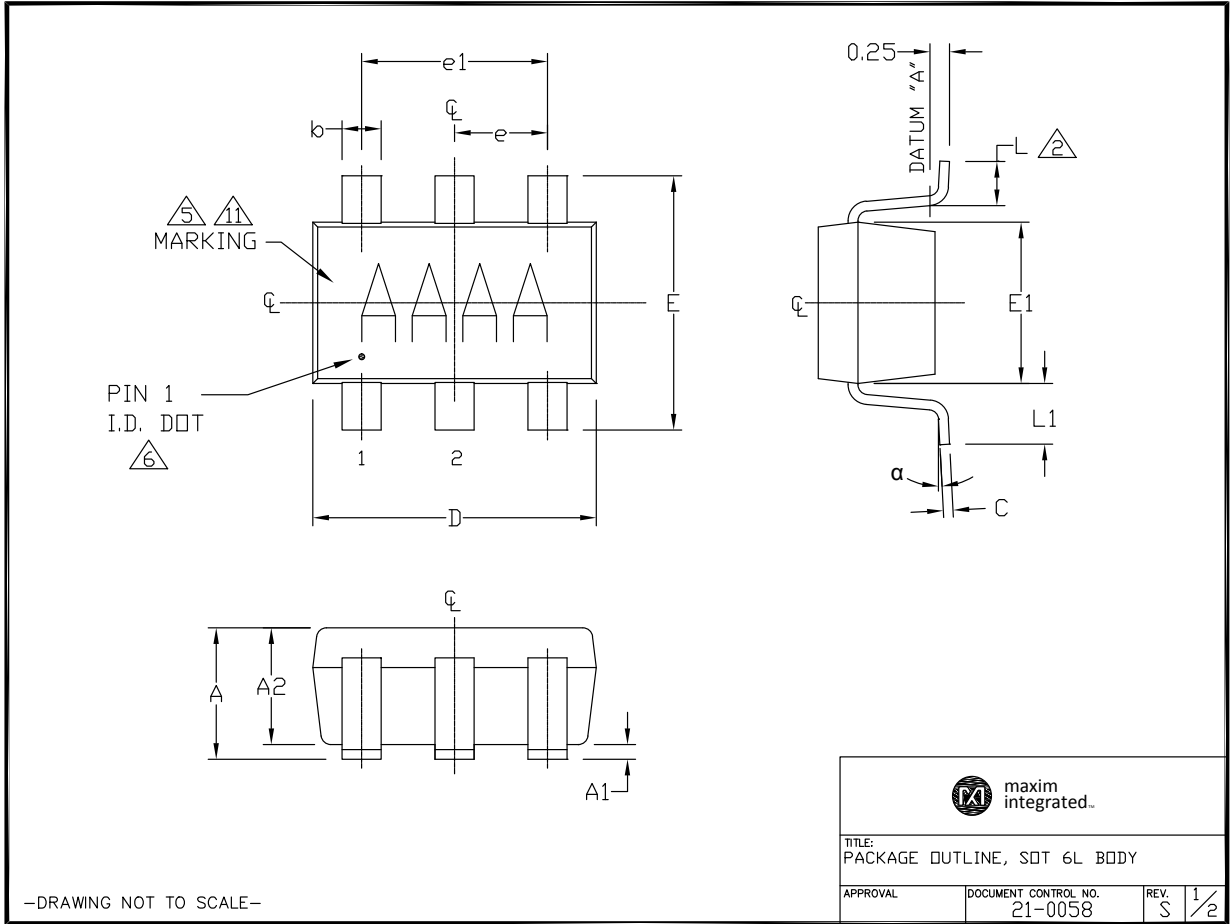
6 SOT23

Package Code	U6+1
Outline Number	21-0058
Land Pattern Number	90-0175
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	230°C/W
Junction to Case (θ_{JC})	76°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note:

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.



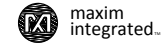
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHER SPECIFIED.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT.
6. PIN 1 I.D. DOT IS $\varnothing 0.3\text{mm}$ MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE EU ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF.		
e1	1.90 BSC.		
e	0.95 BSC.		
a	0°	2.5°	10°

PKG CODES:
 U6-1, U6-1A, U6-2, U6-4,
 U6-4A, U6-5, U6-5A, U6CN-2,
 U6F-6, U6SN-1, U6-8, U6-9,
 U6-1C

** U6-9 TO BE USED FOR RFS0 PARTS ONLY WHICH USES A SI SPACER
 ** U6-5 USES LDV STRESS MOLD COMPOUND



TITLE:
 PACKAGE OUTLINE, SOT 6L BODY

APPROVAL	DOCUMENT CONTROL NO. 21-0058	REV. S	2/2
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-DRAWING NOT TO SCALE-

Electrical Characteristics

($V_{DD} = 3.3\text{V}$, $V_{CM} = 0\text{V}$, $R_{PULLUP} = 100\text{k}\Omega$ from OUT to $V_{PULLUP} = 3.3\text{V}$ (for MAX40001 only), $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE						
V_{DD} Supply Voltage Range	V_{DD}	$V_{REF} < 1.8\text{V}$, guaranteed by PSRR specification	1.7		5.5	V
		$V_{REF} > 1.8\text{V}$, guaranteed by PSRR specification	$V_{REF} + 0.1$		5.5	
V_{DD} Supply Current	I_{DD}	No output or reference load current, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.9	1.7	μA
Power-Up Time				5		μs

Electrical Characteristics (continued)

($V_{DD} = 3.3V$, $V_{CM} = 0V$, $R_{PULLUP} = 100k\Omega$ from OUT to $V_{PULLUP} = 3.3V$ (for MAX40001 only), $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATOR						
Input Common-Mode Voltage Range	V_{CM}	$T_A = +25^\circ C$	-0.2		$V_{DD} + 0.2$	V
		$T_A = -40^\circ C$ to $+125^\circ C$	0		V_{DD}	
Input Offset Voltage	V_{OS}	<i>Note 2</i>	$V_{CM} = 0V$ to $V_{DD} - 1V$		8	mV
			$V_{CM} = V_{DD} - 1V$ to V_{DD} , $T_A = 0^\circ C$ to $+85^\circ C$		10	
			$V_{CM} = V_{DD} - 1V$ to V_{DD} , $T_A = -40^\circ C$ to $+125^\circ C$		14	
Input Offset Drift				27		$\mu V/^\circ C$
Input Hysteresis	V_{HYS}	<i>Note 3</i>		2.5		mV
Input Bias Current		<i>Note 4</i>	$V_{CM} = -0.2V$ to $V_{DD} + 0.2V$, $T_A = +25^\circ C$	1	5	nA
			$V_{CM} = 0V$ to V_{DD} , $T_A = -40^\circ C$ to $+85^\circ C$	1	5	
			$V_{CM} = 0.2V$ to V_{DD} , $T_A = -40^\circ C$ to $+125^\circ C$	1	5	
Input Offset Current		<i>Note 4</i>			5	nA
Input Capacitance		Either input, over V_{CM} range		1.5		pF
Power Supply Rejection Ratio	PSRR	DC, over the entire common-mode input voltage range	60			dB
Common-Mode Rejection Ratio	CMRR	DC, over the entire common-mode input voltage range	46			dB
Output Voltage Swing Low	V_{OL}	Sinking 2mA output current, $V_{OUT} - V_{GND}$			0.4	V
Output Voltage Swing High	V_{OH}	Sourcing 2mA output current, $V_{DD} - V_{OUT}$			0.4	V
Output Leakage Current	I_{O-LKG}	Open-drain only (MAX40001), $V_{DD} = 1.8V$, $V_O = 5.5V$, $T_A = -40^\circ C$ to $+125^\circ C$			100	nA

Electrical Characteristics (continued)

($V_{DD} = 3.3V$, $V_{CM} = 0V$, $R_{PULLUP} = 100k\Omega$ from OUT to $V_{PULLUP} = 3.3V$ (for MAX40001 only), $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay	t_{PD}	100mV overdrive (Note 5)	Output L->H, MAX40000		9.6		μs
			Output L->H, MAX40001, 100k Ω		14		
			Output H->L, MAX40000		3.2		
		20mV overdrive (Note 5)	Output L->H, MAX40000		9.9		
			Output L->H, MAX40001, 100k Ω		14.8		
			Output H->L, MAX40000		5.2		
Rise Time	t_R	Push-pull output stage. 25% to 75%			300		ns
Fall Time	t_F	25% to 75%			52		ns
INTERNAL REFERENCE VOLTAGE							
Reference Voltage	V_{REF}	$T_A = +25^\circ C$	MAX40000ANT12+ T	1.2395	1.252	1.2645	V
			MAX4000_ _ _ _ _16+		1.66		
			MAX4000_ _ _ _ _19+		1.94		
			MAX4000_ _ _ _ _22+		2.22		
		$T_A = -40^\circ C$ to $+85^\circ C$	MAX4000_ _ _ _ _12+		1.252		
			MAX4000_ _ _ _ _16+		1.66		
			MAX4000_ _ _ _ _19+		1.94		
			MAX4000_ _ _ _ _22+		2.22		
		$T_A = -40^\circ C$ to $+125^\circ C$	MAX40000ANT12+ T	1.2207	1.252	1.2833	
			MAX4000_ _ _ _ _16+		1.66		
			MAX4000_ _ _ _ _19+		1.94		
			MAX4000_ _ _ _ _22+		2.22		
Reference Thermal Drift	$V_{REF-TEMPCO}$	Over extended temperature range, $T_A = -40^\circ C$ to $+125^\circ C$			15		ppm/ $^\circ C$
Line Regulation						1200	ppm/V
Load Regulation		$I_{VREFOUT} = \pm 100nA$				0.01	mV/nA

Electrical Characteristics (continued)

($V_{DD} = 3.3V$, $V_{CM} = 0V$, $R_{PULLUP} = 100k\Omega$ from OUT to $V_{PULLUP} = 3.3V$ (for MAX40001 only), $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current			0.1			μA
Voltage Noise		0.1Hz to 10Hz		82		μV_{P-P}
Voltage Noise Density		$C_{REF} = 1nF$, 10Hz to 6kHz		2.19		$\mu V/\sqrt{Hz}$
Capacitive Load Stability					100	pF

Note 1: All specifications are 100% production tested at $T_A = +25^\circ C$. Specification limits over temperature ($T_A = T_{MIN}$ to T_{MAX}) are guaranteed by design, not production tested.

Note 2: Input offset voltage; V_{OS} is defined as the center of the hysteresis band or average of the threshold trip points.

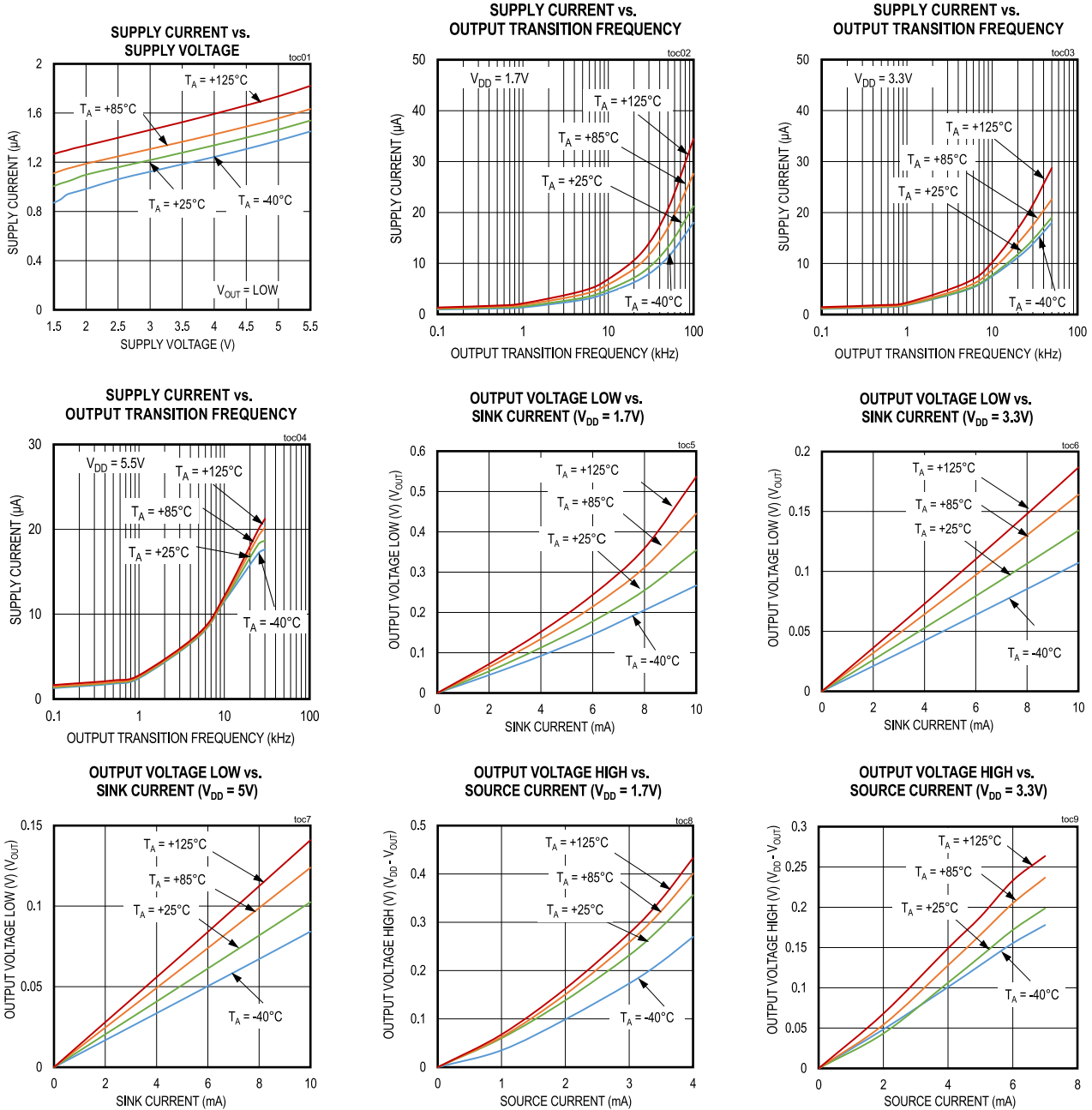
Note 3: The hysteresis-related trip points are defined as the edges of the hysteresis band, measured with respect to the center of the band (i.e., V_{OS}) ([Figure 1](#)).

Note 4: Guaranteed by design and characterization.

Note 5: Specified with an input overdrive ($V_{OVERDRIVE}$) of 100mV and 20mV, and load capacitance of $C_L = 15pF$. $V_{OVERDRIVE}$ is defined above the offset voltage and hysteresis of the comparator input. For the MAX40000/MAX40001, reference voltage error should also be added.

Typical Operating Characteristics

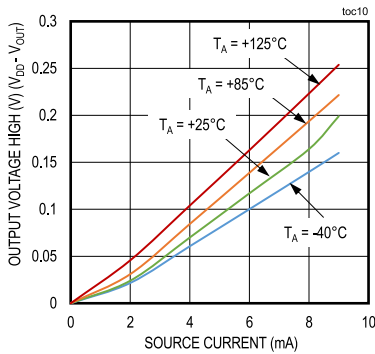
($V_{DD} = 3.3V$, $R_{PULLUP} = 100k\Omega$ from OUT to $V_{PULLUP} = 3.3V$ (for MAX40001 only), $T_A = +25^\circ C$, unless otherwise noted.)



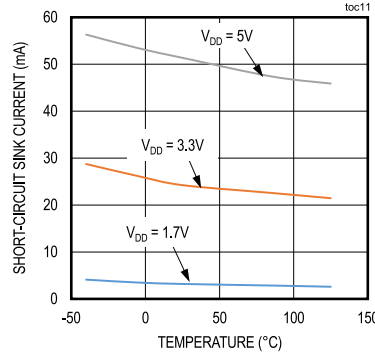
Typical Operating Characteristics (continued)

($V_{DD} = 3.3V$, $R_{PULLUP} = 100k\Omega$ from OUT to $V_{PULLUP} = 3.3V$ (for MAX40001 only), $T_A = +25^\circ C$, unless otherwise noted.)

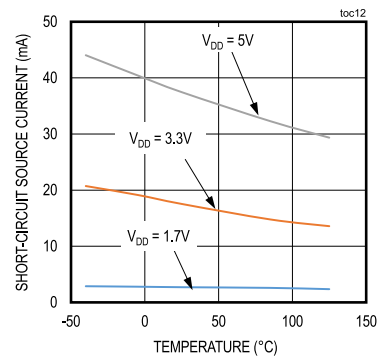
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT ($V_{DD} = 5V$)



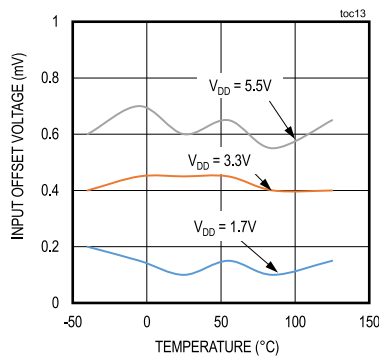
SHORT CIRCUIT SINK CURRENT vs. TEMPERATURE



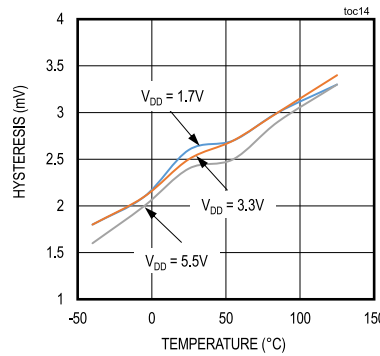
SHORT CIRCUIT SOURCE CURRENT vs. TEMPERATURE



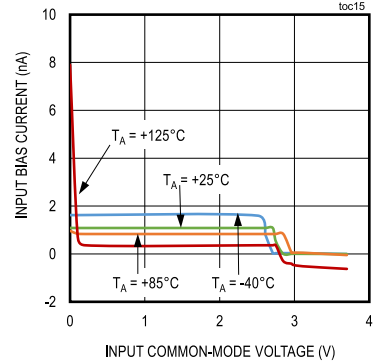
INPUT OFFSET VOLTAGE vs. TEMPERATURE



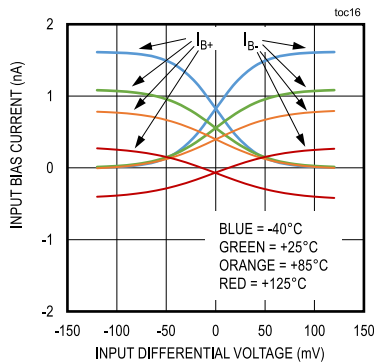
HYSTERESIS vs. TEMPERATURE



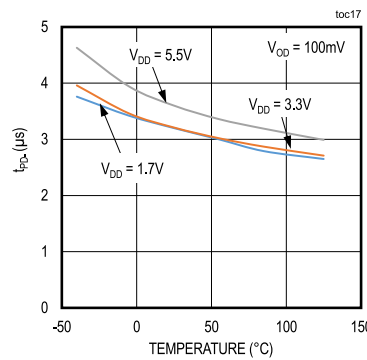
INPUT BIAS CURRENT vs. INPUT COMMON MODE VOLTAGE



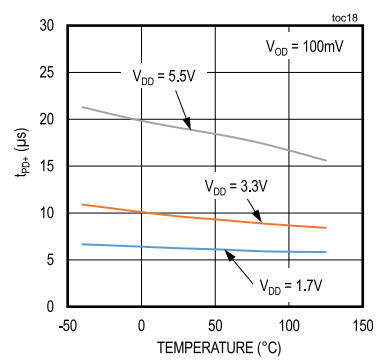
INPUT BIAS CURRENT vs. INPUT DIFFERENTIAL VOLTAGE



PROPAGATION DELAY (tPD+) vs. TEMPERATURE



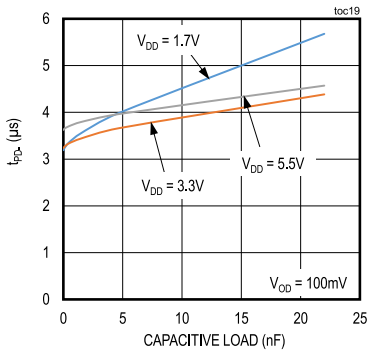
PROPAGATION DELAY (tPD-) vs. TEMPERATURE



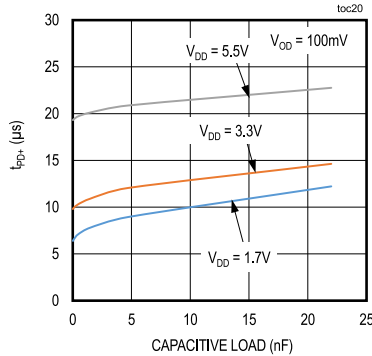
Typical Operating Characteristics (continued)

($V_{DD} = 3.3V$, $R_{PULLUP} = 100k\Omega$ from OUT to $V_{PULLUP} = 3.3V$ (for MAX40001 only), $T_A = +25^\circ C$, unless otherwise noted.)

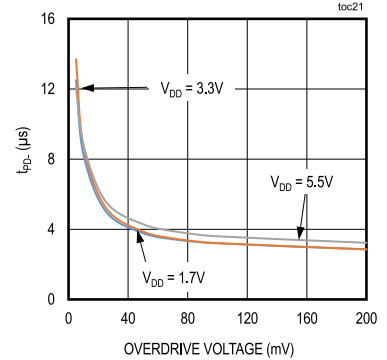
PROPAGATION DELAY (t_{PD}) vs. CAPACITIVE LOAD



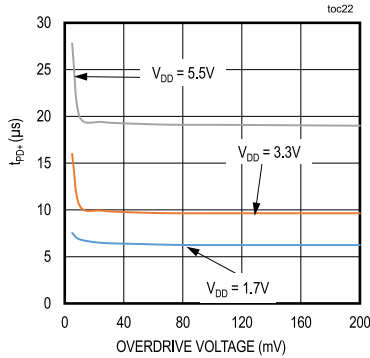
PROPAGATION DELAY (t_{PD+}) vs. CAPACITIVE LOAD



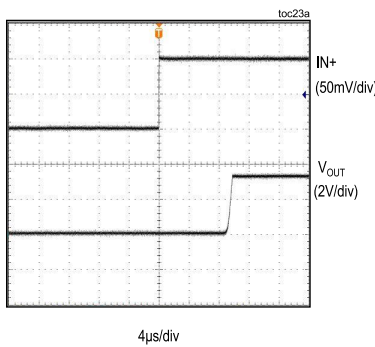
PROPAGATION DELAY (t_{PD-}) vs. INPUT OVERDRIVE



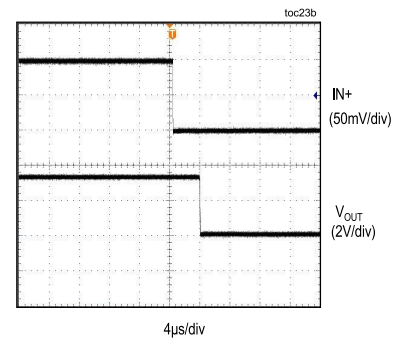
PROPAGATION DELAY (t_{PD+}) vs. INPUT OVERDRIVE



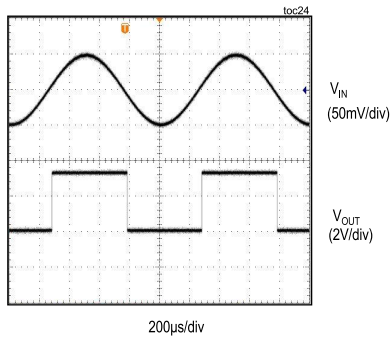
PROPAGATION DELAY t_{PD+} ($V_{DD}=3.3V$)



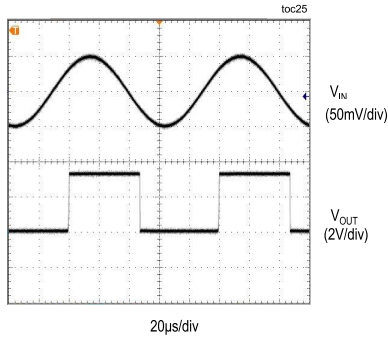
PROPAGATION DELAY t_{PD-} ($V_{DD}=3.3V$)



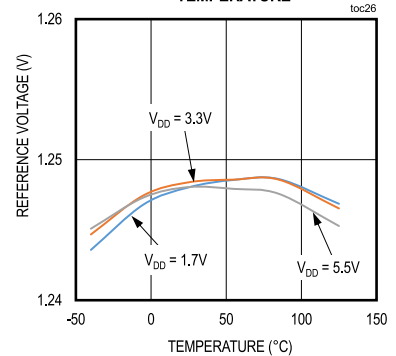
1kHz FREQUENCY RESPONSE ($V_{DD} = 3.3V$)



10kHz FREQUENCY RESPONSE ($V_{CC} = 3.3V$)

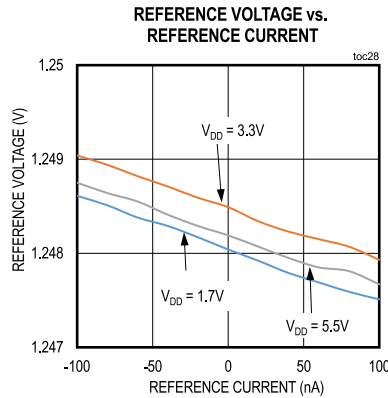
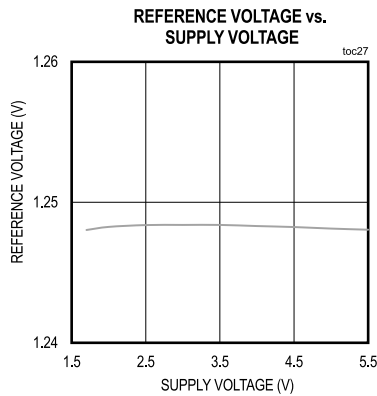


REFERENCE VOLTAGE vs. TEMPERATURE

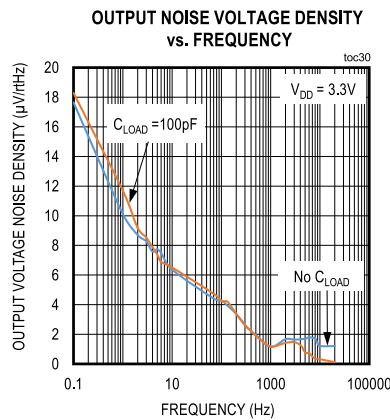
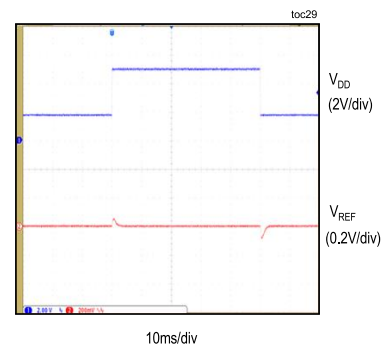


Typical Operating Characteristics (continued)

($V_{DD} = 3.3V$, $R_{PULLUP} = 100k\Omega$ from OUT to $V_{PULLUP} = 3.3V$ (for MAX40001 only), $T_A = +25^\circ C$, unless otherwise noted.)

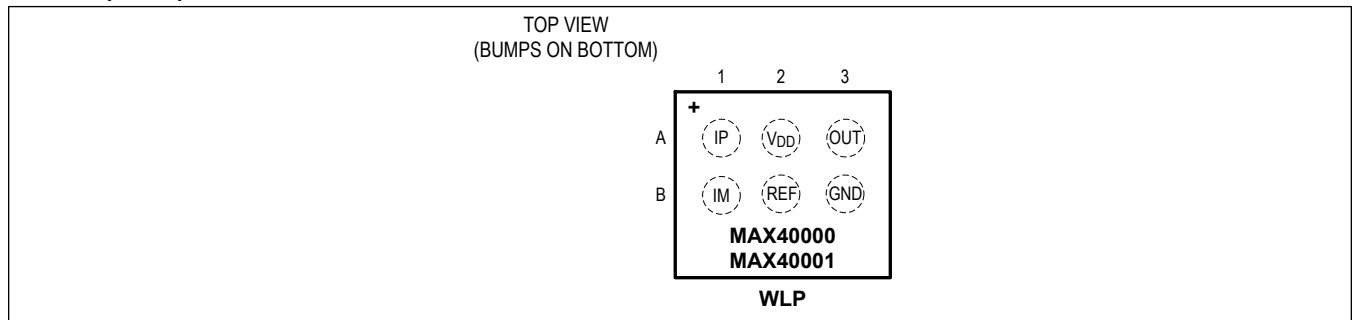


VOLTAGE REFERENCE RESPONSE TO SUPPLY TRANSIENT ($V_{DD} = 1.7$ to $5.5V$)

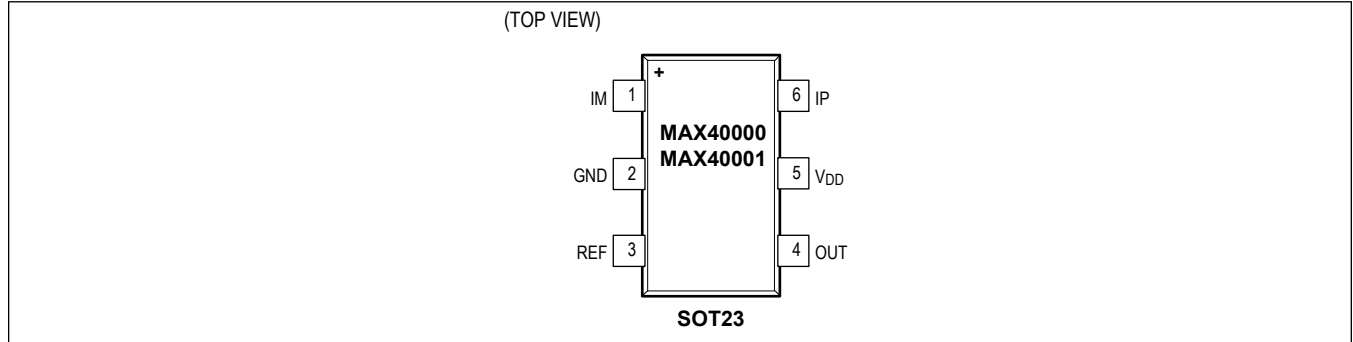


Pin Configurations

BUMP (WLP)



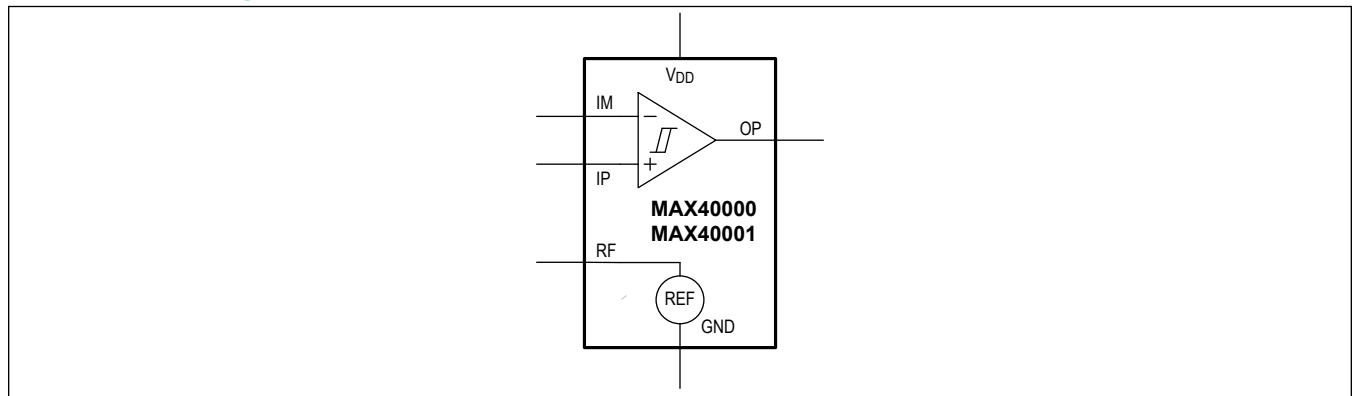
PIN (SOT23)



Pin Description

PIN		NAME	FUNCTION
BUMP (WLP)	PIN (SOT23)		
B1	1	IM	Inverting Input of Comparator
B2	3	REF	Internal Voltage Reference Output. Bypass REF pin with a 0.1µF capacitor to GND as close as possible to the device.
B3	2	GND	Ground
A1	6	IP	Noninverting Input of Comparator
A2	5	V _{DD}	V _{DD} Supply Voltage. Bypass V _{DD} with a 0.1µF capacitor to GND as close as possible to the device pin.
A3	4	OUT	Open-Drain Output (MAX40001)/Push-Pull Output (MAX40000). For the open-drain version, connect a 100kΩ pullup resistor from OUT to any pullup voltage up to 5.5V.

Functional Diagram



Detailed Description

The MAX40000/MAX40001 feature an on-board voltage reference with $\pm 1\%$ initial accuracy. This family of comparators with internal references are available in multiple voltage reference options. The [Ordering Information](#) table provides exact part numbers associated with a particular voltage reference option. The common-mode voltage range of this family extends 200mV beyond the rails, allowing signals slightly beyond the rails to trigger the comparator. The 2.5mV internal hysteresis ensures clean output switching even with slow moving input signals. Large internal output drivers allow rail-to-rail output swing with up to $\pm 2\text{mA}$ loads.

The output stage employs a unique design that minimizes supply current surges while switching, virtually eliminating supply glitches typical of many other comparators. The MAX40000 has a push-pull output stage that sinks as well as sources current. The MAX40001 has an open-drain output stage that can be pulled beyond V_{DD} to a maximum of 5.5V above GND. Multiple comparators with open-drain outputs (OUT) can be connected together in parallel and share a single pullup resistor. This enables user to detect if there is any fault if at least one comparator trips different to other comparators.

Input Stage Circuitry

The input common-mode voltage range extends from -0.2V to $V_{DD} + 0.2\text{V}$. These comparators operate at any differential input voltage within these limits. Input bias current is typically $\pm 1\text{nA}$ if the input voltage is between the supply rails.

Output Stage Structure

The devices contain a unique break-before-make output stage capable of rail-to-rail operation with up to $\pm 2\text{mA}$ loads. Many comparators consume orders of magnitude more current during switching than during steady-state operation. In the [Typical Operating Characteristics](#), the Supply Current graphs show the minimal supply-current increase as the output switching frequency approaches 1kHz. This characteristic reduces the need for power-supply filter capacitors to reduce glitches created by comparator switching currents. In battery-powered applications, this characteristic results in a substantial increase in battery life.

Voltage Reference

The MAX40000/MAX40001 come with different internal voltage reference options that has initial accuracy of $\pm 1\%$. 1.252V, 1.6V, 1.9V, and 2.2V options of internal voltage references are available. The devices' internal reference has a typical temperature coefficient of 15ppm/ $^{\circ}\text{C}$ over the full -40°C to $+125^{\circ}\text{C}$ temperature range. The reference is a very-low-power bandgap cell, with a maximum 10k Ω output impedance. REF pin can source and sink up to 100nA to external circuitry. For applications that need increased drive, buffer REF with a low input-bias current op amp such as the MAX44265. Most applications require no bypass capacitor on REF pin.

Applications Information

Battery-Powered Operation

The MAX40000 and MAX40001 are ideally suited for use with most battery-powered systems. [Table 1](#) lists Alkaline and Lithium-Ion batteries with capacities and approximate operating times for MAX40000 and MAX40001, assuming nominal conditions.

Internal Hysteresis

Many comparators oscillate in the linear region of operation because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal or very close to the voltage on the other input. The MAX40000/MAX40001 have internal 2.5mV hysteresis to counter parasitic effects and noise.

The hysteresis in a comparator creates two trip points: one for upper threshold (V_{TRIP+}) and one for lower threshold (V_{TRIP-}) for voltage transitions on the input signal ([Figure 1](#)). The difference between the trip points is the hysteresis band (V_{HYS}). When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input to move quickly past the other, thus taking the input out of the region where oscillation occurs. [Figure 1](#) illustrates the case in which IM has a fixed voltage applied, and IP is varied. If the inputs were reversed, the figure would be the same, except with an inverted output.

Adding External Hysteresis

In applications requiring more than the internal 2.5mV hysteresis of the devices, additional hysteresis can be added with two external resistors. Since these comparators are intended to use in very low-power systems, care must be taken to minimize power dissipation in the additional circuitry.

Regardless of which approach is employed to add external hysteresis, the external hysteresis will be V_{DD} dependent. Over the full discharge range of battery-powered systems, the hysteresis can change as much as 40%. [Figure 2](#) shown below is simplest circuit for adding external hysteresis. In this example, the hysteresis is defined by:

$$\text{Hysteresis} = \frac{R_G}{R_F} \times V_{DD}$$

Where R_G is the source resistance and R_F is the feedback resistance. Because the comparison threshold is $1/2 V_{DD}$, the MAX40000 was chosen for its push-pull output and lack of reference. This provides symmetrical hysteresis around the threshold.

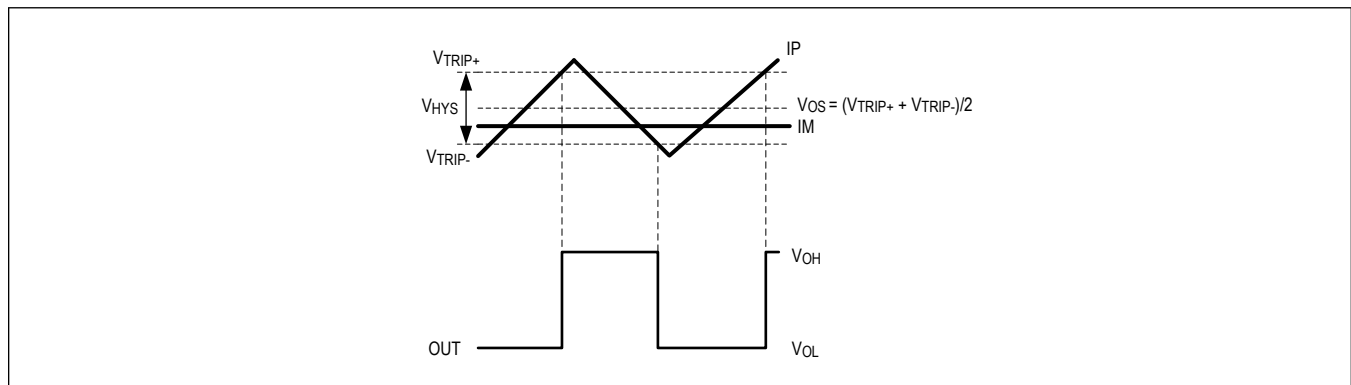


Figure 1. Hysteresis Band

Table 1. Battery Applications Using MAX40000 and MAX40001

BATTERY TYPE	RECHARGEABLE	V _{INITIAL} (V)	V _{END-OF-LIFE} (V)	CAPACITY, AA SIZE (mAh)	MAX40000/MAX40001 OPERATING TIME (hr)
Alkaline (2 Cells)	No	3.0	1.8	2000	1.8 x 10 ⁶
Lithium-Ion (1 Cell)	Yes	3.5	2.7	1000	0.9 x 10 ⁶

Output Considerations

In most cases, the push-pull output of MAX40000 is best for external hysteresis. The open-drain output of the MAX40001 can be used, but the effect of the feedback network and pullup resistor on the actual output high voltage must be considered.

Component Selection

Because the MAX40000/MAX40001 are intended for very low power-supply systems, the highest impedance circuits should be used wherever possible. The offset error due to input-bias current is proportional to the total impedance seen at the input. For example, selecting components for [Figure 2](#), with a target of 50mV hysteresis, a 5V supply, and choosing an R_F of 10MΩ gives R_G as 100kΩ. The total impedance seen at IN+ is therefore 10MΩ || 100kΩ, or 99kΩ. The maximum input bias current of MAX40000/MAX40001 is 1nA; therefore, the error due to source impedance is less than 100μV.

Board Layout and Bypassing

Power-supply bypass capacitors are not typically needed, but use 100nF bypass capacitors close to the device's supply pins when supply impedance is high, supply leads are long, or excessive noise is expected on the supply lines. Minimize signal trace lengths to reduce stray capacitance. A ground plane and surface-mount components are recommended. If the REF pin is decoupled, use a new low-leakage capacitor.

Logic-Level Translator

The [Typical Application Circuit](#) shows an application that converts 5V logic to 3V logic levels. The MAX40001 is powered by the +5V supply voltage to V_{DD}, and the pullup resistor for the MAX40001's open-drain output is connected to the +3V supply voltage. This configuration allows the full 5V logic swing without creating overvoltage on the 3V logic inputs. For 3V to 5V logic-level translations, simply connect the +3V supply voltage to V_{DD} and the +5V supply voltage to the pullup resistor.

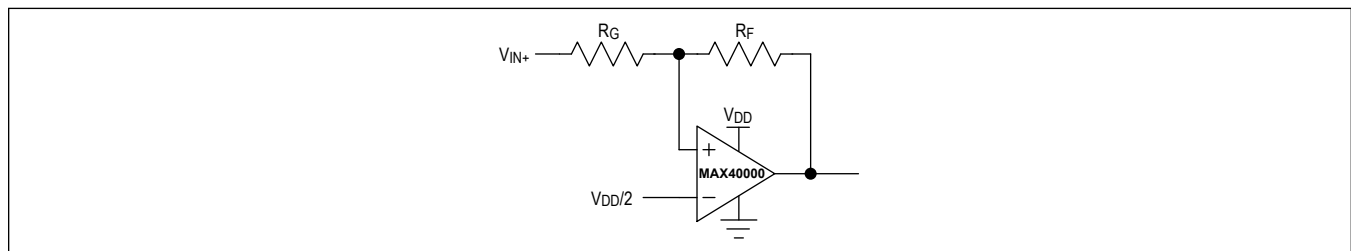
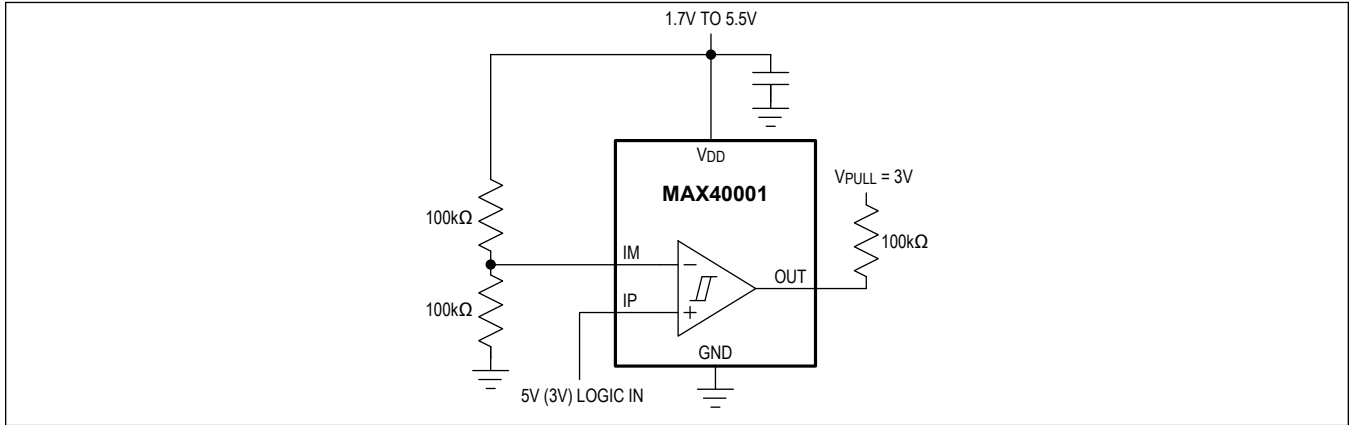


Figure 2. External Hysteresis on MAX40000

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX40000ANT12+T	-40°C to +125°C	6 WLP	+N
MAX40000ANT16+T*	-40°C to +125°C	6 WLP	+O
MAX40000ANT19+T*	-40°C to +125°C	6 WLP	+P
MAX40000ANT22+T*	-40°C to +125°C	6 WLP	+Q
MAX40000AUT12+T	-40°C to +125°C	6 SOT23	-
MAX40000AUT16+T*	-40°C to +125°C	6 SOT23	-
MAX40000AUT19+T*	-40°C to +125°C	6 SOT23	-
MAX40000AUT22+T*	-40°C to +125°C	6 SOT23	-
MAX40001ANT12+T	-40°C to +125°C	6 WLP	+R
MAX40001ANT16+T*	-40°C to +125°C	6 WLP	+S
MAX40001ANT19+T*	-40°C to +125°C	6 WLP	+T
MAX40001ANT22+T	-40°C to +125°C	6 WLP	+U
MAX40001AUT12+T	-40°C to +125°C	6 SOT23	-
MAX40001AUT16+T*	-40°C to +125°C	6 SOT23	-
MAX40001AUT19+T*	-40°C to +125°C	6 SOT23	-
MAX40001AUT22+T	-40°C to +125°C	6 SOT23	-

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

For example, the MAX40000ANT12+T has an onboard 1.2V reference voltage.

Devices without “_” use external reference voltage as supply voltage.

*Future product—contact factory for availability.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/17	Initial release	—
1	3/17	Updated title to include “nanoPower”	1–14
2	4/17	Updated <i>Ordering Information</i> table	13
3	5/17	Updated <i>Ordering Information</i> table	13
4	8/17	Updated <i>Functional Diagram</i> and <i>Ordering Information</i> table	10, 13
5	1/21	Added package outline drawings	6–8
6	5/21	Updated <i>Electrical Characteristics</i> table	9–10

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