*Click **here** to ask an associate for production status of specific part numbers.*

MAX40213

Transimpedance Amplifier with Selectable Gain and Input Current Clamp

General Description

The MAX40213 is a transimpedance amplifier for optical distance measurement receivers in LiDAR applications. Low noise, high gain, low group delay, and fast recovery from overload make this TIA ideal for distance-measurement applications. Important features include 1.1pA/√Hz input-referred noise density, an internal 2A input clamp, pin-selectable 150kΩ and 750kΩ transimpedance (into a 1kΩ load), and wide bandwidth (300MHz, typ). An offset current input allows optional adjustment of input offset current. The MAX40213 has a shutdown (SD) control input that reduces the supply current to 0.01µA. This transimpedance amplifier is available in a 8-bump WLP, and is specified over the -40°C to +85°C operating temperature range.

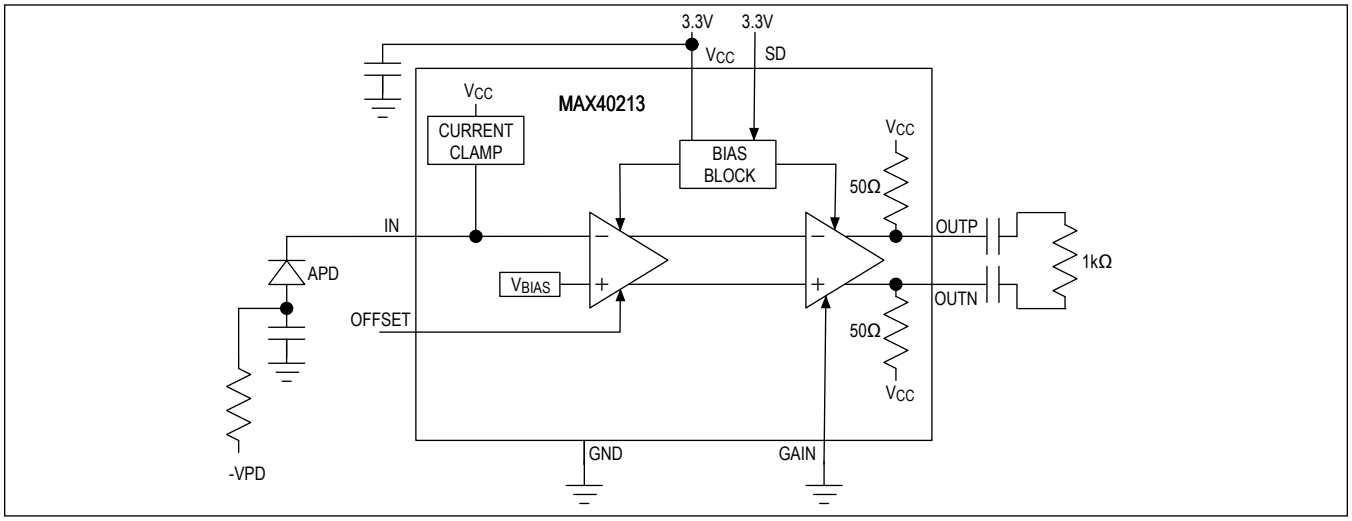
Benefits and Features

- Optimized for C_{IN} = 0.25pF to 5pF
- Bandwidth = 300MHz (typ)
- 1.1pA/√Hz Input-Referred Noise
- Two Pin-Selectable Transimpedance Values (R_L = 1kΩ)
  - 150kΩ
  - 750kΩ
- Internal Clamp for Input Current up to 2A (Transient)
- Fast Overload Recovery: 25ns at 100mA
- Offset Input Provides Offset Adjust Feature
- SD Input Shuts Down Internal Circuitry
- 3.3V Operation
- 1.75mm x 1.24mm, 8-Bump WLP

Applications

- Optical Distance Measurement
- LIDAR Receivers
- Industrial Safety Systems

Typical Application Circuit



Ordering Information **appears at end of data sheet.**

19-100801; Rev 2; 11/21

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

Voltage at V_{CC} ..... -0.3V to +3.6V
Current into IN (10ns pulse, 0.5% duty cycle) .....-2A
Current into IN, OFFSET (Continuous) ..... -10mA to +10mA
Current into LP, GAIN (Continuous)..... -10mA to +10mA
Current into OUTP and OUTN (Continuous)..... -20mA to +20mA
Voltage at OUTN, OUTP ..... V_{CC} + 0.3V
Voltage at OFFSET, LP, GAIN .....-0.3V to V_{CC} + 0.3V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Soldering Temperature (reflow) .....+260°C
Continuous Power Dissipation (T_A = +85°C, derate 11.4mW/°C above +70°C (multilayer board))..... 1951.20mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 WLP

Package Code	W81D1+1
Outline Number	**21-100412**
Land Pattern Number	N/A
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	87.71°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{CC} = +2.9V to +3.5V, 1kΩ AC-coupled load between OUTN and OUTP, T_A = -40°C to +85°C, C_{IN} = 0.5pF (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage	V_{BIAS}	IN and OFFSET		0.78	0.95	V
Transimpedance	Z_{21}	GAIN < V_{IL}, I_{IN} = 500nA$_{P-P}$	80	150	220	kΩ
		GAIN > V_{IH}, I_{IN} = 100nA$_{P-P}$	400	750	1100	
Transimpedance Linearity		GAIN > V_{IH}, Z_{21} = 750kΩ, I_1 = -0.1µA, I_2 = -0.4µA (*Note 2*)	-19		+19	%
		GAIN < V_{IL}, Z_{21} = 150kΩ, I_1 = -0.5µA, I_2 = -2µA (*Note 2*)	-4		+4	
OFFSET Input Transimpedance		GAIN < V_{IL}, I_{IN} = 500nA$_{P-P}$	80	150	220	kΩ
		GAIN > V_{IH}, I_{IN} = 100nA$_{P-P}$	400	750	1100	
Overload Recovery Time		I_{IN} = 1mA		25		ns
		I_{IN} = 10mA		25		
		I_{IN} = 100mA		25		
Gain Change Delay		Delay from change of GAIN state to correct selected gain.		200		ns
Output Common-Mode Voltage			V_{CC} - 0.9	V_{CC} - 0.5	V_{CC} - 0.24	V

Electrical Characteristics (continued)

(V_{CC} = +2.9V to +3.5V, 1kΩ AC-coupled load between OUTN and OUTP, T_A = -40°C to +85°C, C_{IN} = 0.5pF (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Output Offset	ΔV_{OUT}	I_{IN} = 0mA, GAIN = GND			10		mV
		I_{IN} = 0mA, GAIN = V_{CC}			50		
Output Impedance	Z_{OUT}	Single-ended		40	50	65	Ω
Maximum Differential Output Voltage Swing	$V_{OUT(MAX)}$	I_{IN} = 0mA to -200µA pulse, GAIN = GND		440	900	1,470	mV
		I_{IN} = 0mA to -200µA pulse, GAIN = V_{CC}		500	1,000	1,500	
Input Resistance	R_{IN}				175		Ω
AC SPECIFICATIONS							
Bandwidth	BW	GAIN = GND (Note 3)			300		MHz
		GAIN = V_{CC} (Note 3)			300		
Input Noise Density		f = 10MHz			1.1		pA/√Hz
POWER SUPPLY							
Power Supply Current		GAIN = GND or GAIN = V_{CC}	SD = V_{CC}		30	55	mA
Power Supply Current	I_{CC}	GAIN = GND or GAIN = V_{CC}	SD = GND		0.01	2	µA
Shutdown De-Assert Delay		Time from SD > V_{IL} to output common-mode voltage 90% of nominal value. Measured at OUTP and OUTN.			15		µs
LOGIC DC CHARACTERISTICS							
Input Logic 0	V_{IL}	GAIN, SD		-0.3		+0.8	V
Input Logic 1	V_{IH}	GAIN, SD		2.0		V_{CC} + 0.3	V
Logic Input Current		GAIN, SD, -0.3 < V_{IN} < V_{CC} + 0.3V			±0.001	±1.0	µA

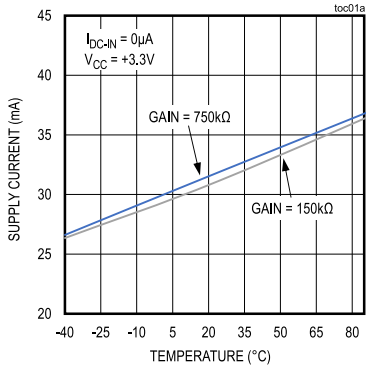
Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Linearity is calculated as follows:
For 150kΩ transimpedance, linearity = (large signal gain at -2µA – large signal gain at -0.5µA)/large signal gain at -0.5µA, where large signal gain at X is (V_{OUT} at I_IN = X - V_{OUT} at I_IN = 0)/X. For 750kΩ transimpedance, linearity = (large signal gain at -0.4µA – large signal gain at -0.1µA)/large signal gain at -0.1µA, where large signal gain at X is (V_{OUT} at I_IN = X - V_{OUT} at I_IN = 0)/X.

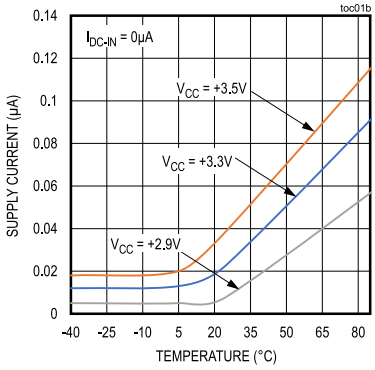
Note 3: -3dB bandwidth is measured relative to the gain at 10MHz.

Typical Operating Characteristics

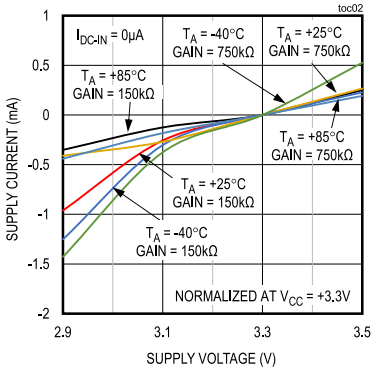
SUPPLY CURRENT vs. TEMPERATURE



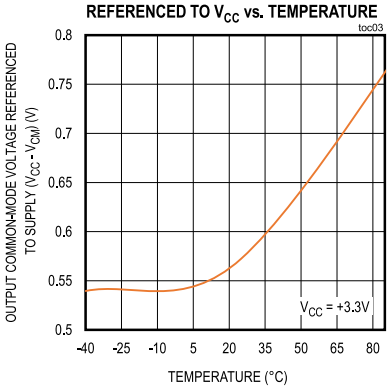
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



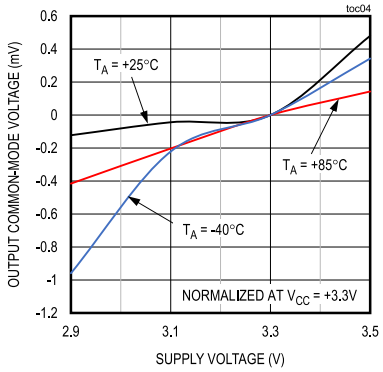
ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



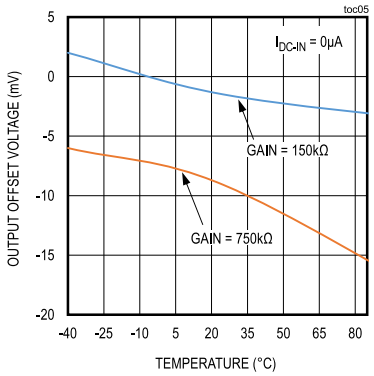
OUTPUT COMMON-MODE VOLTAGE REFERENCED TO V_{CC} vs. TEMPERATURE



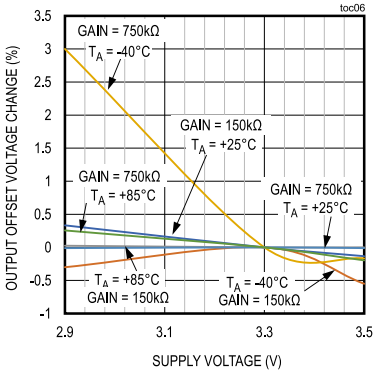
OUTPUT COMMON-MODE VOLTAGE vs. SUPPLY VOLTAGE



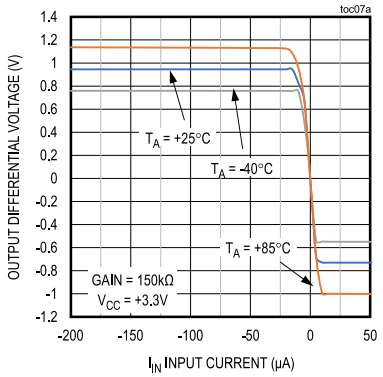
OUTPUT OFFSET vs. TEMPERATURE



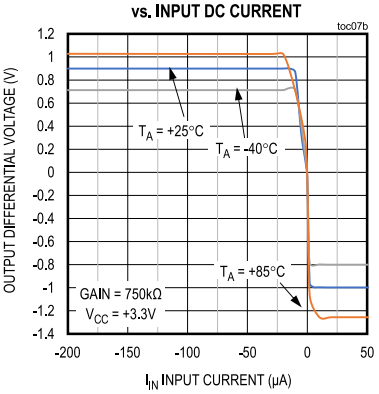
OUTPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC CURRENT

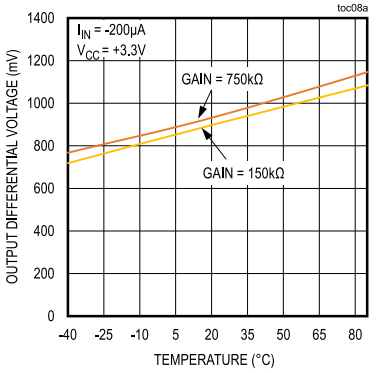


OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC CURRENT

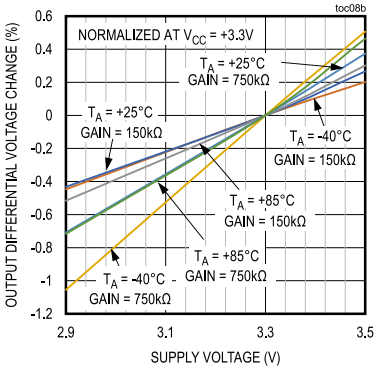


Typical Operating Characteristics (continued)

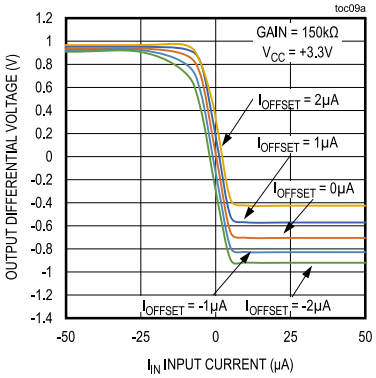
OUTPUT DIFFERENTIAL VOLTAGE vs. TEMPERATURE



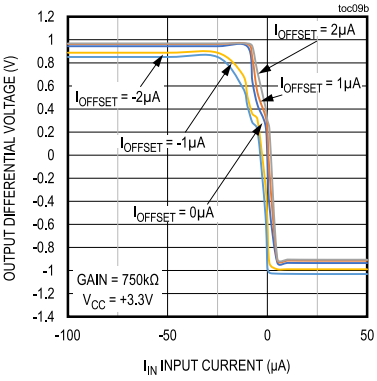
OUTPUT DIFFERENTIAL VOLTAGE vs. SUPPLY VOLTAGE



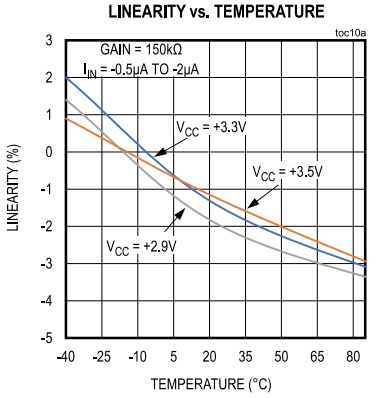
OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC-DC CURRENT



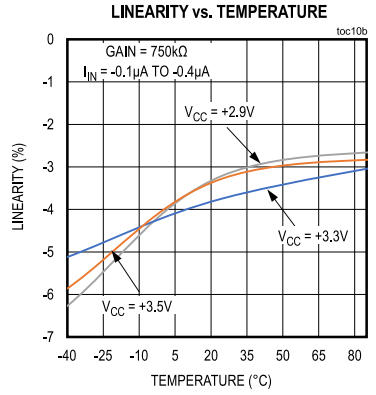
OUTPUT DIFFERENTIAL VOLTAGE vs. INPUT DC-DC CURRENT



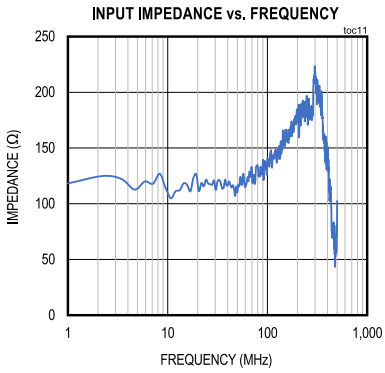
LINEARITY vs. TEMPERATURE



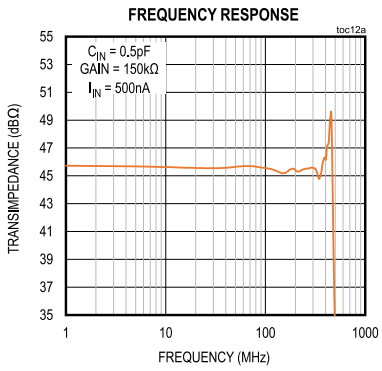
LINEARITY vs. TEMPERATURE



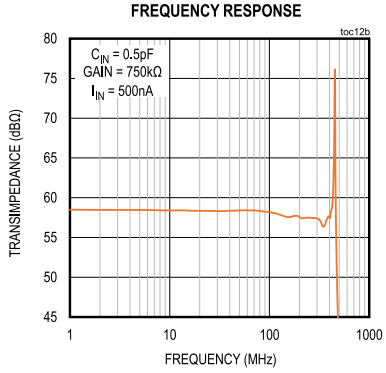
INPUT IMPEDANCE vs. FREQUENCY



FREQUENCY RESPONSE

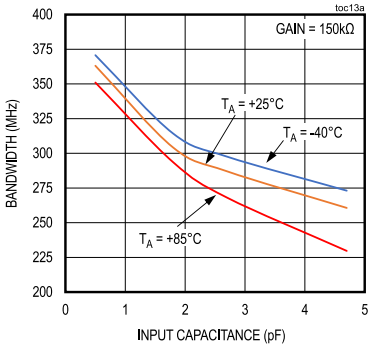


FREQUENCY RESPONSE

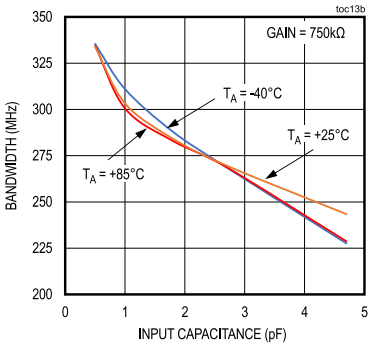


Typical Operating Characteristics (continued)

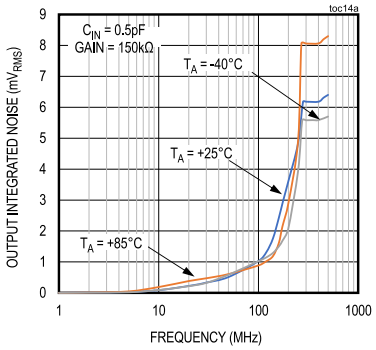
-3dB BANDWIDTH vs. INPUT CAPACITANCE



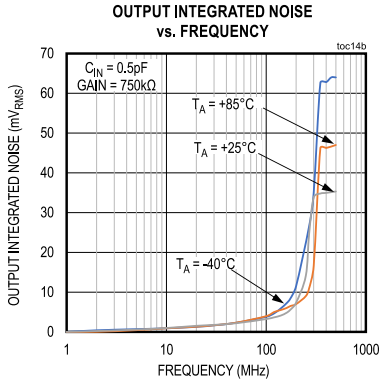
-3dB BANDWIDTH vs. INPUT CAPACITANCE



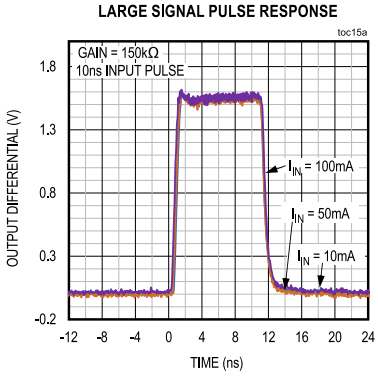
OUTPUT INTEGRATED NOISE vs. FREQUENCY



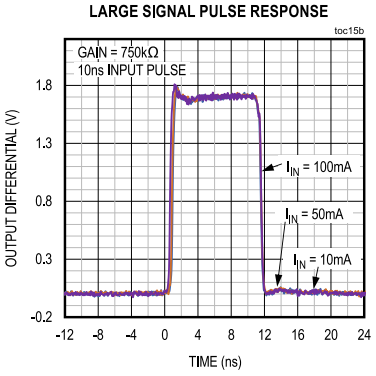
OUTPUT INTEGRATED NOISE vs. FREQUENCY



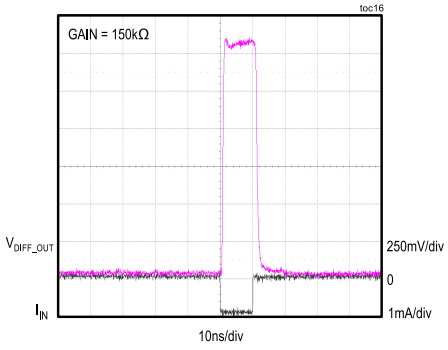
LARGE SIGNAL PULSE RESPONSE



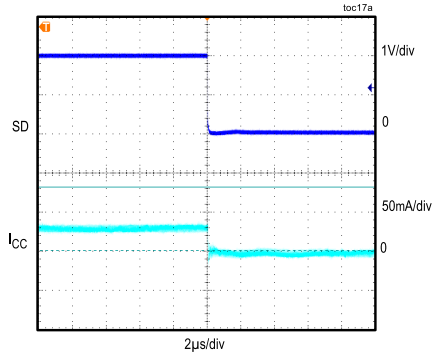
LARGE SIGNAL PULSE RESPONSE



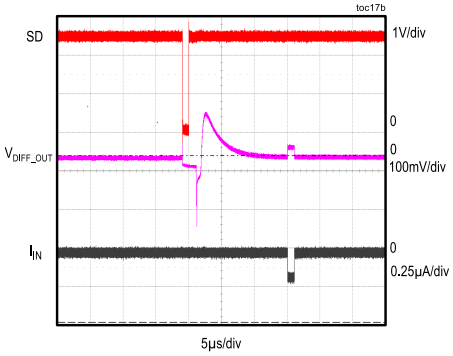
PULSE RESPONSE



SHUTDOWN DELAY RESPONSE

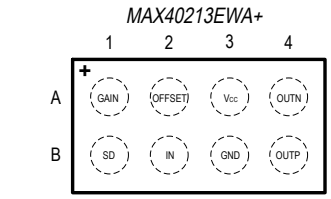


SHUTDOWN DEASSERTED RESPONSE



Pin Configuration

WLP



WLP

Pin Description

PIN	NAME	FUNCTION
A1	GAIN	Gain Select Input 1. Connect to GND or V_{CC} to select the gain.
A2	OFFSET	Offset Adjustment Input. Sink current from this input to adjust the effective input offset current. If offset adjustment is not needed, this pin should be left unconnected.
A3	V_{CC}	+3.3V Supply Voltage
A4	OUTN	Negative 50Ω Output. Increasing input current causes OUT- to decrease.
B1	SD	Enable/Shutdown Input. V_{CC} = normal operation, GND = shutdown.
B2	IN	Signal Input. Connect to photodiode cathode through a coupling capacitor when using positive bias voltage at cathode. Connect to photodiode cathode when using negative bias voltage at anode.
B3	GND	Circuit Ground
B4	OUTP	Positive 50Ω Output. Increasing input current causes OUT+ to increase.

Detailed Description

Gain Stage 1

When a photodiode with negative bias voltage is connected to the TIA input, the signal current flows out of the amplifier's summing node and into the photodiode. The input current flows through an internal load resistor to develop a voltage that is then applied to the input of the second stage. An internal clamp circuit protects against input currents as high as 2A for a 10ns pulse at 0.5% duty cycle. (Longer pulses or higher duty cycles will reduce this value.) The clamp circuit also maintains very fast overload recovery times (about 2ns) for input currents up to 100mA (see the *Typical Operating Characteristics*).

A photodiode with positive bias voltage may be used if it is capacitively coupled to the TIA input. If a photodiode with positive bias voltage is DC-coupled to the TIA input, the TIA will provide gain; however, the maximum input current will be limited to about -2A at 10ns pulse and 0.5% duty cycle.

Gain Stage 2

The second gain stage provides additional gain and converts the transimpedance amplifier's single-ended output into a differential signal.

This stage is designed to drive a 100Ω to 1kΩ differential load between OUT+ and OUT-. For optimum supply noise rejection, the outputs should be terminated with a differential load. The outputs are not intended to drive a DC-coupled grounded load. The outputs should be AC-coupled or terminated to V_{CC}. If a single-ended output is required, both the used and unused outputs should be terminated in a similar manner.

Gain Selection

The GAIN input selects the overall transimpedance as shown in Table 1. After changing the GAIN logic level, the new gain is in effect within 200ns.

Table 1. Gain Selection

GAIN LOGIC LEVEL	NOMINAL TRANSIMPEDANCE
0	150kΩ
1	750kΩ

OFFSET Input

OFFSET is a current input. The offset input current, I_{OFFSET}, is the current flowing from the OFFSET pin. This current affects the TIA's output voltage with a polarity opposite that of the current flowing from IN, so it may be used to effectively apply an offset to the output voltage (see *Typical Operating Characteristics*). OFFSET can be used to adjust the output offset voltage in a negative direction. The OFFSET pin is biased to the same voltage as the IN pin.

The use of OFFSET is optional. If the OFFSET function is not required, simply leave this input unconnected. Do not bypass this input with a capacitor.

SD Input

The MAX40213's SD (shutdown) input accepts a logic signal that can be used to shut down the TIA. Driving this input with a logic-high enables the TIA, while a logic-low disables the circuit and reduces the supply current to 0.01µA (typ).

The transimpedance amplifier takes 15µs for the output common-mode voltage return to active mode from shutdown mode.

Applications Information

Photodiode

Noise performance and bandwidth are adversely affected by capacitance on a TIA's input node. Although the MAX40213 is less sensitive than most TIAs to input capacitance, it is good practice to minimize any unnecessary capacitance. The MAX40213 is optimized for 0.5pF to 5pF of capacitance on the input. Selecting a low-capacitance photodiode helps to minimize the total input capacitance on the input pin, thereby improving noise and bandwidth performance.

Supply Filter

Sensitive optical receivers require wide-band power supply decoupling. Power supply bypassing should provide low impedance between V_{CC} and ground for frequencies between 10kHz and 700MHz. Isolate the amplifier from noise sources with LC supply filters and shielding. Place a supply filter as close to the amplifier as possible.

Layout Considerations

Some critical layout guidelines are listed below.

- A differential microstrip is the recommended layout for the TIA's outputs with terminations done close to the outputs. Care must be taken to avoid unwanted stubs by removing ground below the traces that are not part of the 50Ω termination line leading into input pins. The parasitic capacitance created between traces and ground slow down and even distort the signals by creating reflections on the path.
- The input trace connecting the photodiode to IN should be as short as possible and have ground etched or removed underneath. This will reduce or avoid unwanted parasitic capacitance created in the PCB. Having longer trace lengths increases the parasitic inductance in signal trace paths.
- Use a PC board with a low-impedance ground plane.
- Mount one or more 10nF ceramic capacitors between GND and V_{CC} as close to the pins as possible. Multiple bypass capacitors help to reduce the effect of trace impedance and capacitor ESR.
- Choose bypass capacitors for minimum inductance and ESR.
- When AC-coupling the outputs, use a 1kΩ termination resistor connected directly between OUTP and OUTN after the AC-coupling capacitors, if practical. If the destination inputs cannot be located adjacent to the outputs, use a 100Ω microstrip between the output pins and the termination resistor, which should be close to the inputs of the destination component. This avoids the creation of stub beyond the termination resistor, which causes reflections. The added length of the differential trace has less degrading effects than added stub length.
- Minimize any parasitic layout inductance.
- It is recommended to use higher performance substrate materials (e.g., Rogers).

Typical Application Circuits

AC-Coupled APD Receiver TIA

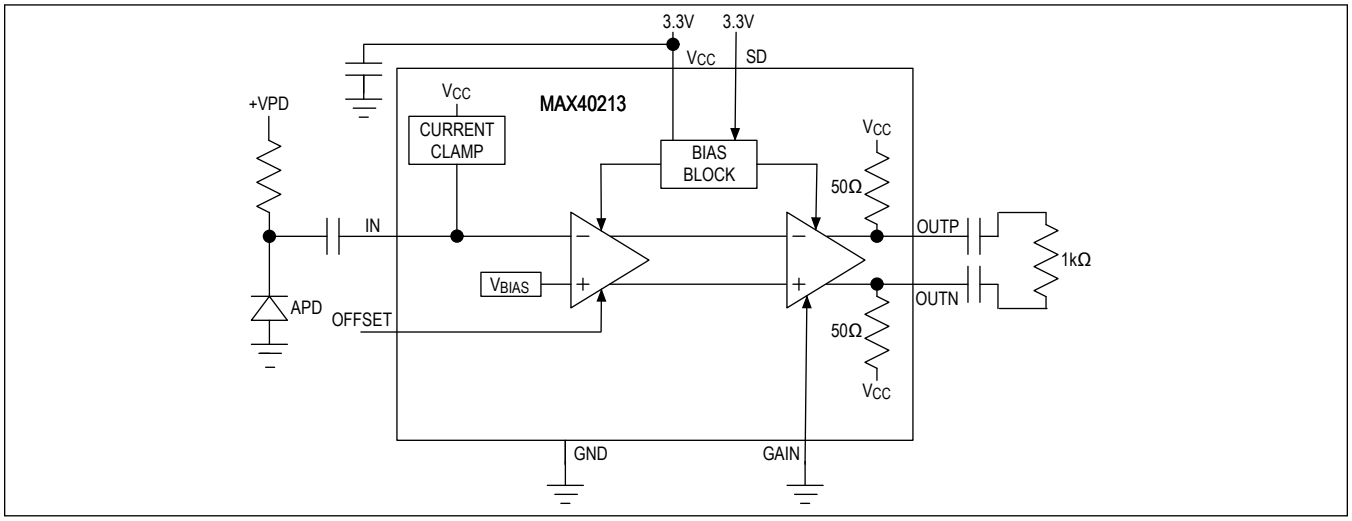


Figure 1. AC-Coupled APD Receiver TIA

The APD's cathode is connected through a coupling capacitor to the TIA's input, with the anode connected to ground. The bias voltage in this case is positive and is connected to the cathode through a resistor. Incident light pulses cause current to flow from the IN pin and into the APD. This input current also flows through an internal resistor to create a voltage, which is then amplified by the second stage to create a differential output signal that can drive a high-speed ADC or comparator.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	TOP MARK
MAX40213EWA+	-40°C to +85°C	8 WLP	+AAR
MAX40213EWA+T	-40°C to +85°C	8 WLP	+AAR

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Release for intro	—
1	5/21	Changed part number and temperature range throughout; updated *Typical Operating Characteristics, Pin Configuration, and Ordering Information* sections	1, 5–10, 13
2	11/21	Updated timing specification in *SD Input* section	11

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