Click here for production status of specific part numbers.

MAX41463/MAX41464

300MHz–960MHz (G)FSK Transmitter with I²C Interface

General Description

The MAX41463/MAX41464 is a UHF sub-GHz ISM/SRD transmitter designed to transmit Frequency-Shift Keying (FSK), or Gaussian (G)FSK (or 2GFSK) data in the 286MHz to 960MHz frequency range. It integrates a fractional phase-locked-loop (PLL) so that a single, low-cost crystal can be used to generate commonly used world-wide sub-GHz frequencies. The fast response time of the PLL allows for frequency-hopping spread spectrum protocols for increased range and security. The chip also features preset modes with pin-selectable frequencies so that only one wire is required for an external microcontroller interface. The only frequency-dependent components required are for the external antenna-matching network. A buffered clock-out signal at 800kHz is also provided. Optionally, the device can be put into programmable mode and programmed using an I²C interface. The crystal-based architecture of the MAX41463/MAX41464 eliminates many of the common problems with SAW-based transmitters by providing greater modulation depth, faster frequency settling, higher tolerance of the transmit frequency, and reduced temperature dependence.

The MAX41463/MAX41464 provides output power up to +13dBm into a 50Ω load while drawing < 12mA at 315MHz. The output load can be adjusted to increase power up to +16dBm, and a PA boost mode can be enabled at frequencies above 850MHz to compensate for losses. The PA output power can also be controlled using programmable register settings in I²C mode.

The MAX41463/MAX41464 also features single-supply operation from +1.8V to +3.6V. The device has an auto-shutdown feature to extend battery life and a fast oscillator wake-up with data activity detection.

The MAX41463/MAX41464 is available in a 10-pin TSSOP package and is specified over the -40°C to +105°C extended temperature range.

Applications

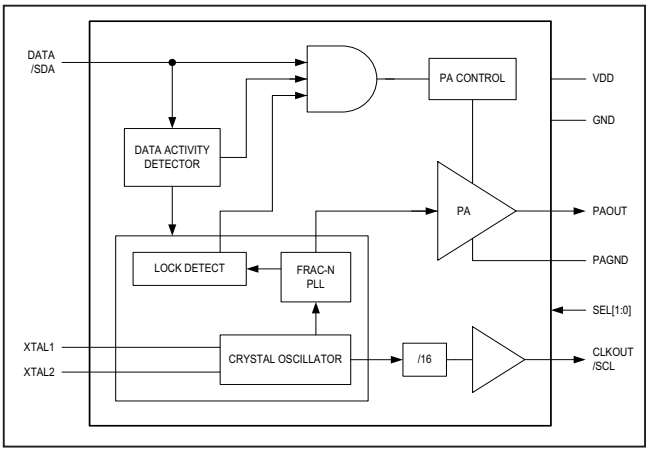
- Building Automation and Security
- Wireless Sensors and Alarms
- Remote and Passive Keyless Entry (RKE/PKE)
- Tire Pressure Monitoring Systems (TPMS)
- Automatic Meter Reading (AMR)
- Garage Door Openers (GDO)
- Radio Control Toys
- Internet of Things (IoT)

Benefits and Features

- Low Implementation Cost
  - Bits-to-RF Single Wire Operation
  - Low Bill-of-Materials (BOM)
  - Uses Single, Low-Cost, 16MHz Crystal
  - Small 3mm x 3mm TSSOP10 Package
- Increased Range, Data Rates, and Security
  - Up to +16dBm PA Output Power
  - Fast Frequency Switching for FHSS/DSSS
  - Fast-On Oscillator: <250µs Startup Time
  - Up to 200kbps NRZ Data Rate
- Extend Battery Life with Low Supply Current
  - < 12mA Typical Current Consumption at 315MHz
  - Selectable Standby and Shutdown Modes
  - Auto Shutdown at < 20nA (typ) Current
- Ease-of-Use
  - Pin-Selectable Frequencies
  - Pin-Compatible ASK and FSK Versions
  - +1.8V to +3.6V Single-Supply Operation
  - Fully Programmable with 400kHz/1MHz I²C Interface

Ordering Information *appears at end of data sheet.*

Simplified Block Diagram



maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +4V
All Others Pins to GND .....-0.3V to (V_{DD} + 0.3)V
Continuous Power Dissipation
(T_A = +70°C, derate 5.6mW/°C above +70°C.).....444.4mW
Operating Temperature Range..... -40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Lead Temperature (reflow).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TSSOP-10

Package Code	U10+2
Outline Number	**21-0061**
Land Pattern Number	**90-0330**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	180 °C/W
Junction to Case (θ_{JC})	36 °C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	113.1 °C/W
Junction to Case (θ_{JC})	36 °C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300-450MHz or +11dBm for 863-928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Voltage	V_{DD}	PA_BOOST = 0		1.8	3	3.6	V
		PA_BOOST = 1		1.8	2.7	3.0	
Operating Current	I_{DD}	FSK (Note 2)	f_{RF} = 315MHz		12	21	mA
			f_{RF} = 434MHz		13	27.5	
			f_{RF} = 863MHz–928MHz		19	39	
			f_{RF} = 315MHz, P_{OUT} = 16dBm (Note 5)		28		
			f_{RF} = 434MHz, P_{OUT} = 16dBm (Note 5)		27		
			f_{RF} = 863MHz–928MHz, P_{OUT} = 16dBm (Note 5)		43		
		FSK, Low Phase Noise mode (Note 2)	f_{RF} = 315MHz		15		
			f_{RF} = 434MHz		17		
			f_{RF} = 863MHz–928MHz		20.5		
		PA off (Note 2)	f_{RF} = 315MHz		2	3	
			f_{RF} = 434MHz		2	3	
			f_{RF} = 863MHz–928MHz		3	4	
		PA off, Low Phase Noise mode (Note 2)	f_{RF} = 315MHz		4		
			f_{RF} = 434MHz		4		
			f_{RF} = 863MHz–928MHz		5		
Standby Current	I_{STDBY}	Crystal oscillator on, everything off.	T_A = 25°C		200	500	µA
			T_A = 105°C		250		
Shutdown Current	I_{SHDN}	Everything off.	T_A = 25°C		50	100	nA
MODULATION PARAMETERS							
FSK Frequency Deviation		Default value			±39		kHz
FSK Minimum Frequency Deviation					±1		kHz
FSK Minimum Frequency Deviation for Gaussian Shaping					±10		kHz
FSK Maximum Frequency Deviation					±100		kHz
Minimum MSK Data Rate		FSK modulation index = 0.5			4		kbps
Maximum NRZ Data Rate					200		kbps

Electrical Characteristics (continued)

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300-450MHz or +11dBm for 863-928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER AMPLIFIER							
Output Power	P_{OUT}	f_{RF} = 300MHz–450MHz (Note 4)			13		dBm
		f_{RF} = 300MHz–450MHz (Note 4, Note 5)			17		
		f_{RF} = 863MHz–928MHz (Note 4)			11		
		f_{RF} = 863MHz–928MHz (Note 4, Note 5), PA_BOOST = 1			16		
Maximum Carrier Harmonics		PA_BOOST = 0. Supply current, output power, and harmonics are dependent on board layout and PAOUT match.			-24		dBc
PLL							
Frequency Range		Low Current mode (default)		286		960	MHz
		Low Phase Noise mode, LODIV = DIV12		286.7		320	
		Low Phase Noise mode, LODIV = DIV8		425		480	
		Low Phase Noise mode, LODIV = DIV4		860		960	
PLL Phase Noise		f_{RF} = 315MHz, Low Current mode (default)	f_{OFFSET} = 200kHz		-82		dBc/Hz
			f_{OFFSET} = 1MHz		-90		
		f_{RF} = 434MHz, Low Current mode (default)	f_{OFFSET} = 200kHz		-80		
			f_{OFFSET} = 1MHz		-90		
		f_{RF} = 915MHz, Low Phase Noise mode	f_{OFFSET} = 200KHz		-82		
			f_{OFFSET} = 1MHz		-104		
LO Divider Settings					4		
					8		
					12		
Minimum Synthesizer Frequency Step					$f_{XTAL}/2^{16}$		Hz
Reference Spur		f_{RF} = 315MHz	$f_{RF} \pm f_{XTAL}$		-67		dBc
		f_{RF} = 434MHz	$f_{RF} \pm f_{XTAL}$		-60		
		f_{RF} = 868MHz	$f_{RF} \pm f_{XTAL}$		-57		
		f_{RF} = 915MHz	$f_{RF} \pm f_{XTAL}$		-56		
Reference Frequency Input Level					500		mV_{P-P}
Frequency Switching Time		26MHz frequency step, 902MHz to 928MHz band, time from end of register write to frequency settled to within 5kHz of desired carrier			50		µs
Loop Bandwidth	LBW				300		kHz

Electrical Characteristics (continued)

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300-450MHz or +11dBm for 863-928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Frequency Divider Range	N			11		72	
Turn-On Time of PLL	t_{PLL}	f_{RF} = 315MHz			30		µs
		f_{RF} = 915MHz			90		
CRYSTAL OSCILLATOR							
Crystal Frequency	f_{XTAL}	Recommended value (Note 3)		12.8	16	19.2	MHz
Crystal Oscillator Startup Time	t_{XO}	Refer to *Preset Mode Transmission* section			243		µs
Frequency Pulling by VDD					3		ppm/V
Crystal Input Capacitance	C_X	Internal capacitance of XTAL1 and XTAL2 pins to ground.			12		pF
CMOS INPUT/OUTPUT							
Input Low Voltage	V_{IL}	SCL/SDA	1.8V compatible			0.36	V
	V_{IL_SEL}	SEL0/SEL1				0.1 x V_{DD3}	
Input High Voltage	V_{IH}	SCL/SDA	1.8V compatible	1.44			V
	V_{IH_SEL}	SEL0/SEL1		0.9 x V_{DD3}			
Input Current	I_{IL}/I_{IH}				±10		µA
Output Low Voltage	V_{OL}	I_{SINK} = 650µA			0.25		V
Output High Voltage	V_{OH}	I_{SOURCE} = 350µA			V_{DD} - 0.25		V
Maximum Capacitance at SEL0/ SEL1 Pins	C_{L_SEL}				10		pF
Maximum Load Capacitance at CLKOUT Pin	C_{LOAD}				10		pF
SERIAL INTERFACE (FIGURE 1)							
SCL Clock Frequency	f_{SCL}			400		1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}			500			ns
Hold Time (Repeated) START Condition	$t_{HD:STA}$			260			ns
Low Period of SCL	t_{LOW}			500			ns
High Period of SCL	t_{HIGH}			260			ns

Electrical Characteristics (continued)

(*Typical Application Circuit*, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +1.8V to +3.6V, T_A = -40°C to +105°C, P_{OUT} = +13dBm for 300-450MHz or +11dBm for 863-928MHz, PA_BOOST = 0, unless otherwise noted. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	Receive	0		150	ns
		Transmit	0			
Data Setup Time	$t_{SU:DAT}$		50			ns
Start Setup Time	$t_{SU:STA}$		260			ns
SDA and SCL Rise Time	t_R				120	ns
SDA and SCL Fall Time	t_F		20 x V_{IO}/5.5		120	ns
Stop Setup Time	$t_{SU:STO}$		260			ns
Noise Spike Reject	t_{SP}			25		ns

Note 1: Supply current, output power and efficiency are greatly dependent on board layout and PA output match.
Note 2: 100% tested at T_A = +25°C. Limits over operating temperature and relevant supply voltage are guaranteed by design and characterization over temperature.
Note 3: Guaranteed by design and characterization. Not production tested.
Note 4: Typical values are average, peak power is 3dB higher.
Note 5: Using high output power match, refer to Table 3.

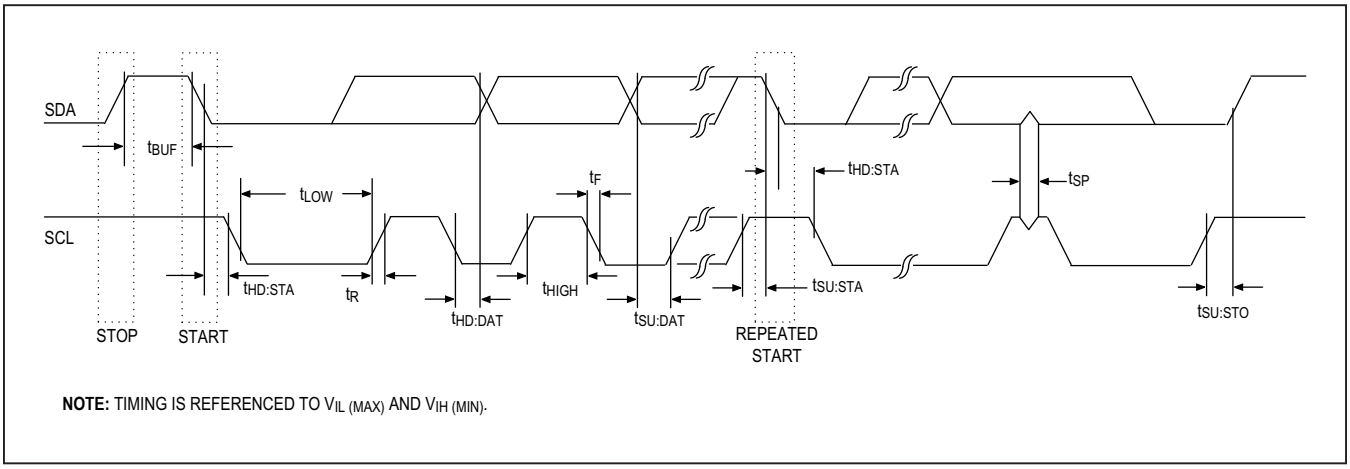
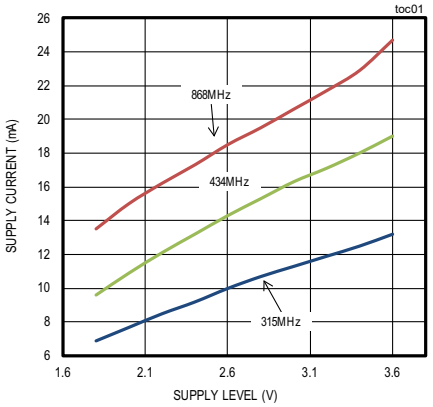


Figure 1. Serial Interface Timing Diagram

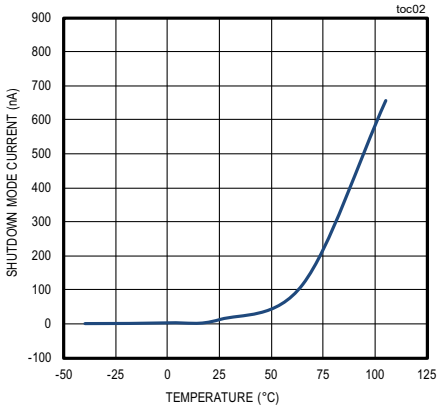
Typical Operating Characteristics

(*Typical Application Circuit*, RF output terminated to 50Ω. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

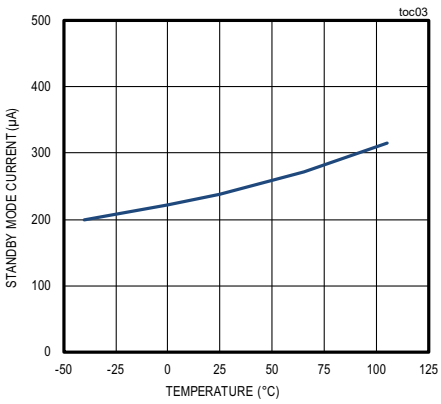
FSK SUPPLY CURRENT vs. VOLTAGE



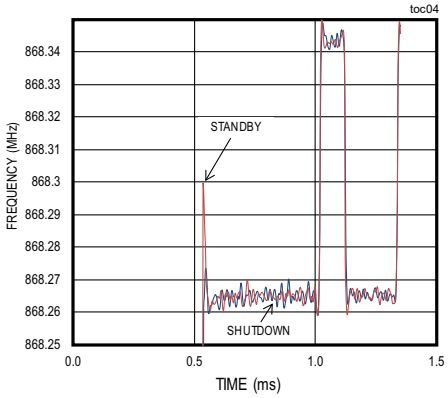
SHUTDOWN CURRENT vs. TEMPERATURE



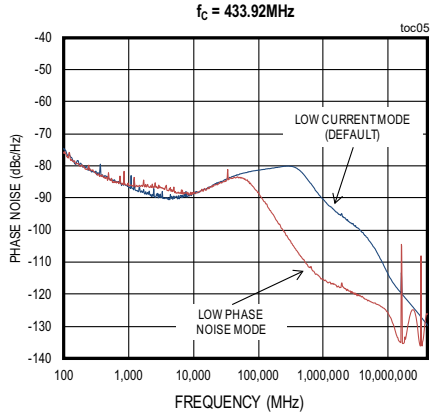
STANDBY CURRENT vs. TEMPERATURE



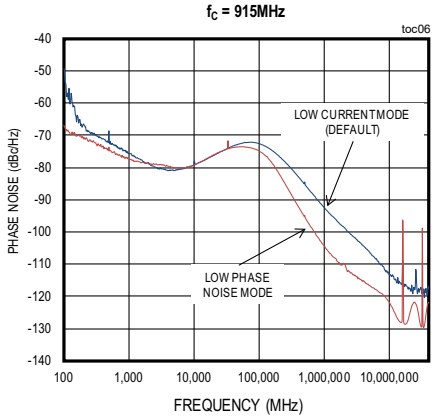
FREQUENCY SETTLING
f_C = 868.3MHz, 2.5kbps



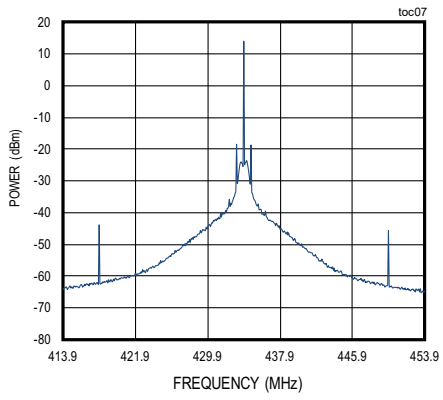
PHASE NOISE vs. OFFSET FREQUENCY
f_C = 433.92MHz



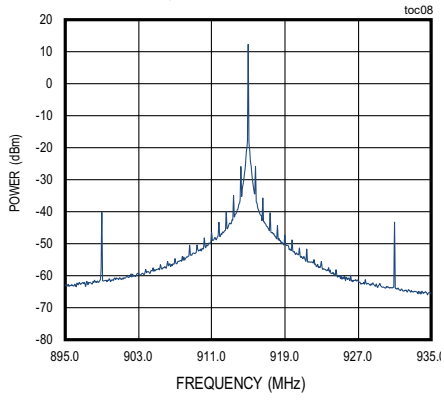
PHASE NOISE vs. OFFSET FREQUENCY
f_C = 915MHz



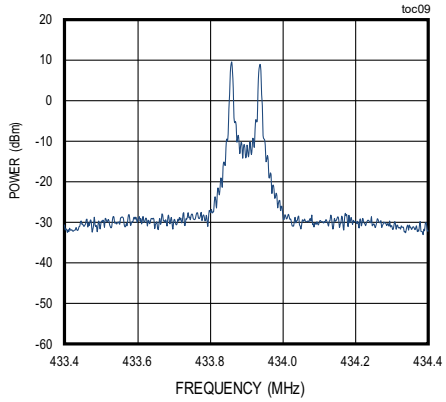
UNMODULATED SPECTRUM OUTPUT
f_C = 433.92MHz, RBW = 3kHz



UNMODULATED SPECTRUM OUTPUT
f_C = 915MHz, RBW = 3kHz



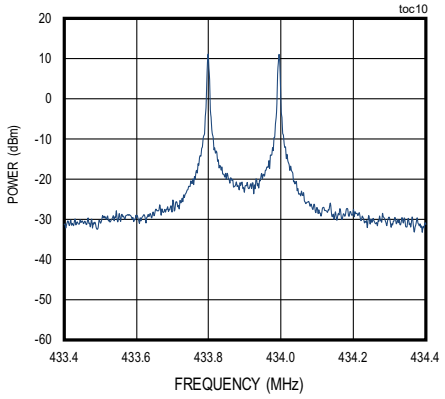
FSK ±39kHz MODULATED SPECTRUM OUTPUT
f_C = 433.92MHz, RBW = 3kHz



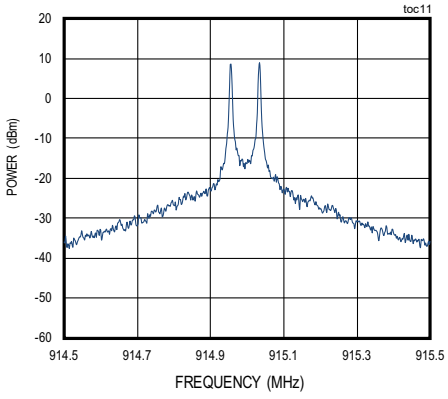
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, RF output terminated to 50Ω. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

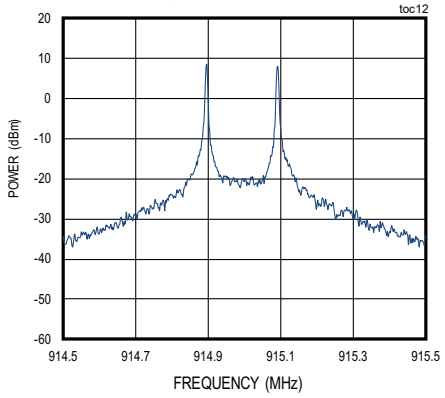
FSK ±100kHz MODULATED SPECTRUM OUTPUT
f_C = 433.92MHz, RBW = 3kHz



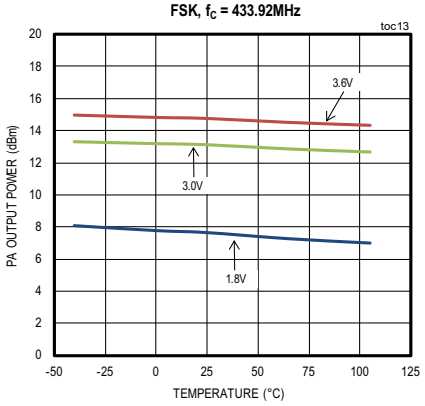
FSK ±39kHz MODULATED SPECTRUM OUTPUT
f_C = 915MHz, RBW = 3kHz



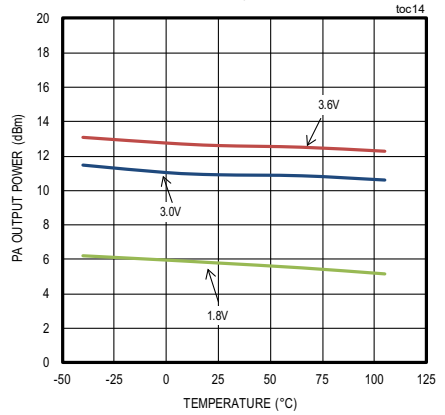
FSK ±39kHz MODULATED SPECTRUM OUTPUT
f_C = 915MHz, RBW = 3kHz



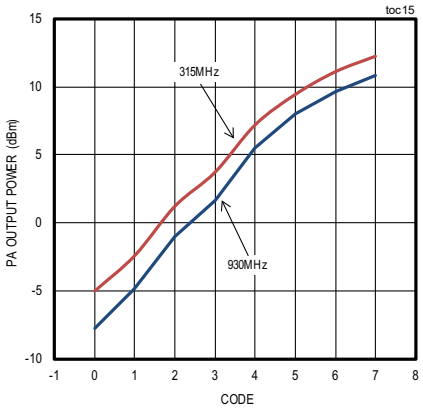
PA POWER OUTPUT vs. TEMPERATURE
FSK, f_C = 433.92MHz



PA POWER OUTPUT vs. TEMPERATURE
ASK, f_C = 930MHz



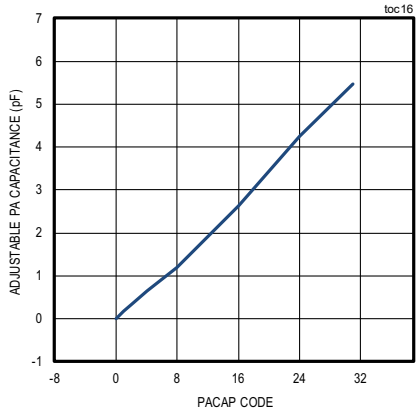
PA OUTPUT POWER vs. PAPWR CODE



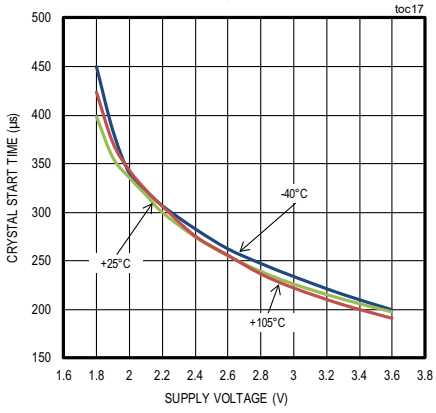
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, RF output terminated to 50Ω. Typical values are at V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

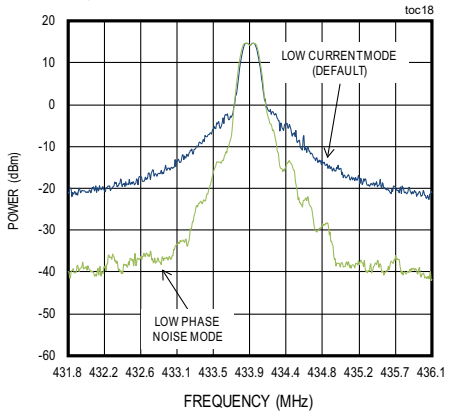
ADJUSTABLE PA CAPACITANCE vs. PACAP CODE
f_C = 434MHz, C_{PA} ≈ 4.7pF



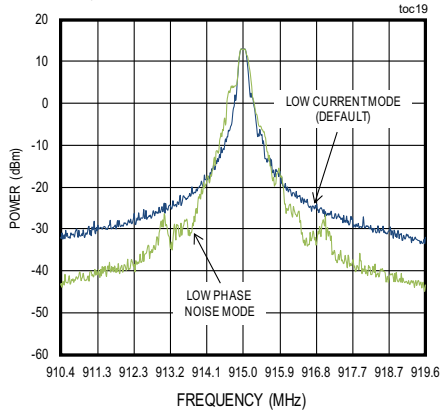
CRYSTAL STARTUP TIME vs. SUPPLY
FSK, f_C = 433.92MHz



FSK SPECTRUM
LOW-CURRENT vs. LOW-PHASE NOISE MODE
f_C = 433.92MHz, ±39kHz, RBW = 100kHz, MAX-HOLD

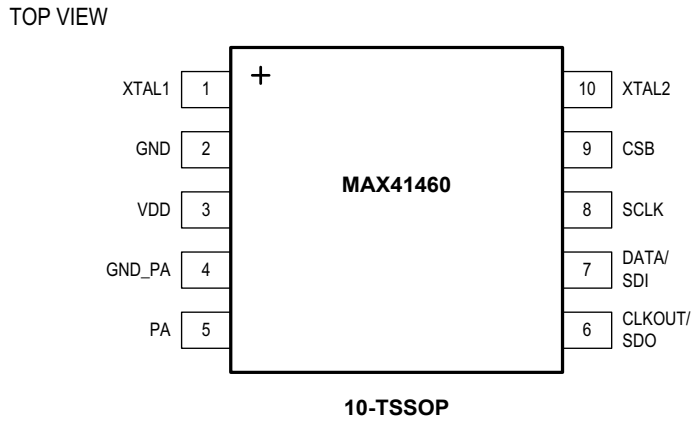


FSK SPECTRUM
LOW-CURRENT vs. LOW-PHASE NOISE MODE
f_C = 915MHz, ±39kHz, RBW = 100kHz, MAX-HOLD



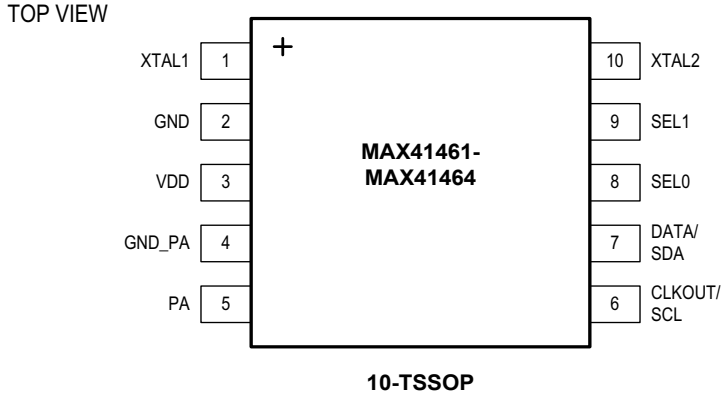
Pin Configurations

MAX41460



10-TSSOP

MAX41461-64



10-TSSOP

Pin Description

PIN		NAME	FUNCTION
MAX41460	MAX41461/ MAX41464		
XTAL2	XTAL2	1	2nd Crystal Input. See *Crystal (XTAL) Oscillator* section.
GND	GND	2	Ground. Connect to system ground.
VDD	VDD	3	Supply Voltage. Bypass to GND with a 100nF capacitor as close to the pin as possible.
GND_PA	GND_PA	4	Ground for the Power Amplifier (PA). Connect to system ground.
PA	PA	5	Power-Amplifier Output. The PA output requires a pullup inductor to the supply voltage, which can be part of the output-matching network to an antenna.
CLKOUT/SDO	CLKOUT/SCL	6	MAX41460: Buffered Clock Output or SPI Data Output. MAX41461–MAX41464: Buffered Clock Output. I2C clock input for register programming when in Serial Interface mode (SEL0 and SEL1 are unconnected or HIZ). The frequency of CLKOUT is 800kHz when not in Program Mode.
DATA/SDI	DATA/SDA	7	MAX41460: Data Input. SPI bus serial data input for register programming when CSB is at logic-low. MAX41461-MAX41464: Data Input. I2C serial data input for register programming when in Serial Interface mode (SEL0 and SEL1 are unconnected or HIZ). When not in Progam mode, DATA also controls the power-up state (see *Auto-Shutdown in Preset Mode* section).
SCLK	SEL0	8	MAX41460: SPI Bus Serial Clock Input. MAX41461-MAX41464: Tri-State Mode Input. See *Preset Modes* for details. For tri-state input open mode, the impedance on the pin must be greater than 1MΩ.
CSB	SEL1	9	MAX41460: SPI Bus Chip Enable. Active-Low. MAX41461-MAX41464: Tri-State Mode Input. See *Preset Modes* for details. For tri-state input open mode, the impedance on the pin must be greater than 1MΩ.
XTAL1	XTAL1	10	1st Crystal Input. See *Crystal (XTAL) Oscillator* section.

Detailed Description

The MAX41463/MAX41464 is part of the MAX4146x family of UHF sub-GHz ISM/SRD transmitters designed to transmit (G)FSK data in the 286MHz to 960MHz frequency range. The MAX4146x family is available in the following versions.

The MAX41460 uses a SPI programming interface, The MAX41461–MAX41464 feature an I²C interface, as well as preset modes (pin-selectable output frequencies using only one crystal frequency). In preset modes, no programming is required and only a single-input data interface to an external micro-controller is needed. The MAX41463/MAX41464 parts are identical when put in I²C programming mode. All MAX4146x versions are fully programmable for all output frequencies, as described in the *Electrical Characteristics* table. The only frequency-dependent components required are for the external antenna match.

The crystal-based architecture of the MAX41463/MAX41464 provides greater modulation depth, faster frequency settling, higher tolerance of the transmit frequency, and reduced temperature dependence. It integrates a fractional phase-locked-loop (PLL) so a single low-cost crystal can be used to generate commonly used world-wide sub-GHz frequencies. A buffered clock-out signal make the device compatible with almost any microcontroller or code-hopping generator.

The MAX41463/MAX41464 provides +13dBm output power into a 50Ω load at 315MHz using an integrated high efficiency power amplifier (PA). The output load can be adjusted to increase power up to +16dBm and a PA boost mode can be enabled at frequencies above 850MHz to compensate for losses. The PA output power can also be controlled using programmable register settings. The MAX41463/MAX41464 feature fast oscillator wake-up upon data activity detection and has an auto-shutdown feature to extend battery life.

The MAX41463/MAX41464 operates at a supply voltage of +1.8V to +3.6V and is available in a 10-pin TSSOP package that is specified over the -40°C to +105°C extended temperature range.

Preset Modes

The MAX41463/MAX41464 contain preset settings depending on the state of pins SEL1 and SEL0. All presets must use a 16MHz crystal. The frequency of the CLKOUT pin is always 800kHz. By default, the frequency deviation is ±39kHz and Gaussian frequency shaping is enabled.

Table 1. MAX4146x Versions

VERSION	MODULATION AND INTERFACE	PRESET FREQUENCIES
MAX41460	ASK/FSK with SPI	No presets, programmable through SPI
MAX41461	ASK (optional I²C)	315/318/319.51/345/433.42/433.92/908/915 [MHz]
MAX41462	ASK (optional I²C)	315/433/433.92/434/868/868.3/868.35/868.5 [MHz]
MAX41463	FSK (optional I²C)	315/433.42/433.92/908/908.42/908.8/915/916 [MHz]
MAX41464	FSK (optional I²C)	315/433.92/868.3/868.35/868.42/868.5/868.95/869.85 [MHz]

Table 2. Programming and Preset Modes

SEL1 STATE	SEL0 STATE	MAX41463	MAX41464
Ground	Ground	I²C Mode	I²C Mode
Ground	Open	315	315
Ground	VDD	916	433.92
Open	Ground	908.42	868.42
Open	Open	908.8	868.95
Open	VDD	908	868.3
VDD	Ground	915	869.85
VDD	Open	433.92	868.5
VDD	VDD	433.42	868.35

Preset Mode Transmission

The wake-up of the device is as follows:

1) The microcontroller sends a wake-up pulse on DATA. The duration of the wake-up pulse should be longer than $t_{XO} + t_{PLL}$.
2) After the falling edge of wake-up pulse, the microcontroller should wait for at least t_{TX} time and start data transmission. In preset mode, t_{TX} = 10 µs.
3) CLKOUT is generated 80 µs after internal 3.2MHz clock is available.

Auto-Shutdown in Preset Mode

The MAX41463/MAX41464 in preset mode has an automatic shutdown feature that places the device in low-power shutdown mode if the DATA input stays at logic 0 for a wait time equal to 2^{12} cycles of the internal 3.2MHz clock. This equates to a wait time of approximately 1.3ms.

When the device is in automatic shutdown, a pulse on DATA initiates the warm up of the crystal and PLL. See the *Preset Mode Transmission* section for requirements on the wake-up pulse.

When the device is operating, each occurrence of logic 1 on the data line resets an internal counter to zero and it begins to count again. If the counter reaches the end-of-count, the device enters shutdown mode.

Power Amplifier

The MAX41463/MAX41464 PA is a high-efficiency, open-drain switching-mode amplifier. In a switching-mode amplifier, the gate of the final-stage FET is driven with a 25% duty-cycle square wave at the transmit frequency. The PA also has an internal set of capacitors that can be switched in and out to present different capacitance values at the PA output using the PACAP[4:0] register values. This allows extra flexibility for tuning the output matching network. When the matching network is tuned correctly, the output FET resonates the attached tank circuit (pullup inductor from PA to VDD) with a minimum amount of power dissipated in the FET. With a proper output-matching network, the PA can drive a wide range of antenna impedances, which include a PCB trace antenna or a 50Ω antenna. The output-matching π-network suppresses the carrier harmonics and transforms the antenna impedance to an optimal impedance at the PA pin. The *Typical Application Circuit* can deliver an output power of +13dBm with a +3.0V supply. Table 3 has approximate PA load impedances for desired output powers.

The PAPWR bits in the PA1 register control the output power of the PA. This setting adjust the number of parallel drivers used, which determine the final output power (see Figure 3).

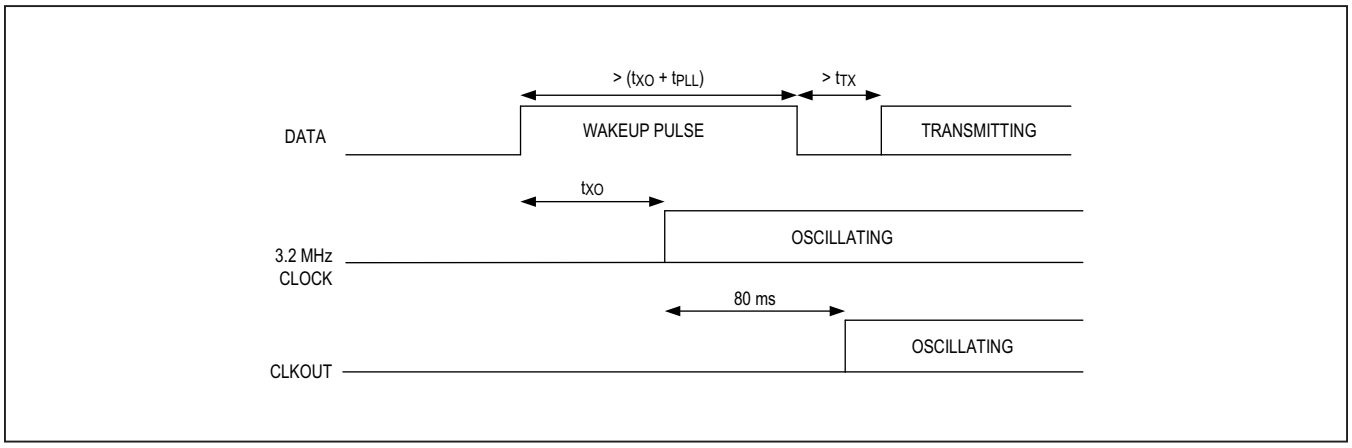


Figure 2. Wake-up timing diagram for preset mode

Boost Mode

The PA can deliver up to 16dBm of output power.

High output power can be achieved in two ways:

- Lower the load impedance for the PA by adjusting the output matching network,
- For frequencies over 850MHz, change the duty cycle of the square wave driving the FET from 25% to 50% by setting PA_BOOST = 1 in register SHDN (0x05) and adjusting the output matching network.

Note that, when using PA_BOOST = 1, the maximum supply voltage should not exceed 3V. For frequencies under 850MHz, the PA_BOOST bit should remain at 0, the output match can be adjusted to provide higher output power.

Programmable Output Capacitance

The MAX41463/MAX41464 has an internal set of capacitors that can be switched in and out to present different capacitor values at the PA output. The capacitors are connected from the PA output to ground. This allows changing the tuning network along with the synthesizer divide ratio each time the transmitted frequency changes, making it possible to maintain maximum transmitter power while moving rapidly from one frequency to another.

The variable capacitor is programmed through register PA2 (0x07) bits 4:0 (PACAP). The tuning capacitor has a nominal resolution of 0.18pF, from 0pF to 5.4pF. In preset mode, the variable capacitor is set to 0pF.

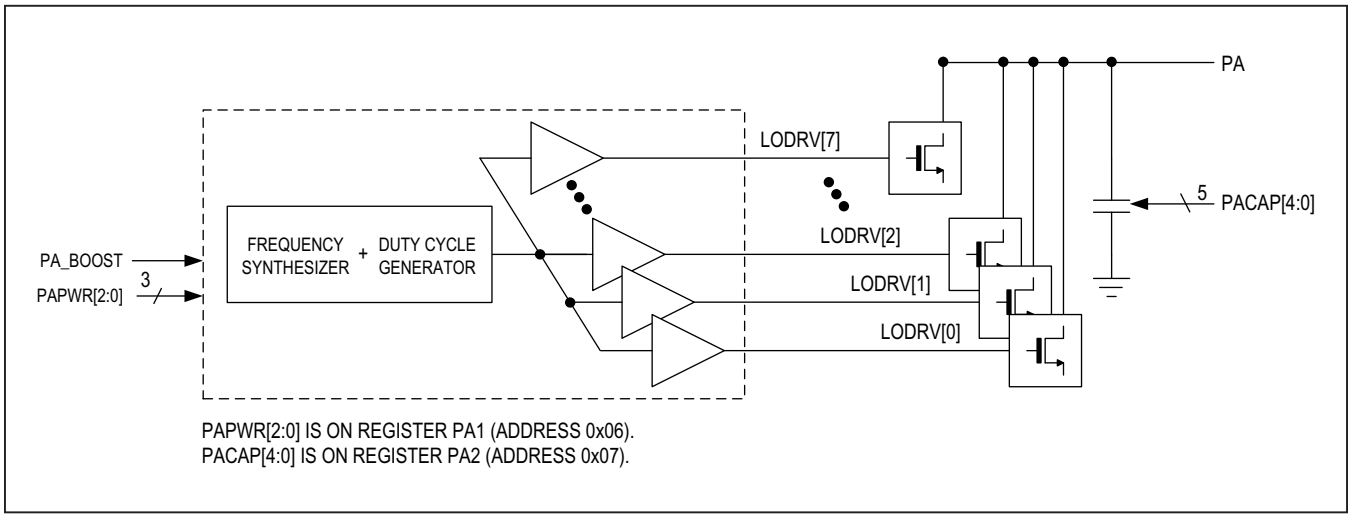


Figure 3. Power Amplifier

Table 3. PA Load Impedance for Desired Output Power

FREQUENCY	OUTPUT POWER	PA LOAD IMPEDANCE
315MHz	13dBm	165Ω
315MHz	16dBm (PA_BOOST = 0)	45Ω
434MHz	13dBm	180Ω
434MHz	16dBm (PA_BOOST = 0)	57Ω
863MHz–928MHz	11dBm	190Ω
863MHz–928MHz	16dBm (PA_BOOST = 1)	34Ω

Refer to the MAX4146x EV Kit User's Guide for details.

Transmitter Power Control

The transmitter power of the MAX41463/MAX41464 can be set in approximately 2.5dB steps by setting PAPWR[2:0] register bits using the I2C interface. The transmitted power (and the transmitter current) can be lowered by increasing the load impedance on the PA. Conversely, the transmitted power can be increased by lowering the load impedance.

Preset Mode Output Power

The output power of the PA in Preset mode (where both SEL0 and SEL1 pins are not connected to GND) is always set for maximum power level (PAPWR[2:0] = 0x7) for a given load impedance. In order to adjust output power levels in preset mode, the load impedance must be adjusted accordingly.

Crystal (XTAL) Oscillator

The XTAL oscillator in the MAX41463/MAX41464 is designed to present a capacitance of approximately 12pF from the XTAL1 and XTAL2 pins to ground. In most cases, this corresponds to a 6pF load capacitance applied to the external crystal when typical PCB parasitics are included. It is very important to use a crystal with a load capacitance equal to the capacitance of the MAX41463/MAX41464 crystal oscillator plus PCB parasitics. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency introducing an error in the reference frequency. The crystal's natural frequency is typically below its specified frequency. However, when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance. Accounting for typical board parasitics, a 16MHz, 12pF crystal is recommended. Note that adding discrete capacitance on the crystal also increases the startup time and adding too much capacitance could prevent oscillation altogether.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE}+C_{LOAD}} - \frac{1}{C_{CASE}+C_{SPEC}}\right) \times 10^6$$

where:

f_P is the amount the crystal frequency pulled in ppm

C_M is the motional capacitance of the crystal

C_{CASE} is the case capacitance

C_{SPEC} is the specified load capacitance

C_{LOAD} is the load capacitance

When the crystal is loaded as specified (i.e., C_{LOAD} = C_{SPEC}), the frequency pulling equals zero. For additional details on crystal pulling and load capacitance affects, refer to *Maxim Tutorial 5422 - Crystal Calculations for ISM RF Products*.

Turn-On Time of Crystal Oscillator

The turn-on time of crystal oscillator (XO), t_{XO}, is defined as elapsed time from the instant of turning on XO circuit to the first rising edge of XO divider clock output. The external microcontroller turns on the XO by,

1) Sending a wakeup pulse for MAX41461–MAX41464 in the preset mode, or
2) Writing to device I2C address for MAX41461–MAX41464 in the I2C mode, or
3) Pulling CSB pin low on the MAX41460.

Crystal Divider

The recommended crystal frequencies are 13.0 MHz, 16.0 MHz, and 19.2 MHz. An internal clock of 3.2MHz±0.1MHz frequency is required. To maintain the internal 3.2MHz time base, XOCLKDIV[1:0] (register CFG1, 0x00, bit 4) must be programmed, based on the crystal frequency, as shown in the table below.

Table 4. Required Crystal Divider Programming

CRYSTAL FREQUENCY	CRYSTAL DIVIDER RATIO	XOCLKDIV[1:0]
13.0MHz	4	00
16.0MHz	5	01
19.2MHz	6	10

Crystal Frequency in Preset Mode

For MAX41463/MAX41464 in preset mode (where *both* SEL0 and SEL1 pins are *not* connected to GND), crystal frequency must be 16MHz to ensure accurate output frequency.

Phase-Locked Loop (PLL)

The MAX41463/MAX41464 utilizes a fully integrated fractional-N PLL for its frequency synthesizer. All PLL components, including loop filter, are included on-chip. The synthesizer has a 16-bit fractional-N topology with a divide ratio that can be set from 11 to 72, allowing the transmit frequency to be adjusted in increments of $f_{XTAL}/65536$. The fractional-N architecture also allows exact FSK frequency deviations to be programmed. FSK deviations as low as ±1kHz and as high as ±100kHz can be set by programming the appropriate registers.

The internal VCO can be tuned continuously from 286MHz to 960MHz in normal mode, and from 286MHz–320MHz, 425MHz–480MHz, and 860MHz–960MHz in low phase noise mode.

Frequency Programming

The desired frequency can be programmed by setting bits FREQ in registers PLL3, PLL4, and PLL5 (0x0B, 0x0C, 0x0D). To calculate the FREQ bits, use:

$$FREQ[23:0] = ROUND\left(\frac{65536 \times f_C}{f_{XTAL}}\right)$$

Follow Table 4 to program the LODIV bits in register PLL1 (0x08) when choosing a LO frequency. It is recommended to leave bits CPVAL and CPLIN at factory defaults. If integer-N synthesis is desired, set bit FRACMODE = 0 in register PLL1.

Fractional-N Spurious

The 16-bit fractional-N, delta-sigma modulator can produce spurious that can show up on the power amplifier output spectrum. If slight frequency offsets can be tolerated, set the LSB of FREQ (register PLL5, bit 0) to logic-high.

Table 5. LODIV Setting

FREQUENCY RANGE	LODIV SETTING
286MHz–960MHz, Low Noise Mode	0x0
286MHz–320MHz, Low Phase Noise	0x3
425MHz–480MHz, Low Phase Noise	0x2
860MHz–960MHz, Low Phase Noise	0x1

Using an odd value (logic 1 at bit 0) of the 24-bit FREQ register will produce lower PLL spurious compared to even values (logic 0 at bit 0).

Turn-on Time of PLL

The turn-on time of PLL, t_{PLL}, is defined as elapsed time from the instant when the XO output is available to the instant when PLL frequency acquisition is complete.

Two-Wire I2C Serial Interface

When pins SEL0 and SEL1 are grounded, the MAX41463/MAX41464 features a 2-wire I2C-compatible serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX41463/MAX41464 and the master at clock frequencies up to 1MHz. The master device initiates a data transfer on the bus and generates the SCL signal to permit data transfer. The MAX41463/MAX41464 functions as an I2C slave device that transfers and receives data to and from the master. Pull SDA and SCL high with external pull-up resistors of 1kΩ or greater, referenced to VDD for proper I2C operation.

One bit transfers during each SCL clock cycle. A minimum of nine clock cycles is required to transfer a byte into or out of the MAX41463/MAX41464 (8 bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

Figure 4 and Figure 5 show I2C Write transaction and I2C Read transaction protocols, respectively.

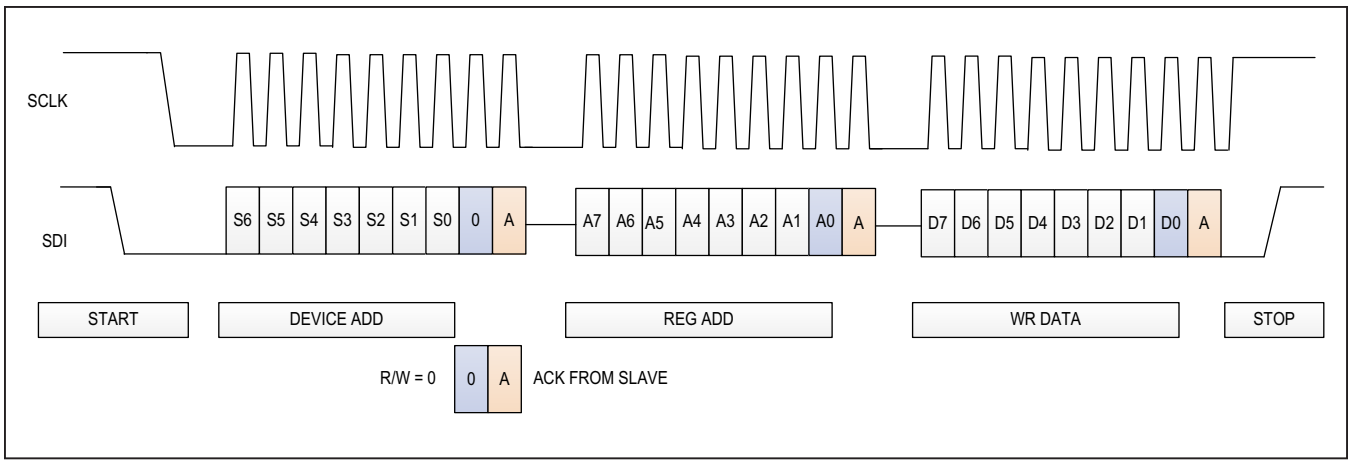


Figure 4. I2C Write

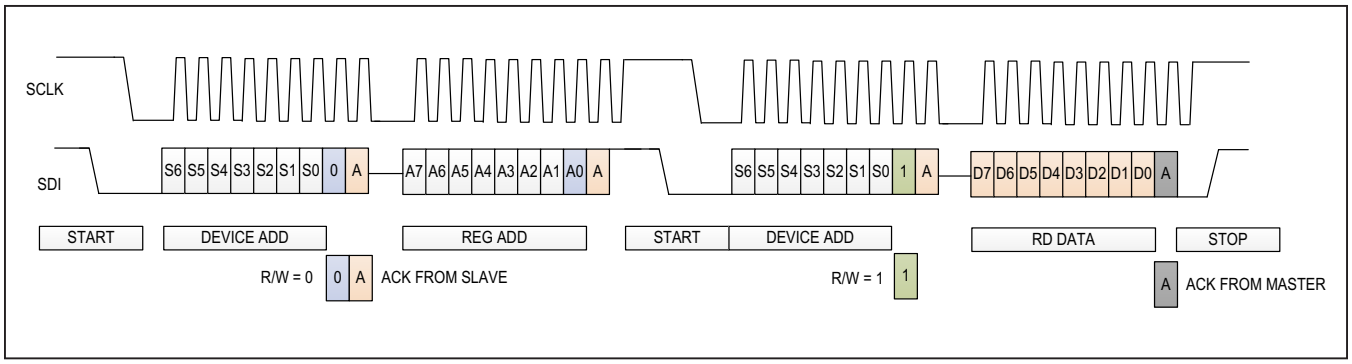


Figure 5. I2C Read

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high.

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX41463/MAX41464 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse.

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master must reattempt communication at a later time.

Slave Address

The MAX41463/MAX41464 has a 7-bit I2C slave address that must be sent to the device following a START condition to initiate communication. The slave address is internally programmed to 0xD2 for WRITE and 0xD3 for READ. The MAX41463/MAX41464 continuously awaits a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges by pulling the SDA line low for one clock period, then it is ready to accept or send data, depending on the R/W bit.

Write Cycle

When addressed with a write command, the MAX41463/MAX41464 allows the master to write to either a single register or to multiple successive registers.

A write cycle begins with the bus master issuing a START condition, followed by the 7 slave address bits and a write bit (R/W = 0). The MAX41463/MAX41464 issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to write to (see *Register Map*). The slave acknowledges the address and the master can then write one byte to the register at the specified address. Data is written beginning with the most significant bit (MSB). The MAX41463/MAX41464 again issues an ACK if the data is successfully written to the register.

The master can continue to write data to the successive internal registers with the MAX41463/MAX41464 acknowledging each successful transfer, or the master can terminate transmission by issuing a STOP condition. The write cycle does not terminate until the master issues a STOP condition.

Figure 6 illustrates I2C Burst Write transaction protocol.

Read Cycle

When addressed with a read command, the MAX41463/MAX41464 allows the master to read back a single register or multiple successive registers.

A read cycle begins with the bus master issuing a START condition, followed by the 7 slave address bits and a write bit (R/W = 0). The device issues an ACK if the slave address byte is successfully received. The bus master must then send the address of the first register it wishes to read. The slave acknowledges the address. A START condition is then issued by the master, followed by the 7 slave address bits and a read bit (R/W = 1). The device issues an ACK if the slave address byte is successfully received. The device starts sending data MSB first with each SCL clock cycle. At the 9th clock cycle, the master can issue an ACK and continue to read successive registers, or the master can terminate the transmission by issuing a NACK. The read cycle does not terminate until the master issues a STOP condition.

Buffered Clock Output

MAX41463/MAX41464 provides a buffered clock output (CLKOUT) on pin 6 of the chip in the preset mode, and the frequency of CLKOUT is 800kHz. In I2C mode, MAX41463/MAX41464 uses pin 6 as the SCL line of the I2C interface.

CLKOUT_DELAY[1:0] (register CFG2, address 0x01, bits 7:6) is only used in the preset modes, with a preset value of 0x02. These two register bits are not used in programming mode.

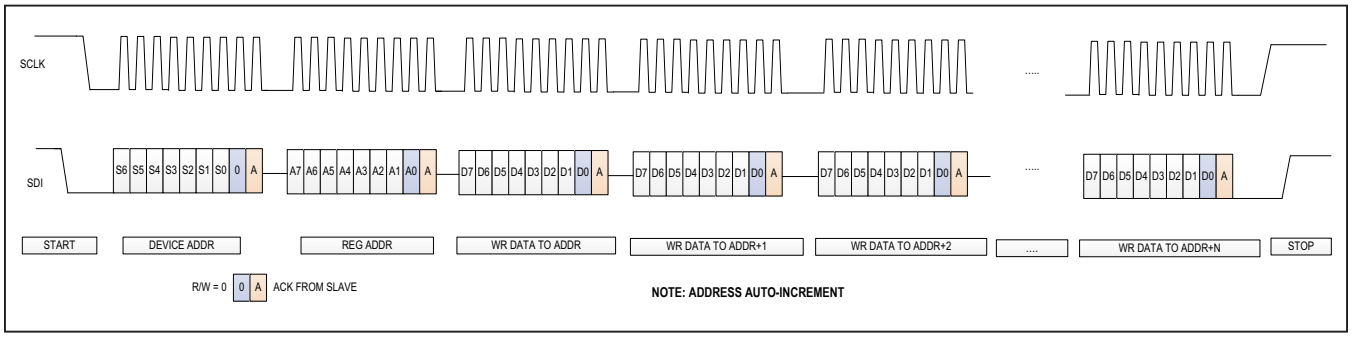


Figure 6. I2C Burst Write

State Diagrams

In the preset mode, the MAX41463/MAX41464 device has two major states: shutdown and transmitter-enabled.

In the shutdown state, the crystal oscillator (XO), the PLL synthesizer, and the power amplifier (PA) are all turned off.

In transmitter-enabled state, XO and PLL are turned on; PA is turned on with a ramp-up process.

After power is applied, the device enters the shutdown state. See *Initial Programming*. A rising edge on DATA (pin 7) initiates the warm-up of the XO and PLL. After PLL is locked, a falling edge on DATA enables the transmitter. The device returns to shutdown state when there is no DATA activity, i.e. DATA stays at 0 for 4096 cycles of the internal 3.2MHz clock.

In the I2C programming mode, the device has four major states: shutdown, programming, transmitter-enabled, and standby.

- Shutdown state: The crystal oscillator (XO), the PLL synthesizer, and the power amplifier (PA) are all turned off.
- Programming state: XO and PLL are turned on; PA is turned off.
- Standby state: XO is turned on; PLL and PA are turned off.
- Transmitter-enabled state: XO and PLL are turned on; PA is turned on with a ramp-up process.

A wakeup byte with 7-bit device address from the I2C bus initiates the warm-up of the XO and PLL.

The device can support two types of I2C transactions: register access only, and register access followed by data transmission. The event trigger of data transmission is a rising edge on I2C_TXEN, which is a special signal with two register-bit aliases I2C_TXEN1 (register CFG6, 0x0A, bit 2) and I2C_TXEN2 (register CFG7, 0x10, bit 2). A rising edge on I2C_TXEN can be generated by clearing I2C_TXEN1 and setting I2C_TXEN2 in a single I2C transaction.

I2C_TXEN is automatically cleared in two cases: 1) wake-up from shutdown, 2) return to programming state from the transmitter-enabled state. In those two cases, a rising edge on I2C_TXEN can be generated by setting I2C_TXEN2 in CFG7, without explicit clearing of I2C_TXEN1.

Data to be transmitted are written into a special register, byte I2C_TX_DATA[7:0] (register I2C3, 0x13, bits 7:0). Automatic incrementing of addresses in I2C burst-write are disabled for this special register. Each data byte written into I2C_TX_DATA will be transferred into a FIFO buffer. The device has an internal 1-bit signal FIFO_STOP. At the end of data transmission, FIFO_STOP is set, and the device references the PWDN_MODE[1:0] (register CFG4, 0x03, bits 1:0) to enter shutdown, standby, or programming state.

In both standby and shutdown states, programming through the I2C interface is not allowed. The device will exit the standby or shutdown state once its 7-bit I2C address is received.

Initial Programming

After turning on power supply (or a soft reset), two I2C transactions are required to initialize the PLL frequency synthesizer. The first transaction ensures register ADDL2 at address 0x1A is written to its default of 0x80. The second transaction burst-writes 20 consecutive registers from address 0x00 to 0x13.

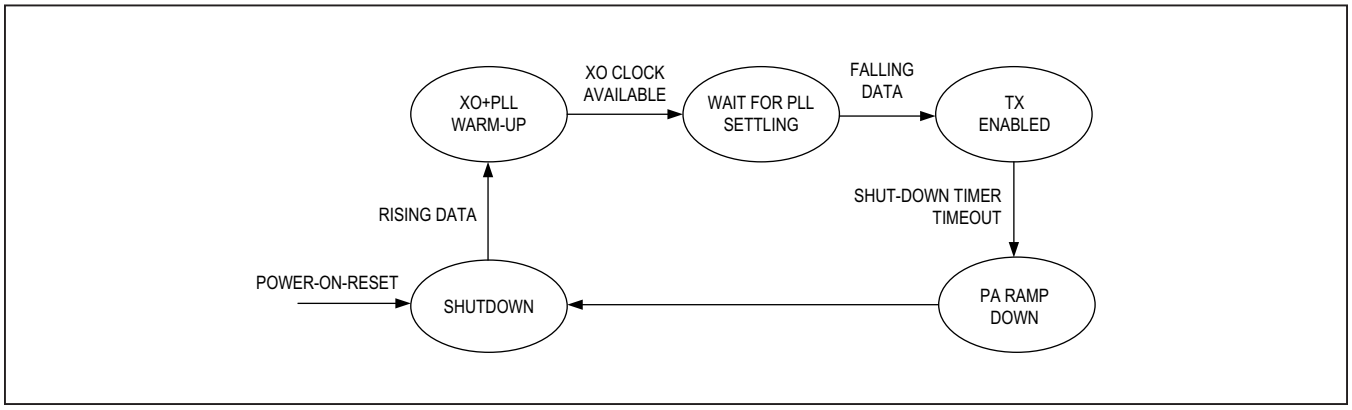


Figure 7. State Diagram in Preset Mode

The device needs to transmit an 8-bit dummy packet for initial programming. The initial programming must clear MODMODE (register CFG1, address 0x00, bit 0), clear I2C_TXEN1 (register CFG6, address 0x0A, bit 2), configure FREQ[23:0] (register PLL3, PLL4 and PLL5) to desired frequency, set I2C_TXEN2 (register CFG7, address 0x10, bit 2), and configure I2C_TX_DATA[7:0] (register I2C3, address 0x13) to 0x00. In addition, BCLK_POSTDIV[2:0], BCLK_PREDIV[7:0], and PKTLEN_MODE should be configured to default values in the register map.

Initial programming cannot be completed by a single burst-write transaction because the I2C_TX_DATA register at address 0x13 is a special register that disables automatic address increment. However, two I2C transactions may be merged to a combined transaction, where each write begins with a START mark and the slave address.

After initial programming, the device will enter the shutdown, standby, or programming state according to the setting of PWDN_MODE[1:0] (register CFG4, address 0x03, bit[1:0]). Configuration register values are retained unless changed by programming.

Startup

Programming Mode

This section assumes that initial programming is done after power on (or soft reset). Until the next time of power off/on (or soft reset), configuration registers are retained unless changed by programming.

Case 1: Using Two I2C Transactions for Startup from Shutdown

The startup of MAX41463/MAX41464 in programming mode, from the shutdown state, uses two I2C transactions: one for configuration update and the other for data transmission. FSK modulation can only be enabled through configuration update because the initial programming must clear MODMODE (register CFG1, address 0x00, bit 0).

In the first I2C transaction, the master device burst-writes consecutive registers that are a portion or all of the 16 registers from address 0x00 to 0x0F. Those consecutive registers may or may not include CFG6. If CFG6 is included, the I2C_TXEN1 bit should be cleared; otherwise, I2C_TXEN1 is automatically cleared in the wake-up from shutdown.

In the second I2C transaction, the master device can set I2C_TXEN2 (register CFG7, address 0x10, bit 2), configure PKTLEN_MODE (register I2C1, address 0x11, bit 7) and PKTLEN[14:0], and write the data to be transmitted into I2C_TX_DATA (register I2C3, address 0x13). Automatic increment of register address during burst write is disabled at address 0x13.

The event-trigger for wake-up is the recognition of I2C address of the device. The event trigger for data transmission is the rising edge I2C_TXEN that has two aliases of I2C_TXEN1 and I2C_TXEN2. The time lag between those two triggers must be longer than $t_{XO}+t_{PLL}$. To meet this requirement, the master device can adjust the wait time between the two I2C transactions.

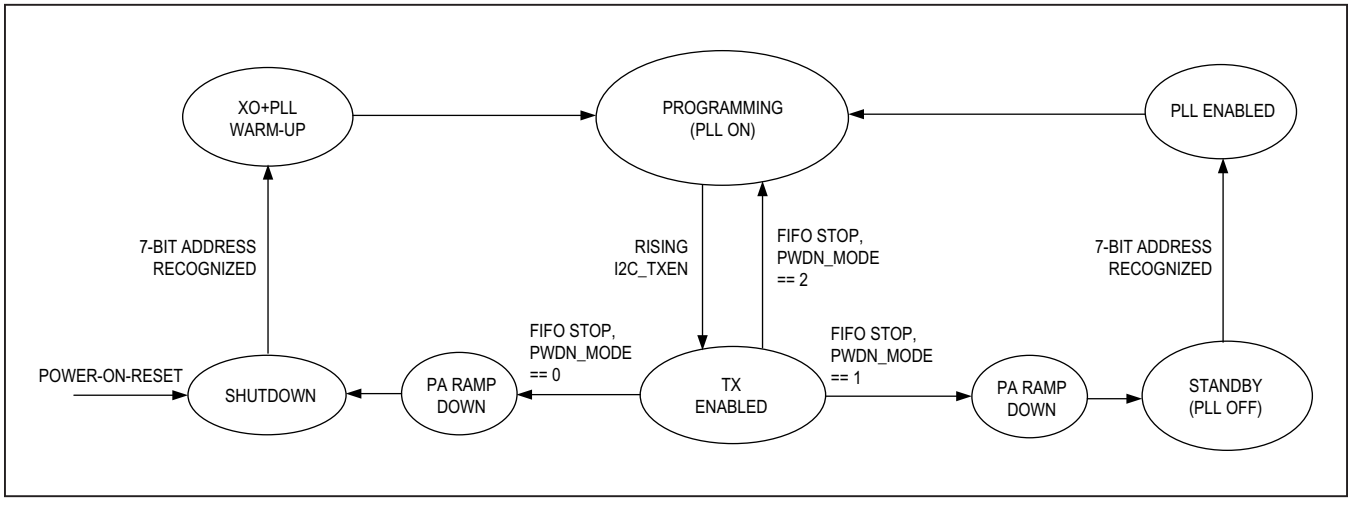


Figure 8. Simplified State Diagram in Programming Mode

Case 2: Using a Single I2C Transaction for Startup from Shutdown (Recommended for Use with I2C Fast Mode)

From shutdown state, the start up of device in programming mode may use a single I2C transaction to burst-write consecutive registers starting from address 0x00. Data to be transmitted are written into I2C_TX_DATA (register I2C3, address 0x13). Automatic incrementing of register addresses during burst-write is disabled at address 0x13. The programming should clear I2C_TXEN1 and set I2C_TXEN2.

The event-trigger for wake-up is the recognition of I2C address of the device. The event-trigger for data transmission is the rising edge of I2C_TXEN that two aliases of I2C_TXEN1 and I2C_TXEN2. The time lag between those two triggers, here 162 cycles of SCL, must be longer than $t_{XO}+t_{PLL}$. To meet this requirement, the fast mode I2C speed with 400kHz SCL is recommended.

Case 3: Using a Combined I2C Transactions for Startup from Shutdown (Recommended for Most I2C Clock Rates)

From shutdown state, the start up of MAX41463/MAX41464 in programming mode can use a combined I2C transaction with repeated START marks. In a combined transaction, the master device can do multiple read/write operations without losing control to other master devices on the I2C bus. For example, the combined transaction can have a burst-read operation followed by a burst-write operation.

In the burst-write operation, the master device should write consecutive registers starting from CFG7 (address 0x10) or any register preceding CFG7. Data to be transmitted are written into I2C_TX_DATA (register I2C3, address 0x13). Automatic incrementing of register addressed during burst-write is disabled at address 0x13. The programming should set I2C_TXEN2 (and clear I2C_TXEN1 if CFG6 is included in the registers to write).

The event-trigger for wake-up is the recognition of device address in the burst-read operation. The event-trigger for data transmission is the rising edge of I2C_TXEN that has two aliases of I2C_TXEN1 and I2C_TXEN2. The time lag between those two triggers must be longer than $t_{XO}+t_{PLL}$. To meet this requirement, the master device can adjust the number of registers to read in the burst-read operation.

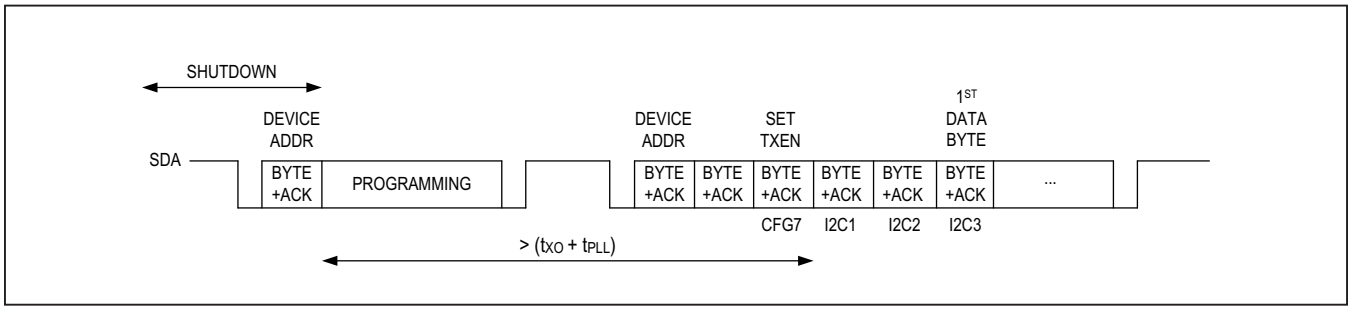


Figure 9. Using two I2C transactions to start data transmission from the shutdown state.

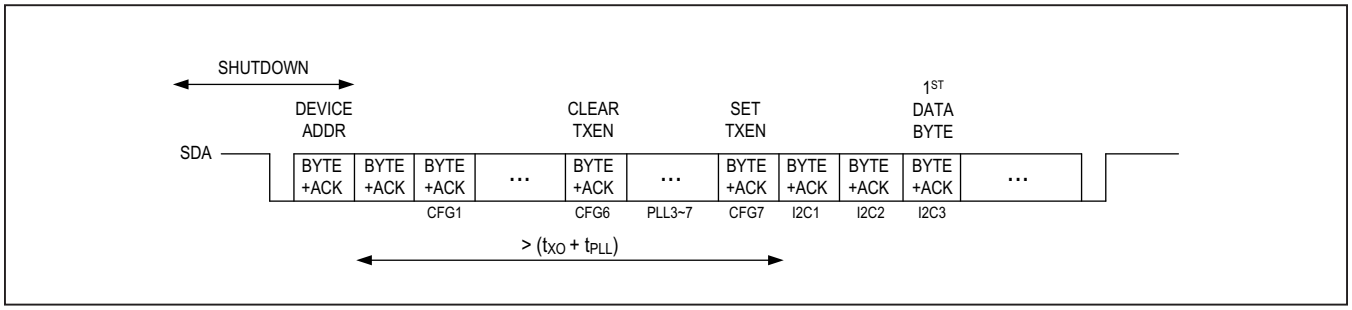


Figure 10. Using a single I2C transaction to start data transmission from the shutdown state.

Case 4: Using a Single I2C Transaction for Startup from Standby (recommended for use with I2C Fast-mode and I2C Fast-mode Plus)

From standby state, the start-up of MAX41463/MAX41464 in programming mode can use a single I2C transaction to burst-write consecutive registers starting from CFG6 (address 0x0A) or any register preceding CFG6. Data to be transmitted are written into I2C_TX_DATA (register I2C3, address 0x13). Automatic incrementing of register addresses during burst-write is disabled at address 0x13. The programming should clear I2C_TXEN1 and set I2C_TXEN2.

The event-trigger for wake-up is the recognition of I2C address of the device. The event-trigger for data transmission is the rising edge of I2C_TXEN that two aliases of I2C_TXEN1 and I2C_TXEN2. The time lag between those two triggers, here ≥ 72 cycles of SCL, must be longer than t_{PLL} for startup from standby. This requirement is met for the fast-mode I2C with 400kHz SCL. In the case of Fast-mode Plus, I2C with 1MHz SCL, the master device can burst-write registers starting from PLL1.

Case 5: Using a Single I2C Transaction for Startup from Programming Mode

The MAX41463/MAX41464 device can transmit a data packet each time in the transmitter-enabled state. After data transmission, the device refers to the setting of PWDN_MODE[1:0] to enter the shutdown, standby, or programming state. If the next data packet requires fast start-up, PWDN_MODE[1:0] can be configured to 2 so that the device returns to the programming state.

Then, the master device can use a single I2C transaction to burst-write consecutive registers starting from CFG7 (address 0x10) or any register preceding CFG7. Data to be transmitted are written into I2C_TX_DATA (register I2C3, address 0x13). Automatic incrementing of register addresses during burst-write is disabled at address 0x13. The programming should set I2C_TXEN2 (and clear I2C_TXEN1 if CFG6 is included in the registers to write). There is no restrictions arising from t_{XO} and t_{PLL}.

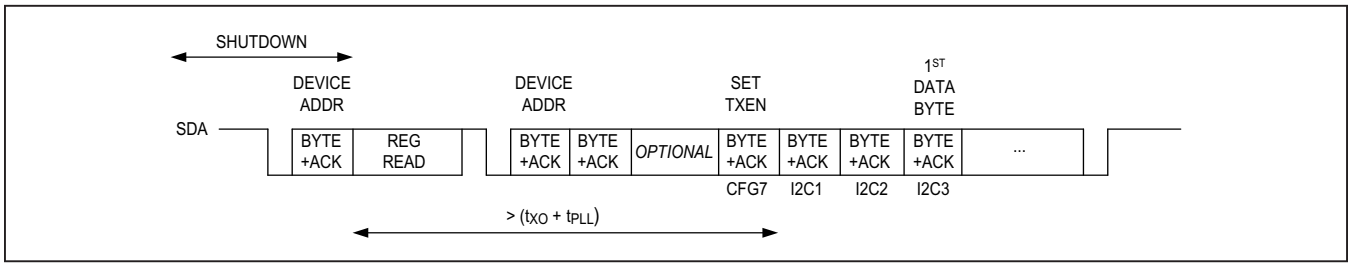


Figure 11. Using a Combined I2C Transaction to Start Data Transmission from the Shutdown State.

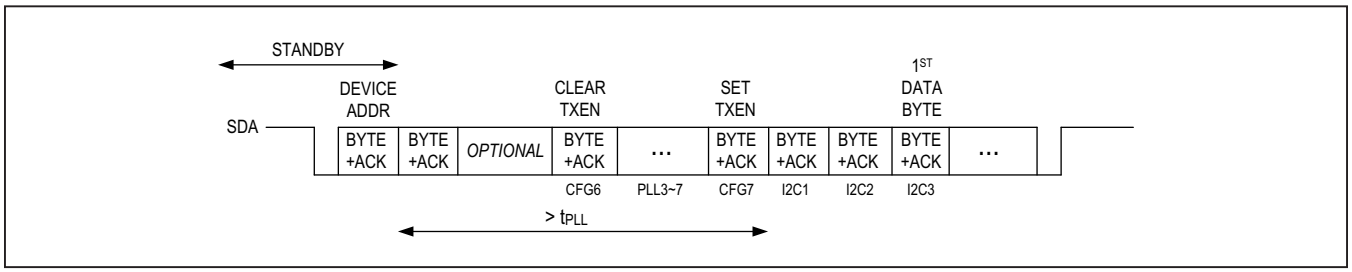


Figure 12. Using a Single I2C Transaction to Start Data Transmission from the Standby State.

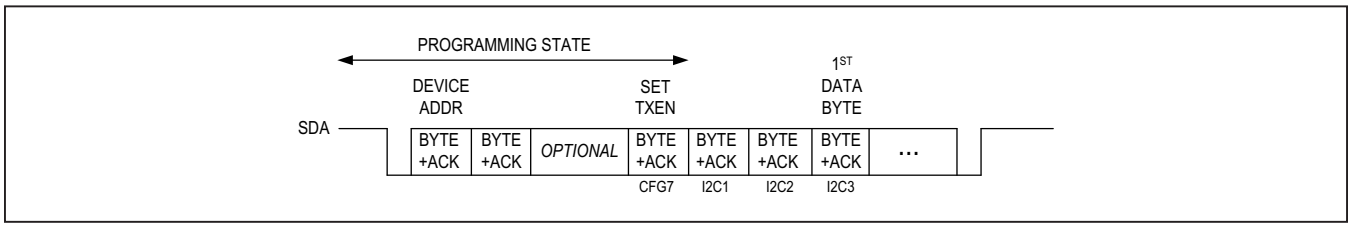


Figure 13. Using a Single I2C Transaction to Start Data Transmission from the Programming State.

FIFO Buffer

The I2C interface is a bus connected to multiple master or slave devices. The microcontroller is a master device and the MAX41463/MAX41464 is a slave device. The microcontroller can initiate communication with the slave device by I2C addressing (e.g., sending a START mark followed by 7-bit device address). The slave device is required to acknowledge every byte transferred through I2C.

For data transmission, the microcontroller can burst-write consecutive registers, including CFG7 and I2C3. The purpose of writing CFG7 is to set I2C_TXEN2 and, therefore, generate a trigger to enable the transmitter. Automatic increment of register address in I2C burst-write is disabled for the I2C3 register, which is also named I2C_TX_DATA. Once the transmitter is enabled, all bytes written to I2C_TX_DATA are moved into a FIFO buffer. The buffer size is 4 bytes. The FIFO buffer is enabled only in the transmitter-enabled state.

A programmable baud-rate clock is used for retrieving and transmitting bits from the FIFO buffer. The baud rate is programmable by BCLK_PREDIV[7:0] (register CFG3, 0x02, bits 7:0) and BCLK_POSTDIV[2:0] (register CFG2, 0x01, bits 2:0) as the following expression:

$$BaudRate = \frac{f_{CLK}}{2 \times (1 + BCLK\_PREDIV) \times 2^{BCLK\_POSTDIV}}$$

where f_{CLK} is the crystal-divider output clock rate (nominally, 3.2 MHz). Valid values of BCLK_PREDIV are from 3 to 255. Valid values of BCLK_POSTDIV are from 1 to 5.

To avoid underflow of the FIFO buffer, the baud-rate must be lower than 8/9 of the SCL clock rate. The device can support three modes of SCL clock frequencies: 100kHz, 400kHz, and 1MHz. In the 100kHz mode, it is recommended to limit baud-rate to no more than 50kbps.

A FIFO overflow is avoided by utilizing the I2C clock stretching mechanism. Clock stretching is done before the ACK bit. There is no clock-stretching timeout.

Each time before data transmission, the I2C1 and I2C2 registers are configured to specify PKTLEN_MODE and PKTLEN[14:0]. Data transmission stops when PKTLEN_MODE is set and the number of bauds transmitted is equal to PKTLEN[14:0]. Data transmission also stops at FIFO underflow or overflow. An internal 1-bit flag FIFO_STOP is set at the end of data transmission. The rising edge of FIFO_STOP serves as the event trigger to disable the transmitter. See the *State Diagrams* section.

When the number of bauds to be transmitted is known before data transmission and less than 32768, it is recommended to set PKTLEN_MODE and configure PKTLEN[14:0] as the number of bauds to be transmitted. Otherwise, clear PKTLEN_MODE and utilize FIFO underflow to stop data transmission. Once the microcontroller stops writing I2C_TX_DATA, FIFO underflow will occur after the data stored in FIFO buffer are transmitted.

Read-only register I2C4, I2C5, and I2C6 are provided to report diagnostic information for the FIFO buffer.

Frequency Hopping

In programming mode, the frequency synthesizer is initialized to a frequency in a selected ISM band by *Initial Programming*. After that, for the purpose of frequency dithering or frequency hopping, the FREQ[23:0] registers can be updated to a new frequency in the same selected band for each data packet to be transmitted.

Because programming is not allowed in the transmitted-enabled state (see the *State Diagrams* section), frequency configuration cannot be changed when PA is enabled. See the *Startup* section for details on how to program the device for data transmission.

After transmitting a data packet, the device enters the shutdown, standby, or programming states according to the setting of PWDN_MODE[1:0] register. The three options have different startup times for transmitting the next data packet.

The startup time from shutdown is at least (t_{XO} + t_{PLL} + t_{TX}), where t_{XO} is the turn-on time of crystal oscillator, t_{PLL} is the turn-on time of PLL, t_{TX} is the turn-on time of transmitter.

The startup time from standby is at least (t_{PLL} + t_{TX}).

The t_{TX} time is 27 cycles of the SCL clock plus 2 cycles of the baud-rate clock. For example, the SCL clock rate is 1MHz, the baud rate is 100kbps, the value of t_{TX} is 47µs. Refer to the *Electrical Characteristics* for typical values of t_{XO} and t_{PLL}.

Register Map

ADDRESS	NAME	MSB							LSB
TX									
0x00	CFG1[7:0]	XOCLKDELAY[1:0]		XOCLKDIV[1:0]		–	FSK-SHAPE	SYNC	MODMODE
0x01	CFG2[7:0]	CLKOUT_DELAY[1:0]		–	–	–	BCLK_POSTDIV[2:0]		
0x02	CFG3[7:0]	BCLK_PREDIV[7:0]							
0x03	CFG4[7:0]	–	–	–	–	–	–	PWDN_MODE[1:0]	
0x04	CFG5[7:0]	–	–	TSTEP[5:0]					
0x05	SHDN[7:0]	–	–	–	–	–	RE-SERVED	RE-SERVED	PA_BOOST
0x06	PA1[7:0]	RESERVED[2:0]			–	–	PAPWR[2:0]		
0x07	PA2[7:0]	–	–	–	PACAP[4:0]				
0x08	PLL1[7:0]	CPLIN[1:0]		FRAC-MODE	RESERVED[1:0]		LODIV[1:0]		LOMODE
0x09	PLL2[7:0]	RE-SERVED	RE-SERVED	–	–	–	–	CPVAL[1:0]	
0x0A	CFG6[7:0]	–	–	–	–	–	I2C_TXEN1	RE-SERVED	RESERVED
0x0B	PLL3[7:0]	FREQ[23:16]							
0x0C	PLL4[7:0]	FREQ[15:8]							
0x0D	PLL5[7:0]	FREQ[7:0]							
0x0E	PLL6[7:0]	–	DELTAF[6:0]						
0x0F	PLL7[7:0]	–	–	–	–	DELTAF_SHAPE[3:0]			
0x10	CFG7[7:0]	–	–	–	–	–	I2C_TXEN2	RE-SERVED	RESERVED
0x11	I2C1[7:0]	PK-TLEN_MODE	PKTLEN[14:8]						
0x12	I2C2[7:0]	PKTLEN[7:0]							
0x13	I2C3[7:0]	I2C_TX_DATA[7:0]							
0x14	I2C4[7:0]	PKT-COM-PLETE	TX_PKTLEN[14:8]						
0x15	I2C5[7:0]	TX_PKTLEN[7:0]							
0x16	I2C6[7:0]	UFLOW	OFLOW	FIFO_EMPTY	FIFO_FULL	–	FIFO_WORDS[2:0]		
0x17	CFG8[7:0]	–	–	–	–	–	–	–	SOFTRESET
0x18	CFG9[7:0]	RESERVED[4:0]					RE-SERVED	RE-SERVED	RESERVED
0x19	ADDL1[7:0]	RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]	
0x1A	ADDL2[7:0]	RE-SERVED	RESERVED[6:0]						

Register Details

CFG1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	XOCLKDELAY[1:0]		XOCLKDIV[1:0]		–	FSKSHAPE	SYNC	MODMODE
Reset	0x2		0x1		–	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
XOCLK DELAY	7:6	Start delay before enabling XO clock to digital block	0x0: No delay. XO clock is immediately enabled to rest of digital block 0x1: XO clock is enabled after 16 cycles to rest of digital block 0x2: XO clock is enabled after 32 cycles to rest of digital block 0x3: XO clock is enabled after 64 cycles to rest of digital block
XOCLKDIV	5:4	XO clock division ratio for digital block	0x0: Divide XO clock by 4 for digital clock 0x1: Divide XO clock by 5 for digital clock. High time is 2 cycles, low time is 3 cycles 0x2: Divide XO clock by 6 for digital clock. 0x3: Divide XO clock by 7 for digital clock. High time is 3 cycles, and low time is 4 cycles.
FSKSHAPE	2	Sets the state of FSK Gaussain Shaping	0x0: FSK Shaping disabled 0x1: FSK Shaping enabled
SYNC	1	Controls if clock output acts as an input. When an input, it will sample the DATA pin.	0x0 0x1
MODMODE	0	Configures modulator mode	0x0: ASK Mode 0x1: FSK Mode

CFG2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	CLKOUT_DELAY[1:0]		–	–	–	BCLK_POSTDIV[2:0]		
Reset	0x2		–	–	–	0x1		
Access Type	Write, Read		–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CLKOUT_ DELAY	7:6	Selects the delay when CLKOUT starts toggling upon exiting SHUTDOWN mode, in divided XO clock cycles	0x0: CLKOUT will start toggling after 64 cycles whenever moving into normal mode from shutdown mode 0x1: CLKOUT will start toggling after 128 cycles whenever moving into normal mode from shutdown mode 0x2: CLKOUT will start toggling after 256 cycles whenever moving into normal mode from shutdown mode 0x3: CLKOUT will start toggling after 512 cycles whenever moving into normal mode from shutdown mode
BCLK_ POSTDIV	2:0	Baud clock post-divider setting.	0x0: RESERVED 0x1: Divide by 1 0x2: Divide by 2 0x3: Divide by 3 0x4: Divide by 4 0x5: Divide by 5 0x6: RESERVED 0x7: RESERVED

CFG3 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	BCLK_PREDIV[7:0]							
Reset	0x3							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
BCLK_ REDIV	7:0	Baud clock predivision ratio. Valid values are from 3 to 255.	0x00: RESERVED 0x01: RESERVED 0x02: RESERVED 0x03: Divide by 3 ... 0xFF: Divide by 255

CFG4 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PWDN_MODE[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PWDN_ MODE	1:0	Power Down Mode Select	0x0: SHUTDOWN low power state is enabled. While entering low power state, XO, PLL, and PA are shutdown. 0x1: STANDBY low power state is enabled. While entering low power state, XO is enabled. PLL and PA are shutdown 0x2: FAST WAKEUP low power state is enabled. While entering low power state, XO and PLL are enabled. PA is shutdown. 0x3: Will revert to 0x2

CFG5 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	TSTEP[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
TSTEP	5:0	Controls GFSK shaping. See *Digital FSK Modulation* section.

SHDN (0x05)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RESERVED	RESERVED	PA_BOOST
Reset	–	–	–	–	–	0x1	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	2	Write to 1 binary.	1
RESERVED	1	Write to 0 binary.	0
PA_BOOST	0	Enables a boost in PA output power for frequencies above 850MHz. This requires a different PA match compared to normal operation.	0x0: PA Output power in normal operation. 0x1: PA Output power in boost mode for more output power.

PA1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			–	–	PAPWR[2:0]		
Reset	0x4			–	–	0x0		
Access Type	Write, Read			–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:5	Write to 100 binary.	100
PAPWR	2:0	Controls the PA output power by enabling parallel drivers.	0x0: Minimum, 1 driver 0x1: 2 Drivers 0x2: 3 Drivers 0x3: 4 Drivers 0x4: 5 Drivers 0x5: 6 Drivers 0x6: 7 Drivers 0x7: 8 Drivers

PA2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PACAP[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PACAP	4:0	Controls shunt capacitance on PA output in fF.	0x00: 0 0x01: 175 0x02: 350 0x03: 525 0x04: 700 0x05: 875 0x06: 1050 0x07: 1225 0x08: 1400 0x09: 1575 0x0A: 1750 0x0B: 1925 0x0C: 2100 0x0D: 2275 0x0E: 2450 0x0F: 2625 0x10: 2800 0x11: 2975 0x12: 3150 0x13: 3325 0x14: 3500 0x15: 3675 0x16: 3850 0x17: 4025 0x18: 4200 0x19: 4375 0x1A: 4550 0x1B: 4725 0x1C: 4900 0x1D: 5075 0x1E: 5250 0x1F: 5425

PLL1 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	CPLIN[1:0]		FRAC-MODE	RESERVED[1:0]		LODIV[1:0]		LOMODE
Reset	0x1		0x1	0x00		0x0		0b0
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CPLIN	7:6	Sets the level of charge pump offset current for fractional N mode to improve close in phase noise. Set to 'DISABLED' for integer N mode.	0x0: No extra current 0x1: 5% of charge pump current 0x2: 10% of charge pump current 0x3: 15% of charge pump current
FRACMODE	5	Sets PLL between fractional-N and integer-N mode.	0x0: Integer N Mode 0x1: Fractional N Mode
RESERVED	4:3	Write to 00 binary.	00
LODIV	2:1		0x0: Disabled 0x1: LC VCO divided by 4 0x2: LC VCO divided by 8 0x3: LC VCO divided by 12
LOMODE	0	Sets LO generation. For lower power, choose LOWCURRENT. For higher performance, choose LOWNOISE.	0x0: Ring Oscillator Mode 0x1: LC VCO Mode

PLL2 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED	–	–	–	–	CPVAL[1:0]	
Reset	0x0	0b0	–	–	–	–	0x0	
Access Type	Write, Read	Write, Read	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Write to 0 binary.	0
RESERVED	6	Write to 0 binary.	0
CPVAL	1:0	Sets Charge Pump Current	0x0: 5µA 0x1: 10µA 0x2: 15µA 0x3: 20µA

CFG6 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	I2C_TXEN1	RESERVED	RESERVED
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TXEN1	2	Enables DATA transmission in I2C mode. Aliased address for I2C_TXEN1.	0x0: Data transmission not enabled in I2C mode. 0x1: Data transmission enabled in I2C mode.
RESERVED	1	Write to 0 binary.	
RESERVED	0	Write to 0 binary.	

PLL3 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	FREQ[23:16]							
Reset	0x13							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FREQ	7:0	FREQ value to PLL. LO frequency= FREQ<23:0>/2^16*fXTAL

PLL4 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	FREQ[15:8]							
Reset	0xB0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FREQ	7:0	FREQ value to PLL

PLL5 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	FREQ[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FREQ	7:0	FREQ value to PLL

PLL6 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	–	DELTAF[6:0]						
Reset	–	0x28						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
DELTAF	6:0	For FSK mode, MODMODE = 1 and FSKSHAPE = 0, sets the frequency deviation from the space frequency for the mark frequency. f_{DELTA} = DELTAF[6:0] * f_{XTAL}/8192

PLL7 (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DELTAF_SHAPE[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DELTAF_SHAPE	3:0	For FSK mode, MODMODE = 1 and FSKSHAPE = 1, sets the frequency deviation from the space frequency for the mark frequency. f_{DELTA} = DELTAF_SHAPE[3:0] * f_{XTAL}/81920

CFG7 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	I2C_TXEN2	RESERVED	RESERVED
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TXEN2	2	Enables DATA transmission in I2C mode. Aliased address for I2C_TXEN1.	0x0: Data transmission not enabled in I2C mode. 0x1: Data transmission enabled in I2C mode.
RESERVED	1	RESERVED	0
Write to 0 binary.			

I2C1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	PKTLEN_ MODE	PKTLEN[14:8]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
PKTLEN_ MODE	7	Packet Length Mode	0x0: PKTLEN[14:0] need not be programmed. FIFO underflow event will be treated as end of packet event. For cases where actual packet length is greater than 32767 bits, it is expected that the µC will pad such a packet to make it an integral multiple of 8-bits 0x1: PKTLEN[14:0] will provide the length of packet. Once FIFO is read for PKTLEN[14:0] bits, or if FIFO underflow, MAX41463/MAX41464 will consider that as an end of packet event.
PKTLEN	6:0	Packet Length	

I2C2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	PKTLEN[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PKTLEN	7:0	Packet Length

I2C3 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	I2C_TX_DATA[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
I2C_TX_DATA	7:0	Transmit data to be written into FIFO for I2C mode of operation. At this address, I2C register address will not auto increment within an I2C transaction burst, and subsequent writes will keep going to FIFO

I2C4 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	PKTCOM-PLETE	TX_PKTLEN[14:8]						
Reset	0x0	0x0						
Access Type	Read Only	Read Only						

BITFIELD	BITS	DESCRIPTION	DECODE
PKTCOM-PLETE	7	Indicates if Packet tranmission is completed	0x0: Packet transmission is not completed 0x1: Packet transmission is completed
TX_PKTLEN	6:0	Provides status information of bits transmitted for the current packet	

I2C5 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	TX_PKTLEN[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TX_PKTLEN	7:0	Provides status information of bits transmitted for the current packet

I2C6 (0x16)

BIT	7	6	5	4	3	2	1	0
Field	UFLOW	OFLOW	FIFO_EMP-TY	FIFO_FULL	–	FIFO_WORDS[2:0]		
Reset	0x0	0x0	0x1	0x0	–	0x0		
Access Type	Read Only	Read Only	Read Only	Read Only	–	Read Only		

BITFIELD	BITS	DESCRIPTION
UFLOW	7	FIFO Underflow status
OFLOW	6	FIFO Overflow status
FIFO_EMPTY	5	FIFO Empty Status
FIFO_FULL	4	FIFO Full Status
FIFO_WORDS	2:0	This field captures the number of locations currently filled in FIFO. Each location corresponds to 8-bit data word

CFG8 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SOFTRE-SET
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SOFTRESET	0	Places DUT into software reset.	0x0: Deassert the reset 0x1: Resets the entire digital, until this bit is set to 0

CFG9 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					RESERVED	RESERVED	RESERVED
Reset	0x0					0x0	0x0	0x0
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:3	Write to 0_0000 binary.	00000
RESERVED	2	Write to 0 binary.	0
RESERVED	1	Write to 0 binary.	0
RESERVED	0	Write to 0 binary.	0

ADDL1 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]		RESERVED[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Write to 00 binary.	00
RESERVED	5:4	Write to 00 binary.	00
RESERVED	3:2	Write to 00 binary.	00
RESERVED	1:0	Write to 00 binary.	00

ADDL2 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED[6:0]						
Reset	0x1	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Write to 1 binary.	1
RESERVED	6:0	Write to 000_0000 binary.	0000000

Applications Information

Power-On Programming

Preset Mode

To ensure the MAX41463/MAX41464 device enters shutdown state after power-on, the DATA pin must be held low at power-on. If the DATA pin cannot be guaranteed low at power-on, then a high value pulldown resistor is recommended. After V_{DD} has settled, a logic low-high-low transition on DATA must occur in the preset mode. If the pulse duration of low-high-low transition is longer than t_{XO} + t_{PLL}, it is a valid wake-up pulse before data transmission. It is also allowed to have a short pulse duration between 5µs and 20µs. The short pulse will not wake up the device.

Programming Mode

After turning on power supply in I2C mode, a logic-high-low-high transition on SDA must occur to minimize leakage current in shutdown state. It is highly recommended that the I2C resistors are connected to the MAX41463/MAX41464 VDD.

Two I2C transactions are required to initialize the PLL frequency synthesizer. The first transaction ensures register ADDL2 at address 0x1A is written to its default of 0x80. The second transaction burst-writes 20 consecutive registers from address 0x00 to 0x13. The device is programmed to transmit a dummy packet with 8 zero bits in ASK mode. There is no RF emission at PA output. See *Initial Programming* section.

For example, the crystal frequency is 16MHz, the RF frequency is 315MHz, the 20 consecutive registers from address 0x00 to 0x13 can be configured as:

[0x90, 0x81, 0x03, 0x00, 0x00, 0x04, 0x80, 0x80, 0x60, 0x00, 0x00, 0xC4, 0xDE, 0x98, 0x28, 0x04, 0x04, 0x00, 0xFF, 0x00]

After initial programming, the device will enter the shutdown, standby, or programming state according to the setting of PWDN_MODE[1:0] (register CFG4, address 0x03, bit[1:0]). Configuration register values are retained unless changed by programming or if the device is powered off or undergoes a SOFTRESET. See the *Startup* section for how to program the device for data transmission.

Digital FSK Modulation

The FSK modulation in MAX41463/MAX41464 is defined by the space frequency and the mark frequency. The space frequency is the lower frequency that represents a logic 0. The mark frequency is the higher frequency that represents a logic 1. The device defaults to Gaussian filtered frequency shaping to help reduce spectral emissions.

The space frequency is defined by the FREQ[23:0] bits (registers PLL3, PLL4, PLL5). To set the space frequency, use the following equation:

$$FREQ[23:0] = \frac{65536 * f_{SPACE}}{f_{XTAL}}$$

The mark frequency is defined by the space frequency plus a frequency deviation. If frequency shaping is disabled by setting FSKSHAPE = 0 (register CFG1, bit 2), the frequency deviation is defined by DELTAF[6:0] (register PLL6, bits 6:0).

$$DELTAF[6:0] = \frac{f_{\Delta} * 8192}{f_{XTAL}}$$

If frequency shaping is enabled by setting FSKSHAPE = 1 (register CFG1, bit 2), the frequency deviation is defined by DETLAF_SHAPE[3:0] (register PLL7, bits 3:0).

$$DELTAF\_SHAPE[3:0] = \frac{f_{\Delta} * 8192}{f_{XTAL} * 10}$$

When FSK shaping is enabled by setting FSKSHAPE = 1, the frequency is transitioned in 16 steps between the two frequencies using a Gaussian filter shape. The time between each step is controlled by TSTEP[5:0] (register CFG5, bits 5:0). The time step can be adjusted based on the data rate.

$$TSTEP[5:0] = minimum\left(64, floor\left(\frac{200000}{f_{DATA\_RATE}}\right)\right) - 1$$

where $f_{DATARATE}$ has a unit of bits per second. For example, if $f_{DATARATE}$ is 47kbps, then TSTEP is floor(200000/47000) -1 = 3.

In the preset mode, the frequency deviation is fixed at 78kHz.and TSTEP = 1.

FSK shaping supports a data rate up to 110kbps. Higher data rates is not recommended.

Tuning Capacitor Settings

The internal variable shunt capacitor, which can be used to match the PA to the antenna with changing transmitter frequency, is controlled by setting the 5-bit cap variable in the registers. This allows for 32 levels of shunt capacitance control. Since the control of these 5 bits is independent of the other settings, any capacitance value can be chosen at any frequency, making it possible to maintain maximum transmitter efficiency while moving rapidly from one frequency to another. The internal tuning capacitor adds 0 to 5.425pF to the PA output in 0.175pF steps.

Crystal Frequency Selection

In order to avoid integer boundary spurs in fractional-N PLL synthesizers, the crystal should be selected so that the RF carrier frequency is more than 0.4MHz apart from the nearest integer multiple of crystal frequency.

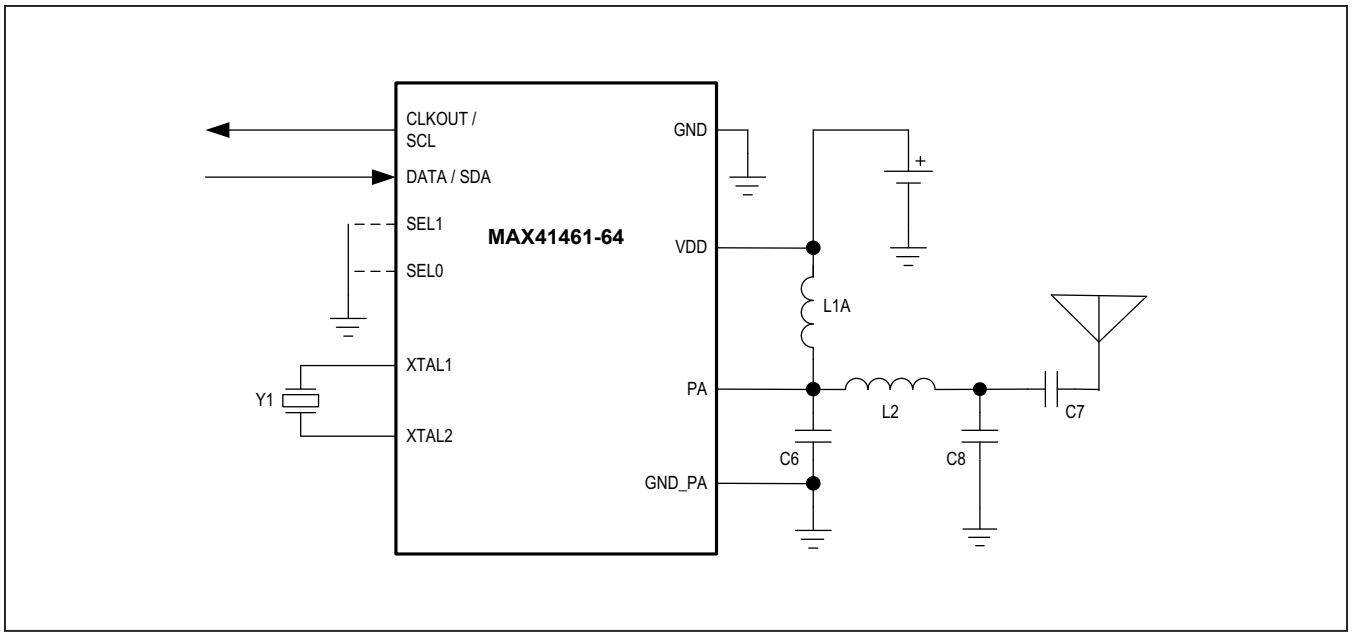
For example, the 16±0.002MHz crystals can be selected for the 433.92MHz RF carrier, which is more than 0.4MHz apart from the nearest integer multiple of crystal frequency at 432±0.054MHz. However, the 16±0.002MHz crystals are not suitable for a RF carrier at 912MHz or 928MHz.

In the programming mode, the crystal divider ratio is programmable. The crystal divider ratio should be configured so that the divided clock frequency is 3.2±0.1MHz. In addition, the PLL synthesizer requires a reference frequency (same as crystal frequency) between 12.8MHz and 19.2MHz. Therefore, when crystal divider ratio is 4, 5, or 6, allowed range of crystal frequency is 12.8MHz~13.2MHz, 15.5MHz~16.5MHz, or 18.6MHz~19.2MHz.

In another example, desired RF frequencies are 319.5MHz, 345.0MHz, and 433.92MHz, and recommended crystal selection is 13±0.002MHz so that integer boundary spurs are completely suppressed for three desired RF frequencies. Nevertheless, the 16±0.002MHz and 19.2±0.002MHz crystals are also acceptable.

In the preset mode, the crystal divider ratio is preset at 5. When the RF carrier frequency is very close to an integer multiple of 16MHz, the crystal selection can change to 16.384MHz or 16.128MHz, and the RF carrier frequency should be preset through OTP memory in production.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX41463GUB+	-40°C to +105°C	TSSOP-10
MAX41463GUB+T	-40°C to +105°C	TSSOP-10
MAX41464GUB+	-40°C to +105°C	TSSOP-10
MAX41464GUB+T	-40°C to +105°C	TSSOP-10

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	11/18	Updated *Ordering Information*	38

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