# MAX41470

# 290MHz to 960MHz ASK/FSK Receiver with SPI Interface

## General Description

The MAX41470 is a high-performance, low-power receiver that is ideal for amplitude shift-keyed (ASK) and frequency shift-keyed (FSK) data. The receiver can be configured for three popular sub-1GHz bands while using a single low-cost 16MHz crystal: 287MHz to 320MHz, 425MHz to 480MHz, and 860MHz to 960MHz.

The MAX41470 is capable of both ASK and FSK reception and is also fully programmable through an SPI interface.

The receiver has excellent RF sensitivity and allows input signals up to 0dBm of power at the RF input. With an integrated IF filter, a few external components, and low operating/power-down currents, the MAX41470 receiver is ideal for cost- and power-sensitive applications. The chip also includes a low-noise amplifier (LNA), fully differential image-rejection mixer, on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO), received signal strength indicator (RSSI), and digital demodulation.

The device operates in the 1.8V to 3.6V supply voltage range and also features a power-saving, fully programmable, self-polling (duty cycling) mode with preamble detection and interrupt output to wake up an external microcontroller unit (MCU).

The parts are available in a 12-pin thin QFN (TQFN) package and are specified for the -40°C to +105°C extended temperature range.

## Applications

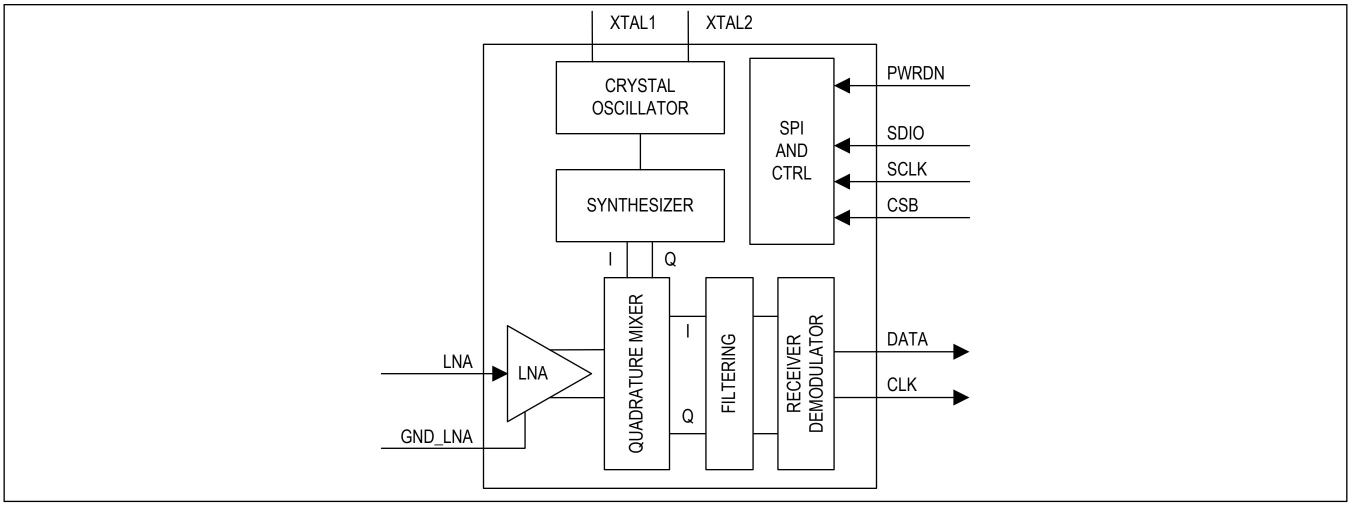
- Home Automation and Security
- Building Access Control
- Garage Door Openers (GDO)
- Remote Keyless Entry (RKE)
- Tire Pressure Monitoring Systems (TPMS)
- Restaurant Pagers

## Benefits and Features

- Low Bill of Materials (BOM)
  - No External Balun, No External Filter, etc.
  - Single Low-Cost 16MHz External Crystal
- Long Range with High Sensitivity
- Low Power Consumption
  - 9mA Operating Supply Current
  - 10nA Power-Down Current
- Self-Polling (Remote Wake-Up) for Reduced Power
  - Preamble Detection with Interrupt Output
  - Average Current as Low as 350µA
  - Duty Cycle Less Than 1% Capable
  - Fast Startup Time
- Automatic Gain Control (AGC) Adjusted Digital RSSI
- Automatic Frequency Control (AFC)
- Fast Frequency Switching Frac-N Synthesizer
- 33dB Calibrated Image Rejection
- Passes ETSI Category 2 Blocking Requirements
- ±2.5kV HBM ESD Protection, ±4kV on LNA Input
- Up to 200kbps Data Rate (NRZ)
- 1.8V to 3.6V Supply Voltage
- -40°C to +105°C Operating Temperature Range
- 4mm x 4mm, 12-TQFN with 0.8mm Pitch

***Ordering Information** appears at end of datasheet.*

## Simplified Block Diagram



## TABLE OF CONTENTS

## TABLE OF CONTENTS (CONTINUED)

## LIST OF FIGURES

## LIST OF TABLES

## Absolute Maximum Ratings

$V_{DD}$ to GND............................................................ -0.3V to +4V
GND_LNA to GND ................................................ -0.3V to 0.3V
All Other Pins to GND ...............................-0.3V to ($V_{DD}$ + 0.3)V
Continuous Power Dissipation (Single Layer Board) ($T_A$ = +70°C, derate 16.9mW/°C above +70°C.).............................. 1349.1mW
Continuous Power Dissipation (Multilayer Board) ($T_A$ = +70°C, derate 24.4mW/°C above +70°C) ...............................1951.2mW
Operating Temperature Range ..........................-40°C to +105°C
Junction Temperature .....................................................+150°C
Storage Temperature Range .............................-40°C to +150°C
Soldering Temperature (reflow) .......................................+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### 12 TQFN

| | |
|---|---|
| Package Code | T1244+4 |
| Outline Number | 21-0139 |
| Land Pattern Number | 90-0068 |
| **Thermal Resistance, Single-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 59.3°C/W |
| Junction to Case ($\theta_{JC}$) | 6°C/W |
| **Thermal Resistance, Four-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 41°C/W |
| Junction to Case ($\theta_{JC}$) | 6°C/W |

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

(*Typical Application Circuit*, typical values are at $V_{DD}$ = +3.0V, $T_A$ = +25°C, ASK at input frequency = 433.92MHz, Manchester encoded, IF = 400kHz, RXBW = 340kHz with 16MHz crystal oscillator, unless otherwise noted. (Note 1))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC SPECIFICATIONS** | | | | | | |
| Supply Voltage | $V_{DD}$ | | 1.8 | | 3.6 | V |
| Supply Current | $I_{VDD\_RCV}$ | | | 9 | 14 | mA |
| Shutdown Current | $I_{SHDN}$ | | | 10 | 1000 | nA |
| Standby Current | $I_{SDBY}$ | | | 320 | | µA |
| Sleep Current | $I_{DD\_SLEEP}$ | | | 1 | | µA |
| **AC SPECIFICATIONS** | | | | | | |
| Frequency Range | | | | 287 to 320,<br>425 to 480,<br>860 to 960 | | MHz |

## Electrical Characteristics (continued)

(*Typical Application Circuit*, typical values are at $V_{DD}$ = +3.0V, $T_A$ = +25°C, ASK at input frequency = 433.92MHz, Manchester encoded, IF = 400kHz, RXBW = 340kHz with 16MHz crystal oscillator, unless otherwise noted. (Note 1))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Maximum Receiver Input Level | $P_{RFIN\_MAX}$ | Modulation depth > 20dB | -20 | 0 | | dBm |
| Maximum Channel Bandwidth | | -3dB bandwidth at 400kHz IF | | 300 | | kHz |
| Minimum Polling Mode Duty Cycle | | | | 0.775 | | % |
| **AC SPECIFICATIONS / SENSITIVITY / FSK** | | | | | | |
| Sensitivity Limit FSK (Note 2) | | RXBW = 340kHz, 100kbps, FSK deviation = ±80kHz, $f_{RF}$ = 868MHz | | -100 | | dBm |
| | | RXBW = 340kHz, 62.5kbps, FSK deviation = ±40kHz | | -106 | | |
| | | RXBW = 24kHz, 10kbps, FSK deviation = ±8kHz | | -116 | | |
| | | RXBW = 12kHz, 2kbps, FSK deviation = ±2kHz | | -120 | | |
| | | RXBW = 12kHz, 250bps, FSK deviation = ±2kHz | | -127 | | |
| **AC SPECIFICATIONS / SENSITIVITY / ASK** | | | | | | |
| Sensitivity Limit ASK (Note 2) | | RXBW = 340kHz, 62.5kbps, $f_{RF}$ = 868MHz, modulation depth ≥ 20dB | | -103 | | dBm |
| | | RXBW = 120kHz, 5kbps | | -116 | | |
| | | RXBW = 120kHz, 2kbps | | -118 | | |
| | | RXBW = 24kHz, 1kbps | | -122 | | |
| | | RXBW = 12kHz, 250bps | | -127 | | |
| **AC SPECIFICATIONS / Startup Time** | | | | | | |
| Maximum Receiver Start-Up Time (Note 2) | | Self-polling mode (DATA high), ASK, 10kbps | | 450 | | µs |
| | | Slave receiver mode, from sleep state to receive ready (including crystal startup time), 10kbps | | 860 | | |
| **AC SPECIFICATIONS / PLL TURN-ON TIME** | | | | | | |
| Minimum Synthesizer Frequency Step | | | | $f_{XTAL}/2^{16}$ | | Hz |
| **AC SPECIFICATIONS / IMAGE REJECTION** | | | | | | |
| Image Rejection | IR_UNCAL | Uncalibrated | | 30 | | dB |
| | IR_CAL | Calibrated | | 33 | | |
| **AC SPECIFICATIONS / BLOCKERS** | | | | | | |
| Minimum Blocking Level | | 3dB desense (Note 3)<br>±2MHz offset | | -58 | | dBm |
| | | ±10MHz offset | | -40 | | |
| Selectivity | | 3dB desense (Note 3)<br>±300kHz offset, IF = 200kHz | | 47 | | dBc |

## Electrical Characteristics (continued)

(*Typical Application Circuit*, typical values are at $V_{DD}$ = +3.0V, $T_A$ = +25°C, ASK at input frequency = 433.92MHz, Manchester encoded, IF = 400kHz, RXBW = 340kHz with 16MHz crystal oscillator, unless otherwise noted. (Note 1))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **AC SPECIFICATIONS / MAXIMUM DATA RATE** | | | | | | |
| Maximum data rate | | Manchester encoded | | 100 | | kbps |
| | | Nonreturn to zero (NRZ) | | 200 | | |
| **AC SPECIFICATIONS / RSSI** | | | | | | |
| RSSI Resolution | | | | ±0.5 | | dB |
| RSSI Linear Dynamic Range | | | 70 | 90 | | dB |
| **AC SPECIFICATIONS / LNA** | | | | | | |
| Input Impedance | | | | 50 | | Ω |
| **CRYSTAL OSCILLATOR** | | | | | | |
| Crystal Frequency | $f_{XTAL}$ | | 12.8 | 16 | 19.2 | MHz |
| Crystal Oscillator Startup Time | $t_{XO}$ | | | 380 | | µs |
| Crystal Load Capacitance | $C_L$ | | | 6 | | pF |
| **CMOS INPUT/OUTPUT (SCLK, SDIO, CSB, PWRDN, DATA)** | | | | | | |
| Input Low Voltage | $V_{IL}$ | 1.8V compatible | | | 0.36 | V |
| Input High Voltage | $V_{IH}$ | 1.8V compatible | 1.44 | | | V |
| Input Current | $I_{IL}/I_{IH}$ | | | ±10 | | µA |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 650µA | | 0.25 | | V |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 350µA | | $V_{DD}$ - 0.25 | | V |
| Maximum Load Capacitance at SDIO/ DATA Pins | $C_{LOAD}$ | | | 10 | | pF |
| PWRDN Pin Glitch Suppression | $t_{GLITCH}$ | Glitches suppressed by PWRDN pin | | 1 | | ns |
| **SERIAL INTERFACE / SPI (FIGURE 1)** | | | | | | |
| SCLK Frequency | $f_{SCLK}$ | $1/t_{SCLK}$ | | | 20 | MHz |
| SCLK to CSB Setup Time | $t_{CSS}$ | | | 10 | | ns |
| SCLK to CSB Hold Time | $t_{CSH}$ | | | 0 | | ns |
| SDIO to SCLK Hold Time | $t_{SDH}$ | Write | | 0 | | ns |
| SDIO to SCLK Setup Time | $t_{SDS}$ | Write | | 5 | | ns |
| Minimum SCLK to SDIO Data Delay | $t_{SDD\_MIN}$ | Read, 10pF load from SDIO to ground | | 1.5 | | ns |
| | | Read, 100pF load from SDIO to ground | | 3.5 | | |
| Maximum SCLK to SDIO Data Delay | $t_{SDD\_MAX}$ | Read, 10pF load from SDIO to ground | | 8 | | ns |
| | | Read, 100pF load from SDIO to ground | | 11 | | |

**Note 1:** 100% tested at $T_A$ = +25°C. Limits over operating temperature and relevant supply voltage are guaranteed by design and characterization over temperature.

**Note 2:** All data rates are Manchester encoded, where 1kbps is equivalent to a 1kHz square wave representing a continuous string of "1" data bits. Average sensitivity at 433.92MHz, BER ≤ 0.2%.

**Note 3:** Power referred to LNA input. Manchester 10kbps data rate, unless otherwise noted.

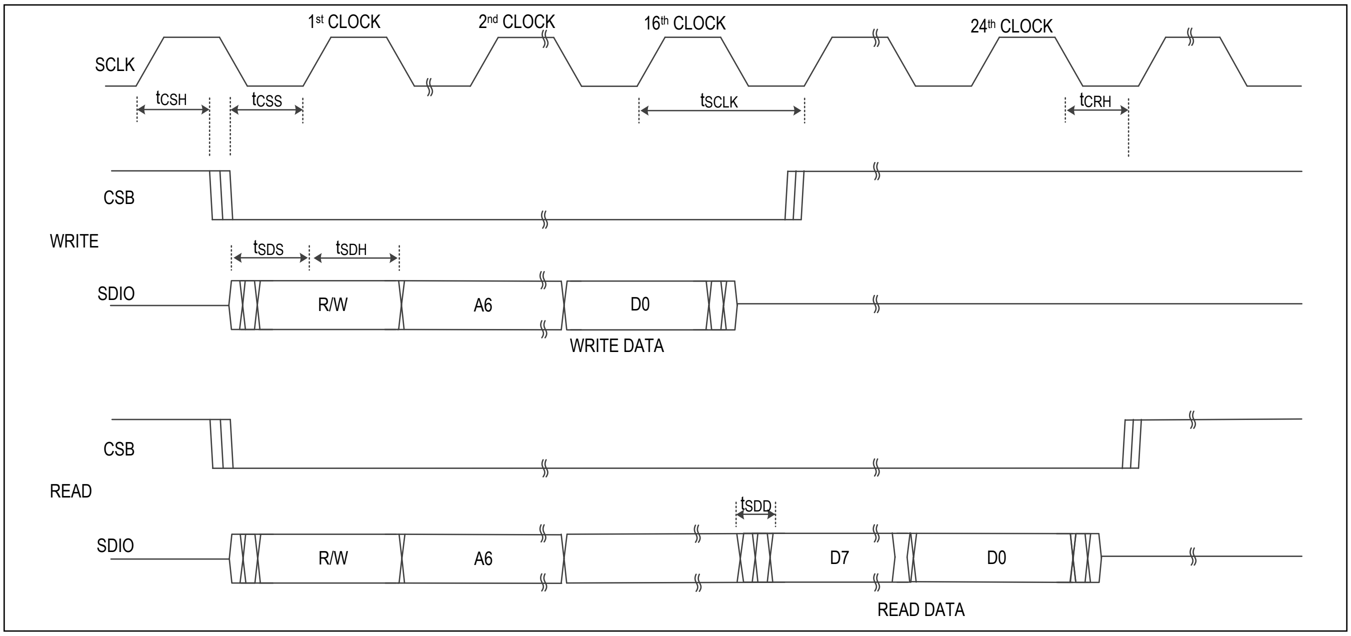
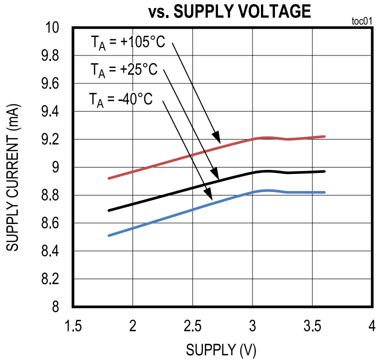


*Figure 1. SPI Serial Timing Interface Timing Diagram*

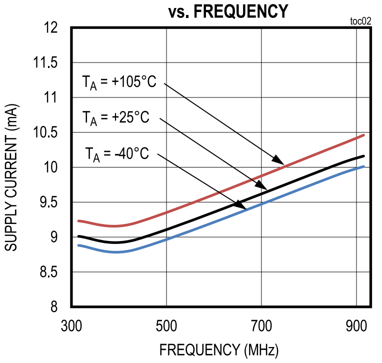
## Typical Operating Characteristics

(*Typical Application Circuit*. Typical values are for ASK at $f_{RF}$ = 433.92MHz, IF = 400kHz, CHF = 340kHz, data rate = 5kbps, $V_{DD}$ = +3V, $T_A$ = +25°C, unless otherwise noted. Sensitivity at 0.2% BER.)

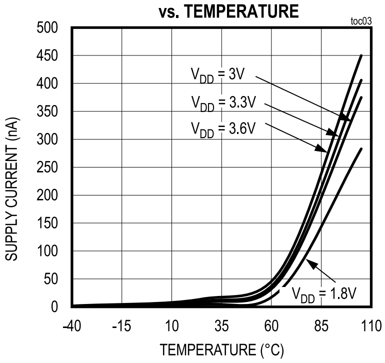
SUPPLY CURRENT vs. SUPPLY VOLTAGE



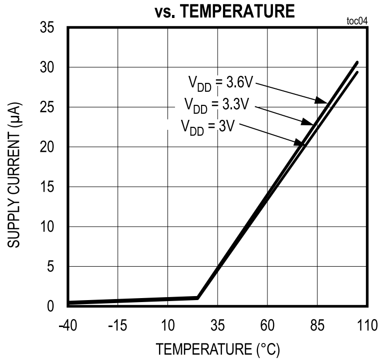
SUPPLY CURRENT vs. FREQUENCY



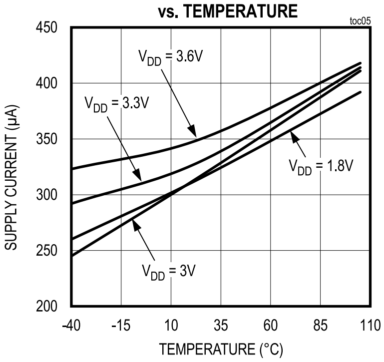
SHUTDOWN CURRENT vs. TEMPERATURE



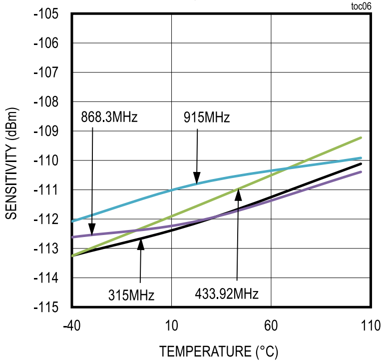
SLEEP CURRENT vs. TEMPERATURE



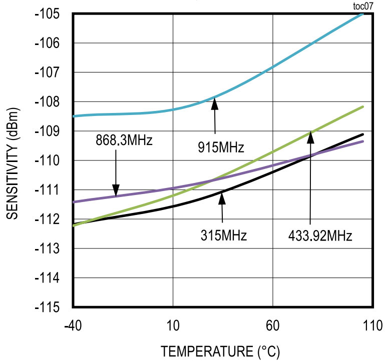
STANDBY CURRENT vs. TEMPERATURE



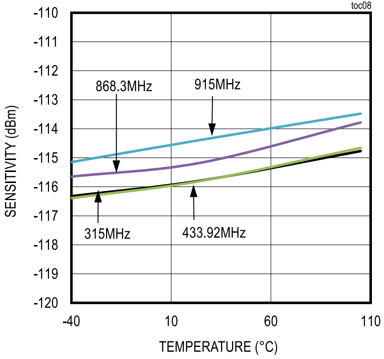
SENSITIVITY vs. TEMPERATURE ASK, IF = 200kHz



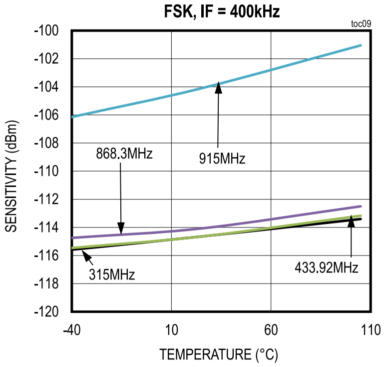
SENSITIVITY vs. TEMPERATURE ASK, IF = 400kHz



SENSITIVITY vs. TEMPERATURE FSK, IF = 200kHz



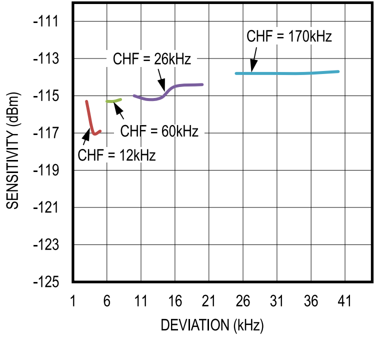
SENSITIVITY vs. TEMPERATURE FSK, IF = 400kHz



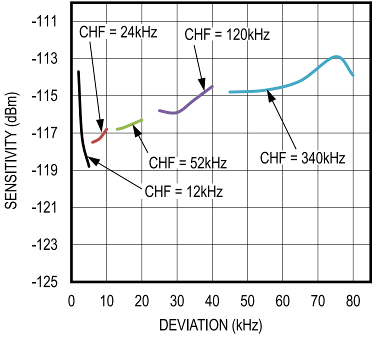
## Typical Operating Characteristics (continued)

(*Typical Application Circuit*. Typical values are for ASK at $f_{RF}$ = 433.92MHz, IF = 400kHz, CHF = 340kHz, data rate = 5kbps, $V_{DD}$ = +3V, $T_A$ = +25°C, unless otherwise noted. Sensitivity at 0.2% BER.)

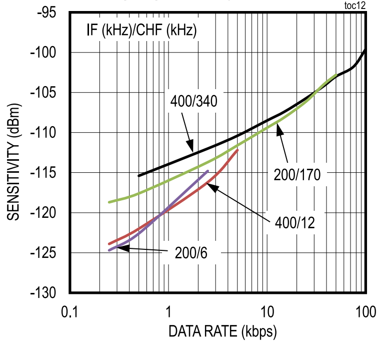
**SENSITIVITY vs. DEVIATION**
**FSK, IF = 200kHz**



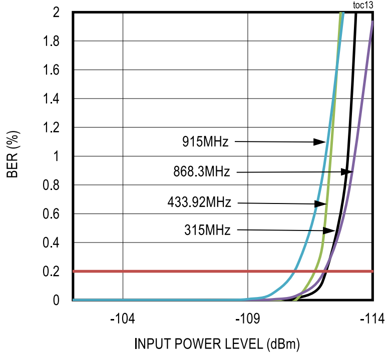
**SENSITIVITY vs. DEVIATION**
**FSK, IF = 400kHz**



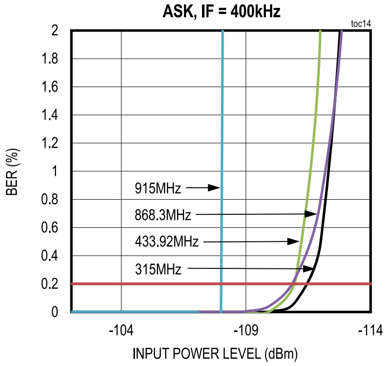
**SENSITIVITY vs. DATA RATE**



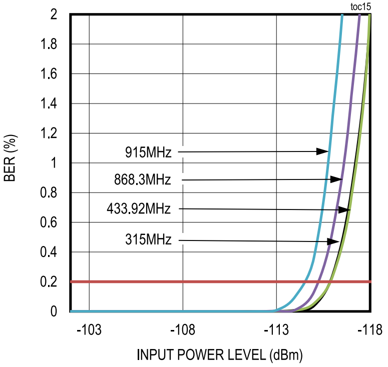
**BER vs. INPUT POWER**
**ASK, IF = 200kHz**



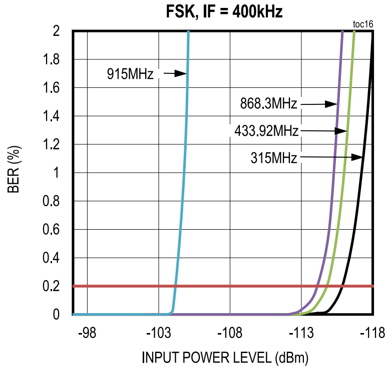
**BER vs. INPUT POWER**
**ASK, IF = 400kHz**



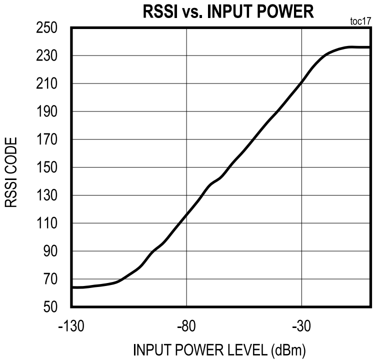
**BER vs. INPUT POWER**
**FSK, IF = 200kHz**



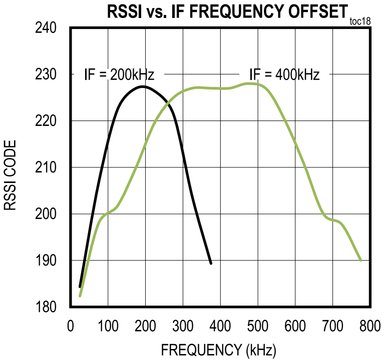
**BER vs. INPUT POWER**
**FSK, IF = 400kHz**



**RSSI vs. INPUT POWER**

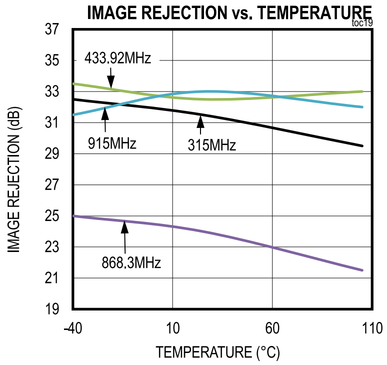


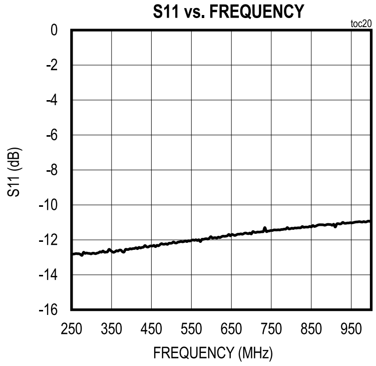
**RSSI vs. IF FREQUENCY OFFSET**

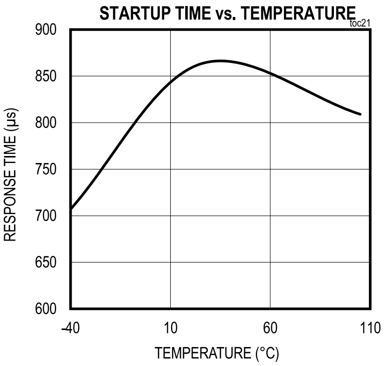


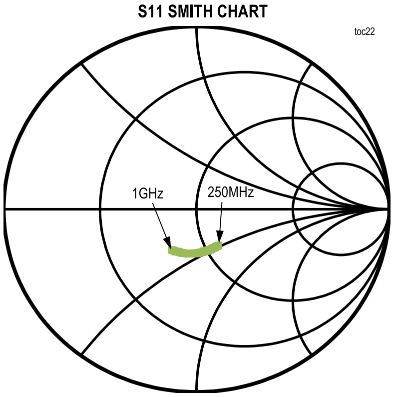
## Typical Operating Characteristics (continued)

(*Typical Application Circuit*. Typical values are for ASK at $f_{RF}$ = 433.92MHz, IF = 400kHz, CHF = 340kHz, data rate = 5kbps, $V_{DD}$ = +3V, $T_A$ = +25°C, unless otherwise noted. Sensitivity at 0.2% BER.)

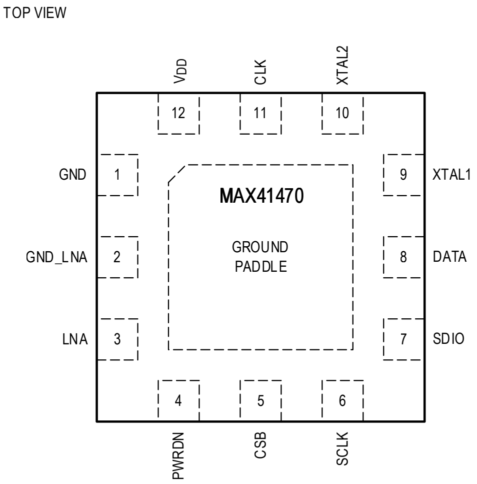








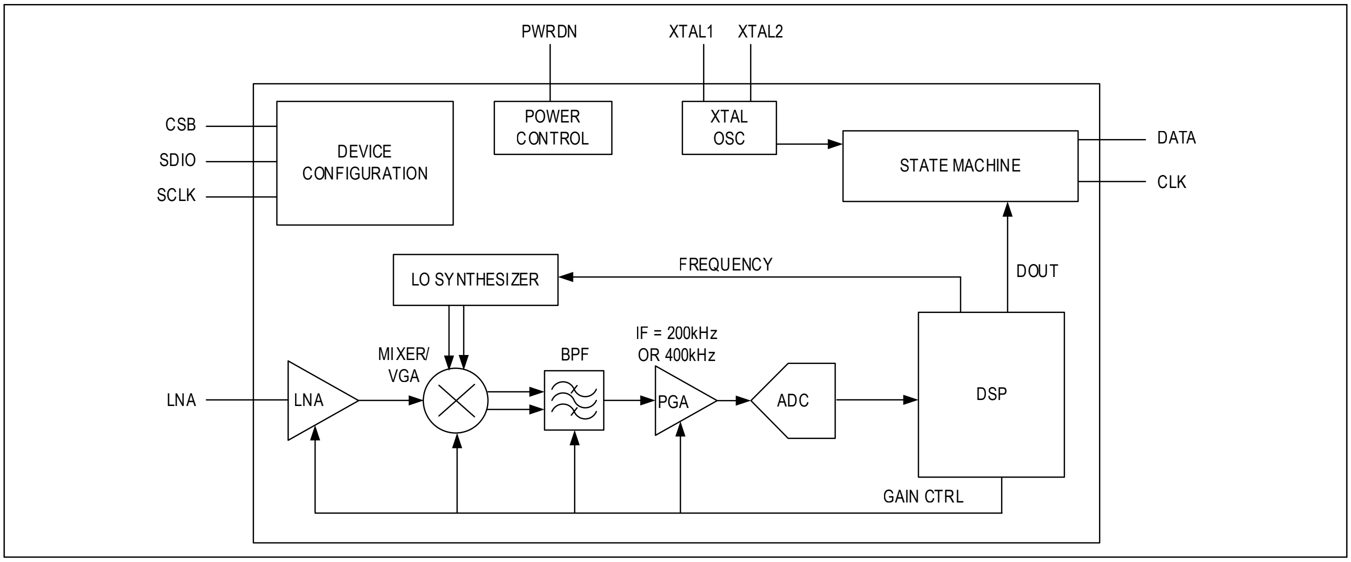
## Pin Configuration



## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | GND_LNA | Ground for Low-Noise Amplifier |
| 3 | LNA | Low-Noise Amplifier Input |
| 4 | PWRDN | Power-Down, Active-High. When the pin is controlled by external MCU, apply logic-high for shutdown mode or logic-low to enable the device. After a falling edge of PWRDN, the internal registers are reset to default values. When the pin is connected to GND, the device cannot enter the lowest current shutdown state.<br>Proper start-up timing is for MCU to drive PWRDN high and wait for 1ms, then drive PWRDN low and wait for 0.2ms before writing to registers. |
| 5 | CSB | Serial Interface Chip Select. Active low. |
| 6 | SCLK | Serial Interface Clock Input for Register Programming |
| 7 | SDIO | Serial Interface Data Input/Output for Register Programming. When CSB is at logic-low. |
| 8 | DATA | Data Output of Demodulated Received Signal |
| 9 | XTAL1 | First Crystal Input. Can be driven single-ended. |
| 10 | XTAL2 | Second Crystal Input |
| 11 | CLK | Recovered Clock Output. If the clock output is disabled, connect to GND. If the clock output is enabled, tie the pin to GND through a 10kΩ resistor. |
| 12 | VDD | Power-Supply Voltage. Connect a 0.01µF capacitor to ground. |
| PADDLE | GND | Ground |

## Functional Diagrams



## Detailed Description

The MAX41470 sub-GHz ISM RF receiver requires very few external components to complete the receiver signal chain from RF to bits. Depending on the signal power, data rates as high as 100kbps Manchester (200kbps NRZ) can be achieved.

This part is designed to receive ASK/OOK or FSK/GFSK modulated data in the 287MHz to 320MHz (nominally 315MHz), 425MHz to 480MHz (nominally 434MHz), and 860MHz to 960MHz (nominally 868MHz or 915MHz) ISM frequency bands.

The architecture of the MAX41470 is a low intermediate frequency (low-IF) receiver with digital demodulation. The antenna received signal is amplified and downconverted to a 400kHz or 200kHz IF. The local oscillator (LO) signal for downconversion is generated from an internal fractional-N PLL synthesizer and an external 16MHz crystal.

The analog receiver bandwidth is 350kHz (when IF = 400kHz) or 175kHz (when IF = 200kHz), corresponding to the IF selection. Digital channel filtering with programmable bandwidth is applied before demodulation. When the data rate is low, a narrow bandwidth channel filter can be selected to achieve high receiver sensitivity. Post-demodulation filtering with a programmable bandwidth is implemented in the digital domain where that filtered output is compared against an adaptive decision threshold to generate a 1-bit oversampled output on the DATA pin.

Supported features of the MAX4147x receiver family include: automatic gain control (AGC), a received signal strength indicator (RSSI), automatic frequency control (AFC), and a frequency error indicator (FEI).

The MAX41470 has an SPI interface to program the internal registers for full control of the device. For $I^2C$ programmability or preset capability, refer to the MAX41473/MAX41474 data sheet. When in programming mode, the MAX41470 can support self-polling operation based on a Manchester-encoded preamble detection to provide an interrupt signal on the DATA pin.

### Power States

The MAX41470 receivers have four power states: Shutdown, Sleep, Standby, and Receive Active. Set the PWRDN pin low to enable (power on) the device and set PWRDN high to disable the radio. When the device is enabled, the device operational states are controlled through the serial interface by the internal registers.

Typically, PWRDN is driven by a GPIO pin from an MCU and must be driven high or low. When PWRDN is connected to GND, the device cannot enter Shutdown state.

## Table 1. Supply Current in Four Power States

| POWER STATE | SUPPLY CURRENT (TYP) | COMMENT |
|---|---|---|
| Shutdown | 10nA | No serial port access, register values lost |
| Sleep | 1µA | Serial port powered, register values retained |
| Standby | 0.32mA | Crystal oscillator powered |
| Receive Active | 9mA | Entire receiver powered |

### State Diagram

While in programming mode, the MAX41470 has two major operational states: slave-receiver and self-polling. While operating as a slave-receiver (SlaveRX), the MAX41470 is fully controlled by an external "master" MCU through the serial interface. In the self-polling operation (PollingRX), the MAX41470 periodically switches between standby and receiving states according to preprogrammed times, interrupts, and MCU control.

Figure 2 is a simplified state diagram of the MAX41470. When the PWRDN pin is set high, the device will enter the low-current Shutdown state. The PWRDN should be held high for at least 1ms before transitioning to low. When the PWRDN pin is driven low, the internal supply is turned on and the device enters the Sleep state with all the internal registers reset to default values. Programming through the serial interface is allowed after a typical turn-on time of 400µs to allow settling of the device. Programming while in the Sleep state is not recommended, except for writing a 1 to the EN_XO bit in order to change the device to the Standby state. It is recommended the user perform serial communications while in the Standby state. To enable SlaveRX operation from the Standby state, the user writes a 0 to the WUT_EN bit and a 1 to the SLAVE_RX_EN bit. All three register bits used to control the power state (EN_XO, WUT_EN, and SLAVE_EN) can be found in the STATE_CTRL1 (0x14) register.

While in the SlaveRX state, the user can read but *not write* values to the DIG_RX registers and, in general, the device configuration cannot be changed while the receiver is active (SlaveRX or PollingRX states). The SlaveRX state does support access to the STATE_CTRL1 (0x14) register, for example, when writing SLAVE_RX_EN = 0 to turn off the receiver and change the device state back to Standby.

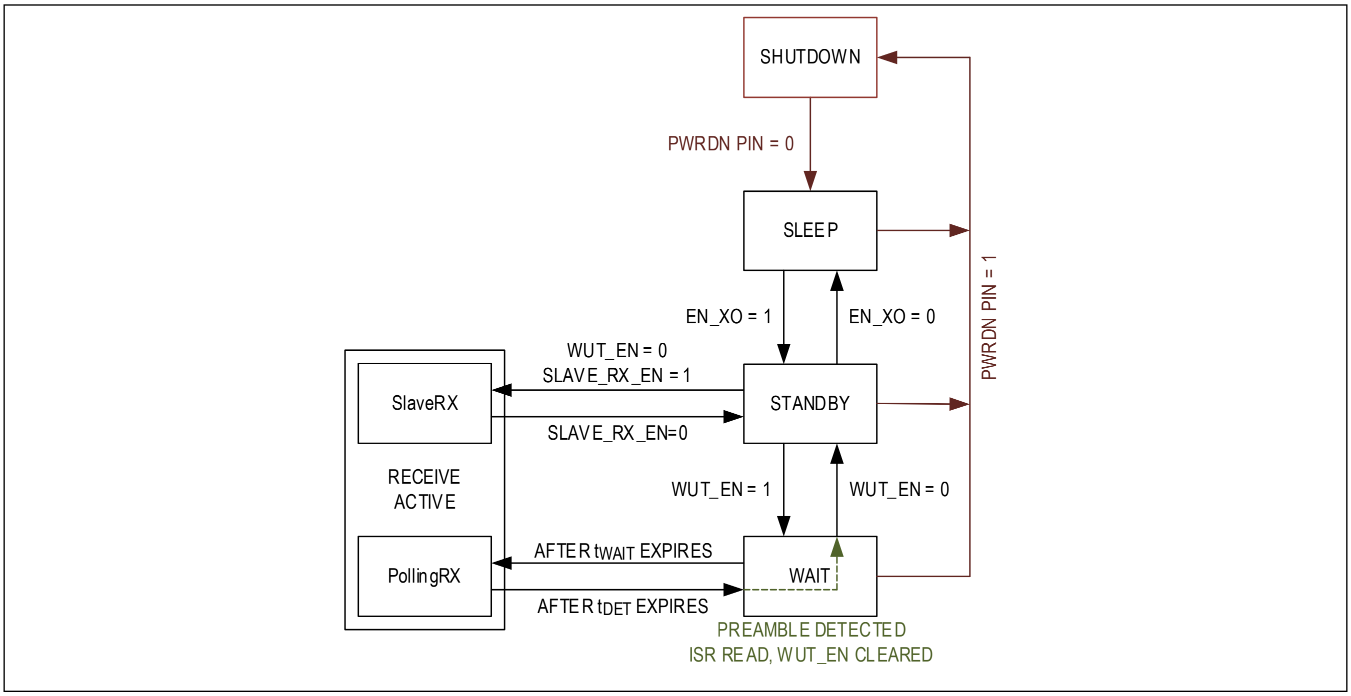


*Figure 2. State Diagram*

## Table 2. State Transition Time

| EVENT | STATE TRANSITION | TYPICAL TIME (µs) |
|---|---|---|
| PWRDN Pin Cleared to 0 | Shutdown to Sleep | 400 |
| EN_XO Bit Set | Sleep to Standby | 380 |
| SLAVE_RX_EN Bit Set | Standby to SlaveRX | 320 |
| SLAVE_RX_EN Bit Cleared | SlaveRX to Standby | 10 |
| EN_XO Bit Cleared | Standby to Sleep | 10 |
| WUT_EN Bit Set | Standby to Wait | 10 |
| PWRDN Pin Set to 1 | From any state to Shutdown | 10 |

### Self-Polling Mode

Self-polling operation is enabled by writing a 1 to the WUT_EN bit while the device is in the Standby state. This allows the user to place the master MCU into a low-power mode, allowing the MAX41470 to automatically toggle between a low-current Wait state and the higher-current PollingRX state. The periodic toggling is controlled by the internal wake-up timer (WUT) signal, which is a pulse chain as illustrated in Figure 3.

The duration the receiver is in the PollingRX state (detection time or $t_{DET}$) is adjustable from 0.48ms to 20.88ms, in 0.08ms steps, by programming the TDET[7:0] field in the WUT1 (0x17) register. This detection time should be set to a value longer than the receiver turn-on time (Table 2) plus the preamble pattern duration. For guaranteed detection, refer to the details under the *Preamble Detector* section. The WUT period is defined as:

$$T_{WUT} = t_{DET} + t_{WAIT} = t_{DET} + N_{RATIO} \times t_{DET} = (1 + N_{RATIO}) \times t_{DET}$$

where $T_{WUT}$ is the wake-up time period, $t_{DET}$ is the programmed detection time, $t_{WAIT}$ is the wait time, and $N_{RATIO}$ is the programmed ratio of $t_{DET}/t_{WAIT}$, thus $T_{WUT}$ is an integer multiple (≥2) of $t_{DET}$.

The ratio of $t_{WAIT}$ to $t_{DET}$ ($N_{RATIO}$) is adjustable from 1 to 128 in step size of 1 by programming the TSBY_TDET_RATIO[6:0] field in the WUT2 (0x18) register. Therefore, the WUT duty cycle is programmable from 1/2 to 1/129. The WUT response time ($t_{1WUT}$) is approximately the same as $t_{WAIT}$.

In self-polling mode, the DATA pin serves as an interrupt source for an MCU. Once a preamble bit pattern is received and validated in the PollingRX state, the PREAMB_DET bit in the interrupt status register ISR (0x13) will be set to 1, and a falling edge will be generated on the DATA pin to wake up an MCU at the completion of the polling cycle. After wakeup, the user must read the ISR (0x13) register to automatically clear the PREAMB_DET bit and WUT_EN bit in the STATE_CTRL1 (0x14) register. The MAX41470 will thus exit self-polling mode and assert the DATA output pin to logic 1. With the read to the ISR register, the resulting state is Standby and a write to the SLAVE_RX_EN bit is required to transition into the SlaveRX state.

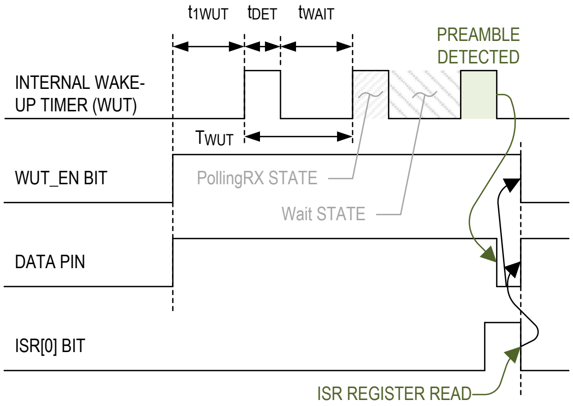


*Figure 3. Wake-Up Timer in Self-Polling Mode*

### Preamble Detector

The MAX41470 provides a preamble detector to be used with the self-polling operation. The preamble must be Manchester encoded as shown in Table 3. The pattern length, from 1 to 16 bits, is set in the PREAMB_LEN[3:0] register field where 0x0 = 1 bit in length and 0xF = 16 bits in length. The non-encoded or raw bit pattern is programmed into PREAMB_WORD[15:0] (addresses 0x0E and 0x0D) noting that PREAMB_WORD[0] is the LSB of the bit pattern and this is the most recent or last bit received from the RF bit stream. As bits are received and demodulated, they are effectively shifted in and compared to the PREAMB_WORD from the LSB to the MSB.

## Table 3. Manchester Encoding for Preamble

| RAW BIT | MANCHESTER EDGE (BAUD) | DECODED BITS |
|---|---|---|
| 0 | ¯\|_ | 10 |
| 1 | _\|¯ | 01 |

For guaranteed preamble detection within the first $t_{DET}$ cycle, the $t_{DET}$ width would allow margin for the case where the first bit of the preamble was not received when $t_{DET}$ state was entered. The resulting equation would be:

$$\text{PREAM\_LEN} + \text{PREAM\_LEN} - 1 = 2 \times \text{PREAM\_LEN} - 1$$

Due to the $t_{DET}$ time range of 0.48ms to 20.88ms, the number of bits that can fit into this range and comply with the guaranteed $t_{DET}$ detection equation of 2 x PREAM_LEN - 1 dictates a limitation on the number of bits detectable given a defined bit rate. For example, if the Manchester data rate is 250bps and guarantee detection with PREAM_LEN = 16, this would equate to 2 x 16 - 1 = 31 bits required. To receive 31 bits at 250bps, it would take the following:

$$\frac{1}{\text{DataRate}} \times \text{bits required} = \frac{1}{250\text{bps}} \times 31\text{bits} = 124\text{ms}$$

But the maximum $t_{DET}$ allowed is 20.88ms. The table below states the limitations for the lower data rates if using the guaranteed timing. If the data rate is above those listed, there is no limitation.

## Table 4. PREAM_LEN Limitation for Guaranteed Detection

| DATA RATE (bps) | MAX PREAM_LEN BITS | $t_{DET}$ DURATION (ms) |
|---|---|---|
| 250 | 3 | 20 |
| 500 | 5 | 18 |
| 1k | 10 | 19 |
| 2k | 16 | 15.5 |

For example, if PREAMB_LEN[3:0] is programmed to 0xA (decimal value 10), then the preamble bit pattern is specified by PREAMB_WORD[10:0], and the preamble is 22 bits after decoding the Manchester edges (or 11 raw bits before encoding). In this example, the five MSBs in the PREAMB_WORD field [15:11] are not used.

The preamble detector is triggered when the received bit stream matches the Manchester version of the PREAMB_WORD without regard to the phase of the pattern. For example, a non-Manchester preamble word of 0xFF = Manchester $0101\ 0101\ 0101\ 0101_b$ and a non-Manchester preamble word of 0x00 = Manchester $1010\ 1010\ 1010\ 1010_b$ would both trigger a matching RF bit stream of $0101...\ 0101_b$.

### DATA Pin

The DATA pin toggles while in the SlaveRX state to output a digital binary representation of received data. The digital base band system has a minimum requirement to oversample the signal by 16x thus limiting the data rate of received signal to no more than 100kbps Manchester (200kbps NRZ).

In self-polling operation, the DATA pin serves as both an interrupt source and the data stream from the digital baseband system. The DATA pin is driven to logic 1 while in the PollingRX state. If no match is made to the preamble pattern, the device will move to the Wait state and the DATA pin will continue to be driven high. Once the preamble pattern is detected in the PollingRX state, a falling edge will be generated on the DATA pin right after the device switches to the Wait state and DATA will be held at logic 0. After the ISR register has been read, the DATA pin will be driven back to logic 1 and the device will be placed into the Standby state (as the WUT_EN bit is cleared automatically).

To begin streaming data from the DATA pin, the receiver needs to be moved from Standby to the SlaveRX state by writing a 1 to the SLAVE_RX_EN bit in the STATE_CTRL (0x14) register. This operation can be performed right after reading the ISR register.

If the ISR register is not read (cleared) within the initial $t_{WAIT}$ time, the receiver will automatically re-enter the PollingRX state and set the DATA pin back to logic 1. Since the ISR was not cleared during the previous cycle, the preamble detect is still triggered and once the $t_{DET}$ time expires, the receiver will again indicate an interrupt by driving the DATA pin to 0 after it re-enters the Wait state. This cycle will continue until the ISR register is cleared.

### Selection of Intermediate Frequency

The IF can be selected between two values by programming the IF_SEL bit in the IF_CHF_SEL (0x02) register.

## Table 5. Intermediate Frequency Selection

| INTERMEDIATE FREQUENCY (kHz) | ANALOG BANDWIDTH (kHz) | IF_SEL |
|---|---|---|
| 400 | 350 | 0 |
| 200 | 175 | 1 |

### Selection of Channel Filter

The digital channel filter (CHF) can be selected by programming the CHF_SEL[2:0] field in the IF_CHF_SEL (0x02) register. Aggregate receiver bandwidth also depends on the IF selection. See Table 6 for digital channel filter settings.

## Table 6. Channel Filter Selection

| 400kHz IF RECEIVER BW (kHz) | 200kHz IF RECEIVER BW (kHz) | CHF_SEL |
|---|---|---|
| 340 | 170 | 0 |
| 120 | 60 | 1 |
| 52 | 26 | 2 |
| 24 | 12 | 3 |
| 12 | 6 | 4 |

### Demodulator Configuration

The modulation mode is selected by programming the ASK_FSK_SEL bit in the IF_CHF_SEL (0x0) register. Write a 0 to the ASK_FSK_SEL bit for ASK modulation, or a 1 to the ASK_FSK_SEL bit for FSK modulation.

The ASK/FSK demodulator configuration depends on the DEMOD_TCTRL[2:0] and DEMOD_FSK[2:0] fields in the DEMOD (0x00) register. DEMOD_TCTRL should be programmed according to the formulas in Table 7:

## Table 7. Recommended Programming of DEMOD_TCTRL

| MODULATION | CONDITIONS | | DEMOD_TCTRL |
|---|---|---|---|
| | ASK_FSK_SEL | ATH_TYPE | |
| FSK | 1 | X | 4 – CHF_SEL |
| ASK | 0 | 0 (preLPF for Manchester) | min(2+SRC_LG, 7) |
| | 0 | 1 (aPD for NRZ) | min(3+SRC_LG, 7) |

The DEMOD_FSK field is used only in FSK mode. There are a total of 28 options for configuring the FSK demodulator, as seen in the following tables:

## Table 8. Options of FSK Demodulator Configuration for 400kHz IF (IF_SEL = 0)

| NOMINAL FSK ±Δf (kHz) | RANGE OF FSK ±Δf (kHz) | IF_SEL | CHF_SEL | DEMOD_FSK |
|---|---|---|---|---|
| 80* | [64, 84] | 0 | 0 | 0 |
| 57 | [50, 67] | 0 | 0 | 1 |
| 44 | [40, 50] | 0 | 0 | 2 |
| 40 | [32, 42] | 0 | 1 | 3 |
| 29 | [25, 33] | 0 | 1 | 4 |
| 22 | [20, 25] | 0 | 1 | 5 |
| 20 | [16, 21] | 0 | 2 | 3 |
| 14 | [12.5, 16.5] | 0 | 2 | 4 |
| 11 | [10, 12.5] | 0 | 2 | 5 |
| 10 | [8, 10.5] | 0 | 3 | 4 |
| 7 | [5.3, 8] | 0 | 3 | 5 |
| 5 | [4, 5.3] | 0 | 4 | 4 |
| 3 | [2.6, 4] | 0 | 4 | 5 |
| 2 | [1.6, 2.6] | 0 | 4 | 6 |

* Default setting

## Table 9. Options of FSK Demodulator Configuration for 200kHz IF (IF_SEL = 1)

| NOMINAL FSK ±Δf (kHz) | RANGE OF FSK ±Δf (kHz) | IF_SEL | CHF_SEL | DEMOD_FSK |
|---|---|---|---|---|
| 40 | [32, 42] | 1 | 0 | 0 |
| 28.5 | [25, 33.5] | 1 | 0 | 1 |
| 22 | [20, 25] | 1 | 0 | 2 |
| 20 | [16, 21] | 1 | 1 | 3 |
| 14.5 | [12.5, 16.5] | 1 | 1 | 4 |
| 11 | [10, 12.5] | 1 | 1 | 5 |
| 10 | [8,10.5] | 1 | 2 | 3 |
| 7 | [6.3, 8.2] | 1 | 2 | 4 |
| 5.5 | [5, 6.3] | 1 | 2 | 5 |
| 5 | [4, 5.2] | 1 | 3 | 4 |
| 3.5 | [2.6, 4] | 1 | 3 | 5 |
| 2.5 | [2, 2.6] | 1 | 4 | 4 |
| 1.5 | [1.3, 2] | 1 | 4 | 5 |
| 1 | [0.8, 1.3] | 1 | 4 | 6 |

### Automatic Gain Control (AGC)

The MAX41470 provides a dual-step feedback AGC, as illustrated in Figure 4. AGC attack, or high-to-low gain switching, happens when the raw RSSI value is higher than a threshold. AGC release, or low-to-high gain switching, happens when the raw RSSI value is lower than a second threshold. The difference between the attack and release thresholds should be large enough to provide hysteresis.

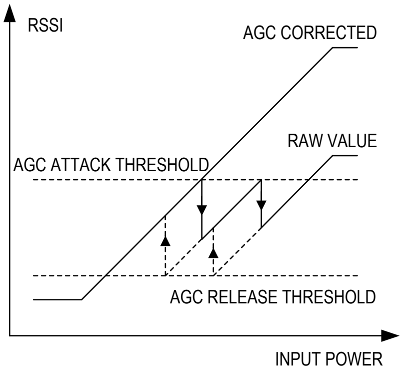


*Figure 4. AGC and RSSI*

The AGC operation mode is controlled by the AGC_EN_BO[1:0] field in the AGC (0x01) register.

## Table 10. AGC Operating Modes

| AUTOMATIC GAIN CONTROL | RSSI DYNAMIC RANGE (TYP) (dB) | AGC_EN_BO | COMMENT |
|---|---|---|---|
| Disabled | 36 | 0 | Not recommended |

## Table 10. AGC Operating Modes (continued)

| | | | |
|---|---|---|---|
| | 42 | 1 | Wider RSSI dynamic range |
| Enabled | 85 | 2* | Best receiver sensitivity |
| | 83 | 3 | Not recommended |

*Default setting

The release threshold of AGC can be fine-tuned by programming the AGC_THREL[3:0] field.

## Table 11. AGC Fine-Tuning for Data Rate

| MODULATION | DATA RATE (kbps) | AGC_THREL |
|---|---|---|
| ASK | ≤26 | 0x9 |
| | >26 | 0xF |
| FSK | ≤51.5 | 0x9 |
| | >51.5 | 0xF |

### Received Signal Strength Indicator (RSSI)

The MAX41470 features an AGC-corrected RSSI, as illustrated in Figure 4. To get a large dynamic range of RSSI, the AGC_EN_BO register should be programmed to enable the AGC.

The RSSI is a dynamic value, readable from the RSSI (0x10) register with a scale of 0.5dB per bit. The RSSI is *not* calibrated based on an absolute power level at the LNA input, so part-to-part variations of receiver front-end gain will affect this RSSI value.

The RSSI functions as a logarithmic envelope detector followed by a peak detector. The discharge slope of the RSSI peak detector is expressed as:

$$PD_{SLOPE} = 1.67 \times 2^{N} \ (\mu s/div)$$

where N = max(IF_SEL + CHF_SEL + DEMOD_TCTRL + RSSI_DT - 1, 0).

Because the RSSI scale is 0.5dB/div, the time constant of 3dB discharge is $(10 \times 2^{N})$ µs.

### Automatic Frequency Control (AFC)

A feedback control loop is used to adjust the PLL synthesizer frequency within a programmable range. The center of the AFC range is programmed by 24-bit frequency word LO_CTR_FREQ[23:0], which can be calculated from the following equation with the default LO injection setting when MIX_HS_LSBAR = 0:

$$LO\_CTR\_FREQ = INT\left(65536\frac{(f_{RF} - f_{IF})}{f_{XTAL}}\right)$$

where $f_{RF}$ is the target RF frequency, $f_{IF}$ is the 200kHz or 400kHz setting programmed with the IF_SEL bit, and $f_{XTAL}$ is the crystal frequency (typically 16MHz).

When MIX_HS_LSBAR = 1, the equation for LO_CTR_FREQ[23:0] is:

$$LO\_CTR\_FREQ = INT\left(65536\frac{(f_{RF} + f_{IF})}{f_{XTAL}}\right)$$

where $f_{RF}$ is the target RF frequency, $f_{IF}$ is the 200kHz or 400kHz setting programmed with the IF_SEL bit, and $f_{XTAL}$ is the crystal frequency (typically 16MHz).

The AFC loop generates a frequency offset from the programmed LO center frequency. The maximum frequency offset is limited by the receiver bandwidth and the AFC_MO[2:0] field setting in the AFC_CFG1 (0x07) register. This maximum offset can be expressed as:

$$f_{OFFSET-MAX} = AFC\_MO \times \frac{f_{XTAL}}{2^{(IF\_SEL + CHF\_SEL + 10)}}$$

where AFC_MO, IF_SEL, and CHF_SEL are programmed register values. When AFC_MO = 0, the PLL synthesizer frequency is fixed and AFC is disabled.

Without AFC, the frequency mismatch between an RF transmitter (Tx) and this receiver (Rx) can be estimated from the crystal accuracy ratings and the operating frequency band. For example, assume the crystal accuracy is ±50ppm for both the Tx and Rx systems and the operating frequency is 434MHz, then the Tx/Rx frequency mismatch can be as high as ±100ppm of the operating frequency, or ±43kHz.

In ASK mode, AFC is not necessary when the receiver bandwidth is sufficiently wide, but AFC is required when a narrow channel filter is selected to achieve a high receiver sensitivity. In FSK mode, AFC is required when the Tx/Rx frequency mismatch is higher than 25% of the frequency deviation.

When a wide channel-filter option is selected (for example CHF_SEL = 0), AFC_MO can be programmed based on an estimate of the Tx/Rx frequency mismatch. For example, when using the 315MHz band, a 16MHz crystal, the wide channel filter (CHF_SEL = 0), and 200kHz IF (IF_SEL = 1), the user can program for a maximum AFC offset of 31.3kHz (AFC_MO = 4). This would be sufficient to allow for a ±100ppm Tx/Rx frequency mismatch in the 315MHz band.

The AFC_LG[1:0] field in AFC_CFG1 (0x07) register controls the AFC loop gain and settling time. This should typically be set to AFC_LG = 3 in ASK mode and AFC_LG = 2 in FSK mode.

### Frequency Error Indicator (FEI)

In programmable mode, the user can read the FEI (0x11) register to determine the frequency error. This value is an 8-bit, signed integer, in two's complement format. The frequency offset generated by AFC can be calculated as:

$$f_{OFFSET} = FEI \times \frac{f_{XTAL}}{2^{(IF\_SEL + CHF\_SEL + 14)}}$$

where FEI, IF_SEL, and CHF_SEL are register values and $f_{XTAL}$ is the crystal frequency (typically 16MHz)

Because the maximum offset is limited by the AFC_MO register field, the absolute value of FEI output is no more than 16 x AFC_MO. For the purpose of frequency tracking, the user can iteratively adjust the LO_CTR_FREQ register value based on an FEI reading.

### AFC Freeze upon Preamble Detection

The operation of AFC relies on an internal frequency detector, which senses errors in the RF frequency and averages the value over a number of received bits.

The changes in frequency inherent in FSK modulation introduces a bit-pattern-dependent, self-noise effect. Therefore, in FSK mode, it is recommended the AFC only be used when employing Manchester encoding and not with NRZ. In a typical data packet, the preamble is Manchester encoded but the payload may not be. With the MAX41470, a form of Manchester encoding must be used for proper preamble detection in the PollingRX mode.

Since the preamble is often an alternating 1 and 0 (or MARK and SPACE), setting PAD_FREEZE_AFC = 1 and AFC_LG = 3 will result in a fast settling of the AFC in roughly 5 bits of RF data.

The AFC starts automatically when the receiver is active (entering the SlaveRX or PollingRX state). While using FSK modulation and in the SlaveRX state, the AFC can be 'frozen' just after a valid preamble pattern is detected. This feature is enabled by setting the PAD_FREEZE_AFC bit to 1 in the AFC_CFG2 (0x08) register. See the *Preamble Detector* section for how to program the preamble bit pattern. The PAD_FREEZE_AFC bit is not available when using ASK modulation (ASK_FSK_SEL = 0).

## Recommended Data Rate and Post Demodulation Filter

The post-demodulation filter (PDF) is a digital filter with programmable bandwidth. The PDF bandwidth selection is closely related to the data rate of the received signal. For example, the bandwidth needed for Manchester encoding is twice that needed for the same bit rate when sending NRZ data. (See Table 3 for more information.)

For a given configuration of IF_SEL, CHF_SEL[2:0], SRC_SM[2:0], and SRC_LG[2:0] fields, the recommended decoded bit rate $R_b$ for Manchester is defined as:

$$R_b = \frac{200\text{kHz}}{2^{(\text{IF\_SEL} + \text{CHF\_SEL} + \text{SRC\_LG})}} \times \frac{4}{8 + \text{SRC\_SM}}$$

where integer values of registers are used in the expression.

Given the difference in NRZ format vs. Manchester data, the recommended decoded bit rate $R_b$ for NRZ would be adjusted to:

$$R_b = \frac{200\text{kHz}}{2^{(\text{IF\_SEL} + \text{CHF\_SEL} + \text{SRC\_LG})}} \times \frac{8}{8 + \text{SRC\_SM}}$$

where integer values of registers are used in the expression.

For additional guidance on setting the SRC_SM and SRC_LG values based on the desired configuration, see the *ASK Receiver Configurations* and *FSK Receiver Configurations* sections. The SRC_SM[2:0] and SRC_LG[2:0] fields are located in the PDF_CFG (0x03) register.

The PDF bandwidth is provided in Table 12:

## Table 12. Post Demodulation Filter Bandwidth

| PDF BANDWIDTH | LD_BW REGISTER |
|---|---|
| $0.6R_b$ | 0* |
| $R_b$ | 1 |

* Default setting

Regardless of the LD_BW setting, the actual transmission data rate should not exceed 1.03 x $R_b$ and should not be any lower than 0.6 x $R_b$ in any configuration.

### ASK Decision Threshold

The digital signal out of the post-demodulation filter is compared with a threshold to make a binary decision, which is subsequently represented as a 0 or 1 on the DATA output pin. When using FSK modulation, the decision threshold is fixed at zero, where a positive value signal represents the MARK frequency and a negative value represents the SPACE frequency. With ASK modulation, the comparison threshold will automatically be adjusted to accommodate changes in signal strength based on user settings.

The MAX41470 provides two ASK threshold adjustment methods set by the user with the ATH_TYPE bit in the ATH_CFG3 (0x06) register. The precharged lowpass filter (preLPF) method is strongly recommended when using Manchester encoding. In the case where Manchester encoding is not used (e.g., in NRZ format, which can result in long consecutive strings of 0s or 1s), the adaptive peak detector (aPD) method should be selected.

The ATH_BW bit in ATH_CFG3 (0x06) register is used only with the preLPF method to control the filter bandwidth. Program ATH_BW to 0 when the Manchester data rate is close to the recommended rate $R_b$ (suggested close values are $1.03R_b$ < data rate < $0.75R_b$; see the *Recommended Data Rate and Post Demodulation Filter* section for the definition of $R_b$). Use ATH_BW = 1 if the transmitter data rate is expected to go as low as $0.6R_b$.

The ATH_DT[1:0] field in the ATH_CFG2 (0x05) register is used only with the aPD method to adjust the peak detector's discharge time. If using Manchester encoding, set ATH_DT to 0 whenever the data rate is close to the recommended $R_b$ value. Set ATH_DT to 1 if the transmitter's Manchester data rate is expected to go as low as $0.6R_b$. In the case of NRZ encoding, set ATH_DT to 3.

The ATH_TC[4:0] field in the ATH_CFG2 (0x05) register is also used only with the aPD method to control the peak detector time constant. Set ATH_TC according to the SRC_LG value using Table 13:

## Table 13. Programming of ATH_TC

| SRC_LG | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|

## Table 13. Programming of ATH_TC (continued)

| **ATH_TC** | 0x14 | 0x12 | 0x10 | 0x0D | 0x09 | 0x07 | 0x05 | 0x04 |
|---|---|---|---|---|---|---|---|---|

The ATH_GC[4:0] field in the ATH_CFG3 (0x06) register should be set based on the values in the IF_SEL and CHF_SEL fields according to Table 14:

## Table 14. Programming of ATH_GC

| **IF_SEL** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** |
|---|---|---|---|---|---|---|---|---|---|---|
| **CHF_SEL** | **0** | **1** | **2** | **3** | **4** | **0** | **1** | **2** | **3** | **4** |
| **ATH_GC** | 0xB | 0x9 | 0x8 | 0x7 | 0x6 | 0xA | 0x7 | 0x6 | 0x5 | 0x4 |

### Lower Bound of ASK Decision Threshold

In both methods of decision threshold generation (preLPF and aPD), the lower bound of the decision threshold is set by the ATH_LB[7:0] field in the ATH_CFG1 (0x04) register. ATH_LB has a range of valid values from -128 to 0 and is represented in two's complement format (e.g., 0x9C = $-100_{dec}$).

To achieve the highest ASK receiver sensitivity combined with fast receiver settling within 2 bits, the optimum ATH_LB value can be found by calibrating the PDF through a collection of output noise statistics. For this calibration process, the LNA input pin must be terminated with 50Ω to ground while the user acquires random samples of the PDF by reading the PDF_OUT(0x12) register when the receiver is in the SlaveRX state. Without the termination, the standard deviation of the PDF_OUT values is much larger than actual. The calculated values below should be used if not terminated properly. The value of ATH_LB should be set using the following formula:

$$\text{ATH\_LB} = \mu + 3\sigma$$

where σ is the standard deviation of PDF_OUT and μ = MEAN(PDF_OUT - 16) when AGC_EN_BO[0] = 0, or μ = MEAN(PDF_OUT) when AGC_EN_BO[0] = 1.

Here, AGC_EN_BO[0] is the LSB of the 2-bit field in the AGC (0x01) register.

In the absence of a calibration value, ATH_LB should be set by calculating a recommended value based on the following formula and tables:

$$\text{ATH\_LB} = \text{MU1} + \text{MU2} - 6$$

where MU1 and MU2 are found using Table 15 and Table 16.

Find a value for MU1 based on the receiver filter settings.

## Table 15. Lookup Table for MU1

| **IF_SEL** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** |
|---|---|---|---|---|---|---|---|---|---|---|
| **CHF_SEL** | **0** | **1** | **2** | **3** | **4** | **0** | **1** | **2** | **3** | **4** |
| **MU1** | -81 | -93 | -102 | -110 | -118 | -90 | -102 | -110 | -118 | -125 |

Calculate the SRC_Ratio using the following formula:

$$\text{SRC\_RATIO} = \text{SRC\_LG} = \log_2(8 + \text{SRC\_SM}) - 3$$

where SRC_LG and SRC_SM are fields in the PDF_CFG (0x03) register.

## Table 16. Lookup Table for MU2

| **SRC_RATIO** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** |
|---|---|---|---|---|---|---|---|---|---|
| **MU2** | 29 | 21 | 15 | 11 | 8 | 6 | 4 | 3 | 2 |

When the SRC_RATIO is not an integer (SRC_SM is non-zero), a linear interpolation should be used to determine the best value for MU2 from the lookup table. The final MU2 value must be rounded to the nearest integer. For example, if SRC_SM = 2 and SRC_LG = 4, the SRC_Ratio is calculated to be 4.3. Using a linear interpolation between SRC_RATIO and MU2, the raw value for MU2 would be 7.4, rounded to a final value of MU2 = 7.

When preLPF is selected (ATH_TYPE = 0), the ATH_LB value may be lower than MU1 + MU2 - 6. As an example, set the ATH_LB field to a value of -127 (0x81 in two's complement) regardless of the IF_SEL and CHF_SEL settings. In this case, each device can deliver its highest sensitivity without calibration, but the receiver settling slows down when the signal power is close to the receiver sensitivity. Because some applications require fast receiver settling, the use case of ATH_LB = -127 is not always recommended, although it is convenient, as a trade-off between sensitivity and settling time.

### Squelching ASK Receiver

In ASK mode, ATH_LB may be programmed higher than the value determined from the threshold calibration measurements or the value calculated from MU1 and MU2. By setting the threshold higher than the calibration or calculated value, the DATA pin could be prevented from toggling just based on RF noise present in the threshold setting process when no transmission signal is present. This is commonly referred to as squelch. The trade-off for squelching the receiver is a commensurate reduction of receiver sensitivity.

## Receiver Sensitivity

Receiver sensitivity is measured and specified as the average LNA input power at a $2x10^{-3}$ bit-error rate (0.2% BER) when testing with Manchester-encoded data which is equivalent to $1x10^{-3}$ bit-error rate (0.1% BER) for NRZ data. For ASK modulation, average power is approximately 3dB lower than peak power.

There are many ways to optimize the sensitivity of the device, such as reducing the channel filter bandwidth, using lower data rates, ensuring that the carrier frequency is not a multiple of the crystal frequency, or even using a high-side LO injection configuration to avoid noise or spurs in the environment.

The configuration tables, Table 17, Table 18, Table 19, and Table 20, identify possible configurations where the highest or best sensitivity is identified in the top rows of each table. Table 19 and Table 20 provide guidance to those systems targeting a 0.8 modulation index.

### ASK Receiver Configurations

### Table 17. ASK Receiver for 400kHz IF

| DATA RATE (kbps) | IF_SEL | CHF_SEL | SRC_SM | SRC_LG |
|---|---|---|---|---|
| 0.25 | 0 | 4 | 4 | 4 |
| 0.25 | 0 | 3 | 4 | 5 |
| 0.5 | 0 | 4 | 4 | 3 |
| 0.5 | 0 | 3 | 4 | 4 |
| 0.5 | 0 | 2 | 4 | 5 |
| 1 | 0 | 3 | 4 | 3 |
| 1 | 0 | 4 | 4 | 2 |
| 1 | 0 | 2 | 4 | 4 |
| 1 | 0 | 1 | 4 | 5 |
| 2 | 0 | 3 | 4 | 2 |
| 2 | 0 | 2 | 4 | 3 |
| 2 | 0 | 1 | 4 | 4 |
| 2 | 0 | 0 | 4 | 5 |
| 5 | 0 | 2 | 2 | 2 |
| 5 | 0 | 1 | 2 | 3 |
| 5 | 0 | 0 | 2 | 4 |
| 10 | 0 | 1 | 2 | 2 |
| 10 | 0 | 0 | 2 | 3 |

## Table 17. ASK Receiver for 400kHz IF (continued)

| | | | | |
|---|---|---|---|---|
| 25 | 0 | 0 | 0 | 2 |
| 62.5 | 0 | 0 | 5 | 0 |

## Table 18. ASK Receiver for 200kHz IF

| DATA RATE (kbps) | IF_SEL | CHF_SEL | SRC_SM | SRC_LG |
|---|---|---|---|---|
| 0.25 | 1 | 3 | 4 | 4 |
| 0.25 | 1 | 2 | 4 | 5 |
| 0.5 | 1 | 3 | 4 | 3 |
| 0.5 | 1 | 2 | 4 | 4 |
| 0.5 | 1 | 1 | 4 | 5 |
| 1 | 1 | 3 | 4 | 2 |
| 1 | 1 | 2 | 4 | 3 |
| 1 | 1 | 1 | 4 | 4 |
| 1 | 1 | 0 | 4 | 5 |
| 2 | 1 | 2 | 4 | 2 |
| 2 | 1 | 1 | 4 | 3 |
| 2 | 1 | 0 | 4 | 4 |
| 5 | 1 | 1 | 2 | 2 |
| 5 | 1 | 0 | 2 | 3 |
| 10 | 1 | 0 | 2 | 2 |

### FSK Receiver Configurations

## Table 19. FSK Receiver for 400kHz IF

| DATA RATE (kbps) | Δf (±kHz) | IF_SEL | CHF_SEL | DMOD_FSK | SRC_SM | SRC_LG |
|---|---|---|---|---|---|---|
| 0.25 | 2 | 0 | 4 | 6 | 4 | 4 |
| 0.25 | 5 | 0 | 4 | 4 | 4 | 4 |
| 0.25 | 10 | 0 | 3 | 4 | 4 | 5 |
| 0.5 | 2 | 0 | 4 | 6 | 4 | 3 |
| 0.5 | 5 | 0 | 4 | 4 | 4 | 3 |
| 0.5 | 10 | 0 | 3 | 4 | 4 | 4 |
| 0.5 | 20 | 0 | 2 | 3 | 4 | 5 |
| 1 | 2 | 0 | 4 | 6 | 4 | 2 |
| 1 | 5 | 0 | 4 | 4 | 4 | 2 |
| 1 | 10 | 0 | 3 | 4 | 4 | 3 |
| 1 | 20 | 0 | 2 | 3 | 4 | 4 |
| 1 | 40 | 0 | 1 | 3 | 4 | 5 |
| 2 | 2 | 0 | 4 | 6 | 4 | 1 |
| 2 | 5 | 0 | 4 | 4 | 4 | 1 |
| 2 | 10 | 0 | 3 | 4 | 4 | 2 |
| 2 | 20 | 0 | 2 | 3 | 4 | 3 |
| 2 | 40 | 0 | 1 | 3 | 4 | 4 |

## Table 19. FSK Receiver for 400kHz IF (continued)

| | | | | | | |
|---|---|---|---|---|---|---|
| 2 | 80 | 0 | 0 | 0 | 4 | 5 |
| 5 | 5 | 0 | 4 | 4 | 2 | 0 |
| 5 | 10 | 0 | 3 | 4 | 2 | 1 |
| 5 | 20 | 0 | 2 | 3 | 2 | 2 |
| 5 | 40 | 0 | 1 | 3 | 2 | 3 |
| 5 | 80 | 0 | 0 | 0 | 2 | 4 |
| 10 | 10 | 0 | 3 | 4 | 2 | 0 |
| 10 | 20 | 0 | 2 | 3 | 2 | 1 |
| 10 | 40 | 0 | 1 | 3 | 2 | 2 |
| 10 | 80 | 0 | 0 | 0 | 2 | 3 |
| 25 | 20 | 0 | 2 | 3 | 0 | 0 |
| 25 | 40 | 0 | 1 | 3 | 0 | 1 |
| 25 | 80 | 0 | 0 | 0 | 0 | 2 |
| 50 | 40 | 0 | 1 | 3 | 0 | 0 |
| 50 | 80 | 0 | 0 | 0 | 0 | 1 |
| 100 | 80 | 0 | 0 | 0 | 0 | 0 |

## Table 20. FSK Receiver for 200kHz IF

| DATA RATE (kbps) | ∆f (±kHz) | IF_SEL | CHF_SEL | DMOD_FSK | SRC_SM | SRC_LG |
|---|---|---|---|---|---|---|
| 0.25 | 5 | 1 | 3 | 4 | 4 | 4 |
| 0.25 | 10 | 1 | 2 | 3 | 4 | 5 |
| 0.5 | 5 | 1 | 3 | 4 | 4 | 3 |
| 0.5 | 10 | 1 | 2 | 3 | 4 | 4 |
| 0.5 | 20 | 1 | 1 | 3 | 4 | 5 |
| 1 | 5 | 1 | 3 | 4 | 4 | 2 |
| 1 | 10 | 1 | 2 | 3 | 4 | 3 |
| 1 | 20 | 1 | 1 | 3 | 4 | 4 |
| 1 | 40 | 1 | 0 | 0 | 4 | 5 |
| 2 | 5 | 1 | 3 | 4 | 4 | 1 |
| 2 | 10 | 1 | 2 | 3 | 4 | 2 |
| 2 | 20 | 1 | 1 | 3 | 4 | 3 |
| 2 | 40 | 1 | 0 | 0 | 4 | 4 |
| 5 | 5 | 1 | 3 | 4 | 2 | 0 |
| 5 | 10 | 1 | 2 | 3 | 2 | 1 |
| 5 | 20 | 1 | 1 | 3 | 2 | 2 |
| 5 | 40 | 1 | 0 | 0 | 2 | 3 |
| 10 | 10 | 1 | 2 | 3 | 2 | 0 |
| 10 | 20 | 1 | 1 | 3 | 2 | 1 |
| 10 | 40 | 1 | 0 | 0 | 2 | 2 |
| 25 | 20 | 1 | 1 | 3 | 0 | 0 |
| 25 | 40 | 1 | 0 | 0 | 0 | 1 |

## Table 20. FSK Receiver for 200kHz IF (continued)

| | | | | | | |
|---|---|---|---|---|---|---|
| 50 | 40 | 1 | 0 | 0 | 0 | 0 |

**Modulation Index Equals Approximately 0.8**

## Table 21. FSK Receiver for 400kHz IF

| DATA RATE (kbps) | Δf (±kHz) | IF_SEL | CHF_SEL | DEMOD_FSK | SRC_SM | SRC_LG |
|---|---|---|---|---|---|---|
| 2.5 | 2 | 0 | 4 | 6 | 2 | 1 |
| 4 | 3 | 0 | 4 | 5 | 5 | 0 |
| 6 | 5 | 0 | 4 | 4 | 0 | 0 |
| 9 | 7 | 0 | 3 | 5 | 3 | 0 |
| 12 | 10 | 0 | 3 | 4 | 0 | 0 |
| 13 | 11 | 0 | 2 | 5 | 7 | 0 |
| 16 | 14 | 0 | 2 | 4 | 3 | 0 |
| 25 | 20 | 0 | 2 | 3 | 0 | 0 |
| 26 | 22 | 0 | 1 | 5 | 7 | 0 |
| 33 | 29 | 0 | 1 | 4 | 4 | 0 |
| 50 | 40 | 0 | 1 | 3 | 0 | 0 |
| 53 | 44 | 0 | 0 | 2 | 7 | 0 |
| 67 | 57 | 0 | 0 | 1 | 4 | 0 |
| 100 | 80 | 0 | 0 | 0 | 0 | 0 |

## Table 22. FSK Receiver for 200kHz IF

| DATA RATE (kbps) | Δf (±kHz) | IF_SEL | CHF_SEL | DEMOD_FSK | SRC_SM | SRC_LG |
|---|---|---|---|---|---|---|
| 1.2 | 1 | 1 | 4 | 6 | 2 | 1 |
| 1.9 | 1.5 | 1 | 4 | 5 | 5 | 0 |
| 3.1 | 2.5 | 1 | 4 | 4 | 0 | 0 |
| 4.5 | 3.5 | 1 | 3 | 5 | 3 | 0 |
| 7 | 5 | 1 | 3 | 4 | 0 | 0 |
| 7 | 6 | 1 | 2 | 5 | 7 | 0 |
| 9 | 7 | 1 | 2 | 4 | 3 | 0 |
| 12 | 10 | 1 | 2 | 3 | 0 | 0 |
| 13 | 11 | 1 | 1 | 5 | 7 | 0 |
| 16 | 14 | 1 | 1 | 4 | 4 | 0 |
| 25 | 20 | 1 | 1 | 3 | 0 | 0 |
| 26 | 22 | 1 | 0 | 2 | 7 | 0 |
| 33 | 29 | 1 | 0 | 1 | 4 | 0 |
| 50 | 40 | 1 | 0 | 0 | 0 | 0 |

### Serial Peripheral Interface (SPI)

The MAX41470 utilizes a 3-wire SPI protocol for programming its receiver registers. The digital I/Os in Table 23 control the operation of the SPI.

## Table 23. SPI Controls

| PIN | DESCRIPTION |
|---|---|
| SCLK | SPI Clock |
| SDIO | SPI Data Input/Output |
| CSB | SPI Chip-Select Bar |

Figure 5 shows the general SPI Write transaction. Figure 6 shows the 3-wire SPI Read transaction. In a read transaction, the dummy byte is required to switch the SDIO line from input mode to output mode.

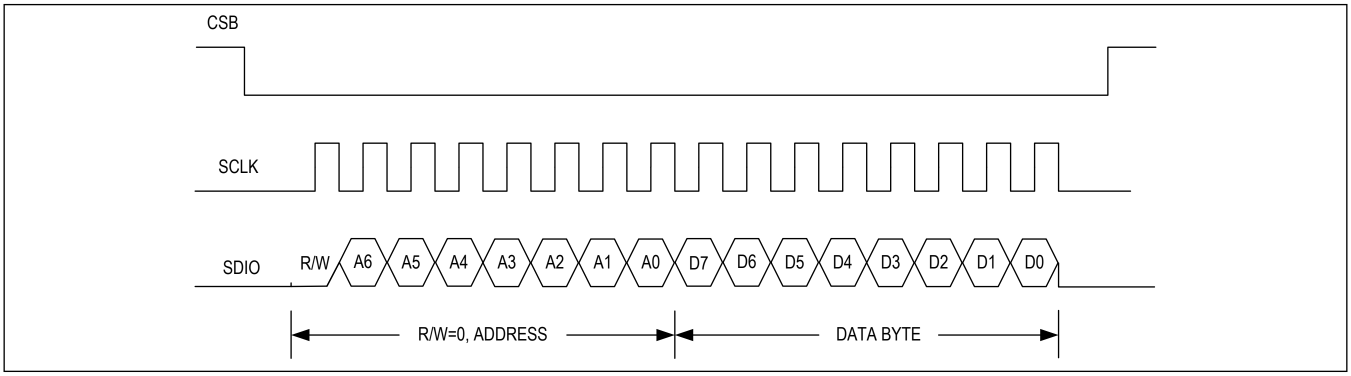


*Figure 5. 3-Wire SPI Write*

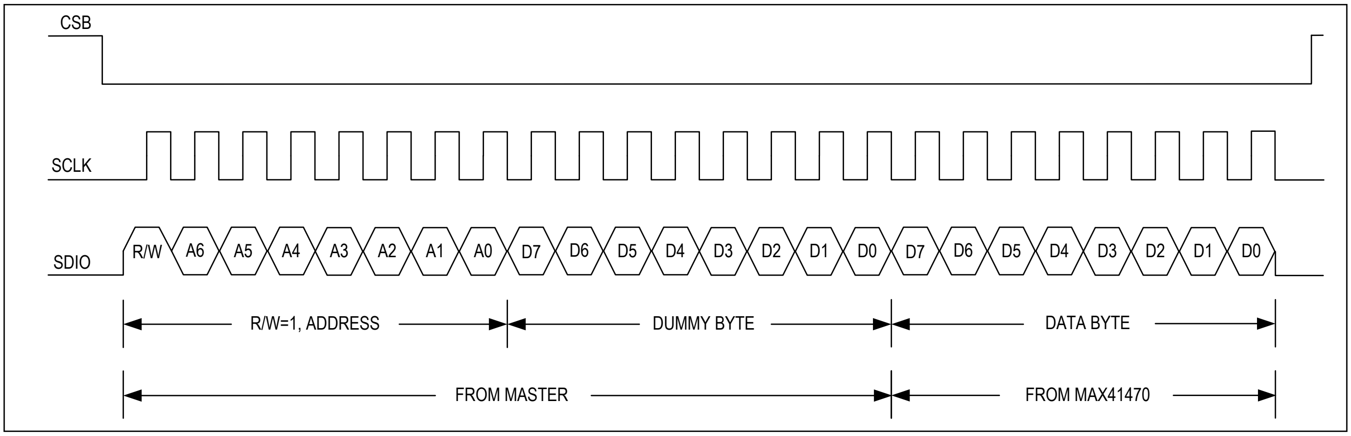


*Figure 6. 3-Wire SPI Read*

The serial interface also allows a burst write or read. Figure 7 shows the data for the sequential addresses occupying the bytes following first data byte.

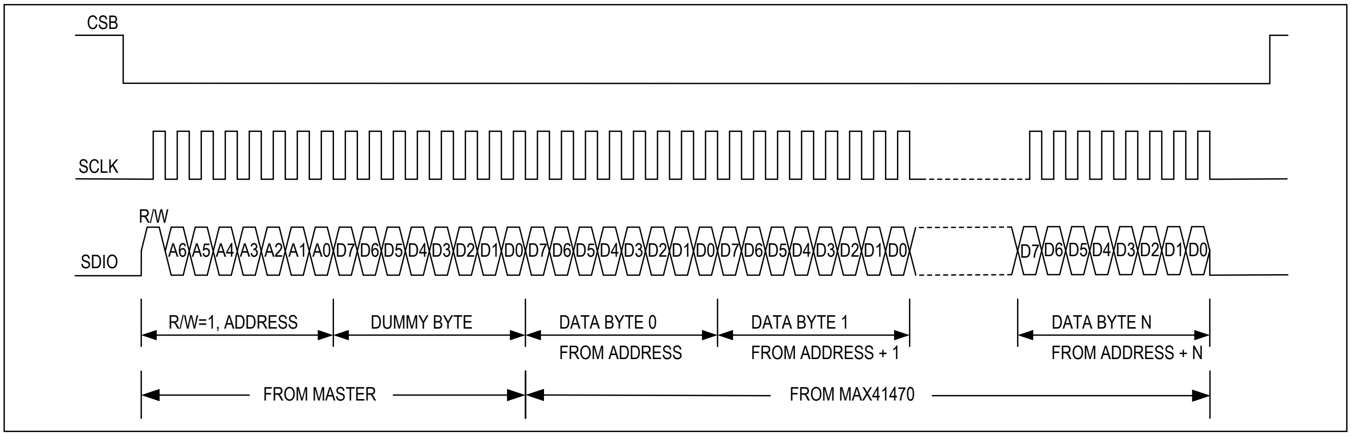


*Figure 7. 3-Wire SPI Burst Read*

## Crystal (XTAL) Oscillator

The XTAL oscillator in the MAX41470 is designed to present a capacitance of approximately 12pF from the XTAL1 and XTAL2 pins to ground. In most cases, this corresponds to a 6pF load capacitance ($C_L$) applied to the external crystal when typical PCB parasitics are included. It is very important to use a crystal with a $C_L$ equal to the capacitance of the MAX41470 crystal oscillator plus PCB parasitics. If a crystal designed to oscillate with a different $C_L$ is used, the crystal is pulled away from its specified oscillation frequency, introducing an error in the reference. The crystal's natural frequency is typically below its specified frequency. However, when loaded with the $C_L$, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the $C_L$. Accounting for typical board parasitics, a 16MHz crystal with 6pF specified $C_L$ is recommended. Please note that adding discrete capacitance on the crystal also increases the startup time, and adding too much capacitance could prevent oscillation altogether.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_P = \frac{C_M}{2}\left(\frac{1}{C_{CASE} + C_{ACTUAL}} - \frac{1}{C_{CASE} + C_L}\right) \times 10^6$$

where: $f_P$ is the amount the crystal frequency pulled in ppm, $C_M$ is the motional capacitance of the crystal (often referred to as $C_1$), $C_{CASE}$ is the case capacitance, $C_L$ is the specified load capacitance, $C_{ACTUAL}$ is the actual load capacitance. When the crystal is loaded as specified (i.e., $C_{ACTUAL} = C_L$), the frequency pulling equals zero. For additional details on crystal pulling and load capacitance affects, refer to *Maxim Tutorial 5422 – Crystal Calculations for ISM RF Products*.

### Crystal Divider

The available crystal frequencies are 12.8MHz, 16.0MHz (default), and 19.2MHz. An internal clock of 3.2MHz ± 0.05MHz frequency is required. To maintain the internal 3.2MHz time base, the XOCLKDIV[1:0] register field in the AFE_CTL1 (0x19) register byte must be programmed based on the crystal frequency, as shown in Table 24.

## Table 24. Required Crystal Divider Programming

| CRYSTAL FREQUENCY (MHz) | CRYSTAL DIVIDER RATIO | XOCLKDIV |
|---|---|---|
| 12.8 | 4 | 0 |
| 16.0 | 5 | 1* |
| 19.2 | 6 | 2 |

* Default value

## Phase-Locked Loop (PLL)

The MAX41470 utilizes a fully integrated fractional-N PLL as its frequency synthesizer. All PLL components, including the loop filter, are on-chip. The internal local oscillator (LO) frequency can be tuned in increments of $f_{XTAL}/65536$ (~244Hz with a 16MHz crystal) from 286MHz to 320MHz, 425MHz to 480MHz, and 860MHz to 960MHz.

### Frequency Programming

The desired frequency can be configured by programming the LO_CTR_FREQ[23:0] (address 0x09, 0x0A, and 0x0B). To calculate the LO_CTR_FREQ bits assuming default low-side LO injection, use the following equation:

$$\text{LO\_CTR\_FREQ}[23:0] = \text{ROUND}\left(\frac{65536(f_{RF} - f_{IF})}{f_{XTAL}}\right)$$

where $f_{IF}$ = 400kHz (IF_SEL = 0) or $f_{IF}$ = 200kHz (IF_SEL = 1), $f_{XTAL}$ is the crystal frequency (typically 16.0MHz), and $f_{RF}$ is the carrier frequency of the RF input. For FSK modulation, $f_{RF}$ is defined as the middle point between the MARK and SPACE frequencies.

For optimum sensitivity, avoid carrier frequencies ($f_{RF}$) values that are multiples of the crystal frequency ($f_{XTAL}$).

See Table 25 to program the LODIV[1:0] register field in the AFE_CTL1 (0x19) register byte when choosing a LO frequency. Always set bit FRACMODE = 1 in the AFE_CTL1 byte to select fractional-N PLL mode.

## Table 25. LODIV Setting

| FREQUENCY RANGE (MHz) | LODIV SETTING [1:0] |
|---|---|
| PLL disabled | 0 |
| 287 to 320 | 3 |
| 425 to 480 | 2 |
| 860 to 960 | 1 |

## Clock Data Recovery

In programmable mode and when SRC_LG and SRC_SM are not both equal to zero, a clock output is available on pin 11, which is recovered from the demodulated data stream. This clock assists with sampling of the DATA pin output by providing a rising edge for the user to latch the DATA signal. Optionally, the output data on the DATA pin can be re-timed internally, which reduces the pulse-width variation of the demodulated bits and thus opens the data eye. The operational mode of the clock data recovery (CDR) function is configured through the CDR_MODE[1:0] register bits in the CDR_CFG1 register (0x35). The use of these bits is shown in the following table:

## Table 26. Clock Data Recovery Operation Mode

| CDR_MODE[1:0] | OPERATIONAL MODE |
|---|---|
| 0* | No clock output, DATA not re-timed |
| 1 | Clock output, DATA not re-timed |
| 2 | No clock output, DATA re-timed |
| 3 | Clock output, DATA re-timed |

* Default programming mode

In the default case, the CDR function is disabled. When CDR_MODE = 1, the recovered clock becomes available on the CLK pin while the DATA output remains unchanged (not re-timed). When CDR_MODE = 2, there is no clock available on the pin, but it is used internally to re-time the DATA output. When CDR_MODE = 3, the recovered clock output is available on the CLK pin and the DATA output is re-timed.

The recovered clock is twice the frequency of the data rate of the received data. For example, a 2kbps received data stream results in a 4kHz recovered clock where the rising edge of each clock is centered on each DATA output bit.

## Power Supply

For operation with a single 1.8V to 3.6V supply, connect a power supply to $V_{DD}$. For proper operation, connect a 0.01µF capacitor from $V_{DD}$ to ground as close as possible to the pin.

## Low-Noise Amplifier (LNA)

The LNA is a broadband gain block that increases the amplitude of a signal received from the antenna. The input of the LNA presents a 50Ω real impedance to the antenna and does not require any matching components. The use of a DC-blocking cap (100pF) is recommended in series with the input to prevent overvoltage conditions if the antenna can be subjected to an external DC voltage.

## Mixer

The mixer is a double-balanced architecture that performs a downconversion of the RF signal to the 400kHz or 200kHz intermediate frequency. The mixer output drives an IF filter and, depending on the value of the MIX_HS_LSBAR bit in the AFE_CTL1 (0x19) register, the LO frequency can be either lower (low-side injection) or higher (high-side injection) than the RF signal.

In normal receiver operation, it is recommended to use low-side injection, thus placing the target RF signal frequency higher than the LO frequency by programming the MIX_HS_LSBAR bit to 0 (default value). The MIX_HS_LSBAR bit can be set to 1 during image rejection (IR) calibration.

## Receiver Latency

Some applications require a low latency or short demodulation time delay of the receiver. For those applications, the LD_BW and LD_BUF bits in the PDF_CFG (0x03) register can be programmed to non-default settings.

### Table 27. Programming of LD_BW and LD_BUF

| CONDITIONS | SETTINGS | | EFFECT |
|---|---|---|---|
| | LD_BW | LD_BUF | |
| All cases | 0 | 0 | Default latency |
| | 1 | 0 | Lower delay PDF |
| (SRC_LG ≥ 3) or<br>(SRC_LG = 2 AND SRC_SM is even) | 1 | 1 | Lowest delay |

The case of LF_BW = 0 and LD_BUF = 1 is reserved. One of the Table 27 combinations above should be configured.

The setting of LD_BW = 1 increases the bandwidth of the receiver and hence reduces the group delay of the PDF at a cost of 0.5dB sensitivity degradation. Also see Table 12.

A lowest-delay buffer is selected when LD_BUF = 1, but this setting is invalid when SRC_LG is set to 1 or 0. Lowest-delay buffer is also invalid when SRC_LG = 2 and SRC_SM is odd.

For example, the data rate is 1.4kbps after Manchester encoding, and the device is configured to IF_SEL = 1, CHF_SEL = 0, SRC_LG = 5, and SRC_SM = 1. The receiver latency from LNA input to DATA output can be reduced from 380µs (default settings) to 200µs (lowest delay settings) by setting LD_BD and LD_BUF to 1.

## NRZ Format

To use a non-return-to-zero (NRZ) data stream with ASK modulation, program ATH_TYPE = 1, ATH_DT = 3, and ATH_TC as noted in Table 13. The length of consecutive 1's (ON) or 0's (OFF) should not exceed 16 bits.

With FSK modulation, the setting of AFC_LG = 0 may be used to support NRZ modulation while avoiding any more than 10 consecutive MARK or SPACE bits. AFC settling requires roughly 100 symbols when AFC_LG = 0, thus this setting is recommended only for cases requiring long data streams at relatively high data rates (e.g., ≥100kbps NRZ).

When using FSK modulation and NRZ encoding in the payload, see the recommended *AFC Freeze upon Preamble Detection* section.

## Image Rejection Calibration

For applications where image rejection is important, the user can calibrate the MAX41470 for improved image rejection. The following procedure can be executed in the user's factory. Throughout the process, the device will be switched between Standby for programming of the IR_ADJUST register in 0x1A and SlaveRX for the active state when the RSSI value is read. The idea of the calibration is to find the minimum point of the RSSI value while sweeping the phase. Based on the increase or decrease of the RSSI values indicates whether the sweep will increase from 0x00 or increase from 0x11. To calibrate the image rejection, use the following procedure:

1. Program the MAX41470 for the desired frequency.
2. Apply an RF tone at the LNA input at the desired frequency and record the RSSI value.
3. Disable the SLAVE_RX_EN bit in register 0x14.
4. Program the MIX_HS_LSBAR bit (register 0x19, bit 3) to the opposite polarity.
    a. This effectively turns the desired frequency into the image frequency.
5. Set the SLAVE_RX_EN bit to enable SlaveRX mode and record the RSSI value.
6. Reset the SLAVE_RX_EN bit to disable SlaveRX mode and program register 0x1A to 0x01.
7. Set the SLAVE_RX_EN bit to enable SlaveRX mode and record the RSSI value.
8. Based on the RSSI values:
    a. If RSSI decreased, image rejection improved. Continue increasing 0x1A from the value of 0x01.
    b. If RSSI increased, image rejection degraded. Continue increasing 0x1A from the value of 0x11.
9. Set the SLAVE_RX_EN bit to enable SlaveRX mode and record the RSSI value
    a. Note: If the RSSI value was higher at 0x01 and 0x11 than 0x00, then the best calibration code is 0x00 - procedure complete.
10. Reset the SLAVE_RX_EN bit to disable SlaveRX mode and increase register 0x1A by 1.
11. Set the SLAVE_RX_EN bit to enable SlaveRX mode and record the RSSI value.
12. If the RSSI went down, continue to increase the register value one code at a time, repeating steps 10 and 11 until there is an increase in the RSSI.
13. When there is an increase in RSSI, subtract 1 from register 0x1A as the final code - procedure complete.

The final code for register 0x1A must be saved in the MCU. It must be programmed each time the MAX41470 enters Standby state.

## Register Map

### Memory Map

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| **DIG_RX** | | | | | | | | | |
| 0x00 | DEMOD[7:0] | RSSI_DT[1:0] | | DEMOD_FSK[2:0] | | | DEMOD_TCTRL[2:0] | | |
| 0x01 | AGC[7:0] | – | – | AGC_THREL[3:0] | | | | AGC_EN_BO[1:0] | |
| 0x02 | IF_CHF_SEL[7:0] | – | – | – | ASK_FSK_SEL | IF_SEL | CHF_SEL[2:0] | | |
| 0x03 | PDF_CFG[7:0] | LD_BUF | LD_BW | SRC_LG[2:0] | | | SRC_SM[2:0] | | |
| 0x04 | ATH_CFG1[7:0] | ATH_LB[7:0] | | | | | | | |
| 0x05 | ATH_CFG2[7:0] | – | ATH_DT[1:0] | | ATH_TC[4:0] | | | | |
| 0x06 | ATH_CFG3[7:0] | – | ATH_TYPE | ATH_BW | ATH_GC[4:0] | | | | |
| 0x07 | AFC_CFG1[7:0] | – | – | – | AFC_MO[2:0] | | | AFC_LG[1:0] | |
| 0x08 | AFC_CFG2[7:0] | – | PAD_FREEZE_AFC | RESERVED[5:0] | | | | | |
| 0x09 | LO_CTR_FREQ3[7:0] | LO_CTR_FREQ[23:16] | | | | | | | |
| 0x0A | LO_CTR_FREQ2[7:0] | LO_CTR_FREQ[15:8] | | | | | | | |
| 0x0B | LO_CTR_FREQ1[7:0] | LO_CTR_FREQ[7:0] | | | | | | | |
| 0x0C | PREAMBLE_CFG1[7:0] | – | – | – | – | PREAMB_LEN[3:0] | | | |
| 0x0D | PREAMBLE_WORD1[7:0] | PREAMB_WORD[7:0] | | | | | | | |
| 0x0E | PREAMBLE_WORD2[7:0] | PREAMB_WORD[15:8] | | | | | | | |
| 0x10 | RSSI[7:0] | RSSI[7:0] | | | | | | | |
| 0x11 | FEI[7:0] | FEI[7:0] | | | | | | | |
| 0x12 | PDF_OUT[7:0] | PDF_OUT[7:0] | | | | | | | |
| 0x13 | ISR[7:0] | – | – | – | – | – | – | – | PREAMB_DET |
| 0x35 | CDR_CFG1[7:0] | – | – | – | – | – | – | CDR_MODE[1:0] | |
| OVERLAP | | | | | | | | | |
| **STATE_CTRL** | | | | | | | | | |
| 0x14 | STATE_CTRL1[7:0] | – | – | – | – | – | EN_XO | WUT_EN | SLAVE_RX_EN |
| 0x15 | STATE_CTRL2[7:0] | – | – | – | – | – | – | RX_STATE[1:0] | |
| 0x16 | STATE_CTRL3[7:0] | – | – | – | – | – | – | RX_RESET_TIME[1:0] | |
| 0x17 | WUT1[7:0] | TDET[7:0] | | | | | | | |
| 0x18 | WUT2[7:0] | – | TSBY_TDET_RATIO[6:0] | | | | | | |
| **ANALOG_FE** | | | | | | | | | |
| 0x19 | AFE_CTL1[7:0] | XOCLKDELAY[1:0] | | XOCLKDIV[1:0] | | MIX_HS_LSBAR | LODIV[1:0] | | FRACMODE |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 0x1A | IR_ADJUST[7:0] | – | – | – | IR_ADJUST[4:0] | | | | |
| 0x1E | PART_NUM[7:0] | PART_NUM[7:0] | | | | | | | |
| 0x1F | REV_NUM[7:0] | – | – | – | – | – | REV_NUM[2:0] | | |
| 0x27 | STATUS[7:0] | – | – | – | – | – | – | RESERVED | PLL_LOCK |

## Register Details

### DEMOD (0x00)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RSSI_DT[1:0] | | DEMOD_FSK[2:0] | | | DEMOD_TCTRL[2:0] | | |
| **Reset** | 0x1 | | 0x0 | | | 0x4 | | |
| **Access Type** | Write, Read | | Write, Read | | | Write, Read | | |

<table>
<tr><th>BITFIELD</th><th>BITS</th><th>DESCRIPTION</th><th>DECODE</th></tr>
<tr><td>RSSI_DT</td><td>7:6</td><td>RSSI Peak Detector Discharge Time</td><td>0x0: 1/2 default value<br>0x1: default value<br>0x2: 2x default value<br>0x3: 4x default value</td></tr>
<tr><td>DEMOD_FSK</td><td>5:3</td><td>Demodulator Parameter #2 to be used only in FSK mode. Must be programmed according to the table of FSK Demodulator Configuration.</td><td>0x0: FSK Demod Config Index = 0, 14<br>0x1: FSK Demod Config Index = 1, 15<br>0x2: FSK Demod Config Index = 2, 16<br>0x3: FSK Demod Config Index = 3, 6, 17, 20<br>0x4: FSK Demod Config Index = 4, 7, 9, 11, 18, 21, 23, 25<br>0x5: FSK Demod Config Index = 5, 8, 10, 12, 19, 22, 24, 26<br>0x6: FSK Demod Config Index = 13, 27<br>0x7: Invalid value</td></tr>
<tr><td>DEMOD_TCTRL</td><td>2:0</td><td>Demodulator Parameter #1
<table>
<tr><th>Conditions</th><th>Recommended Value</th></tr>
<tr><td>ASK_FSK_SEL=1</td><td>4 - CHF_SEL</td></tr>
<tr><td>ASK_FSK_SEL=0, ATH_TYPE=0</td><td>min(2+SRC_LG, 7)</td></tr>
<tr><td>ASK_FSK_SEL=0, ATH_TYPE=1</td><td>min(3+SRC_LG,7)</td></tr>
</table></td><td>0x0: 1/16 Default<br>0x1: 1/8 Default<br>0x2: 1/4 Default<br>0x3: 1/2 Default<br>0x4: Default value<br>0x5: 2x Default<br>0x6: 4x Default<br>0x7: 8x Default</td></tr>
</table>

### AGC (0x01)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | AGC_THREL[3:0] | | | | AGC_EN_BO[1:0] | |
| **Reset** | – | – | 0x9 | | | | 0x2 | |
| **Access Type** | – | – | Write, Read | | | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| AGC_THREL | 5:2 | AGC-Release Threshold Fine Tune. Recommended value is 0x9 when data rate is lower than 52kbps, or 0xF when data rate is higher than 52kbps. | |
| AGC_EN_BO | 1:0 | AGC Operation Mode | 0x0: AGC disabled, max gain<br>0x1: AGC disabled, back off ADC buffer<br>0x2: AGC enabled<br>0x3: AGC enabled, back off ADC buffer |

## IF_CHF_SEL (0x02)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | ASK_FSK_SEL | IF_SEL | CHF_SEL[2:0] | | |
| **Reset** | – | – | – | 0x0 | 0x0 | 0x0 | | |
| **Access Type** | – | – | – | Write, Read | Write, Read | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| ASK_FSK_SEL | 4 | ASK/FSK Selection | 0x0: ASK demodulation<br>0x1: FSK demodulation |
| IF_SEL | 3 | Intermediate Frequency Selection | 0x0: 400kHz<br>0x1: 200kHz |
| CHF_SEL | 2:0 | Channel Filter Selection | 0x0: RXBW = 340kHz or 170kHz<br>0x1: RXBW = 120kHz or 60kHz<br>0x2: RXBW = 52kHz or 26kHz<br>0x3: RXBW = 24kHz or 12kHz<br>0x4: RXBW = 12kHz or 6kHz<br>0x5: Invalid value<br>0x6: Invalid value<br>0x7: Invalid value |

## PDF_CFG (0x03)

Post Demodulation Filter

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | LD_BUF | LD_BW | SRC_LG[2:0] | | | SRC_SM[2:0] | | |
| **Reset** | 0x0 | 0x0 | 0x2 | | | 0x0 | | |
| **Access Type** | Write, Read | Write, Read | Write, Read | | | Write, Read | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| LD_BUF | 7 | Output Buffer Selection. Low delay buffer can only be selected when (SRC_LG ≥ 3) or (SRC_LG = 2 and SRC_SM is even). | 0x0: Default selection<br>0x1: Low delay buffer |
| LD_BW | 6 | Post Demodulation Filter Bandwidth Control | 0x0: Default BW<br>0x1: 1.67x Default BW |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| SRC_LG | 5:3 | "Large" adjustment to the Sample Rate Converter used to calculate the recommended data rate | See Configuration Guidance Tables and Recommended Data Rate Equation<br>0x0: 4x Default<br>0x1: 2x Default<br>0x2: Default rate<br>0x3: 1/2 Default<br>0x4: 1/4 Default<br>0x5: 1/8 Default<br>0x6: 1/16 Default<br>0x7: 1/32 Default |
| SRC_SM | 2:0 | "Small" adjustment to the Sample Rate Converter used to calculate the recommended data rate | See Configuration Guidance Tables and Recommended Data Rate Equation<br>0x0: Default rate<br>0x1: 8/9 Default<br>0x2: 8/10 Default<br>0x3: 8/11 Default<br>0x4: 8/12 Default<br>0x5: 8/13 Default<br>0x6: 8/14 Default<br>0x7: 8/15 Default |

### ATH_CFG1 (0x04)

ASK Threshold Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ATH_LB[7:0] | | | | | | | |
| **Reset** | 0x0 | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| ATH_LB | 7:0 | Parameter #1 for ASK Threshold Generation: lower bound of threshold in 8-bit signed, two's complement format | Valid value from -128 to 0 |

### ATH_CFG2 (0x05)

ASK Threshold Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | ATH_DT[1:0] | | ATH_TC[4:0] | | | | |
| **Reset** | – | 0x0 | | 0x10 | | | | |
| **Access Type** | – | Write, Read | | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| ATH_DT | 6:5 | Parameter #4 for ASK Threshold Generation: peak-hold time control in the "adaptive Peak Detector" (aPD) method | 0x0: Default discharge time, suggested for Manchester data, close to Rb<br>0x1: 2x Discharge time, suggested for Manchester data, lower than Rb<br>0x2: 4x Discharge time<br>0x3: 8x Discharge time, suggested for NRZ data |
| ATH_TC | 4:0 | Parameter #2 for ASK Threshold Generation: to be programmed according to SRC_LG | See Table 13 for guidance |

## ATH_CFG3 (0x06)

ASK Threshold Configuration

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | ATH_TYPE | ATH_BW | ATH_GC[4:0] | | | | |
| **Reset** | – | 0x0 | 0x0 | 0xF | | | | |
| **Access Type** | – | Write, Read | Write, Read | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| ATH_TYPE | 6 | ASK Threshold Adjustment Method | 0x0: Precharged lowpass filter (preLPF) (Manchester)<br>0x1: Adaptive peak detector (aPD)(NRZ) |
| ATH_BW | 5 | Parameter #5 for ASK Threshold Generation: bandwidth control for precharged LPF (preLPF) | 0x0: Default bandwidth<br>0x1: 2x default |
| ATH_GC | 4:0 | Parameter #3 for ASK Threshold Generation: to be programmed according to IF_SEL and CHF_SEL | See Table 14 for guidance |

## AFC_CFG1 (0x07)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | AFC_MO[2:0] | | | AFC_LG[1:0] | |
| **Reset** | – | – | – | 0x0 | | | 0x2 | |
| **Access Type** | – | – | – | Write, Read | | | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| AFC_MO | 4:2 | AFC Frequency Offset Limit | 0x0: AFC disabled<br>0x1: 1/7 Max offset<br>0x2: 2/7 Max offset<br>0x3: 3/7 Max offset<br>0x4: 4/7 Max offset<br>0x5: 5/7 Max offset<br>0x6: 6/7 Max offset<br>0x7: Max offset |
| AFC_LG | 1:0 | AFC Loop Gain Control | 0x0: 1/4 Default<br>0x1: 1/2 Default<br>0x2: Default gain, FSK typical setting<br>0x3: 2x Default, ASK typical setting |

## AFC_CFG2 (0x08)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | PAD_FREEZE_AFC | RESERVED[5:0] | | | | | |
| **Reset** | – | 0x0 | 0x0 | | | | | |
| **Access Type** | – | Write, Read | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| PAD_FREEZE_AFC | 6 | Control bit to Freeze AFC after Preamble Detected. Not used in ASK mode. | 0x0: Not to freeze AFC<br>0x1: Freeze AFC (stop PLL frequency update) once preamble is detected |
| RESERVED | 5:0 | Reserved | Set to 0 |

## LO_CTR_FREQ3 (0x09)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | LO_CTR_FREQ[23:16] | | | | | | | |
| **Reset** | 0x13 | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| LO_CTR_FREQ | 7:0 | LO Center Frequency, upper byte of 24-bit word |

## LO_CTR_FREQ2 (0x0A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | LO_CTR_FREQ[15:8] | | | | | | | |
| **Reset** | 0xA9 | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| LO_CTR_FREQ | 7:0 | LO Center Frequency, middle byte of 24-bit word |

## LO_CTR_FREQ1 (0x0B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | LO_CTR_FREQ[7:0] | | | | | | | |
| **Reset** | 0x9A | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| LO_CTR_FREQ | 7:0 | LO Center Frequency, lower byte of 24-bit word |

## PREAMBLE_CFG1 (0x0C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | PREAMB_LEN[3:0] | | | |
| **Reset** | – | – | – | – | 0xF | | | |
| **Access Type** | – | – | – | – | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| PREAMB_LEN | 3:0 | Preamble Bit Pattern Length before Manchester Coding | Bit Pattern Length = Register Field Value +1 |

## PREAMBLE_WORD1 (0x0D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | PREAMB_WORD[7:0] | | | | | | | |
| **Reset** | 0x0 | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| PREAMB_WORD | 7:0 | Lower Byte of the Preamble Bit Pattern before Manchester Coding |

## PREAMBLE_WORD2 (0x0E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | PREAMB_WORD[15:8] | | | | | | | |
| **Reset** | 0x0 | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| PREAMB_WORD | 7:0 | Upper Byte of the Preamble Bit Pattern before Manchester Coding |

## RSSI (0x10)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RSSI[7:0] | | | | | | | |
| **Reset** | 0x0 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RSSI | 7:0 | Received Signal Strength Indicator (RSSI) | 8-bit unsigned integer |

## FEI (0x11)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | FEI[7:0] | | | | | | | |
| **Reset** | 0x0 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| FEI | 7:0 | AFC Frequency Error Indicator (FEI) | 8-bit signed integer in two's complement format |

## PDF_OUT (0x12)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | PDF_OUT[7:0] | | | | | | | |
| **Reset** | 0x0 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| PDF_OUT | 7:0 | Post Demodulation Filter (PDF) Read Out | 8-bit signed integer in two's complement format |

## ISR (0x13)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | – | PREAMB_DET |
| **Reset** | – | – | – | – | – | – | – | 0b0 |
| **Access Type** | – | – | – | – | – | – | – | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| PREAMB_DET | 0 | Interrupt Status Register Bit 0: preamble detector in self-polling mode | 0x0: No interrupt event<br>0x1: Preamble detected in self-polling |

## CDR_CFG1 (0x35)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | CDR_MODE[1:0] | |
| **Reset** | – | – | – | – | – | – | 0x00 | |
| **Access Type** | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| CDR_MODE | 1:0 | | 0x0: CDR disabled<br>0x1: Clock out enabled, DATAOUT untimed<br>0x2: Clock out disabled, DATAOUT retimed<br>0x3: Clock out enabled, DATAOUT retimed |

## STATE_CTRL1 (0x14)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | EN_XO | WUT_EN | SLAVE_RX_EN |
| **Reset** | – | – | – | – | – | 0x0 | 0x0 | 0x0 |
| **Access Type** | – | – | – | – | – | Write, Read | Write, Read, Dual | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| EN_XO | 2 | XO Enable Bit | 0x0: Disable XO<br>0x1: Enable XO |
| WUT_EN | 1 | Wake-Up Timer (WUT) Enable Bit | 0x0: Disable WUT<br>0x1: Enable WUT |
| SLAVE_RX_EN | 0 | Slave Receiver Enable Bit | 0x0: Disable receiver<br>0x1: Enable receiver |

## STATE_CTRL2 (0x15)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | RX_STATE[1:0] | |
| **Reset** | – | – | – | – | – | – | | |
| **Access Type** | – | – | – | – | – | – | Read Only | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RX_STATE | 1:0 | Receiver State Machine Register | 0x0: Standby<br>0x1: Slave receiver<br>0x2: Wait in self-polling<br>0x3: Polling receiver |

## STATE_CTRL3 (0x16)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | RX_RESET_TIME[1:0] | |
| **Reset** | – | – | – | – | – | – | 0x03 | |
| **Access Type** | – | – | – | – | – | – | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RX_RESET_TIME | 1:0 | Receiver Front-End Turn-On Time | 0x0: 0.08ms<br>0x1: 0.16ms<br>0x2: 0.24ms<br>0x3: 0.32ms |

## WUT1 (0x17)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | TDET[7:0] | | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| TDET | 7:0 | Duration in POLLINGRX State: from 0.48ms to 20.88ms, in step size of 0.08ms | Duration (ms) = 0.48 + 0.08 x (Register Field Value) |

## WUT2 (0x18)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | TSBY_TDET_RATIO[6:0] | | | | | | |
| **Reset** | – | | | | | | | |
| **Access Type** | – | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| TSBY_TDET_RATIO | 6:0 | WUT Duty Cycle Control | Duty Cycle = 1 / (2 + Register Field Value) |

## AFE_CTL1 (0x19)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | XOCLKDELAY[1:0] | | XOCLKDIV[1:0] | | MIX_HS_LSBAR | LODIV[1:0] | | FRACMODE |
| **Reset** | 0x2 | | 0x1 | | 0x0 | 0x01 | | 0x1 |
| **Access Type** | Write, Read | | Write, Read | | Write, Read | Write, Read | | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| XOCLKDELAY | 7:6 | Start Delay before Applying XO Clock to Digital | 0x0: No delay<br>0x1: 16 cycle delay<br>0x2: 32 cycle delay<br>0x3: 64 cycle delay |
| XOCLKDIV | 5:4 | XO Clock Divider Ratio | 0x0: Divide by 4<br>0x1: Divide by 5<br>0x2: Divide by 6<br>0x3: Invalid value |
| MIX_HS_LSBAR | 3 | LO Injection Control | 0x0: Targeted RF frequency higher than LO frequency<br>0x1: Targeted RF frequency lower than LO frequency |
| LODIV | 2:1 | LO Divider Control | 0x0: PLL disabled<br>0x1: 860MHz to 960MHz<br>0x2: 425MHz to 480MHz<br>0x3: 286MHz to 320MHz |
| FRACMODE | 0 | PLL Mode Control: always program to 1 | 0x0: Integer-N PLL<br>0x1: Fractional-N PLL |

## IR_ADJUST (0x1A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | IR_ADJUST[4:0] | | | | |
| **Reset** | – | – | – | 0x00 | | | | |
| **Access Type** | – | – | – | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| IR_ADJUST | 4:0 | Image Rejection Adjustment. See the Image Rejection Calibration section for more information. |

## PART_NUM (0x1E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | PART_NUM[7:0] | | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| PART_NUM | 7:0 | Part Number Designator.<br>Read of part number requires EN_XO = 1 | 0x70 = MAX41470<br>0x73 = MAX41473<br>0x74 = MAX41474 |

## REV_NUM (0x1F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | REV_NUM[2:0] | | |
| **Reset** | – | – | – | – | – | | | |
| **Access Type** | – | – | – | – | – | Read Only | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| REV_NUM | 2:0 | Revision Number of Chip |

## STATUS (0x27)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | RESERVED | PLL_LOCK |
| **Reset** | – | – | – | – | – | – | 0x0 | 0x0 |
| **Access Type** | – | – | – | – | – | – | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RESERVED | 1 | Reserved | Reserved |
| PLL_LOCK | 0 | PLL Lock Status | 0x0: PLL is not locked<br>0x1: PLL is locked |

## Applications Information

### Programming Quick Start

The suggested procedure for operating the device is outlined below.

1) Power on the device with the PWRDN pin controlled by an external MCU. Drive PWRDN to logic-high and wait for at least 1ms, then drive PWRDN to logic-low and wait for at least 0.4ms.

2) Write 0x04 to the STATE_CTRL1 (0x14) register. This will turn on the crystal oscillator and place the device into Standby.

3) Select a quick start configuration of the DIG_RX register bank from Table 28, and write the 16 defined registers from address 0x00-0x0E and 0x19. The configurations provided within the Quick Start Configurations table and other examples assume a crystal frequency of 16MHz and the use of a Manchester-encoded RF signal unless otherwise noted.

4) Setup a modulated RF signal source at the data rate matching the selected Quick Start Configuration.

5) Write 0x05 to the STATE_CTRL1 (0x14) register. This will turn on the receiver and place the device into the SlaveRX state.

6) Turn on the modulated RF signal and observe the DATA pin output.

7) Write 0x00 to the STATE_CTRL1 (0x14) register. This will turn off the receiver and place the device into Sleep.

## Table 28. Quick Start Configurations

| MOD | RF CARRIER (MHz) | Δf (kHz) | DATA RATE (kbps) | SETTINGS (kHz) | | REGISTER ADDRESS 0x00 to 0x0E | REG ADD 0x19 |
|---|---|---|---|---|---|---|---|
| | | | | IF_SEL | CHF_SEL | | |
| ASK | 315 | N/A | 2 | 200 | 170 | [70,38,8,36,167,9,10,31,0,19,172,205,15,0,0] dec | 151 dec |
| | | | | | | [0x46,0x26,0x08,0x24,0xA7,0x09,0x0A,0x1F,0x00,0x13,0xAC,0xCD,0x0F,0x00,0x00] hex | 0x97 hex |
| | | | 1 | 200 | 12 | [68,38,11,20,145,16,5,31,0,19,172,205,15,0,0] dec | 151 dec |
| | | | | | | [0x44,0x26,0x0B,0x14,0x91,0x10,0x05,0x1F,0x00,0x13,0xAC,0xCD,0x0F,0x00,0x00,0x00] hex | 0x97 hex |
| | 433.92 | | 5 | 200 | 170 | [69,38,8,26,170,13,10,31,0,27,27,133,15,0,0] dec | 149 dec |
| | | | | | | [0x45,0x26,0x08,0x1A,0xAA,0x0D,0x0A,0x1F,0x00,0x1B,0x1B,0x85,0x0F,0x00,0x00] hex | 0x95 hex |
| | | | 1 | 200 | 12 | [68,38,11,20,145,16,5,31,0,27,27,133,15,0,0] dec | 149 dec |
| | | | | | | [0x44,0x26,0x0B,0x14,0x91,0x10,0x05,0x1F,0x00,0x1B,0x1B,0x85,0x0F,0x00,0x00] hex | 0x95 hex |
| | 868.3 | | 10 | 400 | 340 | [69,38,0,26,179,13,11,31,0,54,62,102,15,0,0] dec | 147 dec |
| | | | | | | [0x45,0x26,0x00,0x1A,0xB3,0x0D,0x0B,0x1F,0x00,0x36,0x3E,0x66,0x0F,0x00,0x00] hex | 0x93 hex |
| | | | 2 | 400 | 24 | [68,38,3,20,153,16,7,31,0,54,62,102,15,0,0] dec | 147 dec |
| | | | | | | [0x44,0x26,0x03,0x14,0x99,0x10,0x07,0x1F,0x00,0x36,0x3E,0x66,0x0F,0x00,0x00] hex | 0x93 hex |
| FSK | 315 | 40 | 2 | 200 | 170 | [68,38,24,36,0,0,0,30,0,19,172,205,15,0,0] dec | 151 dec |
| | | | | | | [0x44,0x26,0x18,0x24,0x00,0x00,0x00,0x1E,0x00,0x13,0xAC,0xCD,0x0F,0x00,0x00] hex | 0x97 hex |
| | | 5 | 2 | 200 | 12 | [97,38,27,12,0,0,0,30,0,19,172,205,15,0,0] dec | 151 dec |
| | | | | | | [0x61,0x26,0x1B,0x0C,0x00,0x00,0x00,0x1E,0x00,0x13,0xAC,0xCD,0x0F,0x00,0x00] hex | 0x97 hex |

### Table 28. Quick Start Configurations (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | 433.92 | 40 | 5 | 200 | 170 | [68,38,24,26,0,0,0,30,0,27,27,133,15,0,0] dec | 149 dec |
| | | | | | | [0x44,0x26,0x18,0x1A,0x00,0x00,0x00,0x1E, 0x00,0x1B,0x1B,0x85,0x0F,0x00,0x00] hex | 0x95 hex |
| | | 5 | 5 | 200 | 12 | [97,38,27,2,0,0,0,30,0,27,27,133,15,0,0] dec | 149 dec |
| | | | | | | [0x61,0x26,0x1B,0x02,0x00,0x00,0x00,0x1E, 0x00,0x1B,0x1B,0x85,0x0F,0x00,0x00] hex | 0x95 hex |
| | 868.3 | 40 | 50 | 200 | 170 | [68,38,24,0,0,0,0,30,0,54,65,154,15,0,0] dec | 147 dec |
| | | | | | | [0x44,0x26,0x18,0x00,0x00,0x00,0x00,0x1E, 0x00,0x36,0x41,0x9A,0x0F,0x00,0x00] hex | 0x93 hex |
| | | 5 | 5 | 200 | 12 | [97,38,27,2,0,0,0,30,0,54,65,154,15,0,0] dec | 147 dec |
| | | | | | | [0x61,0x26,0x1B,0x02,0x00,0x00,0x00,0x1E, 0x00,0x36,0x41,0x9A,0x0F,0x00,0x00] hex | 0x93 hex |
| | | 80 | 100 | 400 | 340 | [68,62,16,0,0,0,0,30,0,54,62,102,15,0,0] dec | 147 dec |
| | | | | | | [0x44,0x3E,0x10,0x00,0x00,0x00,0x00,0x1E, 0x00,0x36,0x3E,0x66,0x0F,0x00,0x00] hex | 0x93 hex |
| | | 10 | 10 | 400 | 24 | [97,38,19,2,0,0,0,30,0,54,62,102,15,0,0] dec | 147 dec |
| | | | | | | [0x61,0x26,0x13,0x02,0x00,0x00,0x00,0x1E, 0x00,0x36,0x3E,0x66,0x0F,0x00,0x00] hex | 0x93 hex |

## Programming Guide

The following sections provide a variety of setups and some guidance in the required device configuration for each. All example configurations assume the crystal frequency to be 16MHz and Manchester coding, unless otherwise indicated.

### Best ASK Receiver Sensitivity without Calibration

For this setup, the input signal should be Manchester encoded at a data rate close to the recommended bit rate ($R_b$). Keep ATH_TYPE = 0 (default value) to select the precharged lowpass filter (preLPF) method for ASK decision threshold generation.

For simplicity, program ATH_LB = -127 regardless of the selection of IF_SEL and CHF_SEL. The ASK decision threshold is generated from lowpass filter averaging. The ASK receiver settling time can be as long as 12 bits when the expected signal power is same as receiver sensitivity.

For example, assume an ASK signal at 5kbps centered at 433.92MHz where the 170kHz receiver bandwidth option is selected (IF_SEL = 1, CHF_SEL = 0). The programming to match this configuration would result in the DIG_RX register bank (15 consecutive bytes from address 0x00) as decimal [69, 38, 8, 26, 129, 13, 10, 31, 0, 27, 27, 133, 15, 0, 0] or hexidecimal [0x45, 0x26, 0x08, 0x1A, 0x81, 0x0D, 0x0A, 0x1F, 0x00, 0x1B, 0x1B, 0x85, 0x0F, 0x00, 0x00]. In addition, write decimal value 149 or hexidecimal 0x95 to AFE_CTL1 (0x19). Here, the decimal value of LO_CTR_FREQ is 1776517, calculated from $f_{XTAL}$ = 16MHz, $f_{RF}$ = 433.92MHz, and $f_{IF}$ = 200kHz. In addition, in the ATH_LB (0x04) byte, the unsigned 8-bit value of 129 represents a signed 8-bit value of -127 as noted above. For this configuration, the receiver sensitivity might be approximately -115dBm.

If the receiver settling time is a concern, then the ATH_LB can be modified to accommodate a faster time. According to Table 15 and Table 16, the MU1+MU2 value is -80. In order to get nearly optimum sensitivity as well as fast receiver settling, ATH_LB can be programmed to MU1+MU2 - 6, or a value of -86 in this example (equivalent to a decimal value of 170 or hexadecimal value of 0xAA).

### Frequency Acquisition

The AFC can only support a limited adjustment of the LO frequency away from the center frequency given by LO_CTR_FREQ × $\frac{f_{XTAL}}{2^{16}}$. The maximum range of adjustment, referred to as an AFC pull-in range, is

$\frac{\pm \text{AFC\_MO} \times f_{XTAL}}{2^{(\text{IF\_SEL} + \text{CHF\_SEL} + 10)}} = \frac{\pm 7 \times f_{XTAL}}{2^{(\text{IF\_SEL} + \text{CHF\_SEL} + 10)}}$. The actual range of adjustment is programmable from 0 to the pull-in range by setting AFC_MO between 0 and 7. In this section, all examples assume $f_{XTAL}$ = 16MHz.

## Table 29. AFC Pull-In Range (for 16MHz Crystals)

| IF_SEL | CHF_SEL | AFC PULL-IN RANGE (kHz) | RECEIVER BANDWIDTH (kHz) |
|---|---|---|---|
| 0 | 0 | ±109 | 340 |
| 0 | 1 | ±55 | 120 |
| 0 | 2 | ±27 | 52 |
| 0 | 3 | ±14 | 24 |
| 0 | 4 | ±6.8 | 12 |
| 1 | 0 | ±55 | 170 |
| 1 | 1 | ±27 | 60 |
| 1 | 2 | ±14 | 26 |
| 1 | 3 | ±6.8 | 12 |
| 1 | 4 | ±3.4 | 6 |

The initial value of Tx/Rx frequency mismatch can exceed the AFC pull-in range for a narrow-bandwidth configuration. For example, a 100ppm mismatch at 434MHz is ±43.4kHz, which exceeds the AFC pull-in range when (IF_SEL + CHF_SEL) ≥ 2. To address the limited pull-in range issue, we can employ software-aided frequency acquisition.

The LO_CTR_FREQ can be adjusted to correct for the mismatch. This can be done by modifying the frequency until a data packet is successfully recognized. However, the FEI can also be utilized to determine the magnitude and direction of offset. To program different center frequencies, the device must be taken out of active SlaveRX mode by programming the SLAVE_RX_EN to zero prior to reconfiguration of the LO_CTR_FREQ register. Then the device can be programmed to enter the SlaveRX state again.

### Frequency Acquisition Example #1

In this setup, the expected signal is ASK at a 433.92MHz nominal frequency at 5kbps and the 60kHz bandwidth option (IF_SEL = 1 and CHF_SEL = 1).

Observation 1: Program the DIG_RX register bank (15 consecutive bytes from address 0x00) as decimal [68, 38, 9, 18, 162, 16, 7, 31, 0, 27, 27, 133, 15, 0, 0] or hexadecimal [0x44, 0x26, 0x09, 0x12, 0xA2, 0x10, 0x07, 0x1F, 0x00, 0x1B, 0x1B, 0x85, 0x0F, 0x00, 0x00]. In addition, write decimal value 149 or hexadecimal 0x95 to AFE_CTL1 (0x19). Here, the decimal value of LO_CTR_FREQ is 1776517, calculated from $f_{XTAL}$ = 16MHz, $f_{RF}$ = 433.92MHz, and $f_{IF}$=200kHz. When initial Tx/Rx frequency mismatch is less than the AFC pull-in range of ±27kHz, a typical receiver sensitivity of -116dBm can be achieved.

Observation 2: This has the same receiver configuration as Observation 1, but the initial Tx/Rx mismatch increases to ±43.4kHz. In this case, the receiver sensitivity degrades to -112dBm, and the frequency error indicator (FEI) reading saturates at ±112 (decimal value).

Observation 3: Adjust the LO_CTR_FREQ to account for the offset; otherwise, it has the same receiver configuration as Observation 1. Run the receiver with the three bytes of LO_CTR_FREQ programmed to decimal [27, 27, 43] and [27, 27, 223] or hexadecimal [0x1B, 0x1B, 0x2B] and [0x1B, 0x1B, 0xDF]. The typical -116dBm sensitivity can be achieved in at least one case of the receiver running, even if the initial Tx/Rx mismatch is as high as ±43.4kHz.

### Frequency Acquisition Example #2

In this example, the signal is FSK at a 868.3MHz nominal frequency at 10kbps and the 24kHz bandwidth option (IF_SEL = 0 and CHF_SEL = 3). The FSK deviation is at ±8kHz.

Assume that the Tx/Rx frequency mismatch is unknown, but could be as high as ±86.8kHz. In this case, test the receiver running at seven equally spaced frequency points with 24.8kHz spacing. For this setup, the seven LO_CTR_FREQ values would be decimal [3555223, 3555122, 3555020, 3554918, 3554817, 3554715, 3554614].

Assuming the starting point of LO_CTR_FREQ = 3554918, the DIG_RX register bank is programmed as decimal [97, 38, 19, 2, 0, 0, 0, 30, 0, 54, 62, 102, 15, 0, 0] or hexadecimal [0x61, 0x26, 0x13, 0x02, 0x00, 0x00, 0x1E, 0x00, 0x36, 0x3E, 0x66, 0x0F, 0x00, 0x00]. In addition, write decimal value 147 or hexadecimal 0x93 to AFE_CTL1 (0x19). To change LO_CTR_FREQ, exit the SlaveRX state into Standby, write three consecutive addresses from address 0x09, and re-enter the SlaveRX state.

The MCU should be able to recognize a data packet on the DATA pin at one of the seven frequency points. A typical receiver sensitivity of -115dBm should be seen.

### Frequency Acquisition Example #3

For this setup, the ASK signal at 433.92MHz nominal frequency is at 1kbps and configured with the 170kHz bandwidth option (IF_SEL = 1, CHF_SEL = 0). Program the DIG_RX register bank (15 consecutive bytes from address 0x00) as decimal [71, 38, 8, 44, 165, 7, 10, 31, 0, 27, 27, 133, 15, 0, 0] or hexadecimal [0x47, 0x26, 0x08, 0x2C, 0xA5, 0x07, 0x0A, 0x1F, 0x00, 0x1B, 0x1B, 0x85, 0x0F, 0x00, 0x00]. In addition, write decimal value 149 or hexadecimal 0x95 to AFE_CTL1 (0x19). When initial Tx/Rx frequency mismatch is less than ±43.4kHz, typical receiver sensitivity of -118dBm can be achieved. In this example, the frequency mismatch can be determined to ±3kHz accuracy by reading the FEI (0x11) byte.

The next step is to correct the frequency mismatch by reprogramming LO_CTR_FREQ. Increase (or decrease) LO_CTR_FREQ if the FEI reading is positive (or negative). For example, if the FEI reading is -93, then decrease the LO_CTR_FREQ value by 186 counts in this example. In addition, a narrow bandwidth option such as IF_SEL = 1 and CHF_SEL = 3 can be selected to improve sensitivity to approximately -122dBm.

### Frequency Tracking

Once frequency acquisition is achieved, the MCU can read FEI and reprogram LO_CTR_FREQ to track the drift of Tx/Rx frequency mismatch. Such frequency tracking is useful when a narrow bandwidth option is selected.

The frequency offset generated by AFC is expressed as:

$$\mathrm{FEI} \times \frac{f_{\mathrm{XTAL}}}{2^{(\mathrm{IF\_SEL} + \mathrm{CHF\_SEL} + 14)}}$$

where FEI is an integer in the range of [-112, 112]. The MCU can read FEI right after a data packet is recognized in the SlaveRX state, but cannot modify LO_CTR_FREQ unless SLAVE_RX_EN is cleared to move the device state to Standby. Because the resolution of the LO synthesizer is $f_{\mathrm{XTAL}} / 2^{16}$, the MCU can make an incremental change of $\mathrm{FEI} \times \frac{4}{2^{(\mathrm{IF\_SEL} + \mathrm{CHF\_SEL})}}$ on the LO_CTR_FREQ counts.

### Self-Polling Example

In this example, a 1% polling setup is defined. The configuration is set up for ASK at 433.92MHz at a 2kbps data rate, 200kHz IF, and 170kHz CHF. The preamble length (PREAM_LEN[3:0] in the PREAMBLE_CFG1 register at 0x0C) is set to 15 for a final preamble length of 16 bits.

To accommodate the targeted 1% polling cycle, the TSBY_TDET_RATIO[6:0] bits should be set to 0x62 for a value of 98, resulting in a duty cycle of 1/(2 + TSBY_TDET_RATIO) = 1/100 or 1%. For proper detection of the 16-bit preamble, the guaranteed length targeted is calculated as:

$$16 + 16 - 1 = 31 \text{ bits required}$$

$$31 \text{ bits} \times \frac{1}{\text{datarate}} = 31 \times \frac{1}{2\text{kbps}} = 15.5\text{ms}$$

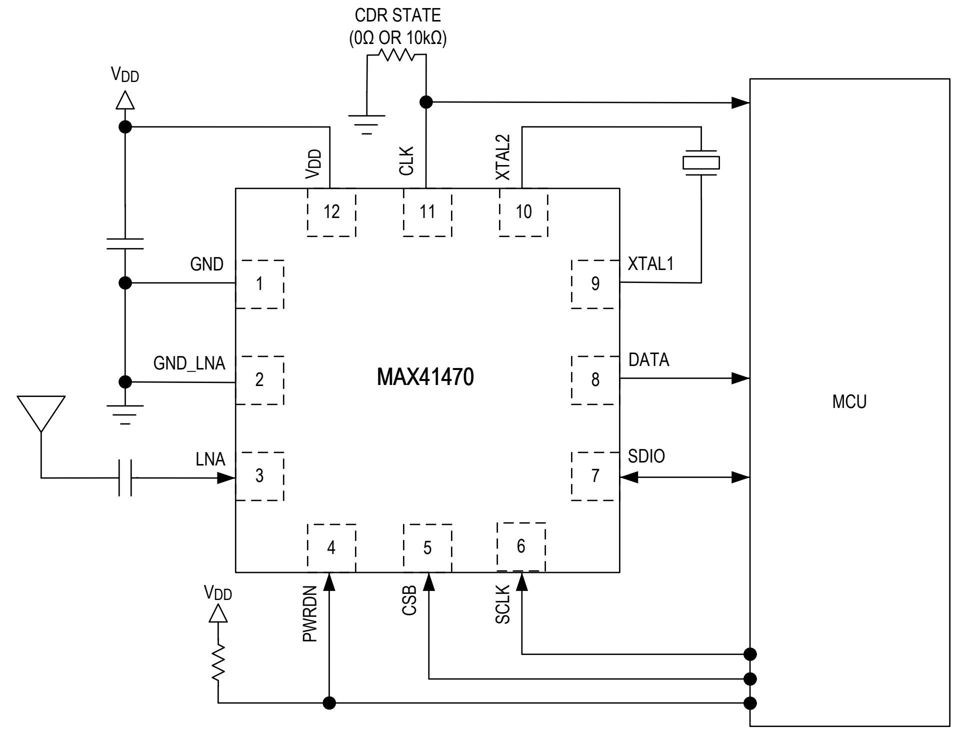
To meet this requirement, the WUT1 (0x17) register bits TDET[7:0] should be set to exceed this duration. Therefore, with WUT1 at 0xBC or 188, the resulting wait duration is:

$$0.48\text{ms} + (t_{\mathrm{DET}} \times 0.08\text{ms}) = 0.48 + (188 \times 0.08) = 15.52\text{ms}$$

This duration exceeds the 15.5ms requirement. To match a Manchester 0x0000 (alternating 1's and 0's), the PREAMBLE_WORD1 and PREAMBLE_WORD2 is each set to 0x00. For this configuration, write the 15 consecutive bytes from address 0x00 as decimal [70, 38, 8, 36, 167, 9, 10, 31, 0, 27, 27, 133, 15, 0, 0] or hexadecimal [0x46, 0x26, 0x08, 0x24, 0xA7, 0x09, 0x0A, 0x1F, 0x00, 0x1B, 0x1B, 0x85, 0x0F, 0x00, 0x00]. In addition, write decimal values of [188, 98, 149] or hexadecimal [0x23, 0x62, 0x95] to registers 0x17, 0x18, and 0x19, respectively.

This full configuration results in a PollingRX time of 15.52ms and a wait time of 1.552s.

## Typical Application Circuit



## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX41470GTC+ | -40°C to +105°C | 12 TQFN |
| MAX41470GTC+T | -40°C to +105°C | 12 TQFN |

*+ Denotes a lead(Pb)-free/RoHS-compliant package*

*T Denotes tape-and-reel*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/20 | Initial release | — |
| 1 | 9/20 | Modified Benefits and Features, Pin Description, State Diagram including Table 2, Programming Quick Start and Typical Application Circuit sections | 1, 13-15, 44, 48 |