

# MAX44250/MAX44251/ MAX44252

## 20V, Ultra-Precision, Low-Noise Op Amps

### General Description

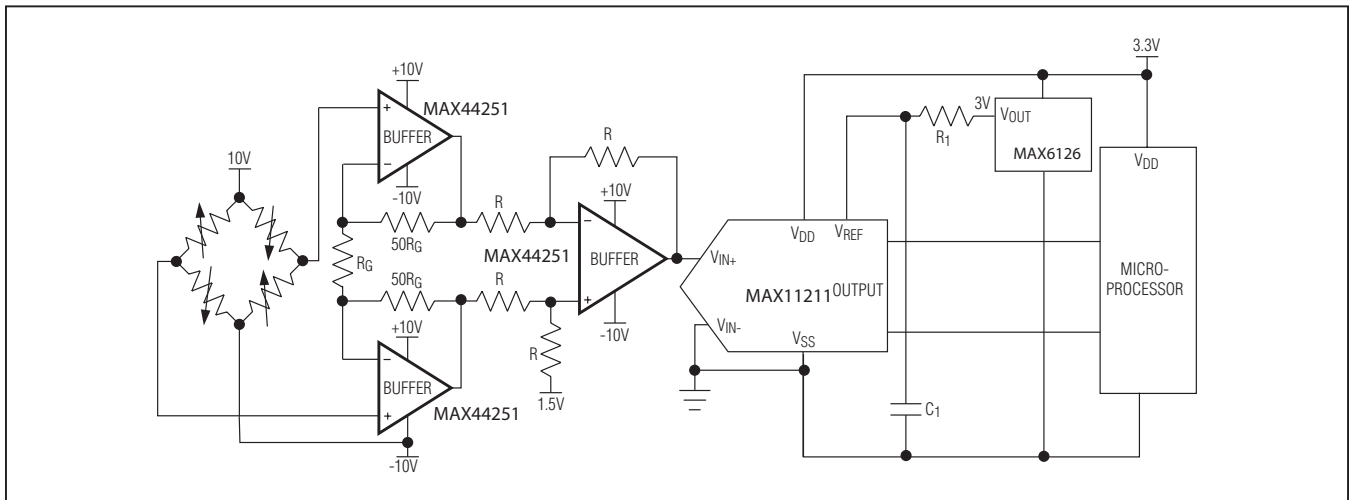
The MAX44250/MAX44251/MAX44252 are 20V, ultra-precision, low-noise, low-drift amplifiers that offer near-zero DC offset and drift through the use of patented auto-correlating zeroing techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of  $1/f$  noise. These single, dual, and quad devices feature rail-to-rail outputs, operate from a single 2.7V to 20V supply or dual  $\pm 1.35V$  to  $\pm 10V$  supplies and consume only 1.15mA per channel, while providing  $5.9nV/\sqrt{Hz}$  input-referred voltage noise. The ICs are unity-gain stable with a gain-bandwidth product of 10MHz.

With excellent specifications such as offset voltage of  $6\mu V$  (max), drift of  $19nV/^\circ C$  (max), and  $123nV_{P-P}$  noise in 0.1Hz to 10Hz, the ICs are ideally suited for applications requiring ultra-low noise and DC precision such as interfacing with pressure sensors, strain gauges, precision weight scales, and medical instrumentation.

The ICs are available in 5-pin SOT23, 8-pin SOT23, 8-pin  $\mu MAX$ <sup>®</sup>, and 14-pin SO packages and are rated over the  $-40^\circ C$  to  $+125^\circ C$  temperature range.

**Ordering Information** appears at end of data sheet.

### Typical Operating Circuit



$\mu MAX$  is a registered trademark of Maxim Integrated Products, Inc.

### Benefits and Features

- High Accuracy Enables Precision Signal Chain Acquisition
  - $6\mu V$  Input Offset Voltage (max) at Room Temperature
  - $TCV_{OS}$  of  $19nV/^\circ C$  (max)
  - Low  $5.9nV/\sqrt{Hz}$  Input-Referred Voltage Noise
  - $123nV_{P-P}$  in 0.1Hz to 10Hz
  - 10MHz Gain-Bandwidth Product
  - Rail-to-Rail Output
  - Fast 400ns Settling Time
- 2.7V to 20V Power-Supply Range Supports Wide Range of Sensors
- Integrated EMI Filter Reduces Impact of Radio Frequency Interference on Signal Chain Performance

### Applications

- Strain Gauges
- Pressure Transducers
- Medical Instrumentation
- Precision Instrumentation
- Load Cell and Bridge Transducer Amplification

**Functional Diagrams** appear at end of data sheet.

### Absolute Maximum Ratings

Supply Voltage ( $V_{DD}$ to $V_{SS}$ ).....	-0.3V to +22V	$\mu$ MAX (derate 4.5 mW/°C above +70°C) .....	362mW
All Other Pins.....	( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ )	SO (derate 8.3 mW/°C above +70°C).....	666.7mW
Short-Circuit Duration to Either Supply Rail .....	1s	Operating Temperature Range .....	-40°C to +125°C
Continuous Input Current (any pin).....	$\pm 20$ mA	Junction Temperature .....	+150°C
Differential Input Voltage.....	$\pm 6$ V	Storage Temperature Range.....	-65°C to +150°C
Maximum Power Dissipation ( $T_A = +70^\circ\text{C}$ )		Lead Temperature (soldering, 10s) .....	+300°C
5-Pin SOT23 (derate 3.1mW/°C above +70°C).....	246.7mW	Soldering Temperature (reflow) .....	+260°C
8-Pin SOT23 (derate 9.1mW/°C above +70°C).....	727mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Package Thermal Characteristics (Note 1)

5-Pin SOT23		$\mu$ MAX	
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) ....	324.3°C/W	Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....	221°C/W
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ).....	82°C/W	Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....	42°C/W
8-Pin SOT23		SO	
Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....	196°C/W	Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....	120°C/W
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ).....	70°C/W	Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....	37°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### Electrical Characteristics

( $V_{DD} = 10V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>POWER SUPPLY</b>							
Supply Voltage Range	$V_{DD}$	Guaranteed by PSRR	2.7		20	V	
Power-Supply Rejection Ratio (Note 3)	PSRR	$V_{DD} = 2.7V$ to $20V$ , $V_{CM} = 0V$	140	145		dB	
Quiescent Current per Amplifier (MAX44250)	$I_{DD}$	$R_L = \infty$	$T_A = +25^\circ\text{C}$		1.22	1.7	mA
			$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			1.85	
Quiescent Current per Amplifier (MAX44251/MAX44252)	$I_{DD}$	$R_L = \infty$	$T_A = +25^\circ\text{C}$		1.15	1.55	mA
			$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			1.75	
Power-Up Time	$t_{ON}$			25		$\mu$ s	
<b>DC SPECIFICATIONS</b>							
Input Common-Mode Range	$V_{CM}$	Guaranteed by CMRR test	$V_{SS} - 0.05$		$V_{DD} - 1.5$	V	
Common-Mode Rejection Ratio (Note 3)	CMRR	$T_A = +25^\circ\text{C}$ , $V_{CM} = -0.05V$ to ( $V_{DD} - 1.5V$ ) $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	133	140		dB	
			130				
Input Offset Voltage (MAX44250) (Note 3)	$V_{OS}$	$T_A = +25^\circ\text{C}$		3	9	$\mu$ V	

**Electrical Characteristics (continued)**

( $V_{DD} = 10V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (MAX44251/ MAX44252)(Note 3)	$V_{OS}$	$T_A = +25^\circ C$			3	6	$\mu V$
		$-40^\circ C < T_A < +125^\circ C$				7	
Input Offset Voltage Drift (MAX44250) (Note 3)	TC $V_{OS}$				5	26	nV/ $^\circ C$
Input Offset Voltage Drift (MAX44251/MAX44252)(Note 3)	TC $V_{OS}$				5	19	nV/ $^\circ C$
Input Bias Current (MAX44250) (Note 3)	$I_B$	$T_A = +25^\circ C$			200	1400	$\mu A$
Input Bias Current (MAX44251/ MAX44252)(Note 3)	$I_B$	$T_A = +25^\circ C$			200	1300	$\mu A$
		$-40^\circ C < T_A < +125^\circ C$				2400	
Input Offset Current (Note 3)	$I_{OS}$				400		$\mu A$
Open-Loop Gain (Note 3)	$A_{VOL}$	$250mV \leq V_{OUT} \leq V_{DD} - 250mV$ , $R_L = 10k\Omega$ to $V_{DD}/2$	$T_A = +25^\circ C$	145	154		dB
			$-40^\circ C < T_A < +125^\circ C$	136			
Output Short-Circuit Current		To $V_{DD}$ or $V_{SS}$	Noncontinuous		96		mA
Output Voltage Low (MAX44250)	$V_{OL}$	$V_{OUT} - V_{SS}$	$R_L = 10k\Omega$ to $V_{DD}/2$		12	26	mV
			$R_L = 2k\Omega$ to $V_{DD}/2$		45	92	
Output Voltage Low (MAX44251/MAX44252)	$V_{OL}$	$V_{OUT} - V_{SS}$	$R_L = 10k\Omega$ to $V_{DD}/2$		12	25	mV
			$R_L = 2k\Omega$ to $V_{DD}/2$		45	85	
Output Voltage High (MAX44250)	$V_{OH}$	$V_{DD} - V_{OUT}$	$R_L = 10k\Omega$ to $V_{DD}/2$		18	40	mV
			$R_L = 2k\Omega$ to $V_{DD}/2$		71	148	
Output Voltage High (MAX44251/MAX44252)	$V_{OH}$	$V_{DD} - V_{OUT}$	$R_L = 10k\Omega$ to $V_{DD}/2$		18	37	mV
			$R_L = 2k\Omega$ to $V_{DD}/2$		71	135	
<b>AC SPECIFICATIONS</b>							
Input Voltage-Noise Density	$e_N$	$f = 1kHz$			5.9		nV/ $\sqrt{Hz}$
Input Voltage Noise		$0.1Hz < f < 10Hz$			123		nV <sub>p-p</sub>
Input Current-Noise Density	$i_N$	$f = 1kHz$			0.6		pA/ $\sqrt{Hz}$
Input Capacitance	$C_{IN}$				2		pF
Gain-Bandwidth Product	GBW				10		MHz
Phase Margin	PM	$C_L = 20pF$			60		Degrees
Slew Rate	SR	$A_V = 1V/V$ , $V_{OUT} = 2V_{p-p}$			8		V/ $\mu s$
Capacitive Loading	$C_L$	No sustained oscillation, $A_V = 1V/V$			500		pF
Total Harmonic Distortion	THD	$V_{OUT} = 2V_{p-p}$ , $A_V = +1V/V$ , $R_L = 10k\Omega$ to $V_{DD}/2$	$f = 1kHz$		-124		dB
			$f = 20kHz$		-119		
Settling Time		To 0.01%, $V_{OUT} = 2V$ step, $A_V = -1V/V$			400		ns

MAX44250/MAX44251/  
MAX44252

20V, Ultra-Precision, Low-Noise Op Amps

Electrical Characteristics

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>							
Quiescent Current Per Amplifier (MAX44250)	$I_{DD}$	$R_L = \infty$	$T_A = +25^\circ C$	1.17	1.65		mA
			$-40^\circ C < T_A < +125^\circ C$			1.80	
Quiescent Current Per Amplifier (MAX44251/MAX44252)	$I_{DD}$	$R_L = \infty$	$T_A = +25^\circ C$	1.1	1.5		mA
			$-40^\circ C < T_A < +125^\circ C$			1.65	
Power-Up Time	$t_{ON}$			25			$\mu s$
<b>DC SPECIFICATIONS</b>							
Input Common-Mode Range	$V_{CM}$	Guaranteed by CMRR test		$V_{SS} - 0.05$		$V_{DD} - 1.5$	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$T_A = +25^\circ C$ , $V_{CM} = -0.05V$ to $(V_{DD} - 1.5V)$		120	129		dB
		$-40^\circ C < T_A < +125^\circ C$		117			
Input Offset Voltage (MAX44250)(Note 3)	$V_{OS}$				3	8.5	$\mu V$
Input Offset Voltage (MAX44251/MAX44252)(Note 3)	$V_{OS}$	$T_A = +25^\circ C$			3	5.5	$\mu V$
		$-40^\circ C < T_A < +125^\circ C$				6.5	
Input Offset Voltage Drift (MAX44250)(Note 3)	TC $V_{OS}$				8	25	nV/ $^\circ C$
Input Offset Voltage Drift (MAX44251/MAX44252)(Note 3)	TC $V_{OS}$				8	18	nV/ $^\circ C$
Input Bias Current (MAX44250)(Note 3)	$I_B$				200	1450	pA
Input Bias Current (MAX44251/MAX44252)(Note 3)	$I_B$	$T_A = +25^\circ C$			200	1100	pA
		$-40^\circ C < T_A < +125^\circ C$				1200	
Input Offset Current (Note 3)	$I_{OS}$				400		pA
Open-Loop Gain (Note 3)	$A_{VOL}$	$250mV \leq V_{OUT} \leq V_{DD} - 250mV$ , $R_L = 10k\Omega$ to $V_{DD}/2$	$T_A = +25^\circ C$	136	151		dB
			$-40^\circ C < T_A < +125^\circ C$	133			
Output Short-Circuit Current		To $V_{DD}$ or $V_{SS}$	Noncontinuous		58		mA
Output Voltage Low (MAX44250)	$V_{OL}$	$V_{OUT} - V_{SS}$	$R_L = 10k\Omega$ to $V_{DD}/2$		5	26	mV
			$R_L = 2k\Omega$ to $V_{DD}/2$		17	46	
Output Voltage Low (MAX44251/MAX44252)	$V_{OL}$	$V_{OUT} - V_{SS}$	$R_L = 10k\Omega$ to $V_{DD}/2$		5	22	mV
			$R_L = 2k\Omega$ to $V_{DD}/2$		17	42	
Output Voltage High	$V_{OH}$	$V_{DD} - V_{OUT}$	$R_L = 10k\Omega$ to $V_{DD}/2$		9	22	mV
			$R_L = 2k\Omega$ to $V_{DD}/2$		29	52	

### Electrical Characteristics (continued)

( $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$ ,  $V_{IN+} = V_{IN-} = V_{DD}/2$ ,  $R_L = 10k\Omega$  to  $V_{DD}/2$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

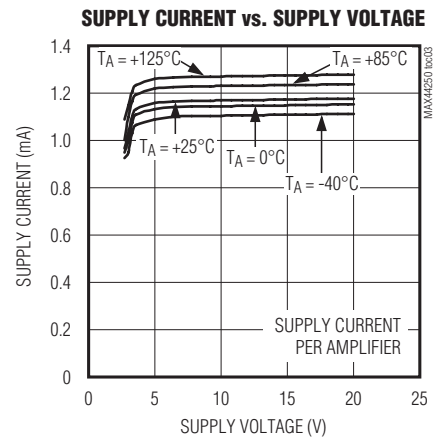
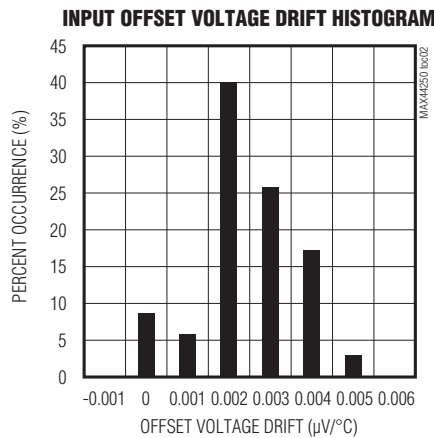
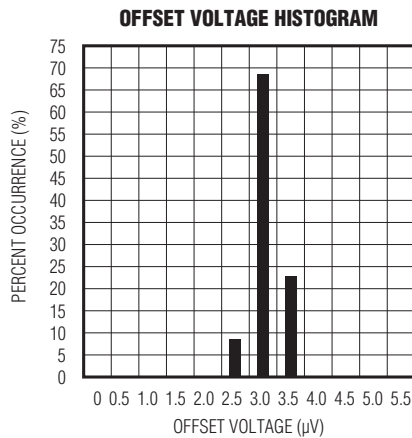
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC SPECIFICATIONS</b>						
Input Voltage-Noise Density	$e_N$	$f = 1kHz$		6.2		$nV/\sqrt{Hz}$
Input Voltage Noise		$0.1Hz < f < 10Hz$		123		$nV_{p-p}$
Input Current-Noise Density	$i_N$	$f = 1kHz$		0.3		$pA/\sqrt{Hz}$
Input Capacitance	$C_{IN}$			2		pF
Gain-Bandwidth Product	GBW			10		MHz
Phase Margin	PM	$C_L = 20pF$		60		Degrees
Slew Rate	SR	$A_V = 1V/V$ , $V_{OUT} = 1V_{P-P}$ , 10% to 90%		5		$V/\mu s$
Capacitive Loading	$C_L$	No sustained oscillation, $A_V = 1V/V$		500		pF
Total Harmonic Distortion	THD	$V_{OUT} = 1V_{P-P}$ , $A_V = +1V/V$ , $V_{CM} = V_{DD}/4$ , $R_L = 10k\Omega$ to $V_{DD}/2$	$f = 1kHz$		-124	dB
			$f = 20kHz$		-100	
Settling Time		To 0.01%, $V_{OUT} = 1V$ step, $A_V = -1V/V$		200		ns

**Note 2:** All devices are 100% production tested at  $T_A = +25^\circ C$ . Temperature limits are guaranteed by design.

**Note 3:** Guaranteed by design.

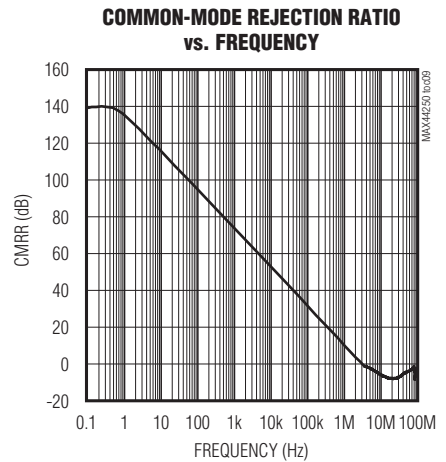
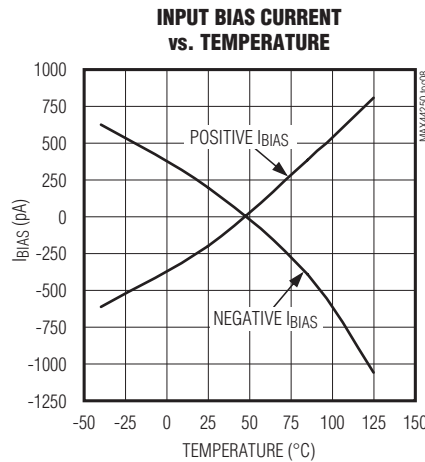
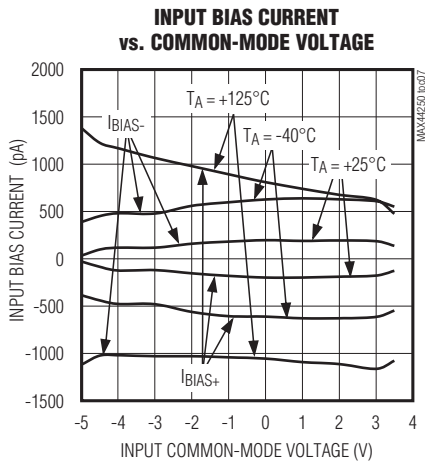
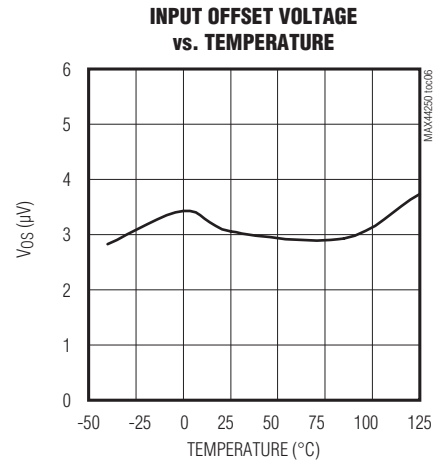
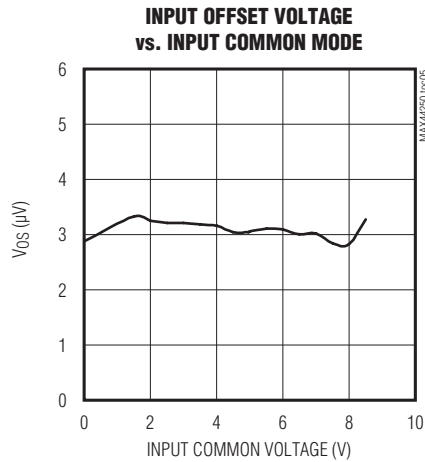
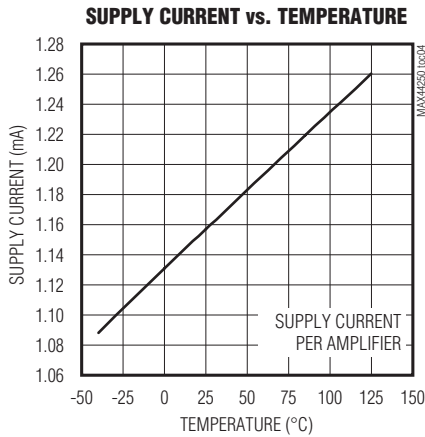
### Typical Operating Characteristics

( $V_{DD} = 10V$ ,  $V_{SS} = 0V$ , outputs have  $R_L = 10k\Omega$  to  $V_{DD}/2$ .  $T_A = +25^\circ C$ , unless otherwise specified.)



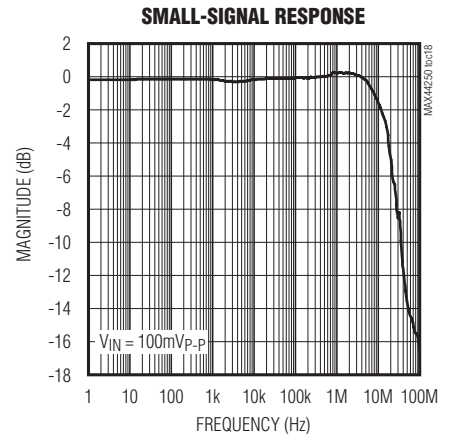
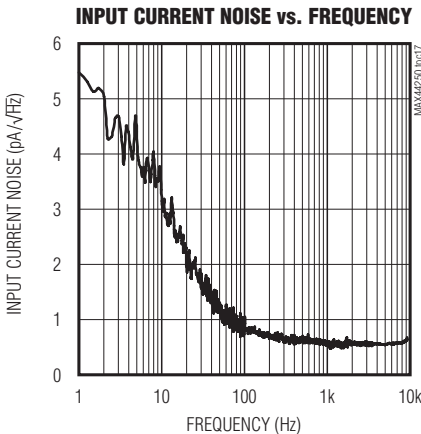
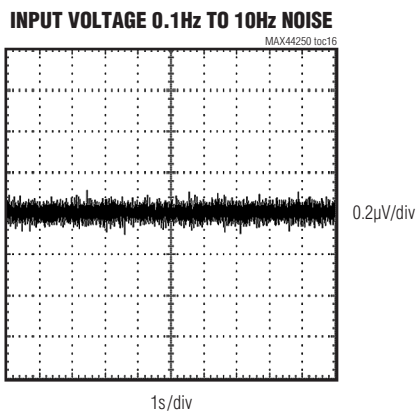
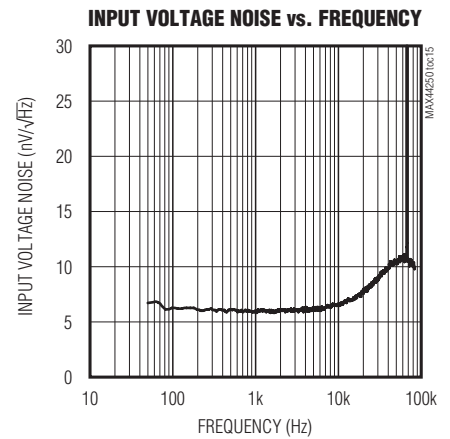
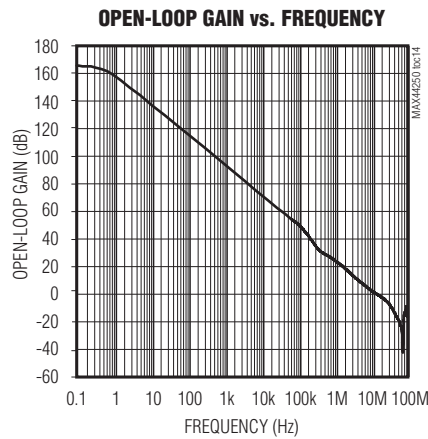
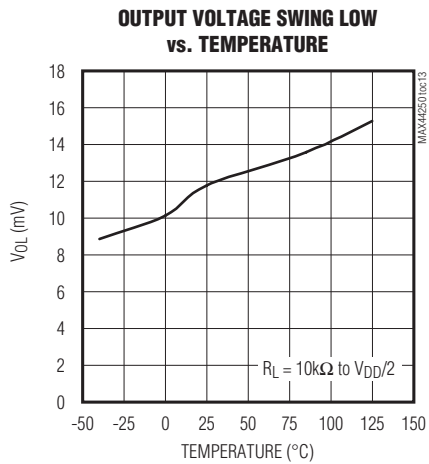
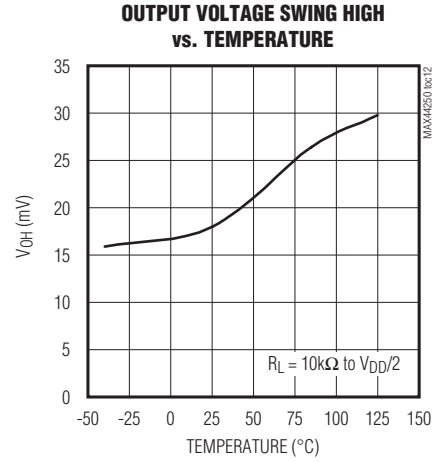
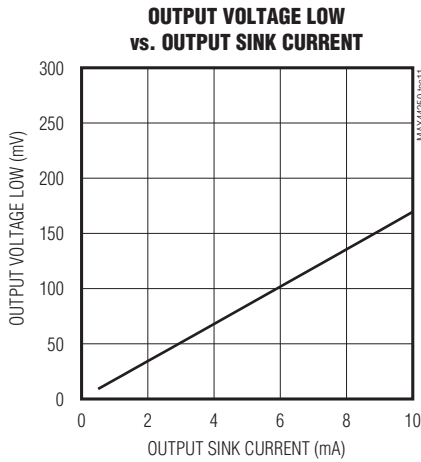
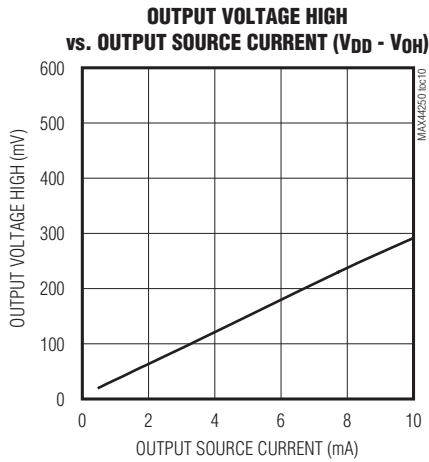
Typical Operating Characteristics (continued)

( $V_{DD} = 10V$ ,  $V_{SS} = 0V$ , outputs have  $R_L = 10k\Omega$  to  $V_{DD}/2$ .  $T_A = +25^\circ C$ , unless otherwise specified.)



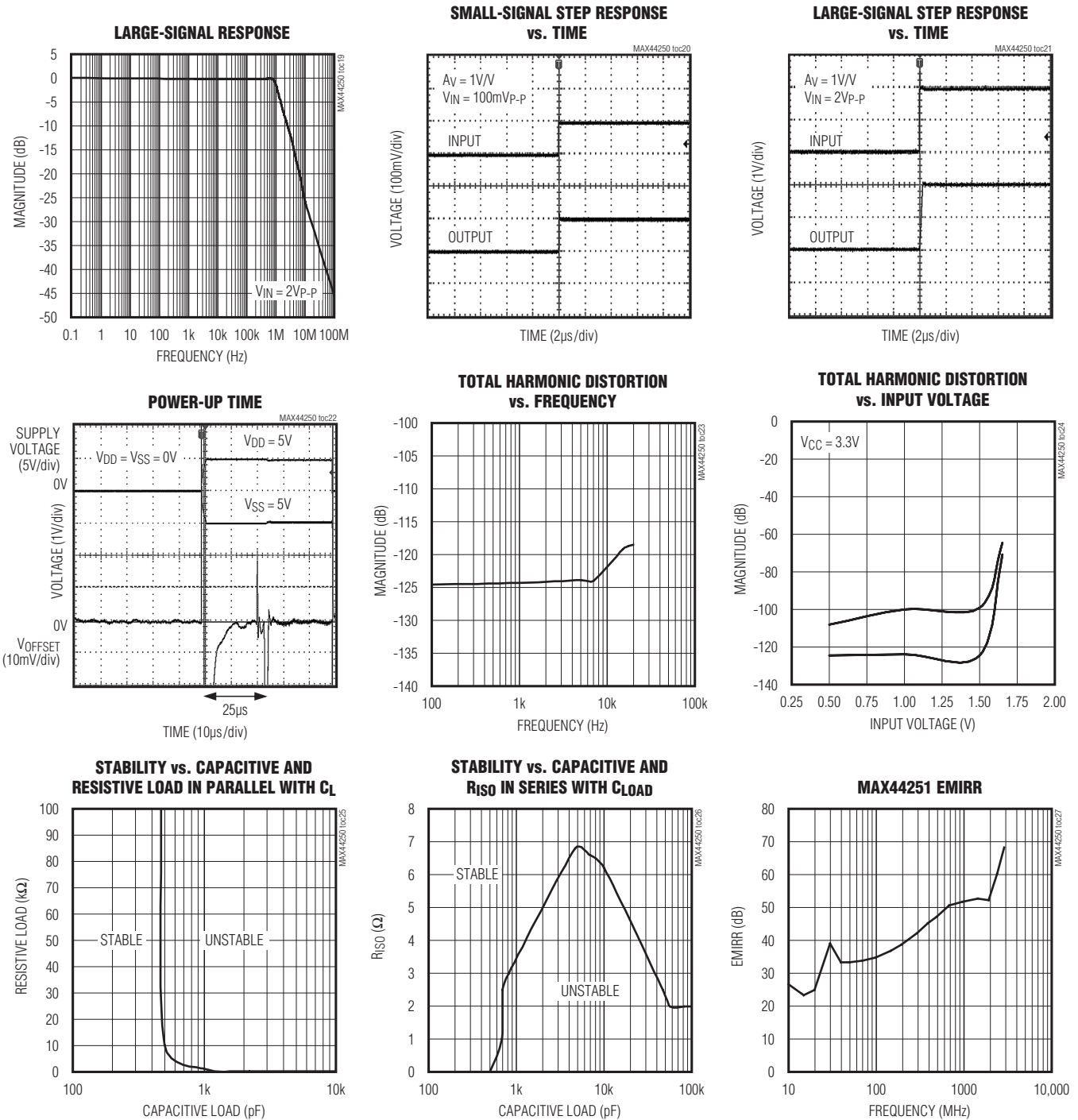
Typical Operating Characteristics (continued)

( $V_{DD} = 10V$ ,  $V_{SS} = 0V$ , outputs have  $R_L = 10k\Omega$  to  $V_{DD}/2$ .  $T_A = +25^\circ C$ , unless otherwise specified.)



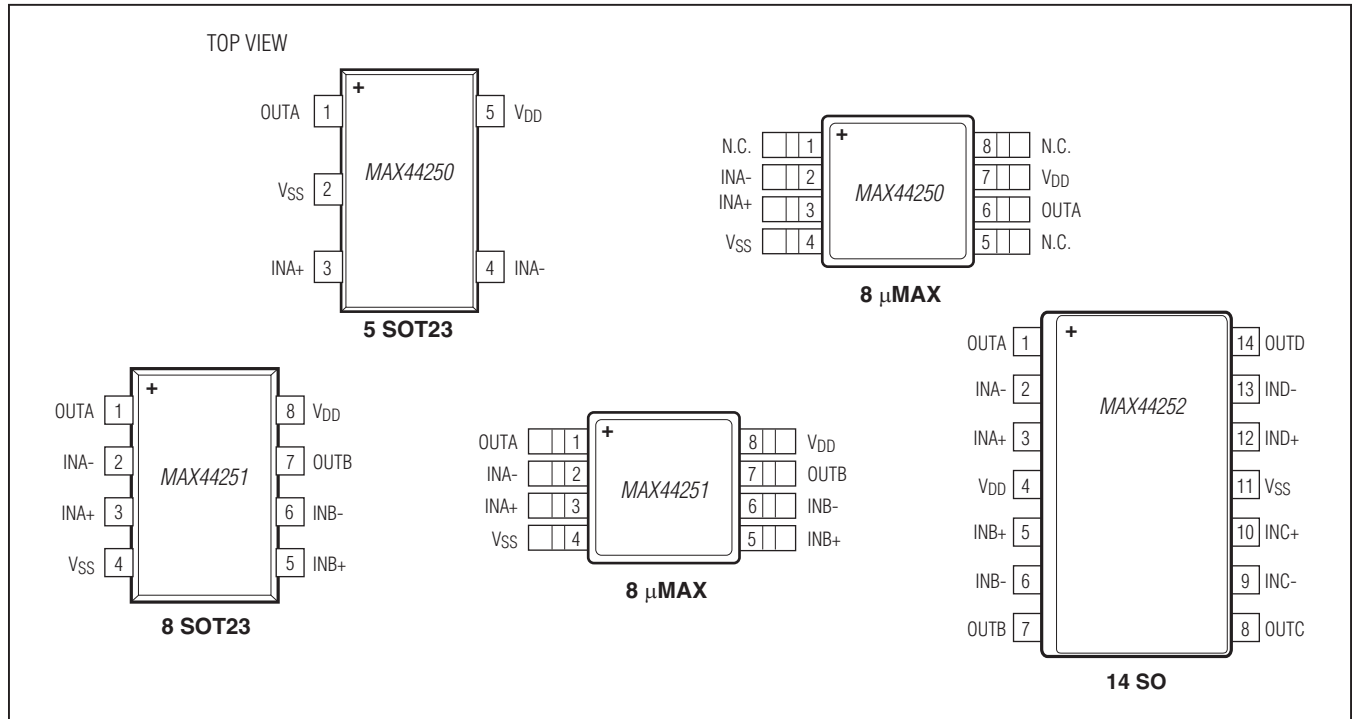
Typical Operating Characteristics (continued)

( $V_{DD} = 10V$ ,  $V_{SS} = 0V$ , outputs have  $R_L = 10k\Omega$  to  $V_{DD}/2$ .  $T_A = +25^\circ C$ , unless otherwise specified.)





### Pin Configurations



### Pin Description

PIN					NAME	FUNCTION
MAX44250		MAX44251		MAX44252		
5 SOT23	8 μMAX	8 SOT23	8 μMAX	14 SO		
1	6	1	1	1	OUTA	Channel A Output
4	2	2	2	2	INA-	Channel A Negative Input
3	3	3	3	3	INA+	Channel A Positive Input
2	4	4	4	11	V <sub>SS</sub>	Negative Supply Voltage
—	—	5	5	5	INB+	Channel B Positive Input
—	—	6	6	6	INB-	Channel B Negative Input
—	—	7	7	7	OUTB	Channel B Output
5	7	8	8	4	V <sub>DD</sub>	Positive Supply Voltage
—	—	—	—	8	OUTC	Channel C Output
—	—	—	—	9	INC-	Channel C Negative Input
—	—	—	—	10	INC+	Channel C Positive Input
—	—	—	—	12	IND+	Channel D Positive Input
—	—	—	—	13	IND-	Channel D Negative Input
—	—	—	—	14	OUTD	Channel D Output
—	1, 5, 8	—	—	—	N.C.	No Connection

### Detailed Description

The MAX44250/MAX44251/MAX44252 are high-precision amplifiers that have less than  $3\mu\text{V}$  of typical input-referred offset and low flicker noise. These characteristics are achieved through an autozeroing technique that samples and finds repeating patterns of signal to cancel the input offset voltage and  $1/f$  noise of the amplifier.

### Autozero

The ICs feature an autozero circuit that allows the devices to achieve less than  $6\mu\text{V}$  (max) of input offset voltage at room temperature and eliminate the  $1/f$  noise.

### Noise Suppression

Flicker noise, inherent in all active devices, is inversely proportional to frequency presented. Charges at the oxide-silicon interface that are trapped-and-released by MOSFET oxide occurs at low frequency more often. For this reason, flicker noise is also called  $1/f$  noise.

Electromagnetic interference (EMI) noise occurs at higher frequency that results in malfunction or degradation of electrical equipment.

The ICs have an input EMI filter to avoid the output getting affected by radio frequency interference. The EMI filter composed of passive devices presents significant higher impedance to higher frequency.

### High Supply Voltage Range

The ICs feature  $1.15\text{mA}$  current consumption per channel and a voltage supply range from either  $2.7\text{V}$  to  $20\text{V}$  single supply or  $\pm 1.35\text{V}$  to  $\pm 10\text{V}$  split supply.

### Applications Information

The ICs are ultra-high-precision operational amplifiers with a high supply voltage range designed for load cell, medical instrumentation and precision instrument applications.

These devices are also designed to interface with pressure transducers and are ideal for precision weight scale application as shown in [Figure 1](#).

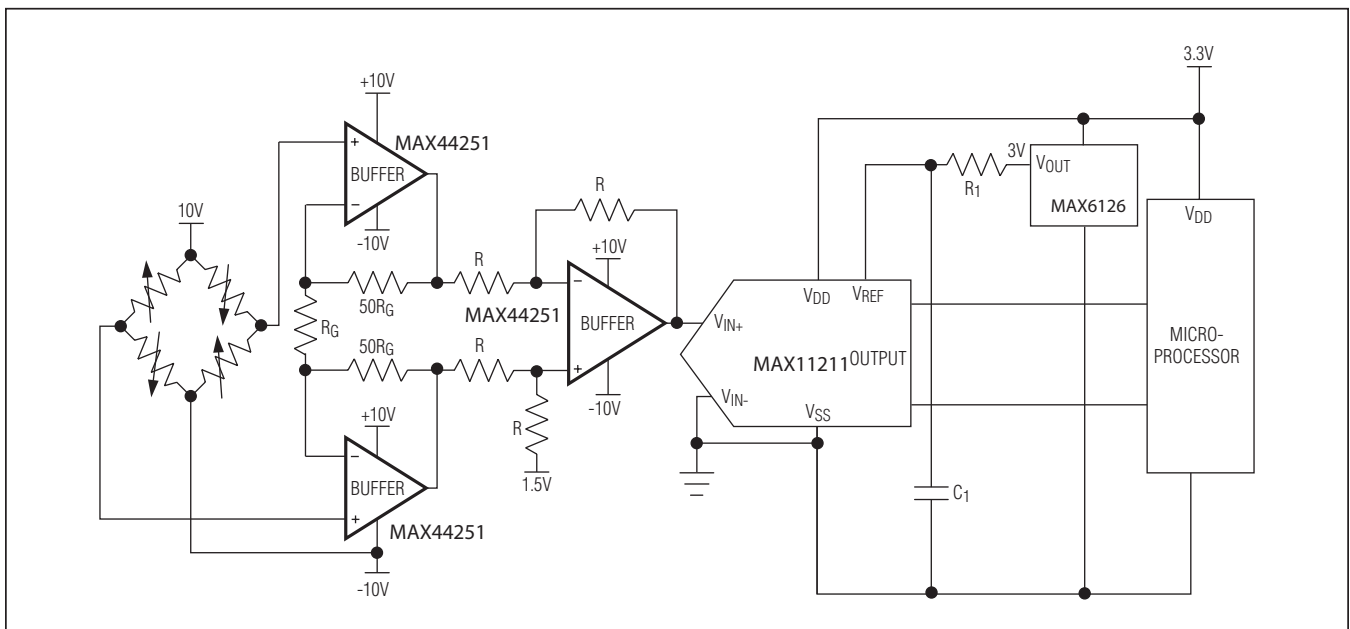


Figure 1. Weight Scale Application Circuit

### ADC Buffer Amplifier

The MAX44250/MAX44251/MAX44252's low input offset voltage, low noise, and fast settling time make these amplifiers ideal for ADC buffers. Weigh scales are one application that often require a low-noise, high-voltage amplifier in front of an ADC. [Figure 1](#) details an example of a load cell and amplifier driven from the same  $\pm 10\text{V}$  supplies, along with the MAX11211 18-bit delta sigma ADC. Load cells produce a very small voltage change at their outputs, therefore driving the excitation source with a higher voltage produces a wider dynamic range that can be measured at the ADC inputs.

The MAX11211 ADC operates from a single 2.7V to 3.6V analog supply, offers 18-bit noise-free resolution and 0.86mW power dissipation. The MAX11211 also offers > 100dB rejection at 50Hz and 60Hz. This ADC is part of a family of 16-, 18-, 20-, and 24-bit delta sigma ADCs with high precision and < 1mW power dissipation.

The MAX44250/MAX44251/MAX44252's low input offset voltage and low noise allow a gain circuit prior to the MAX11211 without losing any dynamic range at the ADC.

### Error Budget Example

When using the ICs as an ADC buffer in strain gauge application, the temperature drift should be taken into consideration to determine maximum input signal. A typical strain gauge has sensitivity specification of just 2mV/V at rated out load. This means that when the strain gauge load cell is powered with 10V, the full-scale output voltage is 20mV. In this application, both offset voltage and drift are critical parameters that directly affect the accuracy of measurement. Even though offset voltage

could be calibrated out, its drift over temperature is still a problem.

The ICs, with a typical offset drift of 5nV/°C, guarantee that the drift over a 10°C range is only 50nV. Setting this equal to 0.5 LSB in a 18-bit system yields a full-scale range of 13mV. With a single 10V supply, an acceptable closed-loop gain of 770V/V provides sufficient gain while maintaining headroom.

### Precision Low-Side Current Sensing

The ICs' autozero feature produces ultra-low offset voltage and drift, making them ideal for precision current-sensing applications. [Figure 2](#) shows the ICs in a low-side current-sense configuration. This circuit produces an accurate output voltage,  $V_{OUT}$  equal to  $I_{LOAD} \times R_{SENSE} \times (1 + R_2/R_1)$ .

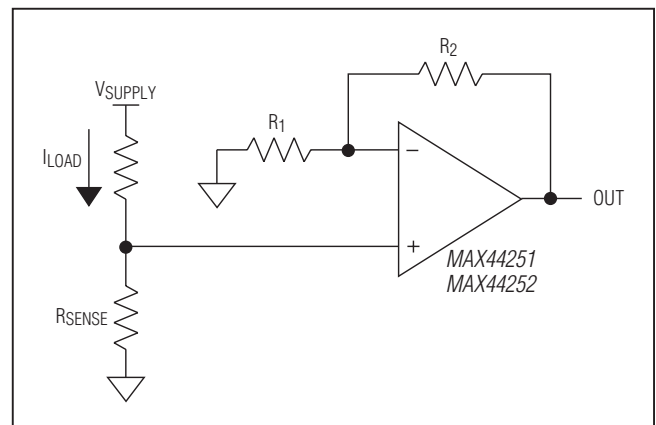
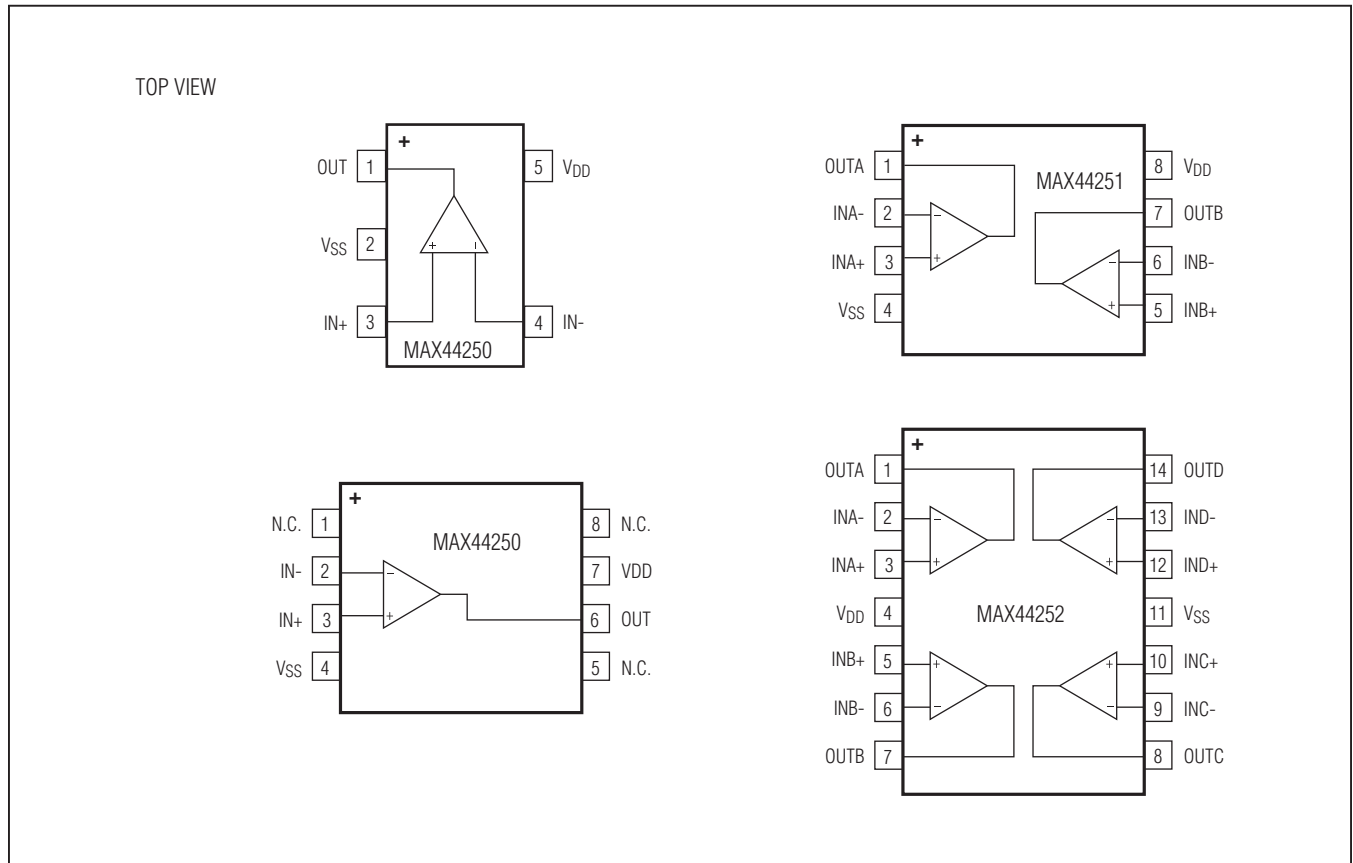


Figure 2. Low-Side Current Sensing

### Functional Diagrams



### Chip Information

PROCESS: BiCMOS

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
<b>MAX44250</b> AUK+	-40°C to +125°C	5 SOT23	AFMA
MAX44250AUA+	-40°C to +125°C	8 μMAX	—
<b>MAX44251</b> AKA+	-40°C to +125°C	8 SOT23	AERC
MAX44251AUA+	-40°C to +125°C	8 μMAX	—
<b>MAX44252</b> ASD+	-40°C to +125°C	14 SO	—

+Denotes a lead(Pb)-free/RoHS-compliant package.

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5+1	<a href="#">21-0057</a>	<a href="#">90-0174</a>
8 SOT23	K8+5	<a href="#">21-0078</a>	<a href="#">90-0176</a>
8 $\mu$ MAX	U8+1	<a href="#">21-0036</a>	<a href="#">90-0092</a>
14 SO	S14M+5	<a href="#">21-0041</a>	<a href="#">90-0112</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/11	Initial release	—
1	12/11	Released the MAX44252 and updated the <i>Typical Operating Characteristics</i>	5, 6, 11
2	8/12	Added the MAX44250 to the data sheet, added MAX44251 EMIRR graph to <i>Typical Operating Characteristics</i> , and revised Figure 2	1–16
3	4/13	Updated <i>General Description</i> , <i>Typical Operating Circuit</i> , and Figure 1	1, 10
4	6/14	Corrected <i>Package Information</i>	13
5	5/15	Added the <i>Benefits and Features</i> section	1
6	1/17	Updated Functional Diagram to fix error	12

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