19-1543; Rev 0; 10/99

EVALUATION KIT AVAILABLE

Ultra-High-Speed, Low-Distortion, Differential-to-Single-Ended Line Receivers with Enable

General Description

The MAX4444/MAX4445 differential line receivers offer unparalleled high-speed, low-distortion performance. Using a three op amp instrumentation amplifier architecture, these ICs have symmetrical differential inputs and a single-ended output. They operate from ±5V supplies and are capable of driving a 100Ω load to ±3.7V. The MAX4444 has an internally set closed-loop gain of +2V/V, while the MAX4445 is compensated for gains of +2V/V or greater, set by an external resistor. A low-power enable mode reduces current consumption to 3.5mA.

Using current-feedback techniques, the MAX4444/MAX4445 achieve a 550MHz bandwidth while maintaining up to a 5000V/µs slew rate. Excellent differential gain/phase and noise specifications make these amplifiers ideal for a wide variety of video and RF signal-processing applications. An evaluation kit is available to speed design.

Features

- **5000V/µs Slew Rate (MAX4444)**
- **+2V/V Internally Fixed Gain (MAX4444)**
- **External Gain Selection (MAX4445, $A_{VCL} \geq$ +2V/V)**
- **550MHz -3dB Bandwidth**
- **-60dB SFDR at 5MHz**
- **Low Differential Gain/Phase: 0.07%/0.05°**
- **Low Noise: 25nV/$\sqrt{Hz}$ at f_{IN} = 100kHz**
- **Low-Power Disable Mode Reduces Quiescent Current to 3.5mA**

Applications

Differential-to-Single-Ended Conversion

Twisted-Pair to Coaxial Converter

High-Speed Instrumentation Amplifier

Data Acquisition

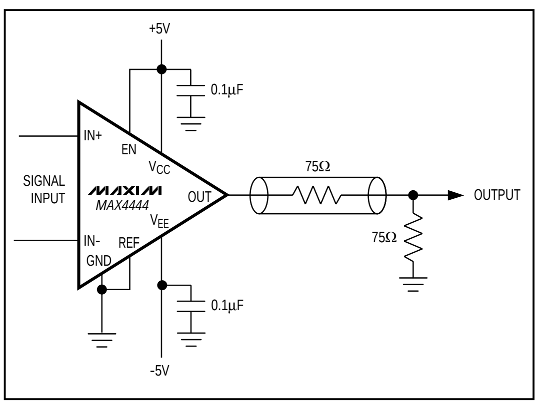
Medical Instrumentation

High-Speed Differential Line Receiver

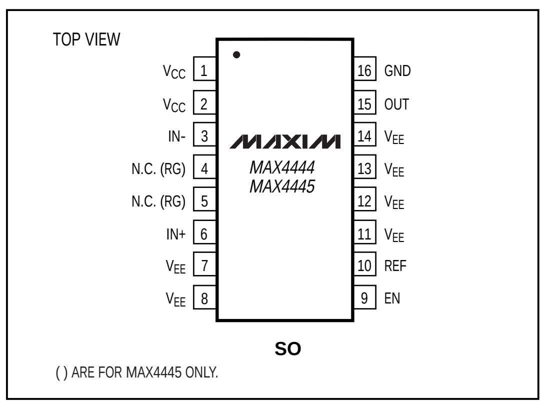
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4444ESE	-40°C to +85°C	16 Narrow SO
MAX4445ESE	-40°C to +85°C	16 Narrow SO

Typical Operating Circuit



Pin Configuration



Ultra-High-Speed, Low-Distortion, Differential-to-Single-Ended Line Receivers with Enable

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} ....+12V
Voltage on IN+, IN-, EN, OUT+,
OUT-, RG, REF.............................(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Current Into IN+, IN-, RG, EN 20mA
Output Short-Circuit Duration ....Indefinite to GND

Continuous Power Dissipation (T_A = +70°C)
16-Pin Narrow SO (derate 20mW/°C above +70°C) ...1600mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{EN} = ≥2V, V_{CM} = 0 , R_L = ∞, REF = GND, A_{VCL} = +2V/V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		Guaranteed by PSRR test	±4.5		±5.5	V
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test	-2.9		2.9	V
Differential Input Voltage Range	V_{DIFF}	Guaranteed by output swing test	-1.7		1.7	V
Input Offset Voltage	V_{OS}			15	65	mV
Input Offset-Voltage Temperature Coefficient	TC_{VOS}			12		µV/°C
Input Bias Current	I_B			10	55	µA
Input Offset Current	I_{OS}			0.25	45	µA
Differential Input Resistance	R_{IN}	-2.9V ≤ V_{IN} ≤ +2.9V		82		kΩ
		-2.9V ≤ V_{CM} ≤ +2.9V		170		
Gain	A_V	-3V ≤ V_{OUT} ≤ +3V, MAX4444		2		V/V
		-3V ≤ V_{OUT} ≤ +3V, MAX4445		(1 + 600/R_G)		
Gain Error		-3V ≤ V_{OUT} ≤ +3V, R_L = 100Ω, MAX4444		0.5	2	%
		-3V ≤ V_{OUT} ≤ +3V, R_L = 100Ω, MAX4445		2.6	8	
Gain-Error Drift		R_L = 100Ω		0.003		%/°C
Output Voltage Swing	V_{OUT}	R_L = 100Ω	±3.4	±3.7		V
		R_L = 50Ω	±3.3	±3.6		
Output Current Drive	I_{OUT}	R_L = 30Ω	90	120		mA
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	53	70		dB
Common-Mode Rejection Ratio	CMRR	-2.9V ≤ V_{CM} ≤ +2.9V	40	55		dB
Disable Output Resistance	$R_{OUT(OFF)}$	V_{EN} = 0, -3.5V ≤ V_{OUT} ≤ +3.5V, MAX4444		1.8		kΩ
EN Logic Low Threshold	V_{IL}				0.8	V
EN Logic High Threshold	V_{IH}		2			V
EN Logic Input Low Current	I_{IL}	V_{EN} = 0		2.2	10	µA
EN Logic Input High Current	I_{IH}	V_{EN} = 5V		2.6	10	µA
Quiescent Current	I_Q	V_{IN} = 0, V_{EN} = 5V		41	55	mA
		V_{IN} = 0, V_{EN} = 0		3.5	5.5	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{EN} = 5V, R_L = 100Ω, REF = GND, A_{VCL} = +2V/V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 100mVp-p			550		MHz
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p			500		MHz
0.1dB Gain Flatness		V_{OUT} = 100mVp-p			80		MHz
Slew Rate (Note 1)	SR	V_{OUT} = 4V step	MAX4444		5000		V/µs
			MAX4445		3800		
		V_{OUT} = 2V step	MAX4444		2400		
			MAX4445		2000		
		V_{OUT} = 1V step			1200		
		V_{OUT} = 0.5V step			600		
Rise Time (Note 1)	t_{RISE}				650		ps
Fall Time (Note 1)	t_{FALL}	V_{OUT} = 4V step			825		ps
		V_{OUT} = 2V step			700		
		V_{OUT} = 1V step			700		
		V_{OUT} = 0.5V step			700		
Settling Time		Settle to 0.1% , V_{OUT} = 2V step			12		ns
SFDR		V_{OUT} = 2Vp-p	f_C = 100kHz		-65		dBc
			f_C = 5MHz		-60		
			f_C = 20MHz		-55		
			f_C = 100MHz		-35		
2nd-Harmonic Distortion		V_{OUT} = 2Vp-p	f_C = 100kHz		-65		dBc
			f_C = 5MHz		-62		
			f_C = 20MHz		-50		
			f_C = 100MHz		-35		
3rd-Harmonic Distortion		V_{OUT} = 2Vp-p	f_C = 100kHz		-90		dBc
			f_C = 5MHz		-72		
			f_C = 20MHz		-62		
			f_C = 100MHz		-55		
Differential Phase Error	DP	NTSC, R_L = 150Ω			0.05		degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω			0.07		%
Input Noise Voltage Density	e_N	f = 100kHz (Note 2)			25		$nV/\sqrt{Hz}$
Input Noise Current Density	i_N	f = 100kHz			1.8		$pA/\sqrt{Hz}$
Output Impedance	Z_{OUT}	f = 10MHz			0.7		Ω
Enable Time	$t_{SHDN(ON)}$	V_{IN} = 1V, V_{OUT} settle to within 10%			80		ns
Disable Time	$t_{SHDN(OFF)}$	V_{IN} = 1V, V_{OUT} settle to within 10%			200		ns
Power-Up Time	t_{ON}	V_{IN} = 1V, V_{OUT} settle to within 10%			0.5		µs
Power-Down Time	t_{OFF}	V_{IN} = 1V, V_{OUT} settle to within 10%			0.3		µs

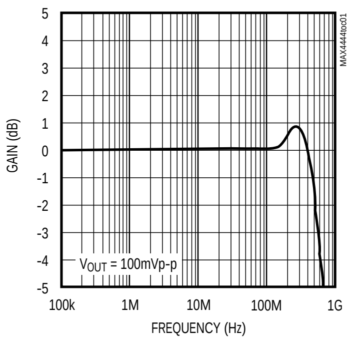
Note 1: Input step voltage has <100ps rise (fall) time. Measured at the output from 10% to 90% (90% to 10%) level.
Note 2: Includes the current noise contribution through the on-die feedback resistor.

Ultra-High-Speed, Low-Distortion, Differential-to-Single-Ended Line Receivers with Enable

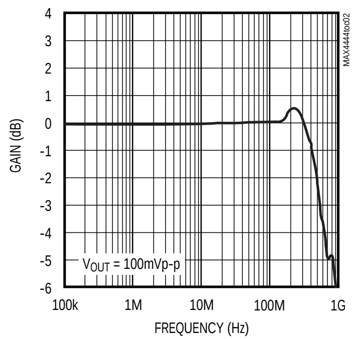
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, V_{EN} = 5V, V_{IN} = V_{IN+} - V_{IN-}, R_L = 100Ω, REF = GND, A_V = +2V/V, T_A = +25°C, unless otherwise noted.)

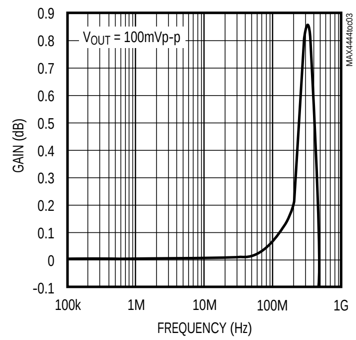
MAX4444
SMALL-SIGNAL GAIN vs. FREQUENCY



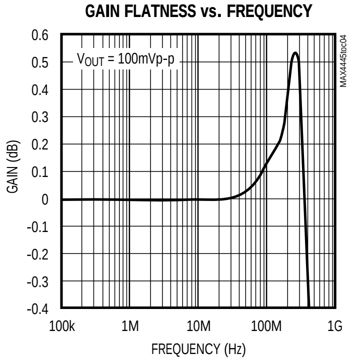
MAX4445
SMALL-SIGNAL GAIN vs. FREQUENCY



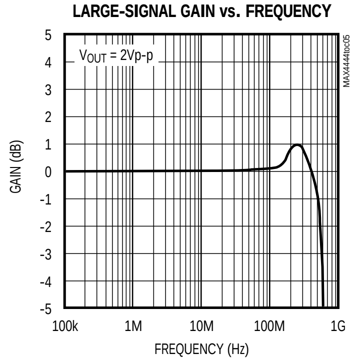
MAX4444
GAIN FLATNESS vs. FREQUENCY



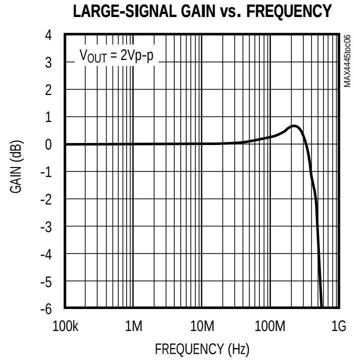
MAX4445
GAIN FLATNESS vs. FREQUENCY



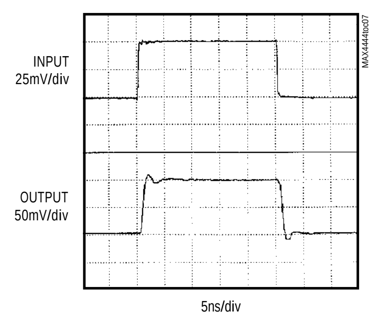
MAX4444
LARGE-SIGNAL GAIN vs. FREQUENCY



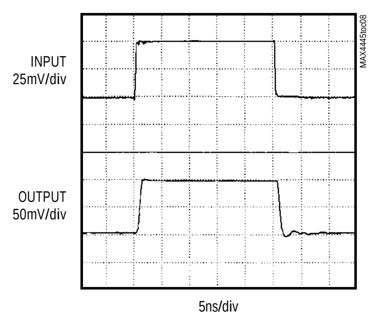
MAX4445
LARGE-SIGNAL GAIN vs. FREQUENCY



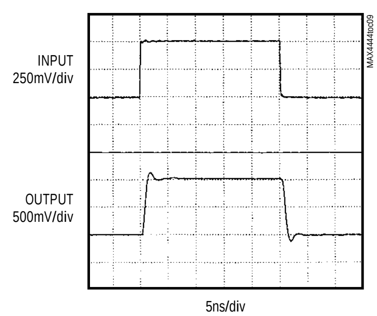
MAX4444
SMALL-SIGNAL PULSE RESPONSE



MAX4445
SMALL-SIGNAL PULSE RESPONSE



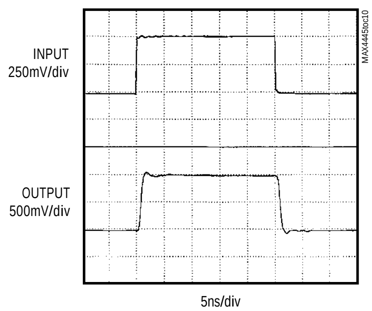
MAX4444
LARGE-SIGNAL PULSE RESPONSE



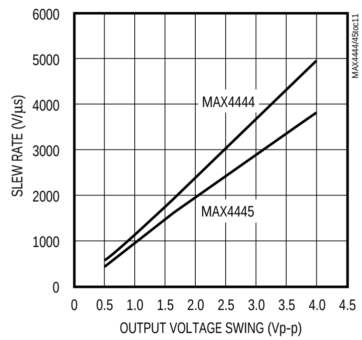
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{EN} = 5V, V_{IN} = V_{IN+} - V_{IN-}, R_L = 100Ω, REF = GND, A_V = +2V/V, T_A = +25°C, unless otherwise noted.)

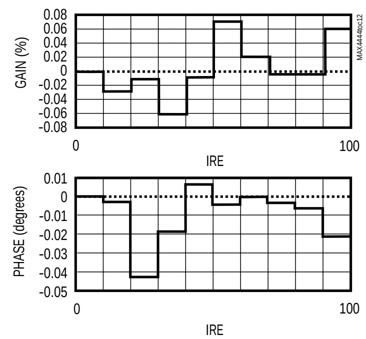
MAX4445 LARGE-SIGNAL PULSE RESPONSE



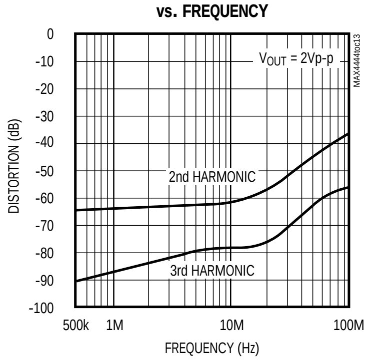
SLEW RATE vs. OUTPUT VOLTAGE SWING



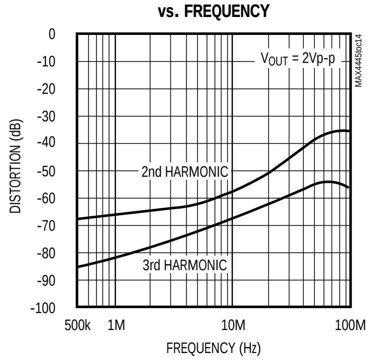
MAX4444 DIFFERENTIAL GAIN AND PHASE



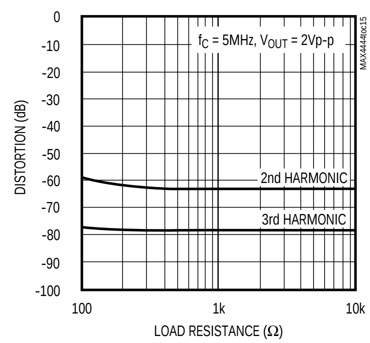
MAX4444 HARMONIC DISTORTION vs. FREQUENCY



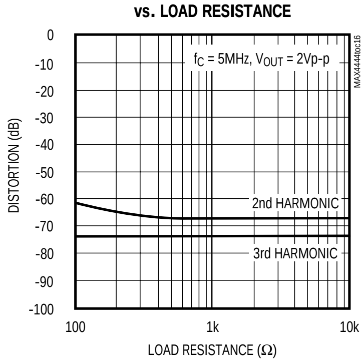
MAX4445 HARMONIC DISTORTION vs. FREQUENCY



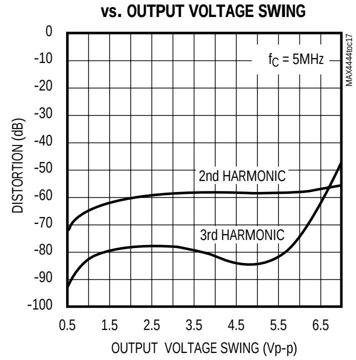
MAX4444 HARMONIC DISTORTION vs. LOAD RESISTANCE



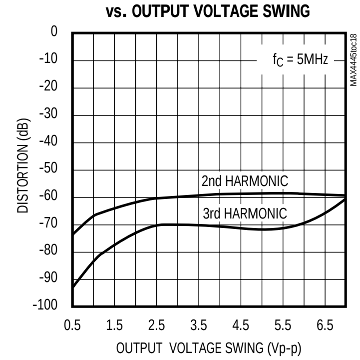
MAX4445 HARMONIC DISTORTION vs. LOAD RESISTANCE



MAX4444 HARMONIC DISTORTION vs. OUTPUT VOLTAGE SWING



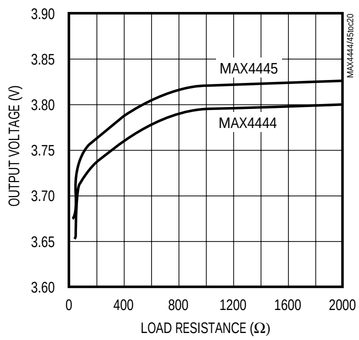
MAX4445 HARMONIC DISTORTION vs. OUTPUT VOLTAGE SWING



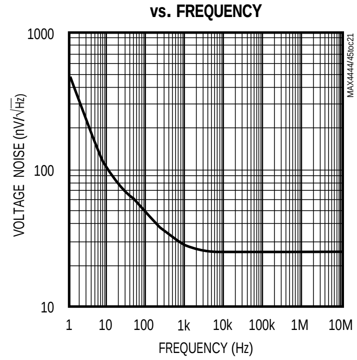
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{EN} = 5V, V_{IN} = V_{IN}+ - V_{IN}-, R_L = 100Ω, REF = GND, A_V = +2V/V, T_A = +25°C, unless otherwise noted.)

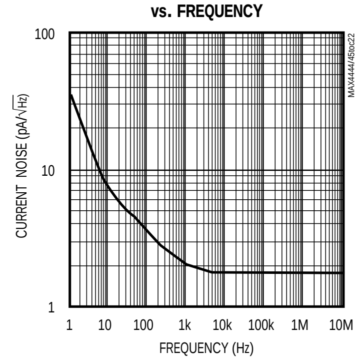
VOLTAGE SWING vs. LOAD RESISTANCE



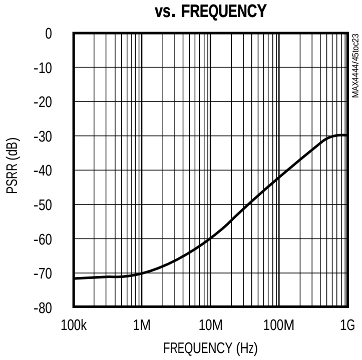
INPUT VOLTAGE NOISE DENSITY vs. FREQUENCY



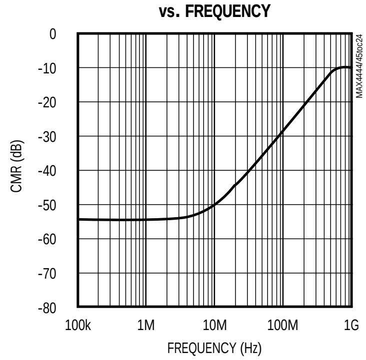
INPUT CURRENT NOISE DENSITY vs. FREQUENCY



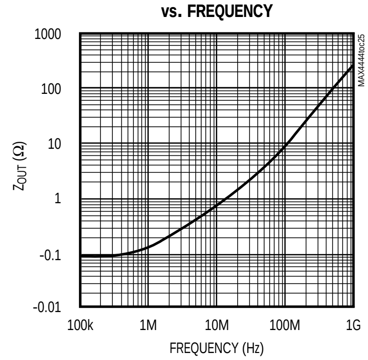
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



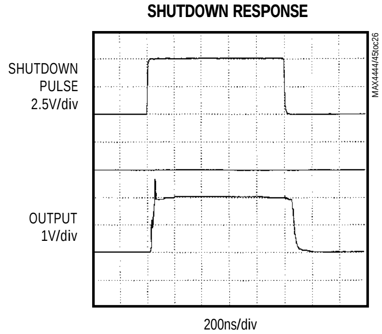
COMMON-MODE REJECTION vs. FREQUENCY



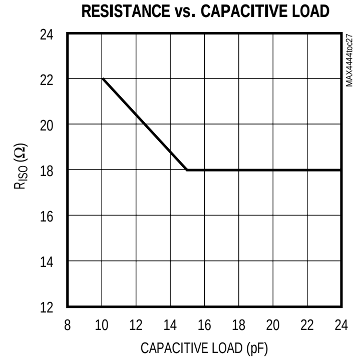
MAX4444 CLOSED-LOOP OUTPUT IMPEDANCE vs. FREQUENCY



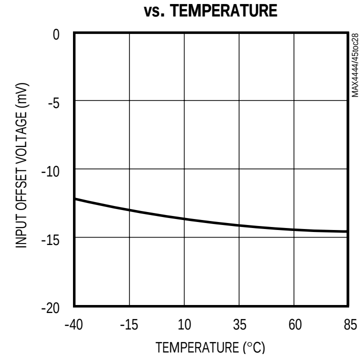
SHUTDOWN RESPONSE



MAX4444 RECOMMENDED ISOLATION RESISTANCE vs. CAPACITIVE LOAD



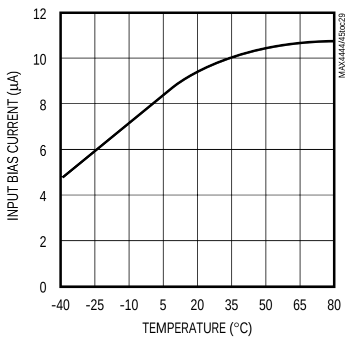
INPUT OFFSET VOLTAGE vs. TEMPERATURE



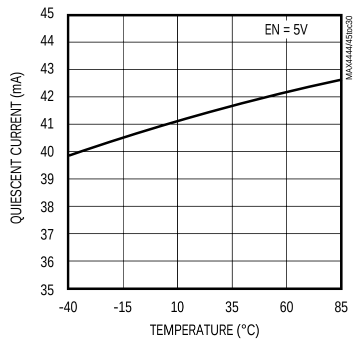
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{EN} = 5V, V_{IN} = V_{IN+} - V_{IN-}, R_L = 100Ω, REF = GND, A_V = +2V/V, T_A = +25°C, unless otherwise noted.)

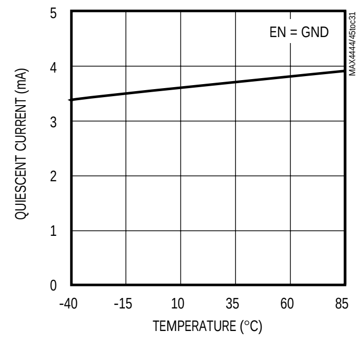
INPUT BIAS CURRENT vs. TEMPERATURE



QUIESCENT CURRENT vs. TEMPERATURE



QUIESCENT CURRENT vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX4444	MAX4445		
1, 2	1, 2	V_{CC}	Positive Power-Supply Input. Bypass with a 0.1µF capacitor to GND.
3	3	IN-	Inverting Amplifier Input
4, 5	—	N.C.	No Connection. Not internally connected. Connect to GND for best AC performance.
—	4, 5	RG	Resistor Gain Input. Connect a resistor between these pins to set closed-loop gain (Figure 1).
6	6	IN+	Noninverting Amplifier Input
7, 8, 11–14	7, 8, 11–14	V_{EE}	Negative Supply Input. Bypass with a 0.1µF capacitor.
9	9	EN	Active-High Enable Input. Connect to V_{CC} for normal operation. Connect to GND for disable mode.
10	10	REF	Reference Input. Connect to midpoint of the two power supplies.
15	15	OUT	Amplifier Output
16	16	GND	Ground

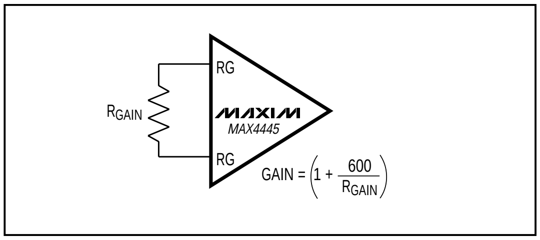


Figure 1. Setting the Amplifier Gain

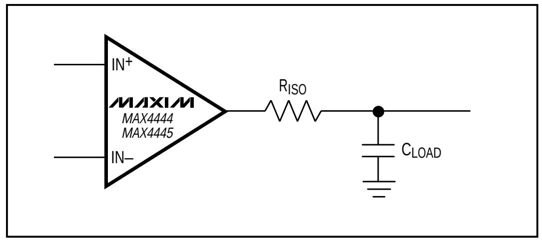


Figure 2. Using an Isolation Resistor for High Capacitive Loads

Detailed Description

The MAX4444/MAX4445 differential-to-single-ended line receivers offer high-speed and low-distortion performance, and are ideally suited for video and RF signal-processing applications. These receivers offer a small-signal bandwidth of 550MHz and have a high slew rate of up to 5000V/µs. Their 120mA output capability allows them to be directly coupled to data acquisition systems.

Applications Information

Grounding Bypassing

Use the following high-frequency design techniques when designing the PC board for the MAX4444/MAX4445.

- Use a multilayer board with one layer dedicated as the ground plane.
- Do not use wire wrap or breadboards due to high inductance.
- Avoid IC sockets due to high parasitic capacitance and inductance.
- Bypass supplies with a 0.1µF capacitor. Use surface-mount capacitors to minimize lead inductance.
- Keep signal lines as short and straight as possible. Do not make 90° turns. Use rounded corners. Do not cross signal paths if possible.
- Ensure that the ground plane is free from voids.

Low-Power Enable Mode

The MAX4444/MAX4445 are disabled when EN goes low. This reduces supply current to only 3.5mA. As the output becomes higher impedance, the effective impedance at the output for the MAX4444 is 1.8kΩ. The effective output impedance for the MAX4445 is 1.8kΩ plus R_{GAIN}.

Setting Gain (MAX4445)

The MAX4445 is stable with a minimum gain configuration of +2V/V. R_{GAIN}, connected between the RG pins, sets the gain of this device as shown in Figure 1. Calculate the expected gain as follows:

$$\text{Gain} = (1 + 600 / R_{GAIN})$$

Driving Capacitive Loads

The MAX4444/MAX4445 are designed to drive capacitive loads. However, excessive capacitive loads may cause ringing or instability at the output as the phase margin of the device reduces. Adding a small series isolation resistor at the output helps reduce the ringing but slightly increases gain error (Figure 2). For recommended values, see *Typical Operating Characteristics*.

Coaxial Line Driver

The MAX4444/MAX4445 are well suited to drive coaxial cables. Their high output current capability can easily drive the 75Ω characteristic impedance of common coaxial cables. Adjust the gain of the MAX4445 to compensate for cable losses to maintain the required levels at the input of the next stage.

Chip Information

TRANSISTOR COUNT: 254

SUBSTRATE CONNECTED TO V_{EE}