



High-Bandwidth, Quad DPDT Switches

General Description

The MAX4760/MAX4760A/MAX4761/MAX4761A (DPDT) analog switches operate from a single +1.8V to +5.5V supply. These switches feature a low 54pF (typ) capacitance for high-speed data switching applications.

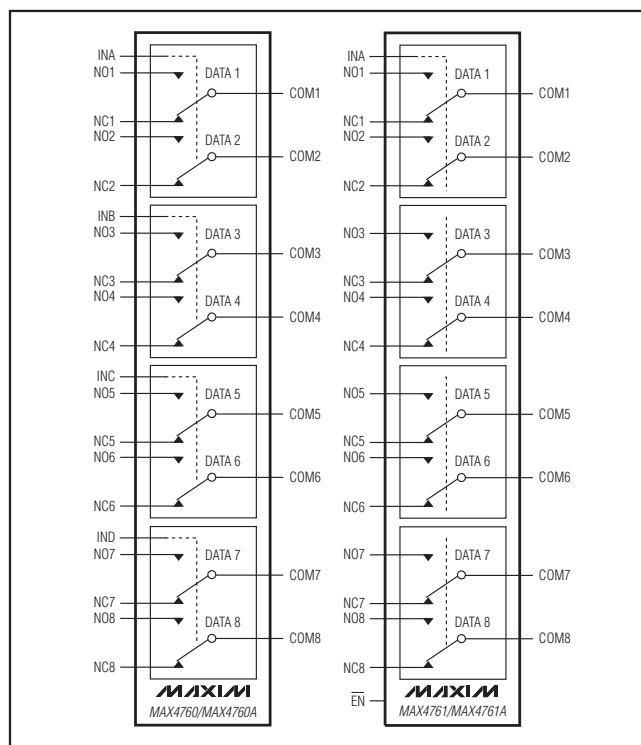
The MAX4760/MAX4760A are quad double-pole/double-throw (DPDT) switches, and the MAX4761/MAX4761A are octal single-pole/double-throw (SPDT) switches. They have eight 2.0Ω (typ) on-resistance, low-capacitance switches to route audio and data signals. The MAX4760/MAX4760A have four logic inputs to control the switches in pairs. The MAX4761/MAX4761A have one logic control input and an enable input (EN) to disable the switches.

The MAX4760/MAX4760A/MAX4761/MAX4761A are available in a small 36-pin (6mm x 6mm) TQFN and 36-bump (3mm x 3mm) chip-scale package (UCSP™).

Applications

USB Signal Switching PDAs/Handheld Devices
Audio-Signal Switching Notebook Computers
Cellular Phones

Functional Diagrams



UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- ◆ USB 1.1 and USB 2.0 (Full Speed 12Mbps) Signal-Switching Compliant
- ◆ Data and Audio Signal Routing
- ◆ Low-Capacitance Data Switches
- ◆ Less than 0.2ns Skew
- ◆ -3dB Bandwidth: 150MHz (typ)
- ◆ 0.2Ω (typ) Channel-to-Channel Matching
- ◆ 0.8Ω (typ) On-Resistance Flatness
- ◆ Rail-to-Rail Signal Handling
- ◆ 0.03% (typ) THD
- ◆ +1.8V to +5.5V Supply Range
- ◆ Low Supply Current with 1.8V Logic Threshold (MAX4760A/MAX4761A)
- ◆ Tiny 36-Bump UCSP (3mm x 3mm)
- ◆ 36-Pin TQFN (6mm x 6mm)
- ◆ -40°C to +85°C Operating Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4760EBX+T	-40°C to +85°C	36 UCSP
MAX4760ETX+T	-40°C to +85°C	36 TQFN-EP**
MAX4760AEWX+T	-40°C to +85°C	36 UCSP
MAX4760AETX+T*	-40°C to +85°C	36 TQFN-EP**
MAX4761EBX+T	-40°C to +85°C	36 UCSP
MAX4761ETX+T	-40°C to +85°C	36 TQFN-EP**
MAX4761AEBX+T*	-40°C to +85°C	36 UCSP
MAX4761AETX+T*	-40°C to +85°C	36 TQFN-EP**

*Future product—contact factory for availability.

**EP = Exposed Pad.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Pin Configurations/Truth Tables and Typical Operating Circuit appear at end of data sheet.

MAX4760/MAX4760A/MAX4761/MAX4761A

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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

V+-0.3V to +6V
IN ₋ , EN (MAX4761)-0.3V to +6V
IN ₋ , EN (MAX4761A)-0.3V to (V+ + 0.3V)
COM ₋ , NO ₋ , NC ₋ (Note 1)-0.3V to (V+ + 0.3V)
Continuous Current	
NO ₋ , NC ₋ , COM ₋±100mA
Peak Current	
(pulsed at 1ms, 10% duty cycle)±200mA
(pulsed at 1ms, 50% duty cycle) ±300mA

Continuous Power Dissipation (T_A = +70°C)

36-Bump UCSP (derate 15.3mW/°C above +70°C)....	1221mW
36-Pin TQFN (derate 26.3mW/°C above +70°C).....	2105mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature.....	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Bump Temperature (soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C

Note 1: Signals on NO₋, NC₋, COM₋ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{COM-} , V _{NO-} , V _{NC-}		T _{MIN} to T _{MAX}	0		V+	V
On-Resistance	R _{ON}	V+ = 2.7V, I _{COM-} = 10mA, V _{NC-} or V _{NO-} = 0V or V+ (Note 4)	+25°C		2.0	3.5	Ω
			T _{MIN} to T _{MAX}			4	
On-Resistance Match Between Channels	ΔR _{ON}	V+ = 2.7V, I _{COM-} = 10mA, V _{NO-} or V _{NC-} = 1.5V (Notes 4, 5)	+25°C		0.2	0.4	Ω
			T _{MIN} to T _{MAX}			0.55	
On-Resistance Flatness	R _{FLAT(ON)}	V+ = 2.7V, I _{COM-} = 10mA, V _{NC-} or V _{NO-} = 0V or V+ (Note 6)	+25°C		0.8	1.5	Ω
			T _{MIN} to T _{MAX}			1.8	
NO ₋ , NC ₋ Off-Leakage Current	I _{NO-(OFF)} , I _{NC-(OFF)}	V+ = 3.6V; V _{COM-} = 3.3V, 0.3V; V _{NO-} or V _{NC-} = 0.3V, 3.3V	+25°C	-5		+5	nA
			T _{MIN} to T _{MAX}	-25		+25	
COM ₋ Off-Leakage Current		V+ = 3.6V (MAX4761/MAX4761A); V _{COM-} = 3.3V, 0.3V; V _{NO-} or V _{NC-} = 0.3V, 3.3V	+25°C	-5	0.1	+5	nA
			T _{MIN} to T _{MAX}	-25		+25	
COM ₋ On-Leakage Current	I _{COM-(ON)}	V+ = 3.6V; V _{COM-} = 3.3V, 0.3V; V _{NO-} or V _{NC-} = 3.3V, 0.3V or unconnected	+25°C	-5		+5	nA
			T _{MIN} to T _{MAX}	-25		+25	
DYNAMIC							
Turn-On Time	t _{ON}	V _{NO-} or V _{NC-} = 1.5V; R _L = 50Ω; C _L = 35pF, Figure 2	MAX4760/ MAX4761	+25°C	45	140	ns
				T _{MIN} to T _{MAX}		150	
			MAX4760A/ MAX4761A	+25°C	400	800	ns
				T _{MIN} to T _{MAX}		800	

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MAX4760/MAX4760A/MAX4761/MAX4761A

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
Turn-Off Time	t _{OFF}	V+ = 2.7V, V _{NO_} or V _{NC_} = 1.5V; R _L = 50Ω; C _L = 35pF, Figure 2	+25°C	25	50	ns	
			T _{MIN} to T _{MAX}	60			
		MAX4760A/MAX4761A	+25°C	300	800	ns	
			T _{MIN} to T _{MAX}	800			
Break-Before-Make	t _{BBM}	V+ = 2.7V, V _{NO_} or V _{NC_} = 1.5V; R _L = 50Ω, C _L = 35pF, Figure 3 (Note 7)	+25°C	100		ns	
			T _{MIN} to T _{MAX}	2			
Skew	t _{SKEW}	R _S = 39Ω, C _L = 50pF, Figure 4 (Note 7)	+25°C	0.2		ns	
Charge Injection	Q	V _{GEN} = 0V, R _{GEN} = 0V, C _L = 1.0nF, Figure 5	+25°C	15		pC	
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C _L = 5pF, R _L = 50Ω	+25°C	150		MHz	
Off-Isolation	V _{ISO}	C _L = 5pF, R _L = 50Ω, V _{COM_} = 1VP-P, f = 100kHz, Figure 6 (Note 8)	+25°C	80		dB	
Crosstalk	V _{CT}	C _L = 5pF, R _L = 50Ω, V _{COM_} = 1VP-P, f = 100kHz, Figure 6 (Note 9)	+25°C	95		dB	
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V _{COM_} = 1VP-P, DC bias = V+/2, R _L = R _S = 600Ω	+25°C	0.03		%	
NO_, NC_ Off-Capacitance	C _{NO_(OFF)} , C _{NC_(OFF)}	V _{NO_} , V _{NC_} = GND, f = 1MHz, Figure 7	+25°C	25		pF	
COM_ On-Capacitance	C _{COM(ON)}	V _{NO_} , V _{NC_} = GND, f = 1MHz, Figure 7	+25°C	54		pF	
COM_ Off-Capacitance	C _{COM(OFF)}	V _{COM_} = GND, f = 1MHz (MAX4761/MAX4761A), Figure 7	+25°C	25		pF	
DIGITAL I/O (IN_, EN)							
Input-Logic High	V _{IH}	V+ = 2.7V to 3.6V	T _{MIN} to T _{MAX}	1.4		V	
		V+ = 3.6V to 5.5V (MAX4760A/MAX4761A)	T _{MIN} to T _{MAX}	1.6			
		V+ = 3.6V to 5.25V (MAX4760/MAX4761)	T _{MIN} to T _{MAX}	2.0			
Input-Logic Low	V _{IL}	V+ = 2.7V to 3.6V	T _{MIN} to T _{MAX}	0.5		V	
		V+ = 3.6V to 5.5V (MAX4760A/MAX4761A)	T _{MIN} to T _{MAX}	0.5			
		V+ = 3.6V to 5.25V (MAX4760/MAX4761)	T _{MIN} to T _{MAX}	0.6			
Input Leakage Current	I _{IN} , I _{EN}	V _{IN} = 0V or V+	T _{MIN} to T _{MAX}	1		μA	

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ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+		T _{MIN} to T _{MAX}	1.8		5.5	V
Power Supply Current	I+	V+ = 4.3V, V _{IN_} = 0V or V+ (MAX4760/MAX4761)	+25°C		0.01		μA
			T _{MIN} to T _{MAX}			1.0	
		V+ = 5.5V, V _{IN_} = 0V or V+ (MAX4760A/MAX4761A)	+25°C		0.01		
			T _{MIN} to T _{MAX}			1.0	
		V+ = 5.5V, V _{IN_} = 1.8V (MAX4760A/MAX4761A)	+25°C		5.5		
			T _{MIN} to T _{MAX}			12	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: UCSP packages are 100% tested at +25°C and limits across the full temperature range are guaranteed by correlation and design. TQFN packages are 100% tested at +85°C and limits across the full temperature range are guaranteed by correlation and design.

Note 4: R_{ON} and ΔR_{ON} matching specifications are guaranteed by design.

Note 5: ΔR_{ON} = R_{ON}(MAX) - R_{ON}(MIN).

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

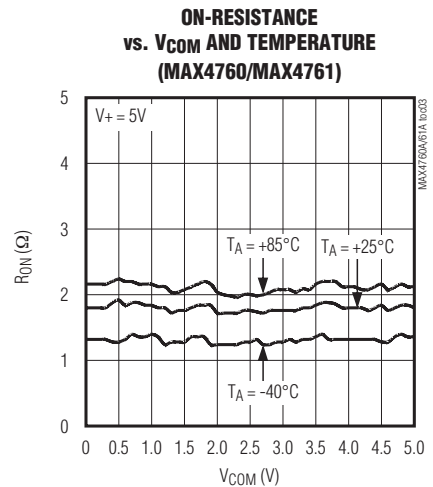
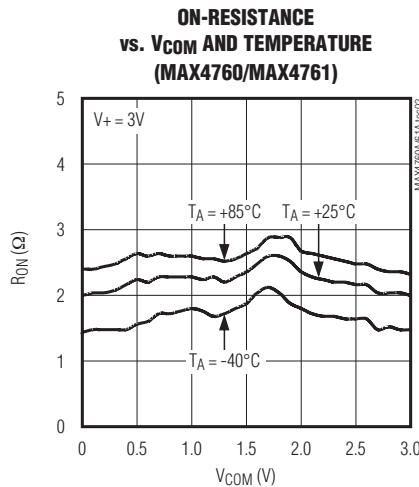
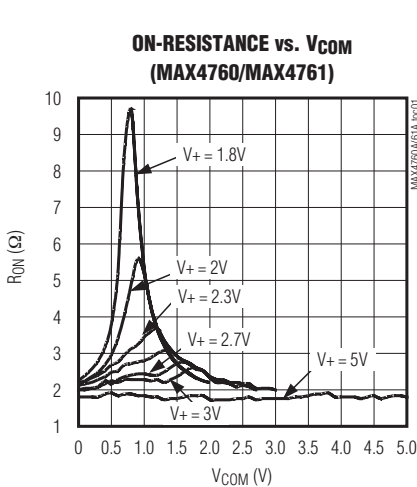
Note 7: Guaranteed by design, not production tested.

Note 8: Off-isolation = 20log₁₀ [V_{COM_}/(V_{NO_} or V_{NC_})], V_{COM_} = output, V_{NO_} or V_{NC_} = input to off switch.

Note 9: Between any two switches.

Typical Operating Characteristics

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

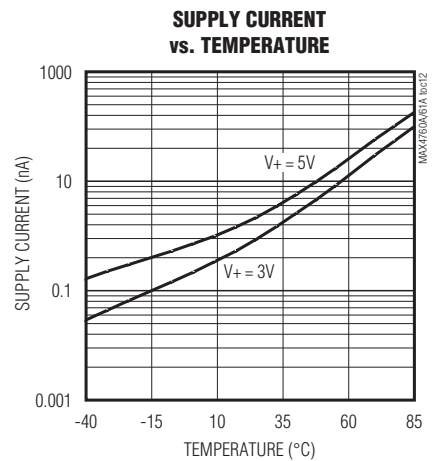
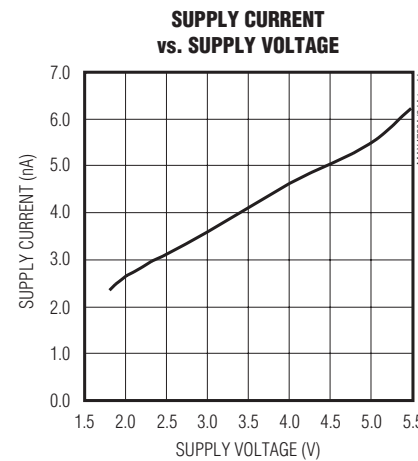
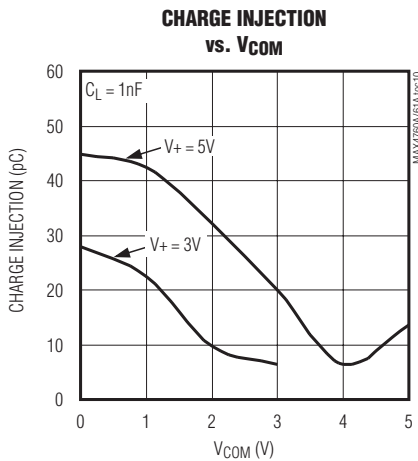
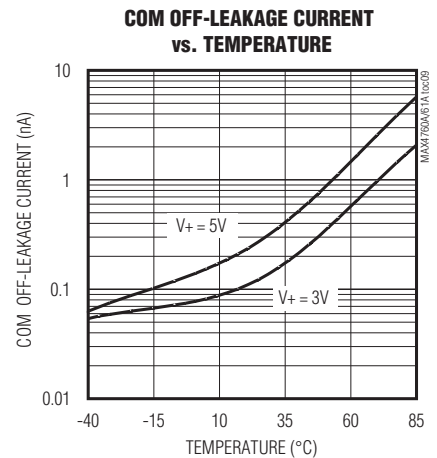
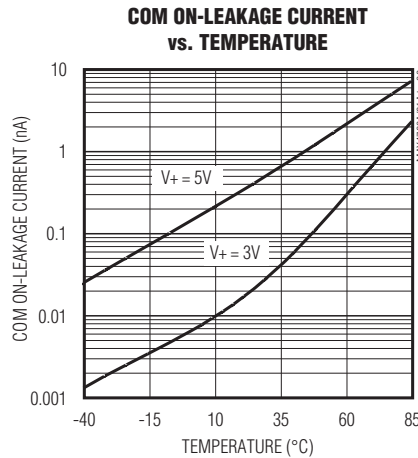
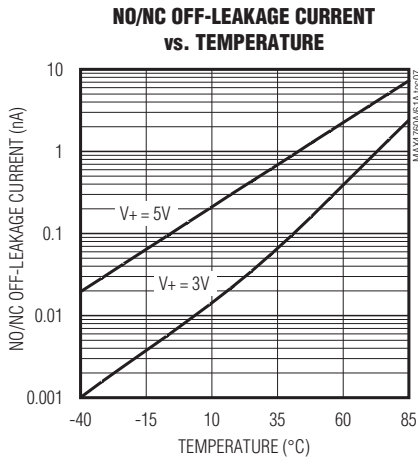
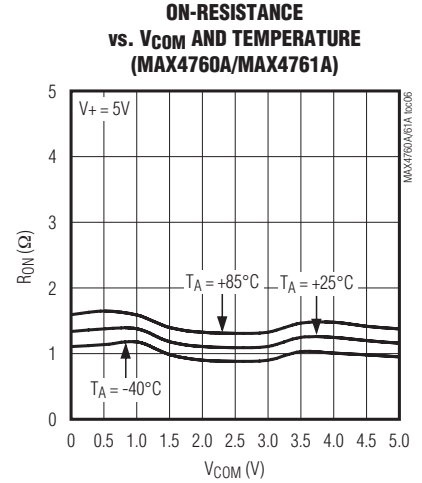
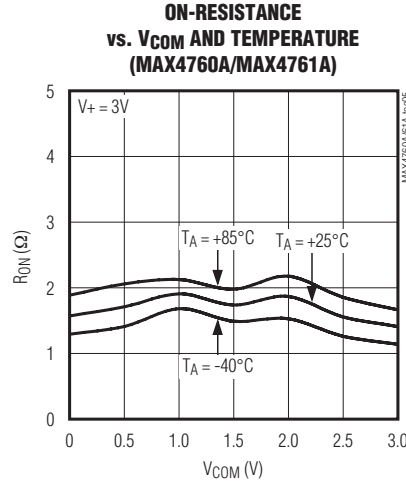
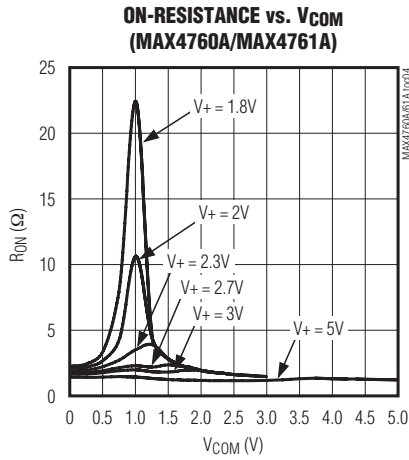


High-Bandwidth, Quad DPDT Switches

Typical Operating Characteristics (continued)

($V_+ = 3V$, $T_A = +25^\circ C$, unless otherwise noted.)

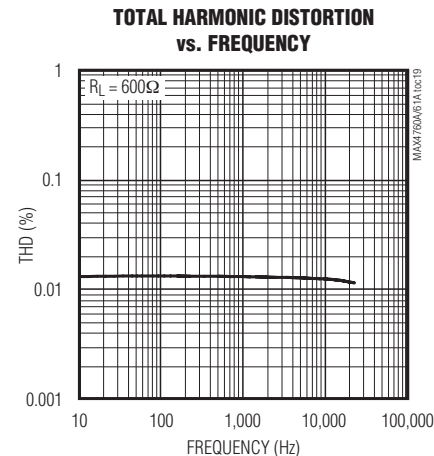
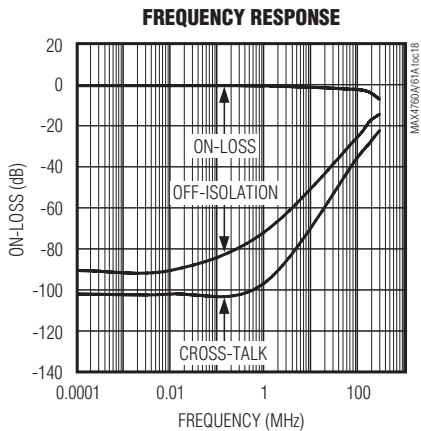
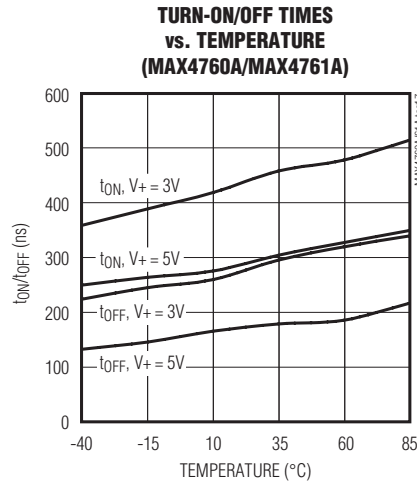
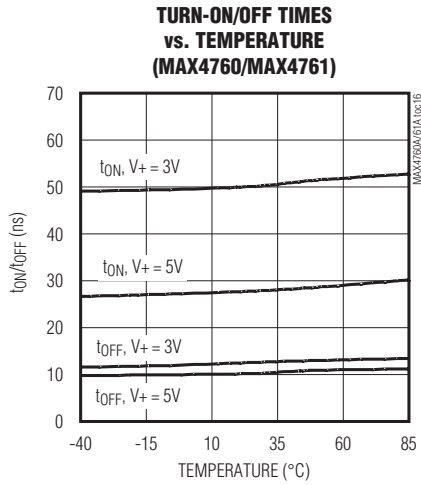
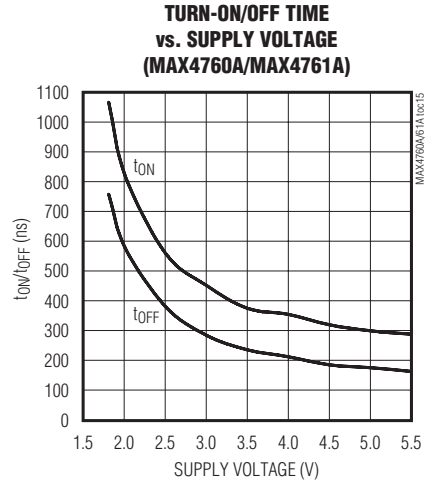
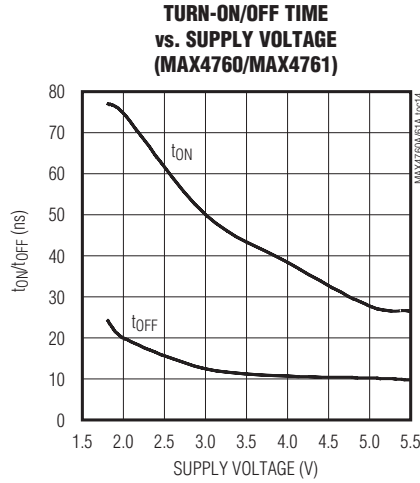
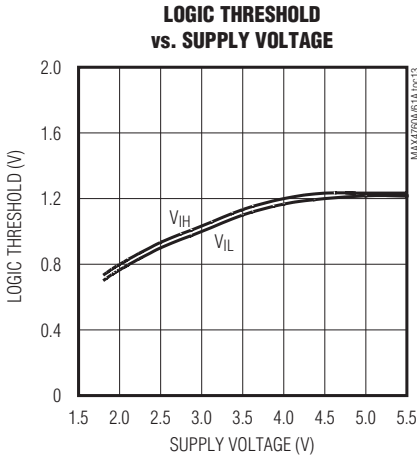
MAX4760/MAX4760A/MAX4761/MAX4761A



High-Bandwidth, Quad DPDT Switches

Typical Operating Characteristics (continued)

($V_+ = 3V$, $T_A = +25^\circ C$, unless otherwise noted.)



High-Bandwidth, Quad DPDT Switches

Pin Description

PIN				NAME	FUNCTION
MAX4760/MAX4760A		MAX4761/MAX4761A			
TQFN-EP	UCSP	TQFN-EP	UCSP		
1	A1	1	A1	NC1	Analog Switch 1, Normally Closed Terminal 1
2	B2	2	B2	COM2	Analog Switch 2, Common Terminal 2
3	A2	3	A2	NC2	Analog Switch 2, Normally Closed Terminal 2
4	A3	4	A3	INA	Logic Control Digital Input for the MAX4760/MAX4760A Switch 1 and Switch 2. Digital control input for all MAX4761/MAX4761A switches.
5	C3, D4	5	C3, D4	V+	Positive Supply Voltage
6	A4	—	—	INB	Logic Control Digital Input for Switches 3 and 4
7	A5	7	A5	NC3	Analog Switch 3, Normally Closed Terminal 3
8	B5	8	B5	COM3	Analog Switch 3, Common Terminal 3
9	A6	9	A6	NC4	Analog Switch 4, Normally Closed Terminal 4
10	B6	10	B6	COM4	Analog Switch 4, Common Terminal 4
11, 14, 17, 29, 32, 35	—	6, 11, 14, 17, 24, 29, 32, 35	A4, F3	N.C.	No Connection. Leave N.C. unconnected.
12	C5	12	C5	NO3	Analog Switch 3, Normally Open Terminal 3
13	C6	13	C6	NO4	Analog Switch 4, Normally Open Terminal 4
15	D6	15	D6	NO8	Analog Switch 8, Normally Open Terminal 8
16	D5	16	D5	NO7	Analog Switch 7, Normally Open Terminal 7
18	E6	18	E6	COM8	Analog Switch 8, Common Terminal 8
19	F6	19	F6	NC8	Analog Switch 8, Normally Closed Terminal 8
20	E5	20	E5	COM7	Analog Switch 7, Common Terminal 7
21	F5	21	F5	NC7	Analog Switch 7, Normally Closed Terminal 7
22	F4	—	—	IND	Logic Control Digital Input for Switches 7 and 8
23	C4, D3	23	C4, D3	GND	Ground
24	F3	—	—	INC	Logic Control Digital Input for Switches 5 and 6
25	F2	25	F2	NC6	Analog Switch 6, Normally Closed Terminal 6
26	E2	26	E2	COM6	Analog Switch 6, Common Terminal 6
27	F1	27	F1	NC5	Analog Switch 5, Normally Closed Terminal 5
28	E1	28	E1	COM5	Analog Switch 5, Common Terminal 5
30	D2	30	D2	NO6	Analog Switch 6, Normally Open Terminal 6
31	D1	31	D1	NO5	Analog Switch 5, Normally Open Terminal 5
33	C1	33	C1	NO1	Analog Switch 1, Normally Open Terminal 1
34	C2	34	C2	NO2	Analog Switch 2, Normally Open Terminal 2
36	B1	36	B1	COM1	Analog Switch 1, Common Terminal 1
—	—	22	F4	EN	Output Enable, Active Low
—	—	—	—	EP	Exposed Pad (TQFN Only). Connect EP to GND.

MAX4760/MAX4760A/MAX4761/MAX4761A

High-Bandwidth, Quad DPDT Switches

Detailed Description

The MAX4760/MAX4760A quad double-pole/double-throw (DPDT) and the MAX4761/MAX4761A octal single-pole/double-throw (SPDT) analog switches operate from a single +1.8V to +5.5V supply. These devices are fully specified for +3V applications.

The MAX4760/MAX4760A/MAX4761/MAX4761A have a guaranteed 2.0Ω (typ) on-resistance to switch data or audio signals. The low 54pF (typ) capacitance and 0.2ns change in skew makes them ideal for data switching applications. The MAX4760/MAX4760A have four logic inputs to control two switches in pairs and the MAX4761/MAX4761A have one logic control input and an enable input (\overline{EN}) to disable the switches.

Applications Information

Digital Control Inputs

The MAX4760/MAX4760A/MAX4761/MAX4761A logic inputs accept up to +5.5V regardless of the supply voltage. For example, with a +3.3V supply, IN_+ can be driven low to GND and high to +5.5V, which allows mixed logic levels in a system. Driving the control logic inputs rail-to-rail also minimizes power consumption.

For the MAX4761/MAX4761A, drive \overline{EN} low to enable. When \overline{EN} is high, COM_+ is high impedance.

Analog Signal Levels

Analog signal inputs over the full voltage range (0V to V_+) are passed through the switch with minimal change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional so NO_+ , NC_+ , and COM_+ can be either inputs or outputs.

Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V_+ supply to other components. A 0.1 μ F capacitor connected from V_+ to GND is adequate for most applications.

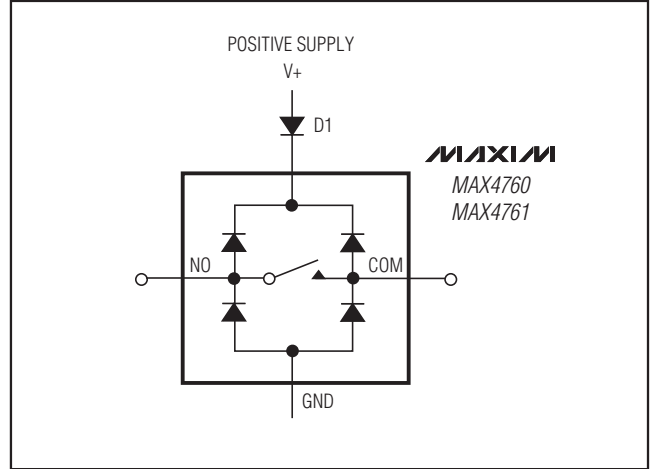


Figure 1. Overvoltage Protection Using an External Blocking Diode

Power-Supply Sequencing

CMOS devices require proper power-supply sequencing. Always apply V_+ before the analog signals, especially if the input signal is not current limited. If sequencing is not possible, and the input signal is not current limited to less than 20mA, add a small-signal diode (Figure 1). Adding the diode reduces the analog range to a diode drop (0.7V) below V_+ and increases the on-resistance slightly. The maximum supply voltage must not exceed +6V at any time.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications* available on Maxim's website at www.maxim-ic.com/ucsp.

High-Bandwidth, Quad DPDT Switches

Timing Circuits/Timing Diagrams

MAX4760/MAX4760A/MAX4761/MAX4761A

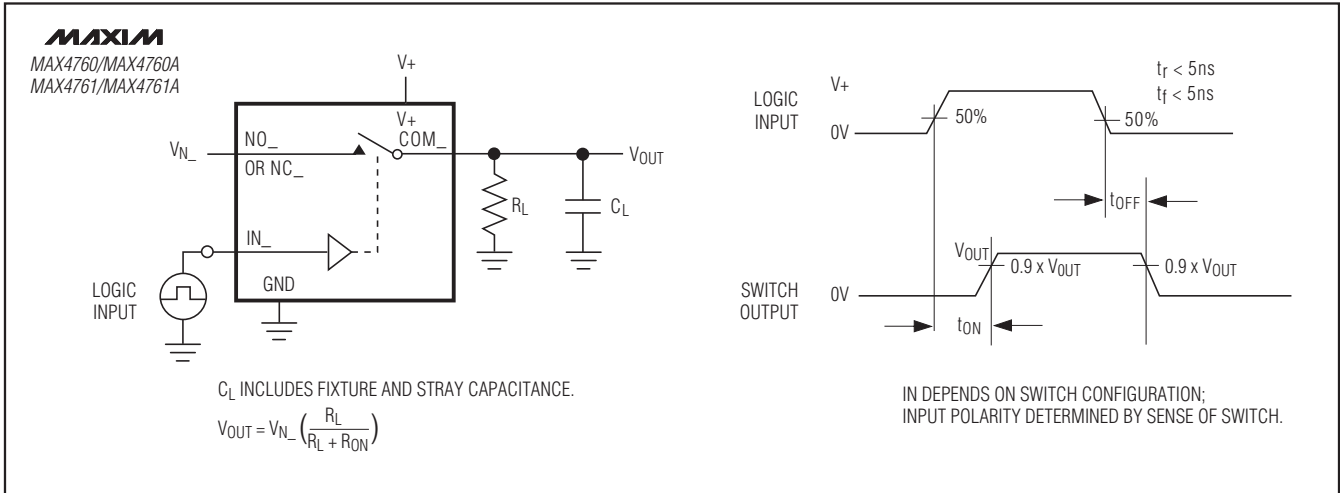


Figure 2. Switching Time

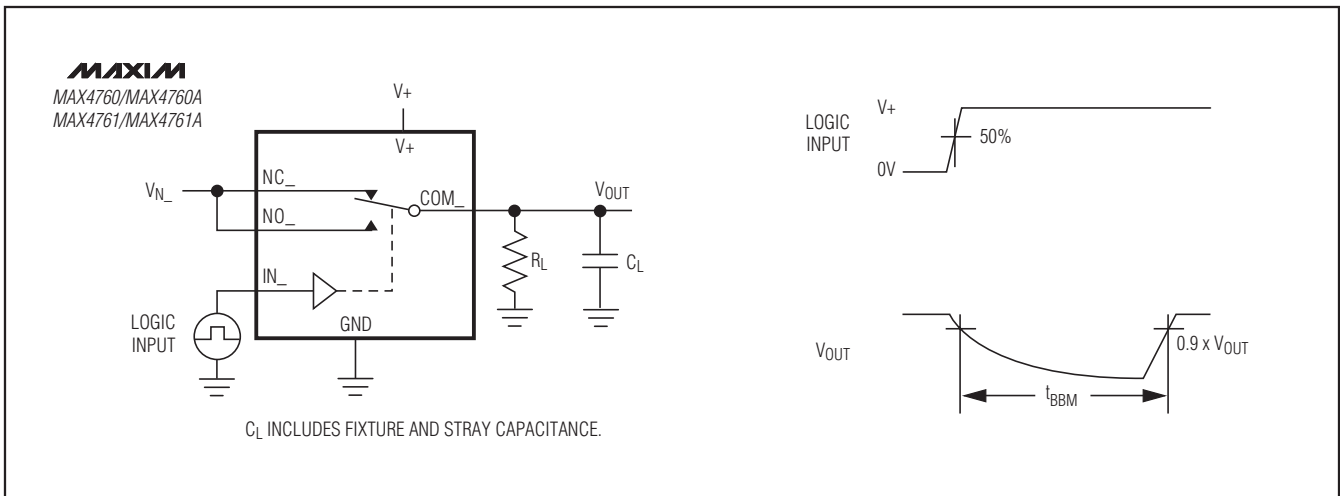


Figure 3. Break-Before-Make Interval

High-Bandwidth, Quad DPDT Switches

Timing Circuits/Timing Diagrams (continued)

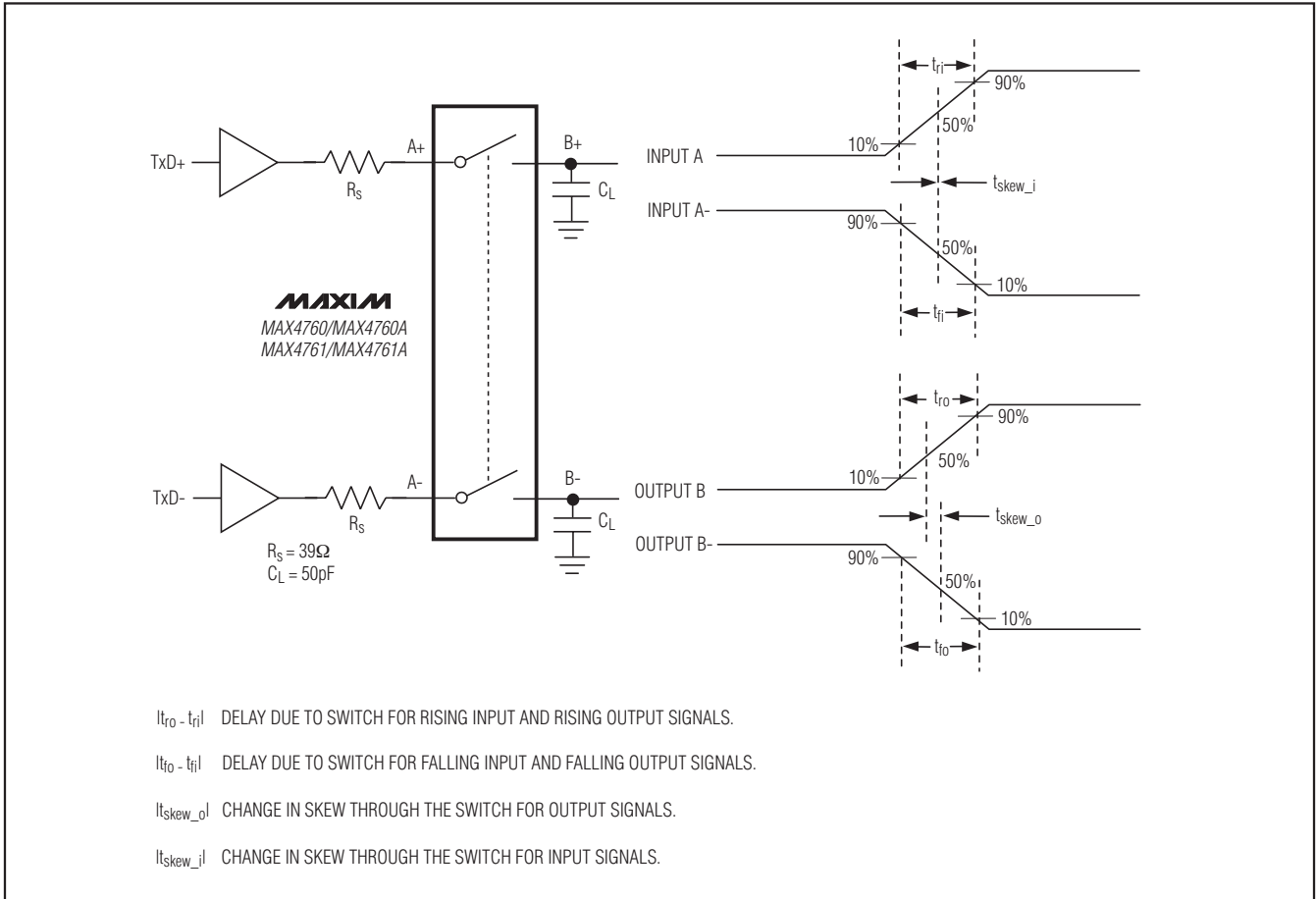


Figure 4. Input/Output Skew Timing Diagram

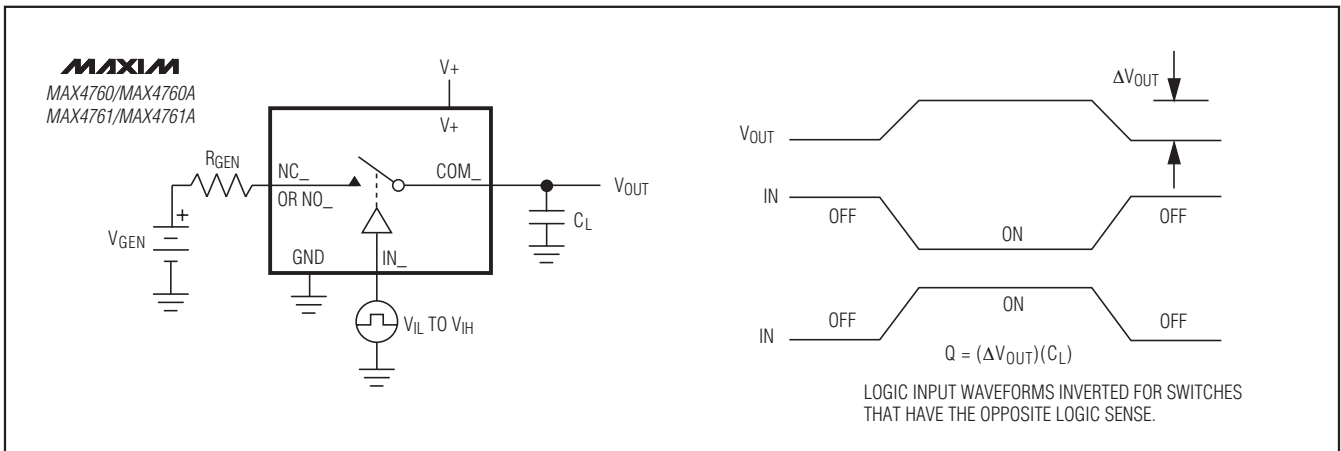


Figure 5. Charge Injection

High-Bandwidth, Quad DPDT Switches

MAX4760/MAX4760A/MAX4761/MAX4761A

Timing Circuits/Timing Diagrams (continued)

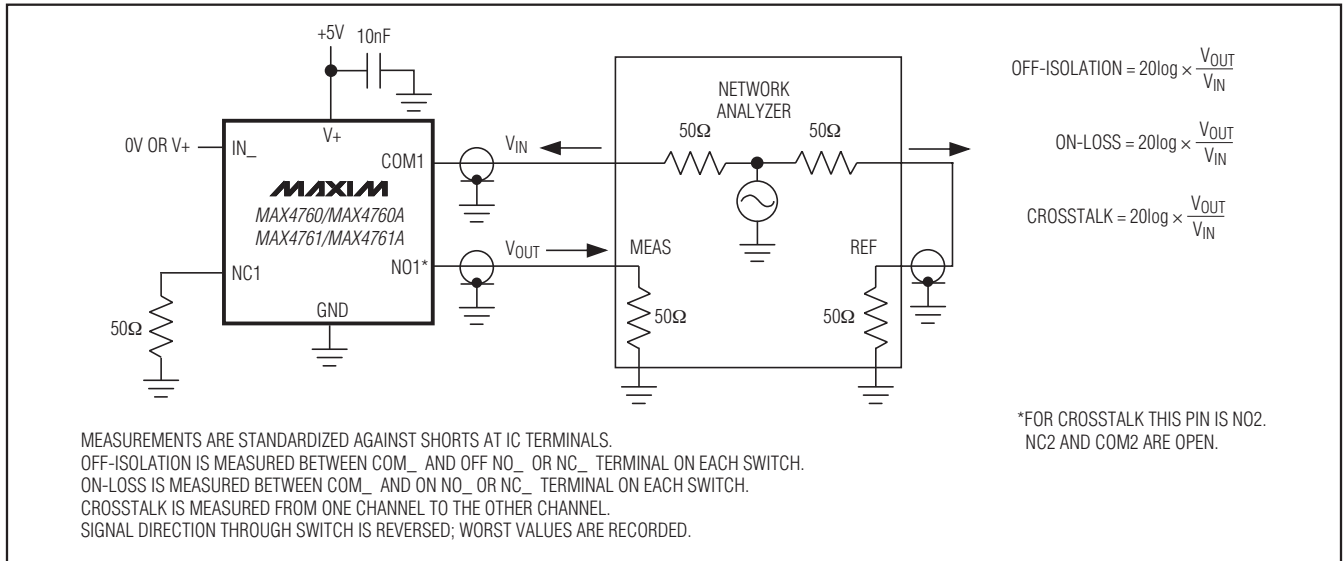


Figure 6. On-Loss, Off-Isolation, and Crosstalk

Typical Operating Circuit

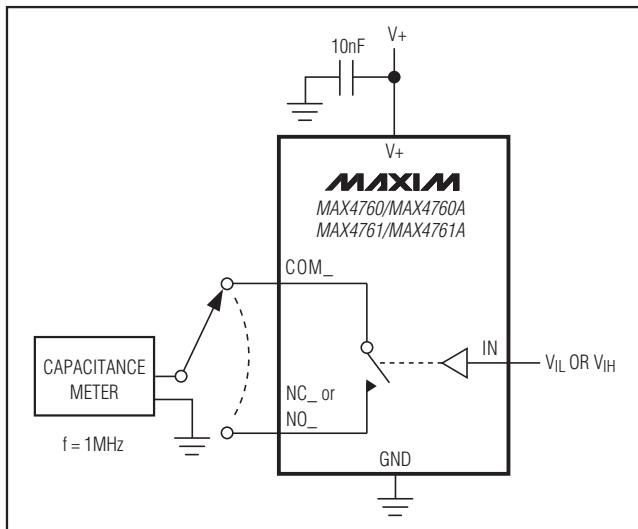
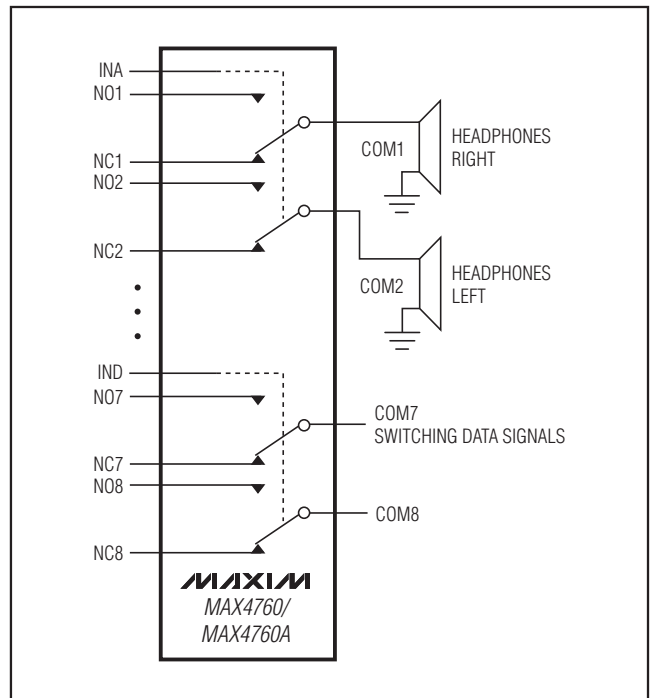


Figure 7. Channel On-/Off-Capacitance



High-Bandwidth, Quad DPDT Switches

Pin Configurations/Truth Tables

TOP VIEW

MAXIM
MAX4760/MAX4760A

(BUMP SIDE DOWN)

UCSP

TQFN

*EXPOSED PADDLE CONNECTED TO GND.

INA	NO1/NO2	NC1/NC2
LOW	OFF	ON
HIGH	ON	OFF
INB	NO3/NO4	NC3/NC4
LOW	OFF	ON
HIGH	ON	OFF
INC	NO5/NO6	NC5/NC6
LOW	OFF	ON
HIGH	ON	OFF
IND	NO7/NO8	NC7/NC8
LOW	OFF	ON
HIGH	ON	OFF

High-Bandwidth, Quad DPDT Switches

Pin Configurations/Truth Tables (continued)

MAX4760/MAX4760A/MAX4761/MAX4761A

TOP VIEW

MAXIM
MAX4761/MAX4761A

(BUMP SIDE DOWN)

1 2 3 4 5 6

A	NC1	NC2	INA	N.C.	NC3	NC4
B	COM1	COM2			COM3	COM4
C	NO1	NO2	V+	GND	NO3	NO4
D	NO5	NO6	GND	V+	NO7	NO8
E	COM5	COM6			COM7	COM8
F	NC5	NC6	N.C.	EN	NC7	NC8

UCSP

	COM1	N.C.	NO2	NO1	N.C.	NO5	NO6	N.C.	COM5
+	36	35	34	33	32	31	30	29	28
NC1	1								27
COM2	2								26
NC2	3								25
INA	4								24
V+	5								23
N.C.	6								22
NC3	7								21
COM3	8								20
NC4	9								19
	10	11	12	13	14	15	16	17	18
COM4		N.C.	NO3	NO4	N.C.	NO8	NO7	N.C.	COM8

TQFN

*EXPOSED PADDLE CONNECTED TO GND.

MAX4761/MAX4761A

EN	INA	NO ₋	NC ₋
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF
HIGH	X	OFF	OFF

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 UCSP	B36-2	21-0082
36 TQFN-EP	T3666-3	21-0141

High-Bandwidth, Quad DPDT Switches

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	4/07	Addition of MAX4760A/MAX4761A	1–14
5	4/09	Revised <i>Ordering Information</i> , <i>Electrical Characteristics</i> table, and <i>Pin Description</i> .	1, 3, 7

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