19-0624; Rev 0; 8/06

1000 Base-T, ±15kV ESD Protection LAN Switches

General Description

The MAX4890E/MAX4892E meet the needs of high-speed differential switching. The devices handle the needs of Gigabit Ethernet (10/100/1000) Base-T switching as well as LVDS and LVPECL switching. The MAX4890E/MAX4892E provide enhanced ESD protection up to ±15kV, and excellent high-frequency response, making the devices especially useful for interfaces that must go to an outside connection.

Both devices provide extremely low capacitance (C_{ON}), as well as low resistance (R_{ON}), for low-insertion loss and very wide bandwidth. In addition to the four pairs of DPDT switches, the MAX4892E provides LED switching for laptop computer/docking station use.

The MAX4890E/MAX4892E are pin-for-pin equivalents to the MAX4890/MAX4892 and can replace these devices for those applications requiring the enhanced ESD protection. Both devices are available in space-saving TQFN packages and operate over the standard -40°C to +85°C temperature range.

Applications

Notebooks and Docking Stations

Servers and Routers with Ethernet Interfaces

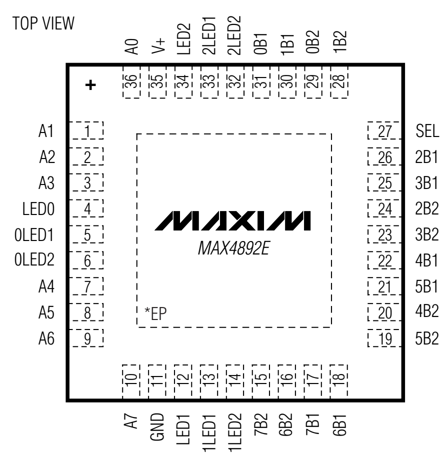
Board-Level Redundancy Protection

SONET/SDH Signal Routing

T3/E3 Redundancy Protection

LVDS and LVPECL Switching

Pin Configurations



TQFN

*EXPOSED PAD CONNECTED TO GND.

Pin Configurations continued at end of data sheet.

Features

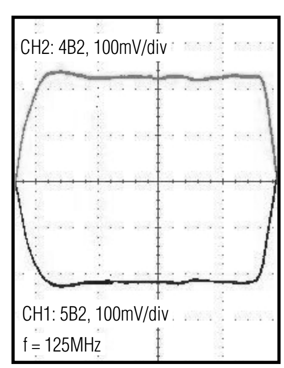
- ♦ ±15kV ESD Protected Per MIL-STD-883, Method 3015
- ♦ Single +3.0V to +3.6V Power-Supply Voltage
- ♦ Low On-Resistance (R_{ON}): 4Ω (typ), 6.5Ω (max)
- ♦ Ultra-Low On-Capacitance (C_{ON}): 8pF (typ)
- ♦ -23dB Return Loss (100MHz)
- ♦ -3dB Bandwidth: 650MHz
- ♦ Optimized Pin Out for Easy Transformer and PHY Interface
- ♦ Built-In LED Switches for Switching Indicators to Docking Station (MAX4892E)
- ♦ Low 450µA (max) Quiescent Current
- ♦ Bidirectional 8 to 16 Multiplexer/Demultiplexer
- ♦ Standard Pin Out, Matching the MAX4890 and MAX4892
- ♦ Space-Saving Lead-Free Packages
  - 32-Pin, 5mm x 5mm, TQFN Package
  - 36-Pin, 6mm x 6mm, TQFN Package

Ordering Information

PART	PIN-PACKAGE	LED SWITCHES	PKG CODE
MAX4890EETJ+	32 TQFN-EP*	—	T-3255-4
MAX4892EETX+	36 TQFN-EP*	3	T-3666-3

+Denotes lead-free package.
***Note:** All devices are specified over the -40°C to +85°C operating temperature range.*
**EP = Exposed pad.*

Eye Diagram



Typical Operating Circuit and Functional Diagrams appear at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V+ .... -0.3V to +4V
All Other Pins.. -0.3V to (V+ + 0.3V)
Continuous Current (A_ to _B_)......................................±120mA
Continuous Current (LED_ to _LED_) .... ±40mA
Peak Current (A_ to _B_)
(pulsed at 1ms, 10% duty cycle) .... ±240mA
Current into Any Other Pin..±20mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) 2.76W
36-Pin TQFN (derate 35.7mW/°C above +70°C) 2.85W
ESD Protection, Human Body Model ....±15kV

Operating Temperature Range .... -40°C to +85°C
Junction Temperature.. +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +3V to +3.6V, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
On-Resistance	R_{ON}	V+ = 3V, $I_{A\_}$ = -40mA, $V_{A\_}$ = 0, 1.5V, 3V	T_A = +25°C		4	5.5	Ω
			T_{MIN} to T_{MAX}			6.5	
On-Resistance LED Switches	R_{ONLED}	V+ = 3V, $I_{LED\_}$ = -40mA, $V_{LED\_}$ = 0, 1.5V, 3V (MAX4892E)				40	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 3V, $I_{A\_}$ = -40mA, $V_{A\_}$ = 0, 1.5V, 3V (Note 2)	T_A = +25°C		0.5	1.5	Ω
			T_{MIN} to T_{MAX}			2	
On-Resistance Flatness	$R_{FLAT(ON)}$	V+ = 3V, $I_{A\_}$ = -40mA, $V_{A\_}$ = 1.5V, 3V			0.01		Ω
Off-Leakage Current	$I_{LA\_(OFF)}$	V+ = 3.6V, $V_{A\_}$ = 0.3V, 3.3V; $V_{\_B1}$ or $V_{\_B2}$ = 3.3V, 0.3V		-1		+1	µA
On-Leakage Current	$I_{LA\_(ON)}$	V+ = 3.6V, $V_{A\_}$ = 0.3V, 3.3V; $V_{\_B1}$ or $V_{\_B2}$ = 0.3V, 3.3V or floating		-1		+1	
ESD PROTECTION							
ESD Protection		Human Body Model (spec MIL-STD-883, Method 3015)			±15		kV
SWITCH AC PERFORMANCE							
Insertion Loss	I_{LOS}	$R_S = R_L$ = 50Ω, unbalanced, f = 1MHz, (Note 2)			0.6		dB
Return Loss	R_{LOS}	f = 100MHz			-23		dB

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +3V to +3.6V, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

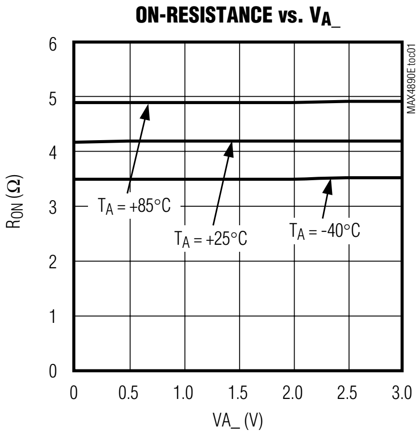
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk	V_{CT1}	Any switch to any switch; $R_S = R_L$ = 50Ω, unbalanced, Figure 1	f = 25MHz		-50		dB
	V_{CT2}		f = 125MHz		-26		
SWITCH AC CHARACTERISTIC							
-3dB Bandwidth	BW	$R_S = R_L$ = 50Ω, unbalanced			650		MHz
Off-Capacitance	C_{OFF}	f = 1MHz, _B_, A_			3.5		pF
On-Capacitance	C_{ON}	f = 1MHz, _B_, A_			6.5		pF
Turn-On Time	t_{ON}	$V_{A\_}$ = 1V, R_L, 100Ω, Figure 2				50	ns
Turn-Off Time	t_{OFF}	$V_{A\_}$ = 1V, R_L, 100Ω, Figure 2				50	ns
Propagation Delay	t_{PLH}, t_{PHL}	$R_S = R_L$ = 50Ω, unbalanced, Figure 3			0.1		ns
Output Skew Between Ports	$t_{SK(o)}$	Skew between any two ports, Figure 4			0.01		ns
SWITCH LOGIC							
Input-Voltage Low	V_{IL}	V+ = 3.0V				0.8	V
Input-Voltage High	V_{IH}	V+ = 3.6V		2.0			
Input-Logic Hysteresis	V_{HYST}	V+ = 3.3V			100		mV
Input Leakage Current	I_{SEL}	V+ = 3.6V, V_{SEL} = 0 or V+		-5		+5	µA
Operating Supply-Voltage Range	V+			3.0		3.6	V
Quiescent Supply Current	I+	V+ = 3.6V, V_{SEL} = 0 or V+			280	450	µA

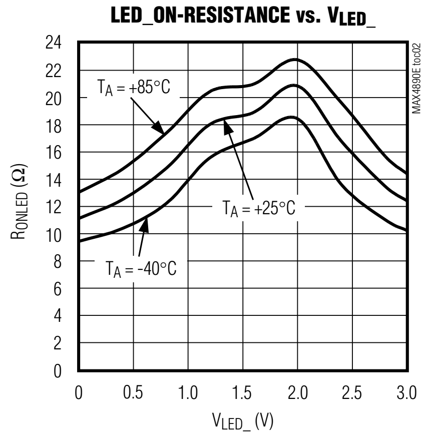
Note 1: Specifications at -40°C are guaranteed by design.
Note 2: Guaranteed by design.

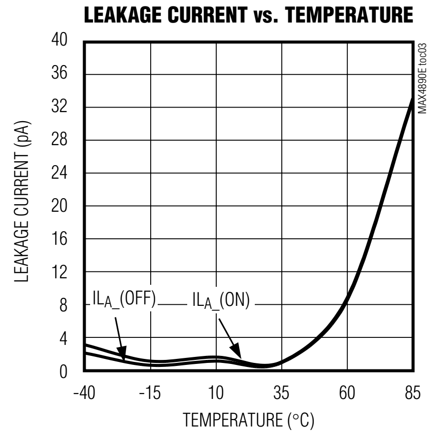
1000 Base-T, ±15kV ESD Protection LAN Switches

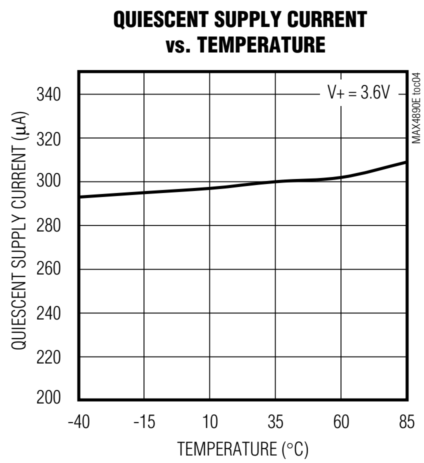
Typical Operating Characteristics

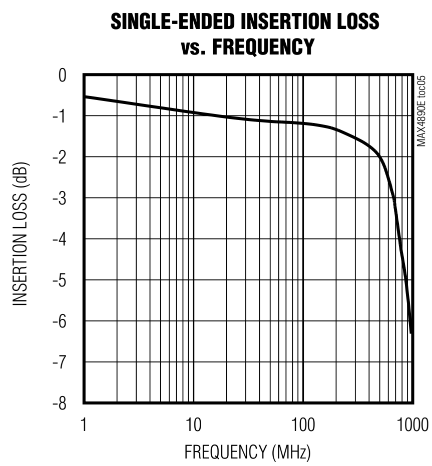
(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)











Pin Description

PIN		NAME	FUNCTION
MAX4892E	MAX4890E		
1	32	A1	Differential PHY Interface Pair. Connect to the Ethernet PHY.
2	1	A2	Differential PHY Interface Pair. Connect to the Ethernet PHY.
3	2	A3	Differential PHY Interface Pair. Connect to the Ethernet PHY.
4	—	LED0	LED0 Input
5	—	0LED1	0LED1 Output. Drive SEL low (SEL = 0) to connect LED0 to 0LED1.
6	—	0LED2	0LED2 Output. Drive SEL high (SEL = 1) to connect LED0 to 0LED2.
7	7	A4	Differential PHY Interface Pair. Connect to the Ethernet PHY.
8	8	A5	Differential PHY Interface Pair. Connect to the Ethernet PHY.
9	9	A6	Differential PHY Interface Pair. Connect to the Ethernet PHY.
10	10	A7	Differential PHY Interface Pair. Connect to the Ethernet PHY.
11	11	GND	Ground
12	—	LED1	LED1 Input
13	—	1LED1	1LED1 Output. Drive SEL low (SEL = 0) to connect LED1 to 1LED1.
14	—	1LED2	1LED2 Output. Drive SEL high (SEL = 1) to connect LED1 to 1LED2.
15	13	7B2	B2 Differential Pair
16	14	6B2	B2 Differential Pair
17	15	7B1	B1 Differential Pair
18	16	6B1	B1 Differential Pair
19	17	5B2	B2 Differential Pair
20	18	4B2	B2 Differential Pair
21	19	5B1	B1 Differential Pair
22	20	4B1	B1 Differential Pair
23	21	3B2	B2 Differential Pair
24	22	2B2	B2 Differential Pair
25	23	3B1	B1 Differential Pair
26	24	2B1	B1 Differential Pair
27	29	SEL	Select Input. SEL selects switch connection. See the Truth Table (Table1).
28	25	1B2	B2 Differential Pair
29	26	0B2	B2 Differential Pair
30	27	1B1	B1 Differential Pair
31	28	0B1	B1 Differential Pair
32	—	2LED2	2LED2 Output. Drive SEL high (SEL = 1) to connect LED2 to 2LED2.
33	—	2LED1	2LED1 Output. Drive SEL low (SEL = 0) to connect LED2 to 2LED1.
34	—	LED2	LED2 Input
35	30	V+	Positive-Supply Voltage Input. Bypass to GND with a 0.1µF ceramic capacitor.
36	31	A0	Differential PHY Interface Pair. Connect to the Ethernet PHY.
—	3-6, 12	N.C.	No Connection. Not internally connected.
—	—	EP	Exposed Pad. Connect exposed pad to GND or leave it unconnected.

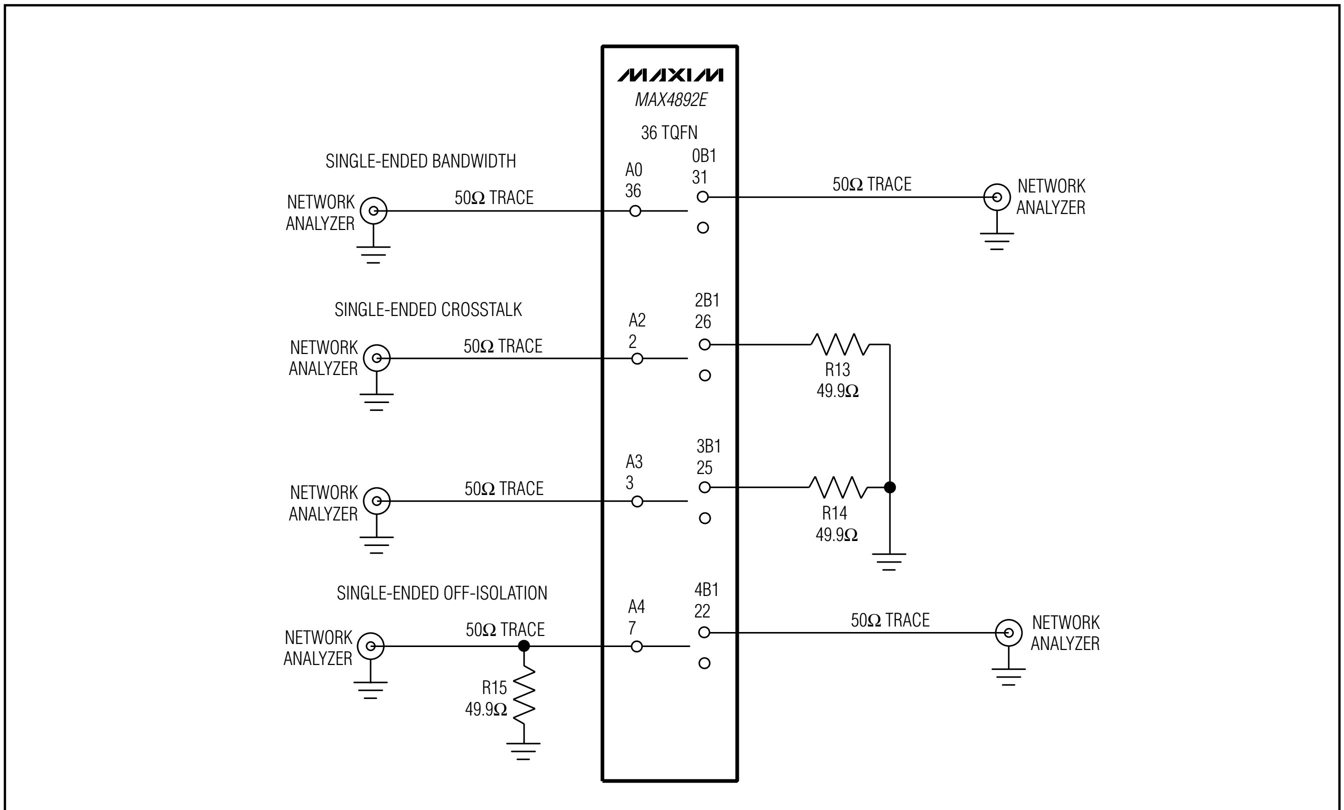


Figure 1. Single-Ended Bandwidth, Crosstalk, and Off-Isolation

Detailed Description

The MAX4890E/MAX4892E are high-speed analog switches targeted for 1000 Base-T applications. In a typical application, the MAX4890E/MAX4892E switch the signals from two separate interface transformers and connect the signals to a single 1000 Base-T Ethernet PHY (see the *Typical Operating Circuit*). This configuration simplifies docking station design by avoiding signal reflections associated with unterminated transmission lines in a T configuration. The MAX4890E/MAX4892E are protected against ±15kV electrostatic discharge (ESD) shocks. The MAX4892E also includes LED switches that allow the LED output signals to be routed to a docking station along with the Ethernet signals. See the *Functional Diagrams.*

With their low resistance and capacitance, as well as high ESD protection, the MAX4890E/MAX4892E can be used to switch most low-voltage differential signals, such as LVDS, SEREDES, and LVPECL, as long as the signals do not exceed maximum ratings of the devices.

The MAX4890E/MAX4892E switches provide an extremely low capacitance and on-resistance to meet Ethernet insertion and return-loss specifications. The MAX4892E features three built-in LED switches.

The MAX4890E/MAX4892E incorporate a unique architecture design utilizing only n-channel switches within the main Ethernet switch, reducing I/O capacitance and channel resistance. An internal two-stage charge pump with a nominal output of 7.5V provides the high voltage needed to drive the gates of the n-channel switches while maintaining a consistently low R_{ON} throughout the input signal range. An internal bandgap reference set to 1.23V and an internal oscillator running at 2.5MHz provide proper charge-pump operation. Unlike other charge-pump circuits, the MAX4890E/MAX4892E include internal flyback capacitors, reducing design time, board space, and cost.

Table 1. Truth Table

SEL	CONNECTION
0	A_ to _B1, LED_ to _LED1
1	A_ to _B2, LED_ to _LED2

Digital Control Inputs

The MAX4890E/MAX4892E provide a single digital control SEL. SEL controls the switches as well as the LED switches as shown in Table 1.

Analog Signal Levels

The on-resistance of the MAX4890E/MAX4892E is very low and stable as the analog input signals are swept from ground to V+ (see the *Typical Operating Characteristics*). The switches are bidirectional, allowing A_ and _B_ to be configured as either inputs or outputs.

ESD Protection

The MAX4890E/MAX4892E are characterized using the Human Body Model for ±15kV of ESD protection. Figure 5 shows the Human Body Model. This model consists of a 100pF capacitor charged to the ESD voltage of interest which is then discharged into the test device through a 1.5kΩ resistor. All signal and control pins are ESD protected to ±15kV HBM (Human Body Model).

Applications Information

Typical Operating Circuit

The *Typical Operating Circuit* shows the MAX4890E/MAX4892E in a 1000 Base-T docking station application.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled-impedance pc board traces as short as possible. Ensure that bypass capacitors are as close as possible to the device. Use large ground planes where possible.

Chip Information

PROCESS: BiCMOS

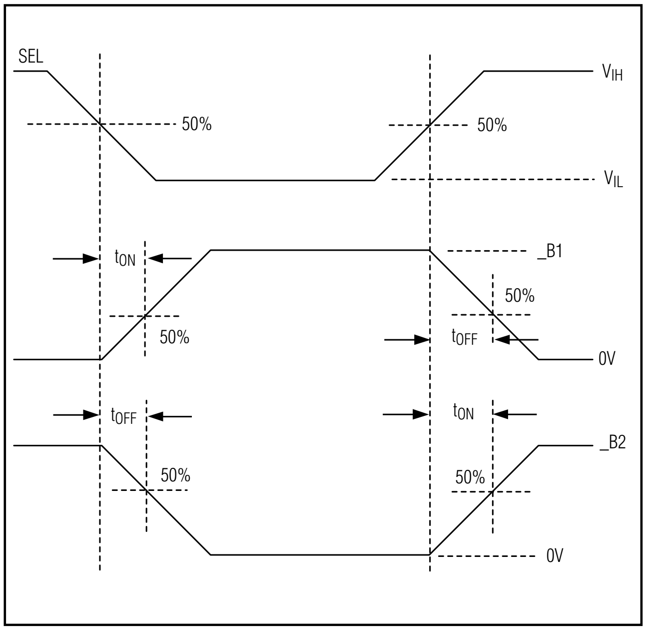


Figure 2. Turn-On and Turn-Off Times

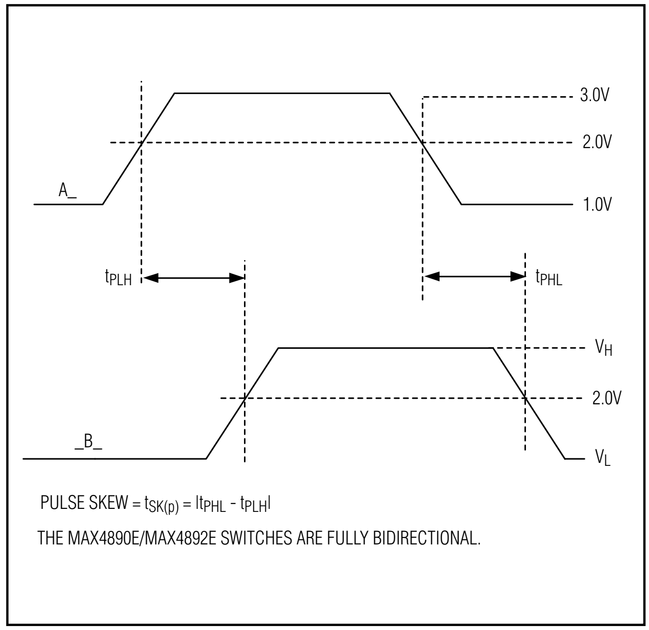


Figure 3. Propagation Delay Times

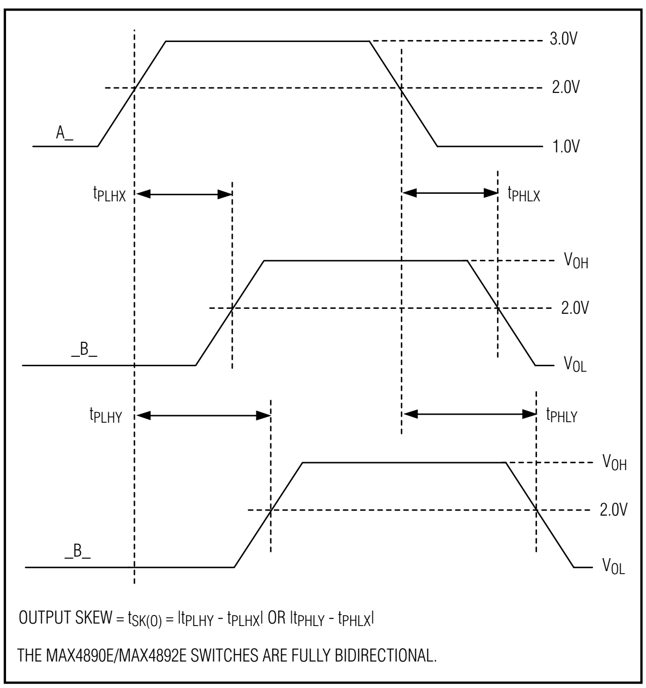


Figure 4. Output Skew

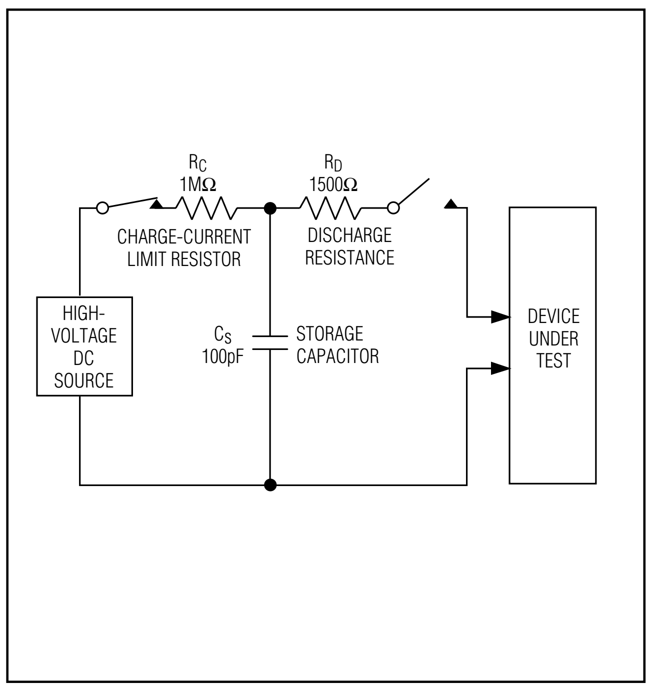
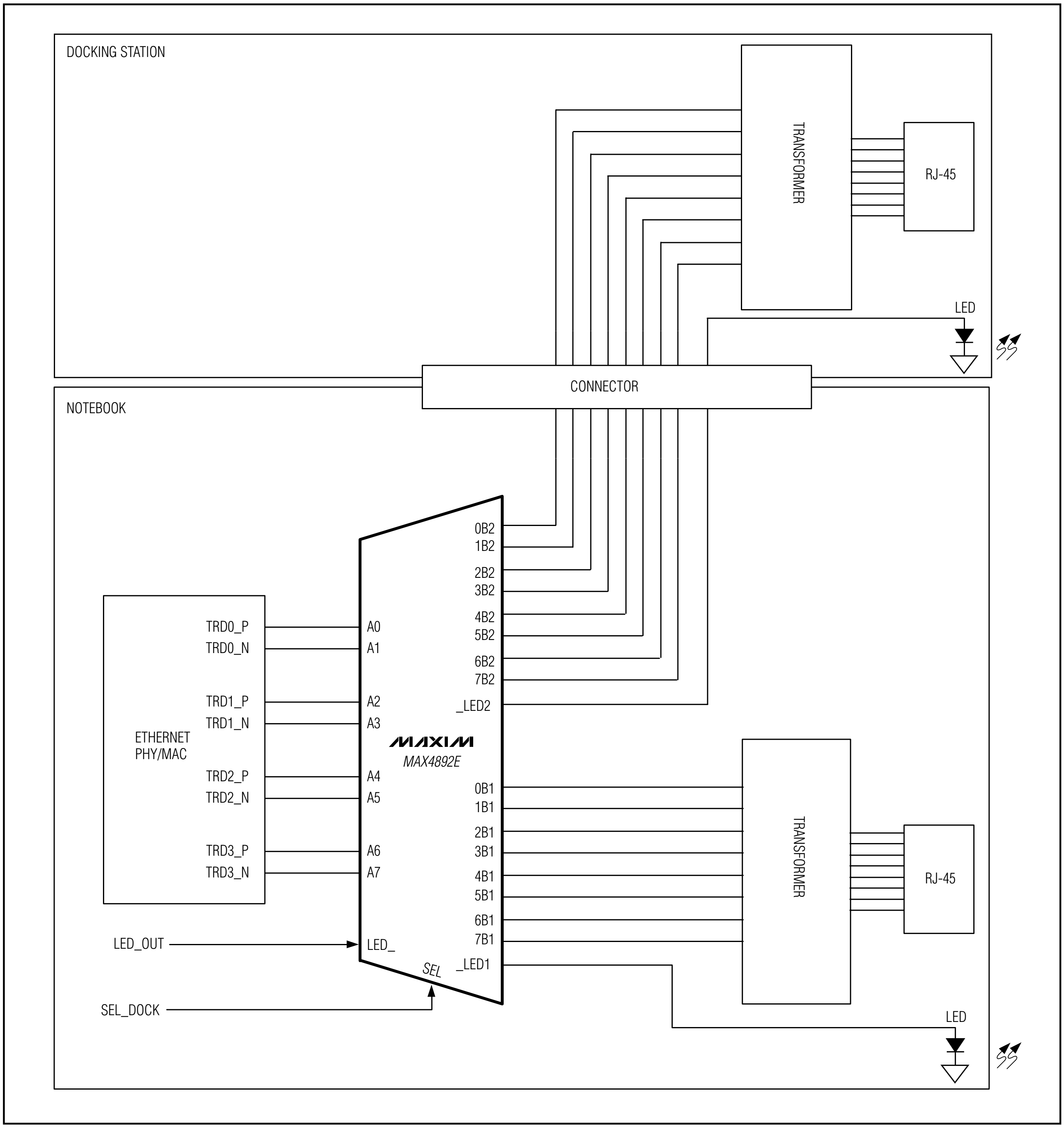
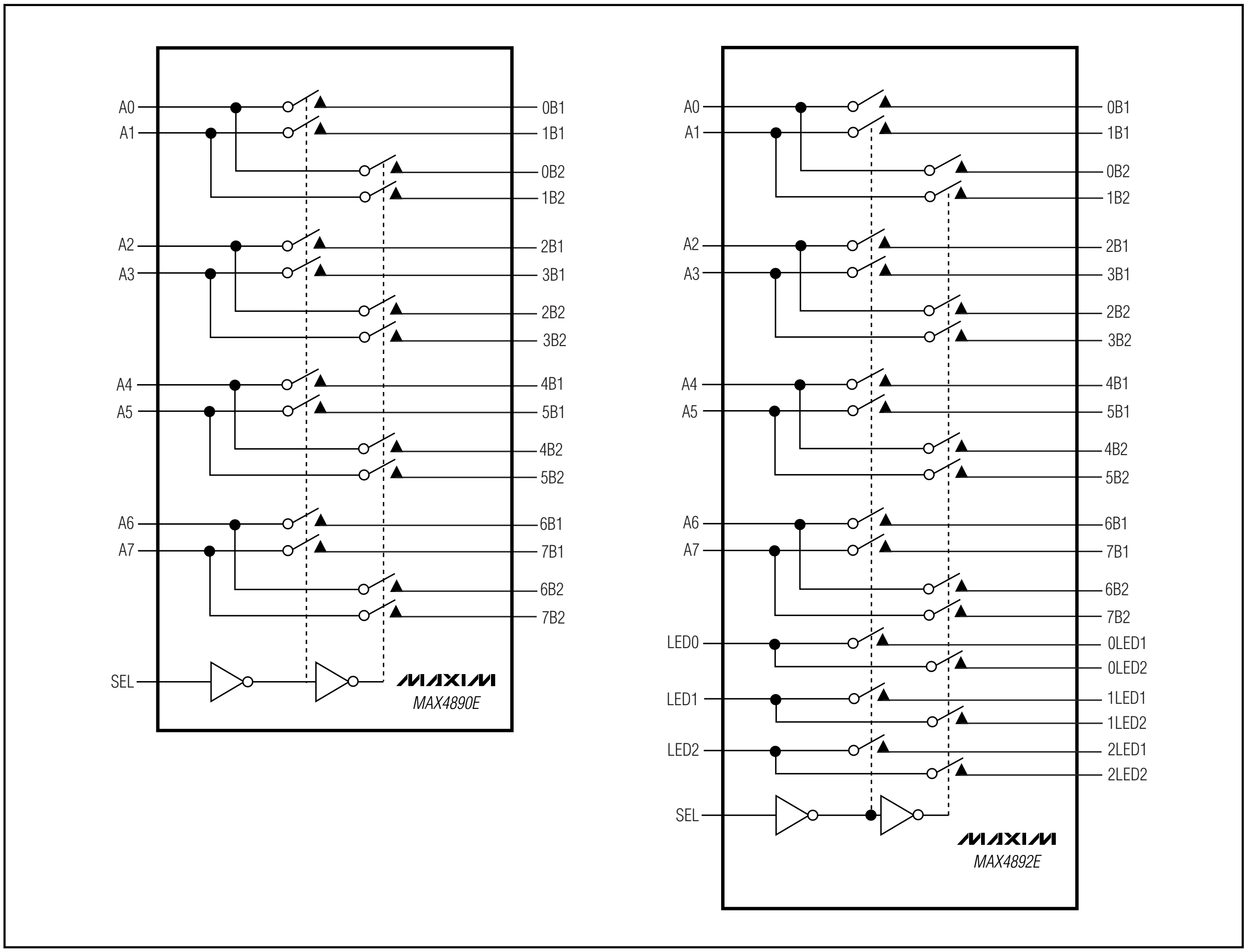


Figure 5. Human Body ESD Test Model (MIL-STD-883, Method 3015)

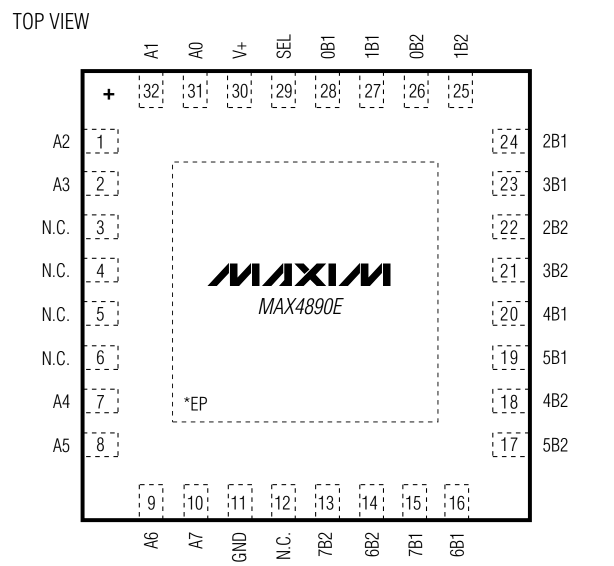
Typical Operating Circuit



Functional Diagrams



Pin Configurations (continued)

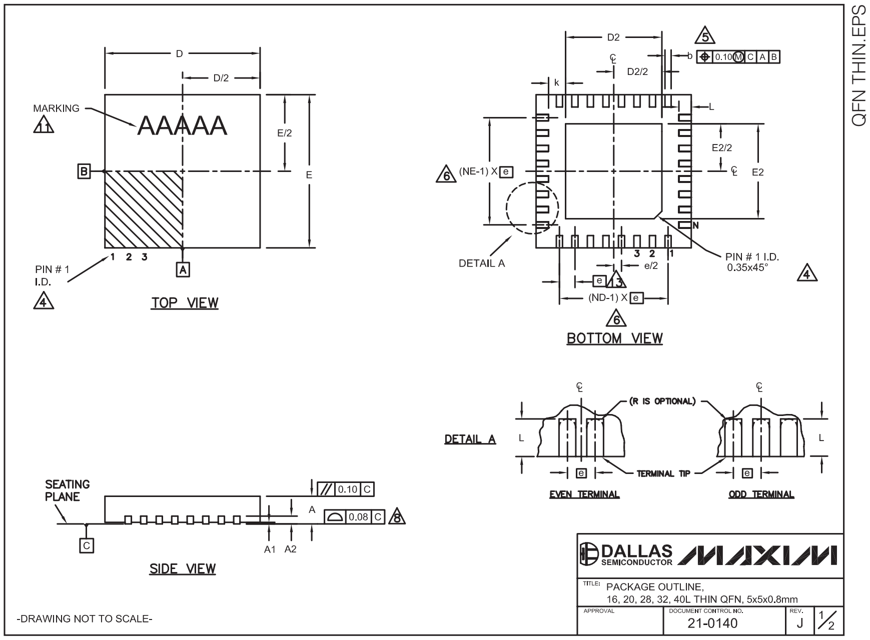


TQFN

*EXPOSED PADDLE CONNECTED TO GND.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

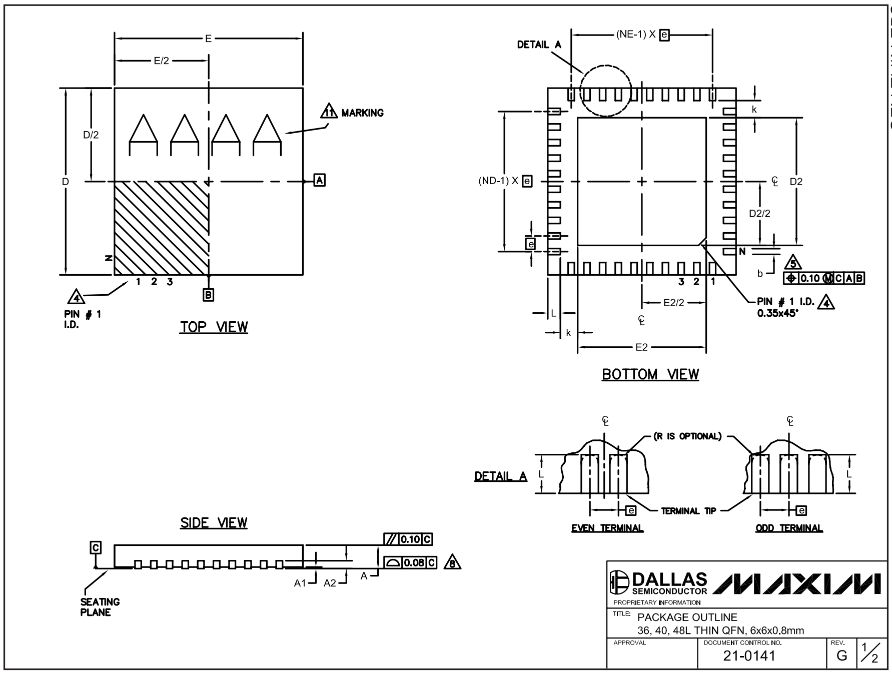
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. J | 2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL | DOCUMENT CONTROL NO. 21-0141 | REV. G | 2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.