19-4591; Rev 0; 4/09

EVALUATION KIT AVAILABLE

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

General Description

The MAX4940/MAX4940A integrated circuits generate high-voltage, high-frequency, unipolar or bipolar pulses from low-voltage logic inputs. These quad/dual pulsers feature independent logic inputs, independent high-voltage pulser outputs with active clamps and independent high-voltage supply inputs.

The MAX4940/MAX4940A feature quad, high-voltage pulsers with 8.5Ω output impedance for the high-voltage outputs and a 21Ω impedance for the active clamp. The high-voltage outputs can provide 2.0A (typ) output current.

All devices use two logic inputs per channel to control the positive and negative pulses. The MAX4940/MAX4940A have a dedicated input to control the active clamp. All devices feature an independent enable input EN. All digital inputs are CMOS compatible (see the *Ordering Information/Selector Guide).*

The MAX4940/MAX4940A are available in a 56-pin, 8mm x 8mm, TQFN exposed pad package and are specified over the 0°C to +70°C commercial temperature range.

Warning: *Exercise caution. The MAX4940/MAX4940A are designed to operate with high voltages.*

Applications

Ultrasound Medical Imaging

Flaw Detection

Piezoelectric Drivers

Test Instruments

Cleaning Equipment

Features

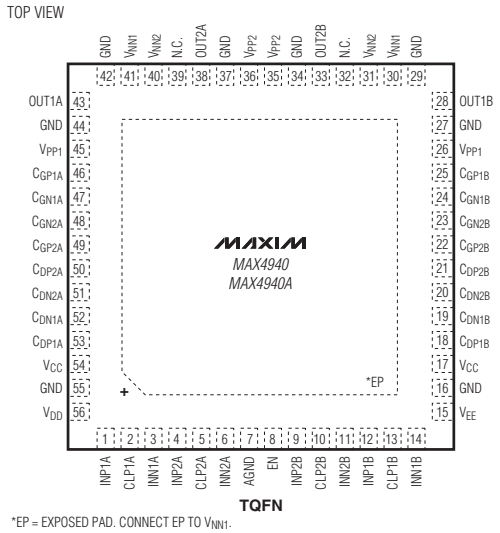
- **High-Density Quad-Channel Pulser in One Package**
- **0 to +220V Unipolar or ±110V Bipolar Outputs**
- **8.5Ω (typ) Output Impedance and 2.0A (typ) Output Current**
- **21Ω (typ) Always-On Active Clamp with Integrated Blocking Diodes**
- **Integrated Output Diodes (MAX4940A Only)**
- **No Special Power-Supply Sequencing Required for Trilevel Applications**
- **Matched Rise/Fall Times and Matched Propagation Delays**
- **CMOS-Compatible Logic Inputs**
- **56-Pin, 8mm x 8mm, TQFN Package**

Ordering Information/ Selector Guide

PART	OUTPUT BLOCKING DIODE	OUTPUT CURRENT (A)	PIN-PACKAGE
MAX4940CTN+	None	2.0 (typ)	56 TQFN-EP*
MAX4940ACTN+	OUT2A, OUT2B	2.0 (typ)	56 TQFN-EP*

Note: *Devices operate over the 0°C to +70°C temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{DD} Logic Supply Voltage .....-0.3V to +6V
V_{CC} Output Driver Positive Supply Voltage.....-0.3V to +15V
V_{EE} Output Driver Negative Supply Voltage .....-15V to +0.3V
$V_{PP\_}$ High-Positive Supply Voltage.....-0.3V to ($V_{NN\_}$ + 220V)
$V_{NN\_}$ Low-Negative Supply Voltage .....-220V to +0.3V
V_{PP1} - V_{NN1}, V_{PP2} - V_{NN2} Supply Voltage .....-0.6V to +250V
INP_, INN_, CLP_, EN Logic Input..... -0.3V to (V_{DD} + 0.3V)
$C_{GN\_}$ Voltage ..... (-0.3V + $V_{NN\_}$) to (+15V + $V_{NN\_}$)
$C_{GP\_}$ Voltage.....(+0.3V + $V_{PP\_}$) to (-15V + $V_{PP\_}$)
$C_{DP\_}$, $C_{DN\_}$ Voltage.....-0.3V to V_{CC}
Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above +70°C).....3809mW
Thermal Resistance (Note 1)
θ_{JA}.....21°C/W
θ_{JC} .....1°C/W
Operating Temperature Range ..... 0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{CC} = +12V, V_{EE} = -12V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V_{DD}, V_{CC}, V_{EE}, $V_{PP\_}$, $V_{NN\_}$)						
Logic Supply Voltage	V_{DD}		2.37	3	6	V
Positive Drive Supply Voltage	V_{CC}		4.75	12	12.6	V
Negative Drive Supply Voltage	V_{EE}		1.05 x ($-V_{CC}$)	$-V_{CC}$	0.95 x ($-V_{CC}$)	V
High-Side Supply Voltage	V_{PP1}		0		+200	V
Low-Side Supply Voltage	V_{NN1}		-200		0	V
High-Side Supply Voltage	V_{PP2}		0		V_{PP1}	V
Low-Side Supply Voltage	V_{NN2}		V_{NN1}		0	V
$V_{PP\_}$ - $V_{NN\_}$ Supply Voltage			0		+200	V
SUPPLY CURRENT (for single channel)						
V_{DD} Supply Current	I_{DD}	$V_{INN\_}$/$V_{INP\_}$/$V_{CLP\_}$ = 0 or V_{DD}, V_{EN} = 0			1	µA
		V_{EN} = V_{DD}, $V_{CLP\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{INP\_}$, f = 5MHz, one channel switching		100	200	µA
V_{CC} Supply Current	$I_{CC\_}$	V_{EN} = 0 (static)			1	µA
		V_{EN} = V_{DD} (static)			10	
		V_{EN} = V_{DD}, $V_{CLP\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{INP\_}$, f = 5MHz, V_{CC} = +12V, V_{DD} = +3V, one channel switching		36		mA
		V_{EN} = V_{DD}, $V_{CLP\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{INP\_}$, f = 5MHz, V_{CC} = +5V, V_{DD} = +3V, one channel switching		15		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +12V, V_{EE} = -12V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{EE\_}$ Supply Current	$I_{EE\_}$	V_{EN} = 0 or V_{DD} (static)			1	µA
		V_{EE} = -5V, V_{EN} = V_{DD}, $V_{CLP\_}$ = V_{DD}, PRF = 10kHz, f = 5MHz, four pulses, no load, one channel switching			100	
		V_{EE} = -12V, V_{EN} = V_{DD}, $V_{CLP\_}$ = V_{DD}, PRF = 10kHz, f = 5MHz, four pulses, no load, one channel switching			200	
$V_{PP\_}$ Supply Current	$I_{PP\_}$	V_{EN} = 0 or V_{DD} (static)			1	µA
		V_{EN} = V_{DD}, $V_{CLP\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{INP\_}$, f = 5MHz, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, no load, one channel switching		9		mA
		V_{EN} = V_{DD}, $V_{CLP\_}$ = 0 or V_{DD}, $V_{PP\_}$ = +80V, $V_{NN\_}$ = -80V, PRF = 10kHz, f = 10MHz, four pulses, no load, one channel switching		0.6		
$V_{NN\_}$ Supply Current	$I_{NN\_}$	V_{EN} = 0 or V_{DD} (static)			1	µA
		V_{EN} = V_{DD}, $V_{CLP\_}$ = 0 or V_{DD}, $V_{INN\_}$ = $V_{INP\_}$, f = 5MHz, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V, no load, one channel switching		9		mA
		V_{EN} = V_{DD}, $V_{INC\_}$ = 0 or V_{DD}, $V_{PP\_}$ = +80V, $V_{NN\_}$ = -80V, PRF = 10kHz, f = 10MHz, four pulses, no load, one channel switching		0.6		
LOGIC INPUTS (EN, INN_, INP_, CLP_)						
Low-Level Input Voltage	V_{IL}				0.25 x V_{DD}	V
High-Level Input Voltage	V_{IH}		0.75 x V_{DD}			V
Logic-Input Capacitance	C_{IN}			5		pF
Logic-Input Leakage	I_{IN}	V_{IN} = 0 or V_{DD}		0	±1	µA
OUTPUT (OUT_)						
OUT_ Output-Voltage Range	$V_{OUT\_}$	No load at OUT_	$V_{NN\_}$		$V_{PP\_}$	V
		100mA load (MAX4940), V_{CC} = +12V ±5%	$V_{NN\_}$ + 1.5		$V_{PP\_}$ - 1.5	V
		100mA load (MAX4940A), V_{CC} = +12V ±5%	$V_{NN\_}$ + 2.5		$V_{PP\_}$ - 2.5	V
Low-Side Output Impedance (MAX4940)	R_{OLS}	$I_{OUT\_}$ = -50mA, V_{CC} = +12V ±5%		7.5	14	Ω
		$I_{OUT\_}$ = -50mA, V_{CC} = +5V ±5%		8	18	Ω
High-Side Output Impedance (MAX4940)	R_{OHS}	$I_{OUT\_}$ = -50mA, V_{CC} = +12V ±5%		9	14	Ω
		$I_{OUT\_}$ = -50mA, V_{CC} = +5V ±5%		10.5	18	Ω

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +12V, V_{EE} = -12V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Side Output Impedance (MAX4940A)	R_{OLS}	$I_{OUT\_}$ = -50mA	V_{CC} = +12V ±5%		8.5	17	Ω
			V_{CC} = +5V ±5%		10.0	21	
High-Side Output Impedance (MAX4940A)	R_{OHS}	$I_{OUT\_}$ = -50mA	V_{CC} = +12V ±5%		11.5	17	Ω
			V_{CC} = +5V ±5%		13.0	21	
Low-Side Signal CLAMP Output Impedance	R_{OLSC}	$I_{OUT\_}$ = -50mA	V_{CC} = +12V ±5%		18.7	45	Ω
			V_{CC} = +5V ±5%		20	60	
High-Side Signal CLAMP Output Impedance	R_{OHSC}	$I_{OUT\_}$ = -50mA	V_{CC} = +12V ±5%		26.5	45	Ω
			V_{CC} = +5V ±5%		37.0	60	
PEAK CURRENT							
Low-Side Output Current	I_{OL}	V_{CC} = +12V ±5%, $V_{OUT\_}$ - $V_{NN\_}$ = 100V		1.3	2.0		A
High-Side Output Current	I_{OH}	V_{CC} = +12V ±5%, $V_{OUT\_}$ - $V_{PP\_}$ = 100V		1.3	2.0		A
Low-Side Output Current Clamp	I_{OLC}	V_{CC} = +12V ±5%, $V_{OUT\_}$ = +40V		0.47	0.9		A
High-Side Output Current Clamp	I_{OHC}	V_{CC} = +12V ±5%, $V_{OUT\_}$ = +40V		0.47	0.9		A
Off-Output Capacitance	$C_{O(OFF)}$	MAX4940, MAX4940A (OUT1_)			75		pF
		MAX4940A (OUT2_)			45		
Off-Output Leakage Current	I_{LK}	$V_{NN\_}$ = -100V, $V_{PP\_}$ = +100V, V_{EN} = 0, $V_{OUT\_}$ = -100V to +100V				±1	µA
GATE-SOURCE RESISTANCE							
Gate-Source Resistance	R_{GS}	V_{EN} = V_{DD}		5	7.5	10	kΩ
DYNAMIC CHARACTERISTICS (R_L = 100Ω, C_L = 100pF, unless otherwise noted)							
Logic Input-to-Output Rise Propagation Delay (Figure 1)	t_{PLH}	INN_/INP_ at 50% to OUT_ 10/90%, V_{CC} = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V			15		ns
Logic Input-to-Output Fall Propagation Delay (Figure 1)	t_{PHL}	INN_/INP_ at 50% to OUT_ 10/90%, V_{CC} = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V			15		ns
Logic Input-to-Output Rise Propagation Delay Clamp (Figure 1)	t_{PLO}	INN_/INP_ at 50% to OUT_ 10/90%, V_{CC} = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V			15		ns
Logic Input-to-Output Fall Propagation Delay Clamp (Figure 1)	t_{PHO}	INN_/INP_ at 50% to OUT_ 10/90%, V_{CC} = +12V, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V			15		ns
OUT_ Rise Time (GND to $V_{PP\_}$) (Figure 1)	t_{ROP}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, 10% to 90%, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$			9	20	ns
OUT_ Rise Time ($V_{NN\_}$ to $V_{PP\_}$) (Figure 1)	t_{RNP}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, 10% to 90%, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$			10.5	35	ns
OUT_ Fall Time (GND to $V_{NN\_}$) (Figure 1)	t_{FON}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, 10% to 90%, $V_{CC\_}$ = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$			9	20	ns
OUT_ Fall Time ($V_{PP\_}$ to $V_{NN\_}$) (Figure 1)	t_{FPN}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, 10% to 90%, V_{CC} = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$			10.5	35	ns
OUT_ Rise Time ($V_{NN\_}$ to GND) (Figure 1)	t_{RNO}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, 10% to 90%, V_{CC} = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$			17	35	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{CC} = +12V, V_{EE} = -12V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

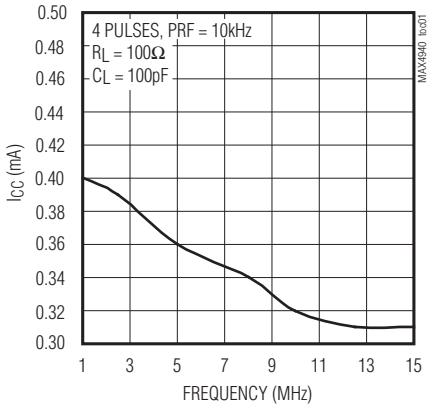
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT_ Fall Time ($V_{PP\_}$ to GND) (Figure 1)	t_{FPO}	$V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, 10% to 90%, V_{CC} = +12V ±5%, $V_{EE\_}$ = -$V_{CC\_}$		17	35	ns
Output Enable Time from EN (Figure 2)	t_{EN}	$V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V			100	ns
Output Disable Time from EN (Figure 2)	t_{DI}	$V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V			150	ns
2nd Harmonic Distortion LV	THD2_LV	$f_{OUT\_}$ = 5MHz, $V_{PP\_}$ = -$V_{NN\_}$ = +5V, V_{CC} = +12V		-40		dB
2nd Harmonic Distortion HV	THD2_HV	$f_{OUT\_}$ = 5MHz, $V_{PP\_}$ = -$V_{NN\_}$ = +50V, V_{CC} = +12V, 10 periods		-45		dB
Pulse Cancellation	2HD	$f_{OUT\_}$ = 5MHz, $V_{PP\_}$ = -$V_{NN\_}$ = +50V, V_{CC} = +12V, 10 periods, 1st harmonic cancellation		-43		dB
RMS Output Jitter	t_J			10		ps
Crosstalk	CT	Adjacent channels, f = 5MHz		-60		dB

Note 2: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +70°C. Specifications at T_A = 0°C are guaranteed by design.

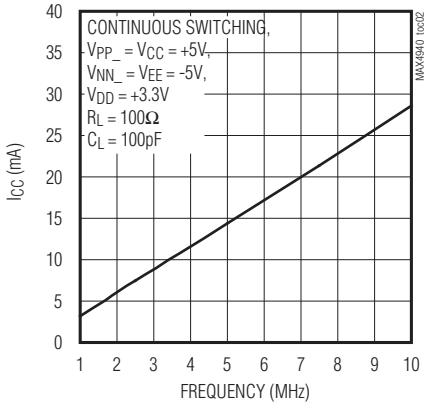
Typical Operating Characteristics

(V_{DD} = +3.3V, V_{CC} = +12V, V_{EE} = -12V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, f_{OUT} = 5MHz, R_L = 100Ω, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

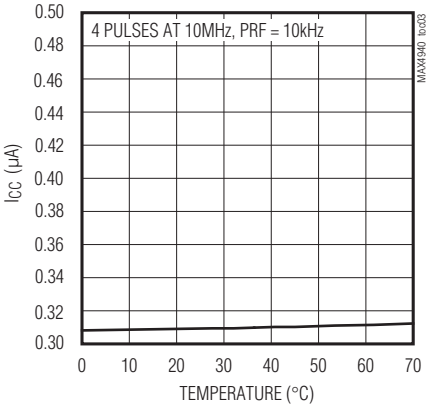
I_{CC} vs. OUTPUT FREQUENCY



I_{CC} vs. OUTPUT FREQUENCY



I_{CC} vs. TEMPERATURE

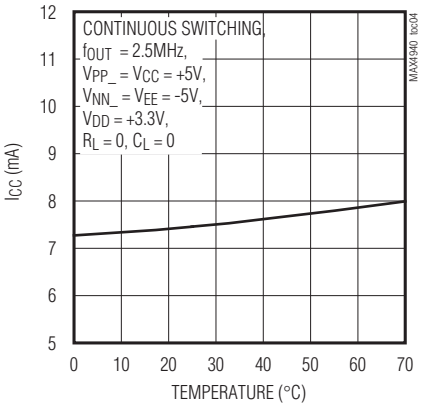


Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

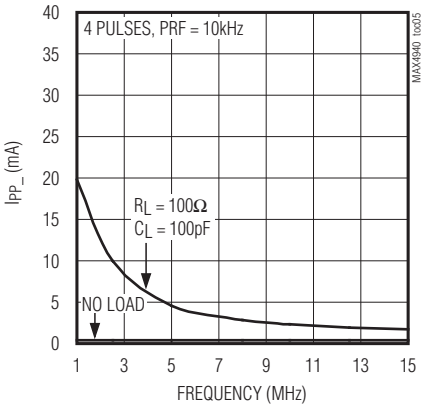
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{CC} = +12V, V_{EE} = -12V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, f_{OUT} = 5MHz, R_L = 100Ω, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

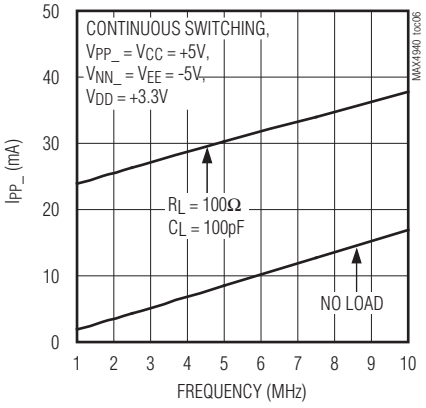
I_{CC} vs. TEMPERATURE



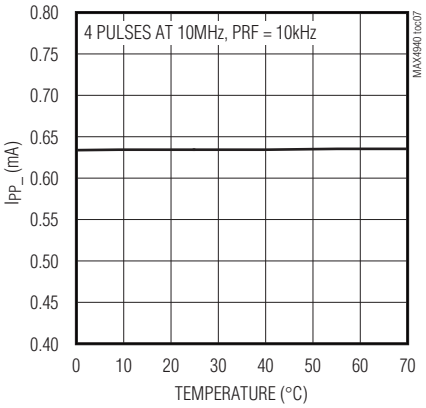
$I_{PP\_}$ vs. OUTPUT FREQUENCY



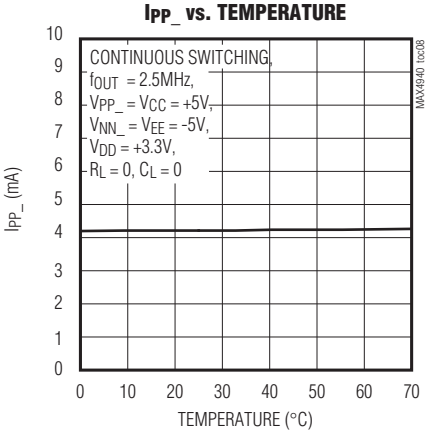
$I_{PP\_}$ vs. OUTPUT FREQUENCY



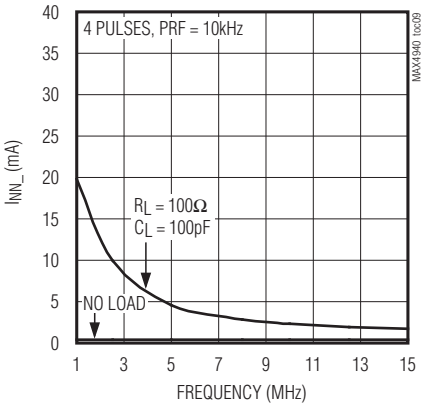
$I_{PP\_}$ vs. TEMPERATURE



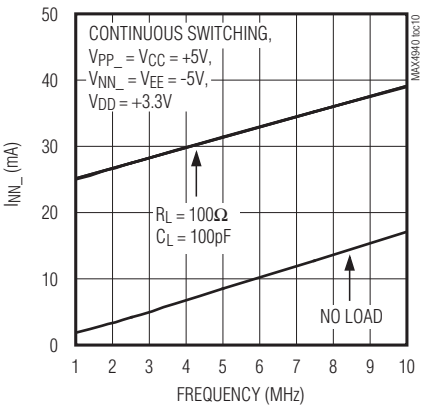
$I_{PP\_}$ vs. TEMPERATURE



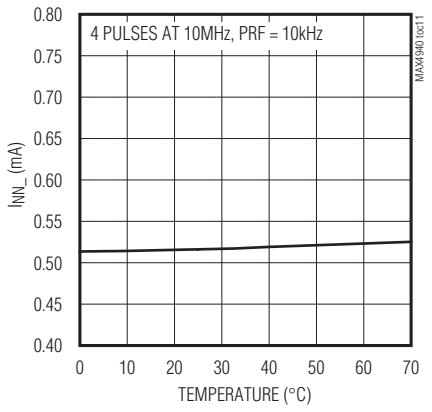
$I_{NN\_}$ vs. OUTPUT FREQUENCY



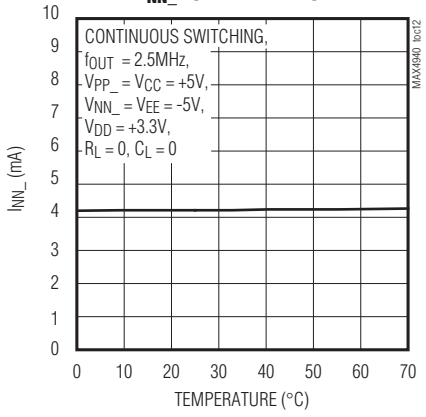
$I_{NN\_}$ vs. OUTPUT FREQUENCY



$I_{NN\_}$ vs. TEMPERATURE



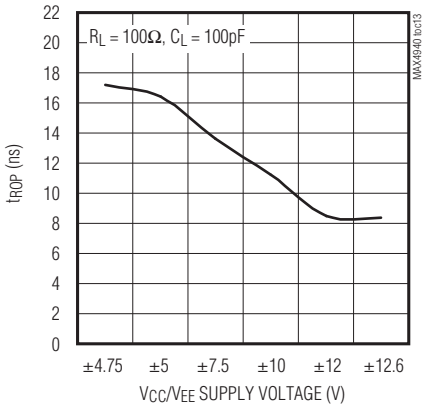
$I_{NN\_}$ vs. TEMPERATURE



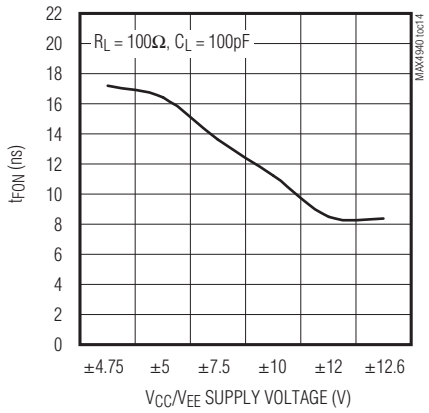
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, V_{CC} = +12V, V_{EE} = -12V, $V_{PP\_}$ = +100V, $V_{NN\_}$ = -100V, f_{OUT} = 5MHz, R_L = 100Ω, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

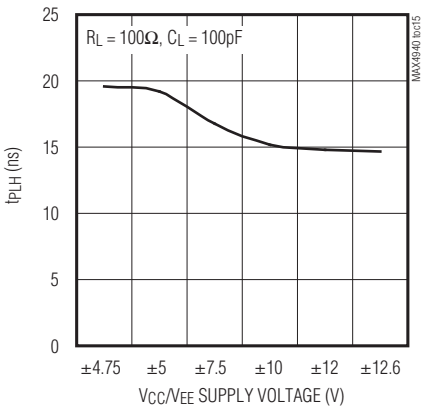
OUT_ RISE TIME (GND TO $V_{PP\_}$) vs. V_{CC}/V_{EE} SUPPLY VOLTAGE



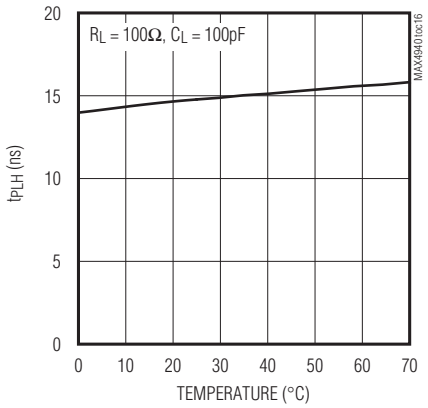
OUT_ FALL TIME (GND TO $V_{NN\_}$) vs. V_{CC}/V_{EE} SUPPLY VOLTAGE



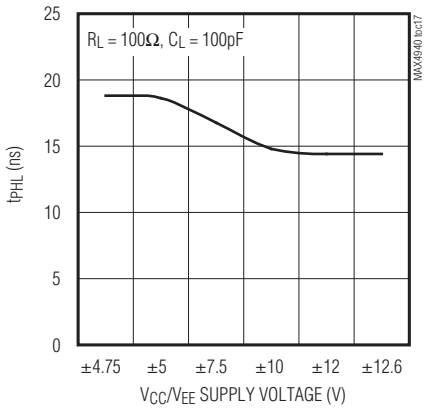
INP_ TO OUT_ RISE PROPAGATION DELAY vs. V_{CC}/V_{EE} SUPPLY VOLTAGE



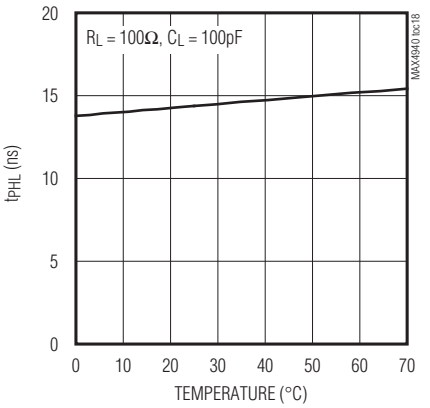
INP_ TO OUT_ RISE PROPAGATION DELAY vs. TEMPERATURE



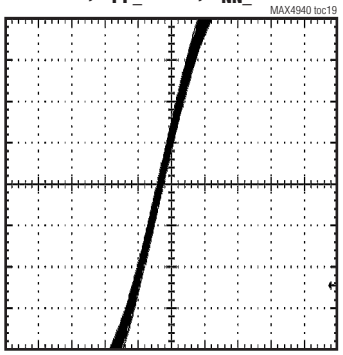
INP_ TO OUT_ FALL PROPAGATION DELAY vs. V_{CC}/V_{EE} SUPPLY VOLTAGE



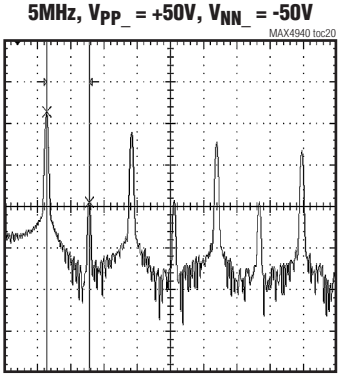
INP_ TO OUT_ FALL PROPAGATION DELAY vs. TEMPERATURE



JITTER
5MHz, $V_{PP\_}$ = +5V, $V_{NN\_}$ = -5V



SPECTRUM
5MHz, $V_{PP\_}$ = +50V, $V_{NN\_}$ = -50V



Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Pin Description

PIN	NAME	FUNCTION
1	INP1A	Channel 1A High-Side Logic Input. See the *Truth Tables* section.
2	CLP1A	Channel 1A Clamp Logic Input. Clamp is turned on when CLP1A is high and when INP1A and INN1A are low. See the *Truth Table* section.
3	INN1A	Channel 1A Low-Side Logic Input. See the *Truth Tables* section.
4	INP2A	Channel 2A High-Side Logic Input. See the *Truth Tables* section.
5	CLP2A	Channel 2A Clamp Logic Input. Clamp is turned on when CLP2A is high and when INP2A and INN2A are low. See the *Truth Tables* section.
6	INN2A	Channel 2A Low-Side Logic Input. See the *Truth Tables* section.
7	AGND	Analog Ground. Must be connected to common GND.
8	EN	Enable Logic Input. Drive EN high to enable OUT1A, OUT1B, OUT2A, and OUT2B.
9	INP2B	Channel 2B High-Side Logic Input. See the *Truth Tables* section.
10	CLP2B	Channel 2B Clamp Logic Input. Clamp is turned on when CLP2B is high and when INP2B and INN2B are low. See the *Truth Tables* section.
11	INN2B	Channel 2B Low-Side Logic Input. See the *Truth Tables* section.
12	INP1B	Channel 1B High-Side Logic Input. See the *Truth Tables* section.
13	CLP1B	Channel 1B Clamp Logic Input. Clamp is turned on when CLP1B is high and when INP1B and INN1B are low. See the *Truth Tables* section.
14	INN1B	Channel 1B Low-Side Logic Input. See the *Truth Tables* section.
15	V_{EE}	Negative Supply Input. Gate-drive supply voltage for the clamp. Bypass V_{EE} to GND with a 0.1µF capacitor as close as possible to the device.
16, 27, 29, 34, 37, 42, 44, 55	GND	Ground
17, 54	V_{CC}	Gate-Drive Supply Voltage Input. Bypass V_{CC} to GND with a 0.1µF capacitor as close as possible to the device.
18	C_{DP1B}	Channel 1B High-Side Driver Output. Connect a 3.3nF capacitor between C_{DP1B} and C_{GP1B} as close as possible to the device.
19	C_{DN1B}	Channel 1B Low-Side Driver Output. Connect a 3.3nF capacitor between C_{DN1B} and C_{GN1B} as close as possible to the device.
20	C_{DN2B}	Channel 2B Low-Side Driver Output. Connect a 3.3nF capacitor between C_{DN2B} and C_{GN2B} as close as possible to the device.
21	C_{DP2B}	Channel 2B High-Side Driver Output. Connect a 3.3nF capacitor between C_{DP2B} and C_{GP2B} as close as possible to the device.
22	C_{GP2B}	Channel 2B High-Side Gate Input. Connect a 3.3nF capacitor between C_{DP2B} and C_{GP2B} as close as possible to the device.
23	C_{GN2B}	Channel 2B Low-Side Gate Input. Connect a 3.3nF capacitor between C_{DN2B} and C_{GN2B} as close as possible to the device.
24	C_{GN1B}	Channel 1B Low-Side Gate Input. Connect a 3.3nF capacitor between C_{DN1B} and C_{GN1B} as close as possible to the device.
25	C_{GP1B}	Channel 1B High-Side Gate Input. Connect a 3.3nF capacitor between C_{DP1B} and C_{GP1B} as close as possible to the device.

Pin Description (continued)

PIN	NAME	FUNCTION
26, 45	V_{PP1}	Channel 1A, 1B High-Side Positive Supply Voltage Input. Bypass V_{PP1} to GND with a 0.1µF capacitor as close as possible to the device.
28	OUT1B	Channel 1B Output
30, 41	V_{NN1}	Channel 1A, 1B Low-Side Negative Supply Voltage Input. Bypass V_{NN1} to GND with a 0.1µF capacitor as close as possible to the device.
31, 40	V_{NN2}	Channel 2A, 2B Low-Side Negative Supply Voltage Input. Bypass V_{NN2} to GND with a 0.1µF capacitor as close as possible to the device.
32, 39	N.C.	No Connection. Not connected internally.
33	OUT2B	Channel 2B Output
35, 36	V_{PP2}	Channel 2A, 2B High-Side Positive Supply Voltage Input. Bypass V_{PP2} to GND with a 0.1µF capacitor as close as possible to the device.
38	OUT2A	Channel 2A Output
43	OUT1A	Channel 1A Output
46	C_{GP1A}	Channel 1A High-Side Gate Input. Connect a 3.3nF capacitor between C_{DP1A} and C_{GP1A} as close as possible to the device.
47	C_{GN1A}	Channel 1A Low-Side Gate Input. Connect a 3.3nF capacitor between C_{DN1A} and C_{GN1A} as close as possible to the device.
48	C_{GN2A}	Channel 2A Low-Side Gate Input. Connect a 3.3nF capacitor between C_{DN2A} and C_{GN2A} as close as possible to the device.
49	C_{GP2A}	Channel 2A High-Side Gate Input. Connect a 3.3nF capacitor between C_{DP2A} and C_{GP2A} as close as possible to the device.
50	C_{DP2A}	Channel 2A High-Side Driver Output. Connect a 3.3nF capacitor between C_{DP2A} and C_{GP2A} as close as possible to the device.
51	C_{DN2A}	Channel 2A Low-Side Driver Output. Connect a 3.3nF capacitor between C_{DN2A} and C_{GN2A} as close as possible to the device.
52	C_{DN1A}	Channel 1A Low-Side Driver Output. Connect a 3.3nF capacitor between C_{DN1A} and C_{GN1A} as close as possible to the device.
53	C_{DP1A}	Channel 1A High-Side Driver Output. Connect a 3.3nF capacitor between C_{DP1A} and C_{GP1A} as close as possible to the device.
56	V_{DD}	Logic-Supply Voltage Input. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to the device.
—	EP	Exposed Pad. EP must be connected to V_{NN1}.

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Detailed Description

The MAX4940/MAX4940A are quad high-voltage, high-speed pulsers that can be independently configured for either unipolar/bipolar/multilevel pulse outputs (see Figures 5 and 6.). These devices have independent logic inputs for full pulse control and independent active clamps. The clamp input, CLP_, can be set high to activate the clamp automatically when the device is not pulsing to the positive or negative high-voltage supplies.

Logic Inputs (INP_, INN_, CLP_, EN)

INP_ controls the on and off states of the high-side FET, INN_ controls the on and off states of the low-side FET, and CLP_ controls the active clamp. A global enable input (EN) can be used to enable/disable all channels. These signals give complete control of the output stage of each driver (see the *Truth Tables* section for all logic combinations). The MAX4940/MAX4940A logic inputs are CMOS logic compatible and the logic levels are referenced to V_{DD} for maximum flexibility. The low 5pF (typ) input capacitance of the logic inputs reduce loading and increase switching speed.

Truth Tables

MAX4940

INPUTS				OUTPUTS	STATE
EN	INP_	INN_	CLP_	OUT_	
0	X	X	X	High impedance	Powered up, INP_/INN_ disabled.
1	0	0	0	High impedance	Powered up, all inputs enabled.
1	0	0	1	GND	Powered up, all inputs enabled.
1	0	1	X	$V_{NN\_}$	Powered up, all inputs enabled.
1	1	0	X	$V_{PP\_}$	Powered up, all inputs enabled.
1	1	1	X	Not allowed	Not allowed.

MAX4940A

INPUTS				OUTPUTS	STATE
EN	INP1A INP1B	INN1A INN1B	CLP1A CLP1B	OUT1A OUT1B	
0	X	X	X	High impedance	Powered up, INP_/INN_ disabled.
1	0	0	0	High impedance	Powered up, all inputs enabled.
1	0	0	1	GND	Powered up, all inputs enabled.
1	0	1	0	$V_{NN\_}$	Powered up, all inputs enabled.
1	1	0	0	$V_{PP\_}$	Powered up, all inputs enabled.
1	1	1	1	Not allowed	Not allowed.

INPUTS				OUTPUTS	STATE
EN	INP2A INP2B	INN2A INN2B	CLP2A CLP2B	OUT2A OUT2B	
0	X	X	X	High impedance	Powered up, INP_/INN_ disabled.
1	0	0	0	High impedance	Powered up, all inputs enabled.
1	0	0	1	GND	Powered up, all inputs enabled.
1	0	1	X	$V_{NN\_}$	Powered up, all inputs enabled.
1	1	0	X	$V_{PP\_}$	Powered up, all inputs enabled.
1	1	1	X	Not allowed	Not allowed.

X = Don't care.
0 = Logic-low.
1 = Logic-high.

Active Clamps

The MAX4940/MAX4940A feature an integrated active clamp circuit to improve pulse quality and reduce 2nd harmonic distortion. The clamp circuit consists of an n-channel (DC-coupled) and a p-channel (DC-coupled) high-voltage FETs that are switched on or off by the logic clamp input (CLP_).

The MAX4940/MAX4940A feature protected clamp devices, allowing the clamp circuit to be used in bipolar pulsing circuits (see Figures 3 and 4). A diode in series with the OUT_ output prevents the body diode of the low-side FET from turning on when a voltage lower than GND is present. Another diode in series with the OUT_ output prevents the body diode of the high-side FET from turning on when a voltage higher than ground is present. The MAX4940/MAX4940A have an active clamp on all outputs.

For the MAX4940 only, the user can connect the active clamp input (CLP_) to a logic-high voltage and drive only the INP_ and INN_ inputs to minimize the number of signals used to drive the device. In this case, whenever both the INP_ and INN_ inputs are low and the CLP_ input is high, the active clamp circuit pulls the output to GND (see the *Truth Tables* section for more information).

Integrated Blocking Diodes (MAX4940A Only)

The high-voltage OUT2A/OUT2B outputs of the MAX4940A feature integrated blocking diodes that allow the user to implement multilevel pulsing by connecting the outputs of multiple pulser channels in parallel. Internal diodes in series with the OUT2A and OUT2B outputs prevent the body diode of the high-side and low-side FETs from switching on when a voltage greater than V_{NN2} or V_{PP2} is present on the output (see Figure 4).

Thermal Protection

A thermal shutdown circuit with a typical threshold of +155°C prevents damage due to excessive power dissipation. When the junction temperature exceeds T_J = +155°C, all outputs are disabled. Normal operation typically resumes after the IC's junction temperature drops below +130°C.

Applications Information

AC-Coupling Capacitor Selection

The value of all AC-coupling capacitors (between $C_{DP\_}$ and $C_{GP\_}$, and between $C_{DN\_}$ and $C_{GN\_}$) should be between 1nF to 10nF. The voltage rating of the capacitor should be greater than $V_{PP\_}$ and $V_{NN\_}$. The capacitors should be placed as close as possible to the device.

Power Dissipation

The power dissipation of the MAX4940/MAX4940A consists of three major components caused by the current consumption from V_{CC}, $V_{PP\_}$, and $V_{NN\_}$. The sum of these components (P_{VCC}, $P_{VPP\_}$, and $P_{VNN\_}$) must be kept below the maximum power-dissipation limit. See the *Typical Operating Characteristics* section for more information on typical supply currents versus switching frequencies.

The device consumes most of the supply current from V_{CC} supply to charge and discharge internal nodes such as the gate capacitance of the high-side FET (C_P) and the low-side FET (C_N). Neglecting the small quiescent supply current and a small amount of current used to charge and discharge the capacitances at the internal gate clamp FETs, the power consumption can be estimated as follows:

$$P_{VCC} = \left[\left(C_N \times {V_{CC}}^2 \times f_{IN}\right) + \left(C_P \times {V_{CC}}^2 \times f_{IN}\right)\right] \times (BRF \times BTD)$$

$$f_{IN} = f_{INN\_} + f_{INP\_}$$

where $f_{INN\_}$ and $f_{INP\_}$ are the switching frequency of the inputs INN_, INP_, respectively, and where BRF is the burst response frequency, and BTD is the burst time duration. The typical values of the gate capacitances are C_N = 1.2µF, C_P = 0.4µF.

See the *Typical Operating Characteristics* for $V_{PP\_}$ and $V_{NN\_}$ power consumption.

Power Supplies and Bypassing

The MAX4940/MAX4940A operate from independent supply voltage sets (only V_{DD}, V_{CC}, and V_{EE} are common to all channels). V_{PP1}/V_{NN1} supply two channels and V_{PP2}/V_{NN2} supply the other two channels. The logic input circuit operates from a +2.37V to +6V single supply (V_{DD}). The level-shift driver dual supplies, V_{CC}/V_{EE} operate from ±4.75V to ±12.6V.

The $V_{PP\_}$/$V_{NN\_}$ high-side and low-side supplies are driven from a single positive supply up to +220V, from a single negative supply up to -220V, or from ±110V dual supplies. Either $V_{PP\_}$ or $V_{NN\_}$ can be set at 0. Bypass each supply input to ground with a 0.1µF capacitor as close as possible to the device.

Depending on the applications, additional bypassing may be needed to maintain the input of both $V_{NN\_}$ and $V_{PP\_}$ stable during output transitions. For example, with C_{OUT} = 100pF and R_{OUT} = 100Ω load, the use of an additional 10µF (typ) electrolytic capacitor is recommended.

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Exposed Pad and Layout Concerns

The MAX4940/MAX4940A provide an exposed pad (EP) underneath the TQFN package for improved thermal performance. EP is internally connected to V_{NN1}. Connect EP to V_{NN1} externally. To aid heat dissipation, connect EP to a similarly sized pad on the component side of the PCB. This pad should be connected through the solder-side copper by several plated holes to a large heat spreading copper area to conduct heat away from the device.

The MAX4940/MAX4940A high-speed pulsers require low-inductance bypass capacitors to their supply inputs. High-speed PCB trace design practices are recommended. Pay particular attention to minimize trace lengths and use sufficient trace width to reduce inductance. Use of surface-mount components is recommended.

Supply Sequencing

In a typical trilevel application when V_{NN1} and V_{NN2} are externally shorted ($V_{NN1} = V_{NN2}$), the MAX4940/MAX4940A do not require any power sequencing. In general, and in particular for the multilevel application, V_{NN1} must be less than or equal to V_{NN2} ($V_{NN1} \leq V_{NN2}$) at all times. No other power-supply sequencing is required for the MAX4940/MAX4940A.

Timing Diagrams

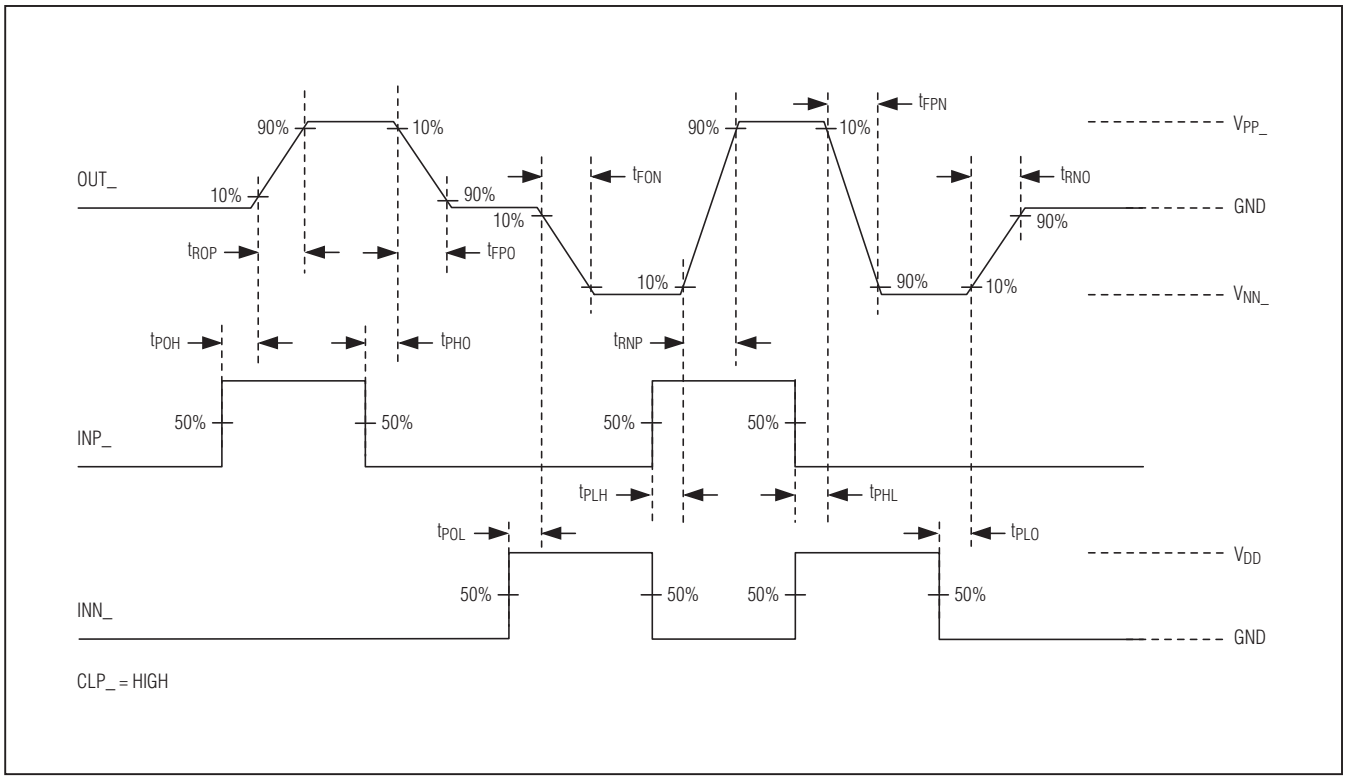


Figure 1. Detail Timing (R_L = 100Ω, C_L = 100pF)

Timing Diagrams (continued)

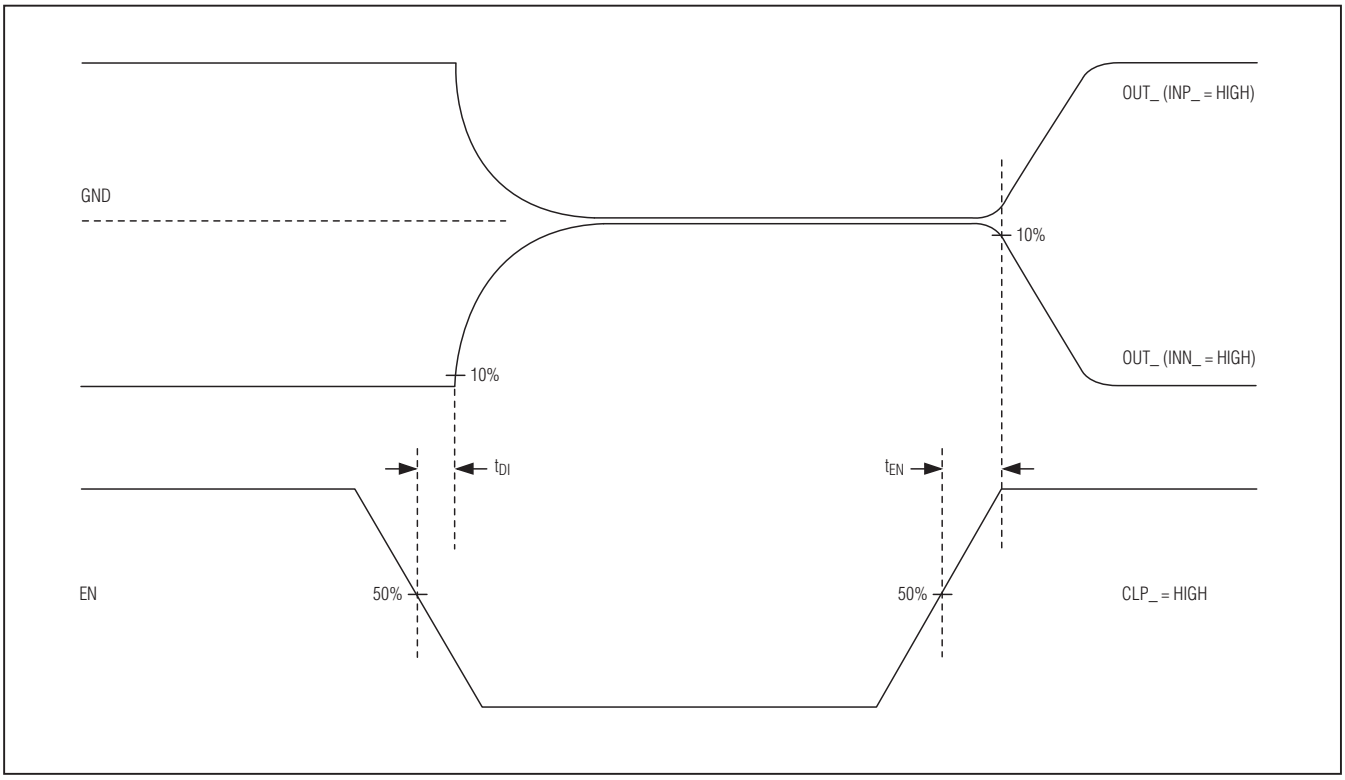


Figure 2. Enable Timing (R_L = 100Ω, C_L = 100pF)

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Functional Diagrams

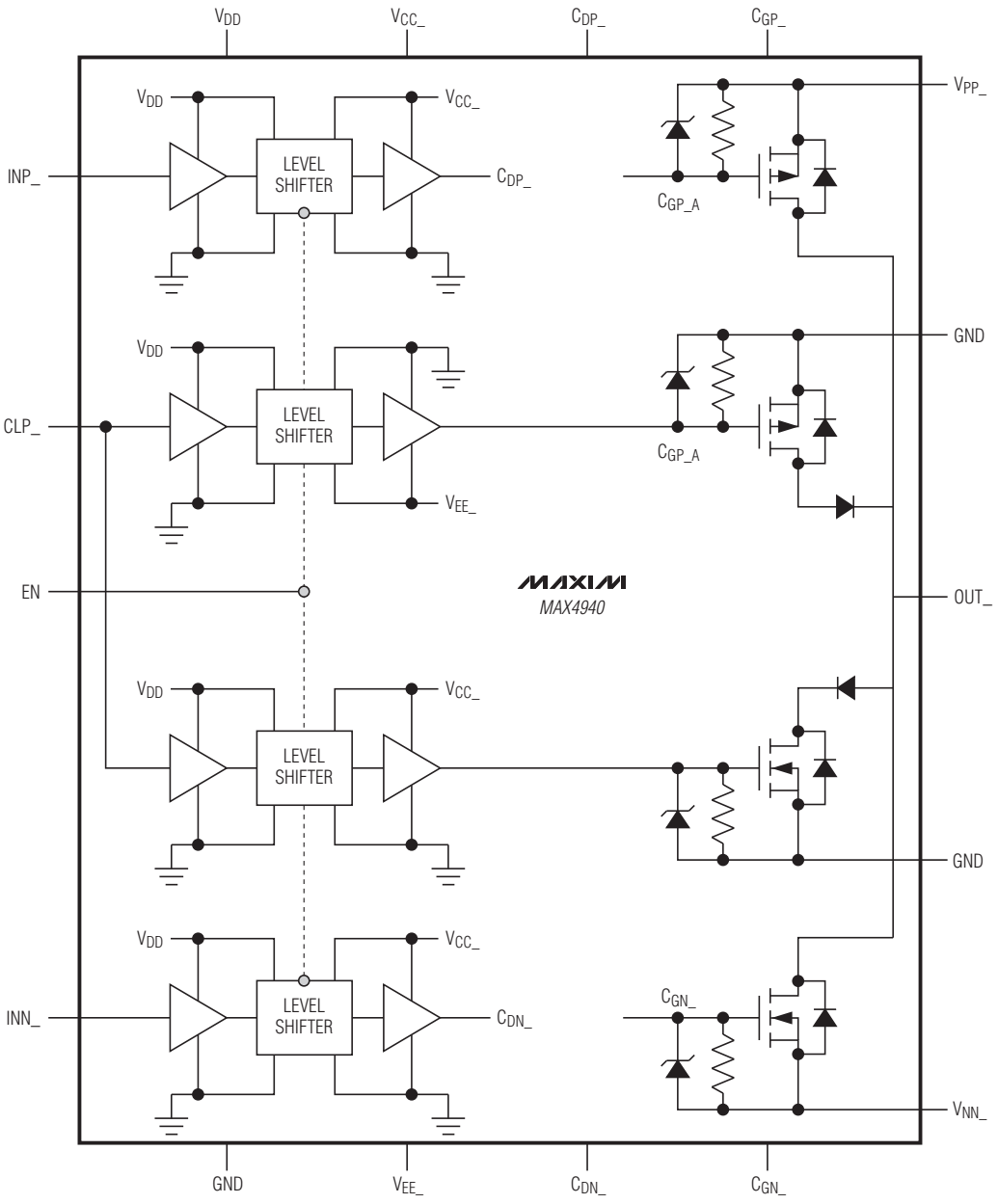


Figure 3. MAX4940 Simplified Functional Diagram for One Channel

Functional Diagrams (continued)

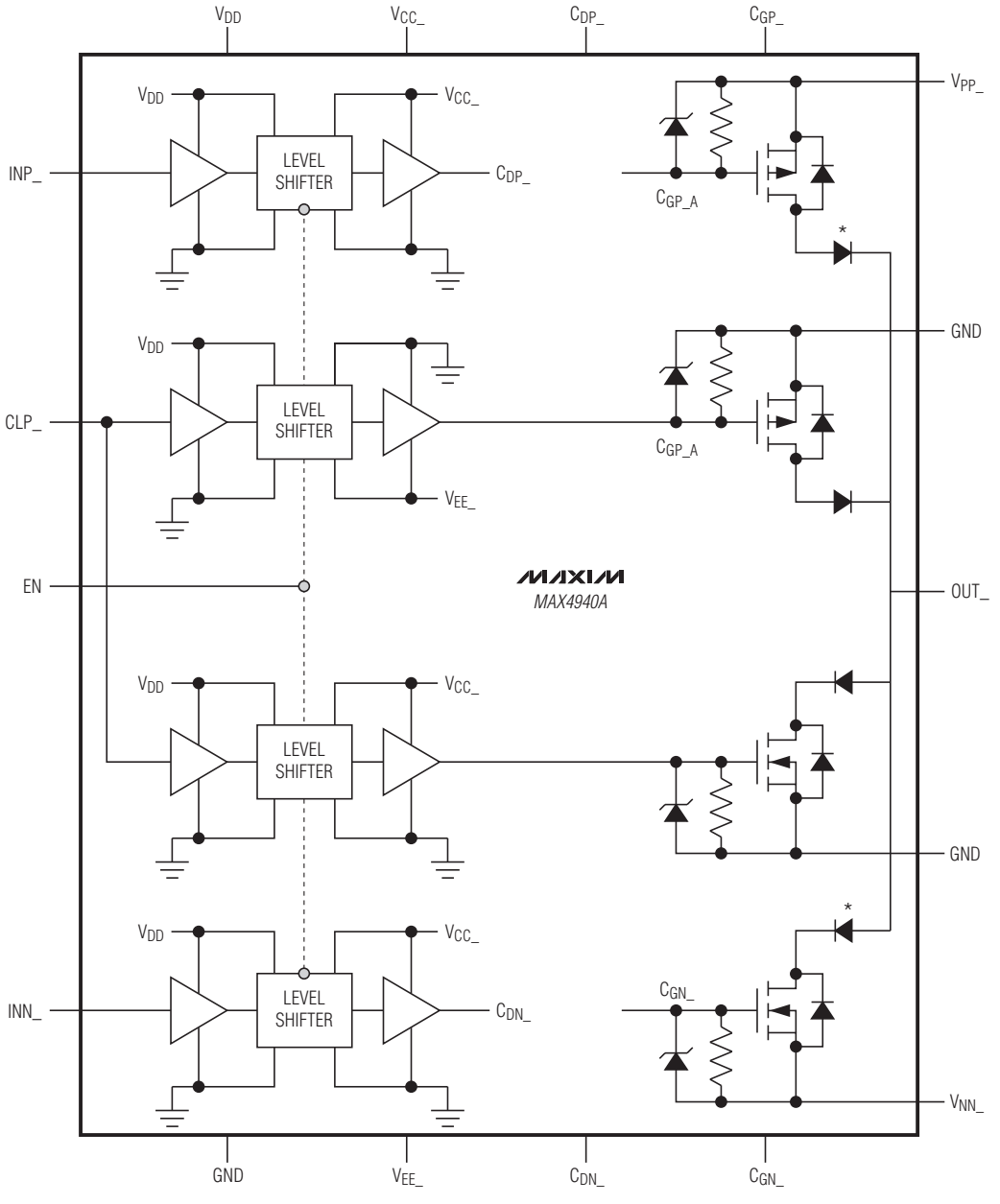


Figure 4. MAX4940A Simplified Functional Diagram for One Channel

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Typical Application Circuits

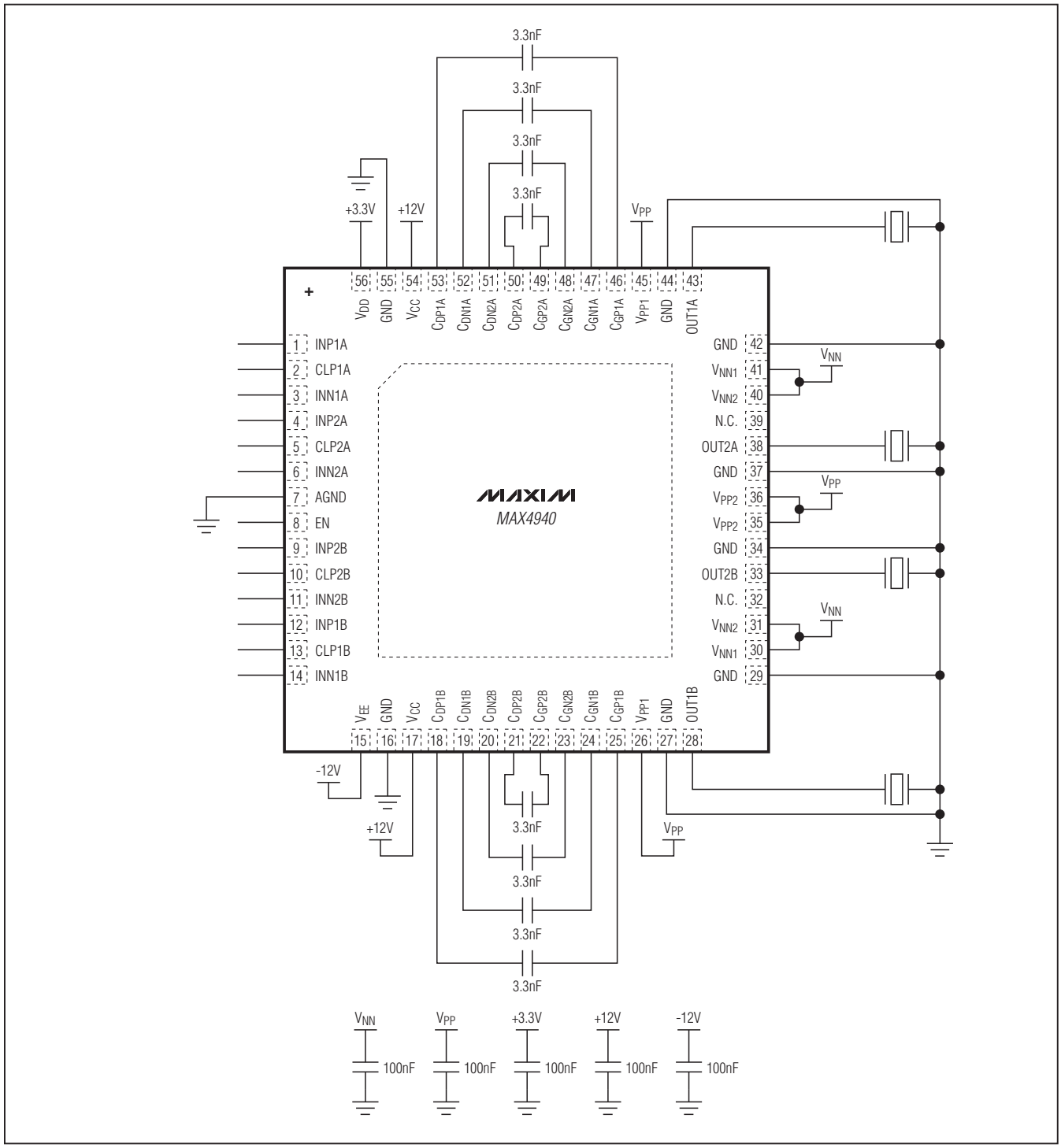


Figure 5. MAX4940 Quad Pulsing with Always-On Active Return-to-Zero

Typical Application Circuits (continued)

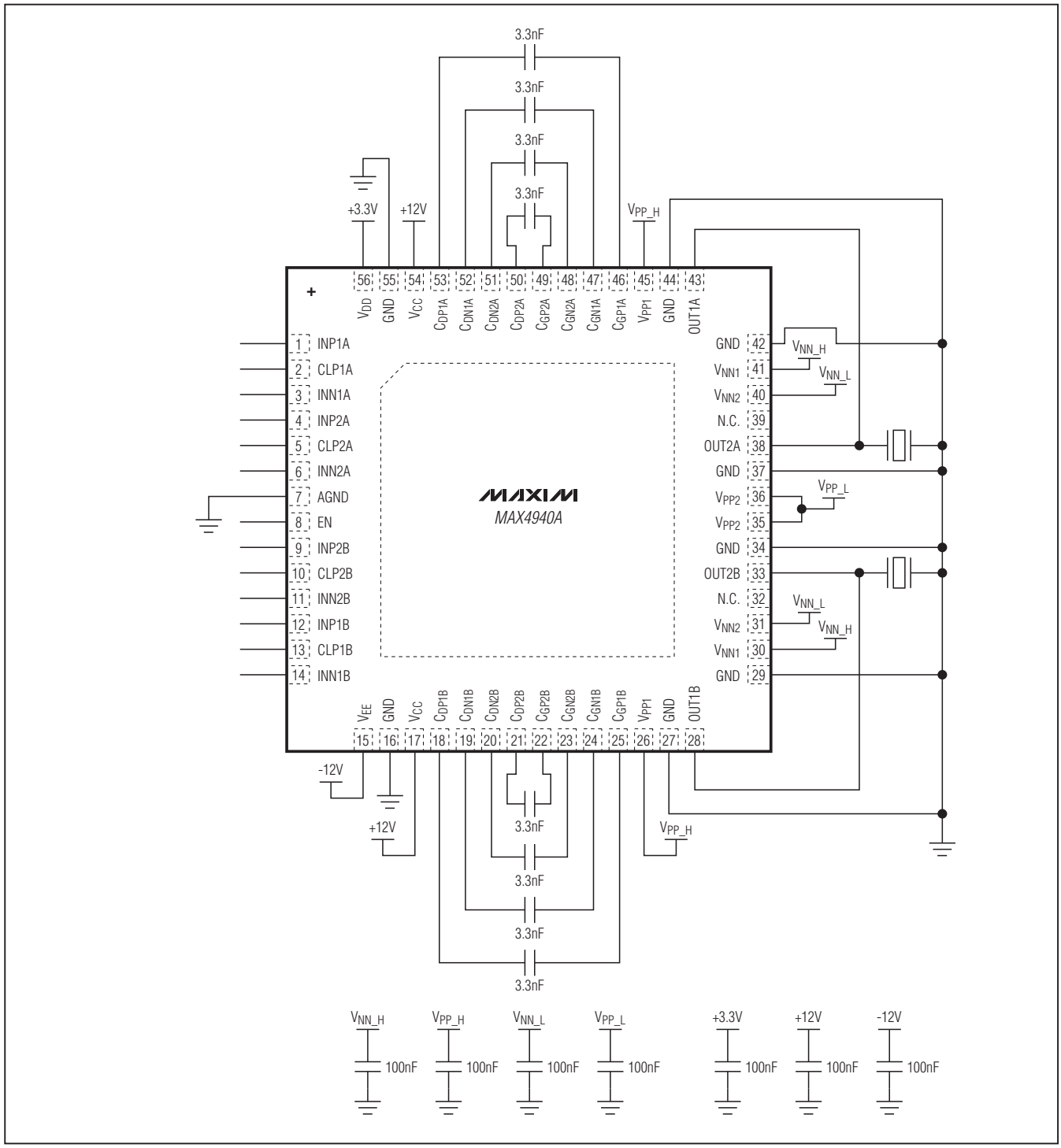


Figure 6. MAX4940A Dual Five-Level Pulsing

Dual/Quad, Unipolar/Bipolar, High-Voltage Digital Pulsers

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

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56 TQFN	T5688-3	21-0135

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