19-1143; Rev 0; 10/96

EVALUATION KIT AVAILABLE

MAXIM

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

MAX498/MAX499

General Description

The MAX498/MAX499 are high-speed, quad/triple, single-pole/double-throw video switches with on-board closed-loop buffer amplifiers. The buffer amplifiers feature +6dB gain (A_{VCL} = 2V/V), 250MHz -3dB bandwidth, 70MHz 0.1dB gain flatness, and 1250V/µs slew rate. Fast switching time (3ns) and fast settling time (12ns for a 4V step) make these devices excellent choices for a wide variety of video applications. The low differential gain/phase errors (0.03%/0.06°) and wide bandwidth make them ideal for both composite-video and RGB applications. The amplifiers are capable of delivering ±2.5V into back-terminated 50Ω or 75Ω cables, and they deliver ±2V to a 75Ω load, allowing multiple cables to be driven from a single output.

For implementation of large switch arrays, a low-power disable mode places the amplifier outputs in a high-impedance state. Channel selection and output enable/disable are controlled by four TTL/CMOS-compatible logic inputs. Each video input is isolated by an AC-ground pin, which minimizes channel-to-channel capacitance and reduces crosstalk to 90dB at 10MHz.

The four-channel MAX498 dissipates 390mW (typical) from ±5VDC power supplies with all output buffers enabled. Power consumption is reduced to 130mW with all buffers disabled. The corresponding dissipation for the three-channel MAX499 is 300mW enabled and 100mW disabled.

Applications

- Video Switching and Routing
- Broadcast-Quality Composite-Video Multiplexing
- Workstations
- Video Editing
- Broadcast and High-Definition TV Systems
- Multimedia Products
- Medical Imaging

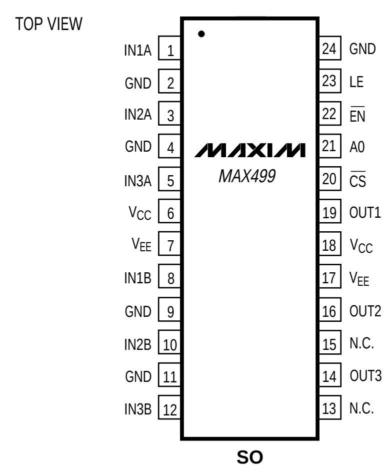
Features

- ♦ **High Speed:**
  250MHz Small-Signal -3dB Bandwidth
  135MHz Full-Power -3dB Bandwidth
- ♦ **70MHz 0.1dB Gain Flatness**
- ♦ **1250V/µs Slew Rate**
- ♦ **12ns to 0.1% Settling Time**
- ♦ **0.03°/0.06% Differential Phase/Gain Error**
- ♦ **2pF Input Capacitance**
- ♦ **3ns Channel-Switching Time**
- ♦ **120mVp-p Channel-Switching Transient**
- ♦ **Three-State Output Allows Large Switch Arrays**
- ♦ **Directly Drives 50Ω or 75Ω Back-Terminated Cables**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX498CWI	0°C to +70°C	28 SO
MAX499CWG	0°C to +70°C	24 SO

Pin Configurations



MAX498 appears at end of data sheet.

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})....................+12V
Voltage on IN__ to GND ....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Voltage on Digital Inputs
(LE, $\overline{EN}$, A0, $\overline{CS}$)....................-0.3V to (V_{CC} + 0.3V)
Voltage on OUT_ (disabled) ....±4V
Output Short-Circuit Duration
to -4V ≤ OUT_ ≤ +4V ....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin SO (derate 11.76mW/°C above +70°C)............941mW
28-Pin SO (derate 12.5mW/°C above +70°C)....................1W
Operating Temperature Range ....0°C to +70°
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $V_{IN\_\_}$ = 0V, R_L = 150Ω, LE = $\overline{EN}$ = $\overline{CS}$ = 0V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			±1.25	±1.70		V
Voltage Gain	A_V	R_L = 150Ω, -1.25V ≤ V_{IN} ≤ +1.25V		1.985		2.030	V/V
		R_L = 75Ω, -1.0V ≤ V_{IN} ≤ +1.0V		1.965		2.030	
Input Offset Voltage	V_{OS}				±2	±9	mV
Input Offset Voltage Drift	TCV_{OS}				±50		µV/°C
Input Bias Current	I_B				±1	±7	µA
Input Resistance	R_{IN}	-1.25V ≤ V_{IN} ≤ +1.25V		200	700		kΩ
Input Capacitance	C_{IN}	Channel on or off			2		pF
Output Short-Circuit Current	$I_{OUT(SC)}$	-3.5V ≤ OUT_ ≤ +3.5V (Note 1)			120		mA
Output Current	$I_{OUT\_}$	-2.0V ≤ $V_{OUT\_}$ ≤ +2.0V, R_L = 75Ω		±27	±40		mA
On Output Resistance	R_{OUT}				0.15		Ω
On Output Impedance		f = 10MHz			3.0		Ω
Off Output Resistance		-2.50V ≤ V_{OUT} ≤ +2.50V		1.0	1.2		kΩ
Operating Supply-Voltage Range				±4.50		±5.50	V
Positive Power-Supply Rejection	PSR+	4.50V ≤ V_{CC} ≤ 5.50V, V_{EE} = -5.0V		55	72		dB
Negative Power-Supply Rejection	PSR-	-5.50V ≤ V_{EE} ≤ -4.5V, V_{CC} = +5.0V		55	72		dB
Logic Low Voltage	V_{INLL}			0.8			V
Logic High Voltage	V_{INLH}					2	V
Logic Input Current	I_{INL}	0V ≤ V_{INL} ≤ V_{CC}		-10		130	µA
Positive Supply Current	I_{CC}	$\overline{EN}$ = 0	MAX498		40	52	mA
			MAX499		31	41	
		$\overline{EN}$ = 1	MAX498		14	17	
			MAX499		11	14	
Negative Supply Current	I_{EE}	$\overline{EN}$ = 0	MAX498		38	50	mA
			MAX499		29	39	
		$\overline{EN}$ = 1	MAX498		12	15	
			MAX499		9	12	

Note 1: Limited by package power dissipation.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $V_{IN\_\_}$ = 0V, R_L = 100Ω, LE = $\overline{EN}$ = $\overline{CS}$ = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal, -3dB Bandwidth	BW_{-3dB}	V_{IN} ≤ 100mVp-p		250		MHz
±0.1dB Gain Flatness		V_{IN} ≤ 100mVp-p		70		MHz
Full-Power, -3dB Bandwidth	FPBW	V_{OUT} = ±2V		135		MHz
Slew Rate	SR	V_{OUT} = 4V step		1250		V/µs
Settling Time	t_S	0.1%, V_{OUT} = 4V step		12		ns
Input Voltage Noise Density		f = 100kHz		7.8		nV/√Hz
Input Current Noise Density		f = 100kHz		2.6		pA/√Hz
Total Harmonic Distortion	THD	f = 10MHz		-50		dB
Spurious-Free Dynamic Range	SFDR	f_C = 3MHz		-66		dBc
Adjacent-Channel Crosstalk		f = 10MHz (Note 2)		90		dB
All-Hostile Crosstalk		f = 10MHz (Note 3)		62		dB
Off-Isolation		$\overline{EN}$ = 1, f = 10MHz (Note 4)		81		dB
Differential Gain	Diff Gain	f = 3.58MHz (Note 5), R_L = 150Ω		0.03		%
Differential Phase	Diff Phase	f = 3.58MHz (Note 5), R_L = 150Ω		0.06		degrees

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $V_{IN\_\_}$ = 0V, R_L = 150Ω, LE = $\overline{EN}$ = $\overline{CS}$ = 0V, T_A = 0°C to +70°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
A0/$\overline{EN}$ to $\overline{CS}$ Setup Time	t_{SU}	LE = high (Note 6)		8			ns
A0/$\overline{EN}$ to $\overline{CS}$ Hold Time	t_H	LE = high (Note 6)				4	ns
$\overline{CS}$ Pulse Width	t_{CS}	(Note 6)		15			ns
Channel-Switching Propagation Delay	t_{PD}	(Note 7)			20		ns
Channel-Switching Time	t_{SW}	(Note 8)			3		ns
Channel-Switching Transient		V_{INA} = V_{INB} = 0V	Positive		70		mV
			Negative		50		
Enable/Disable Switching Transient		V_{INA} = V_{INB} = 0V	Positive		10		mV
			Negative		150		
Amplifier-Disable Time	t_{OFF}	(Note 9)			16		ns
Amplifier-Enable Time	t_{ON}	(Note 10)			24		ns

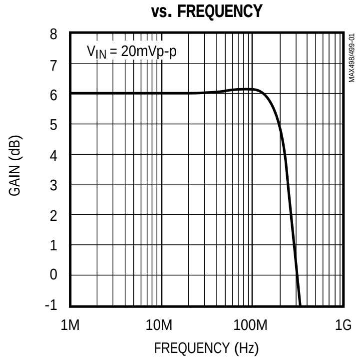
Note 2: Test-channel input grounded through a 50Ω resistor. Adjacent channel driven to a 2Vp-p output with a 10MHz sine wave (Figure 9).
Note 3: Same as Note 2, except all channels but the test channel are driven to a 2Vp-p output with a 10MHz sine wave (Figure 9).
Note 4: Test-channel input connected to a $2V_{p-p}$ sine wave at 10MHz. The test channel's output is measured with the outputs disabled (Figure 9).
Note 5: Input test signal is a 3.58MHz sine wave of 40IRE amplitude, superimposed on a 0IRE to 100IRE linear ramp (Figure 10).
Note 6: Guaranteed by design.
Note 7: V_{INA} = +1V, V_{INB} = -1V, delay from $\overline{CS}$ to 10% of V_{OUT}.
Note 8: V_{INA} = +1V, V_{INB} = -1V, delay from $\overline{CS}$ to 10% of V_{OUT}.
Note 9: Delay from $\overline{EN}$ to 90% of V_{OUT}.
Note 10: Delay from $\overline{EN}$ to 10% of V_{OUT}.

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

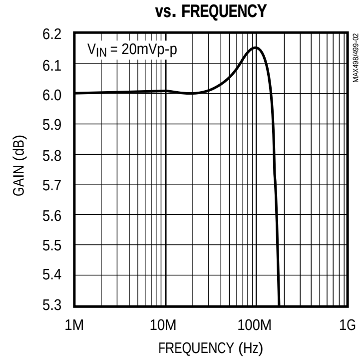
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

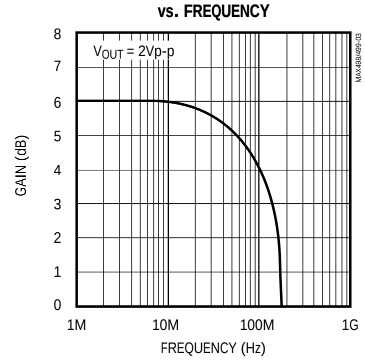
SMALL-SIGNAL GAIN vs. FREQUENCY



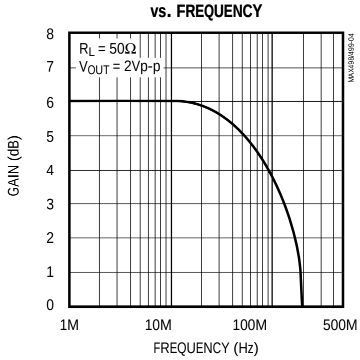
GAIN FLATNESS vs. FREQUENCY



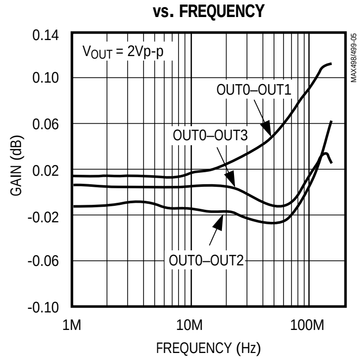
LARGE-SIGNAL GAIN vs. FREQUENCY



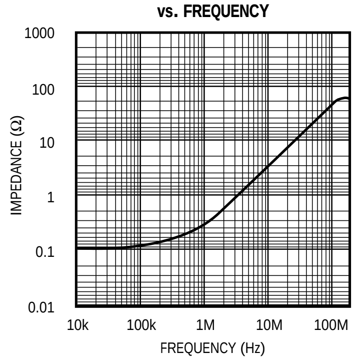
LARGE-SIGNAL GAIN vs. FREQUENCY



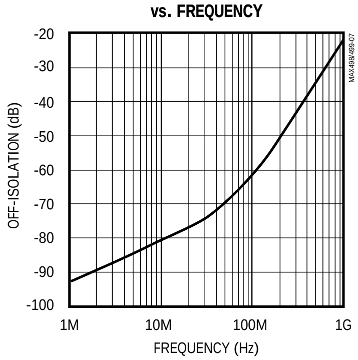
LARGE-SIGNAL GAIN vs. FREQUENCY



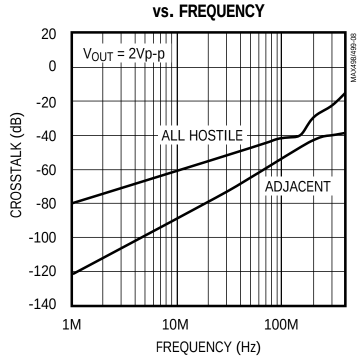
OUTPUT IMPEDANCE vs. FREQUENCY



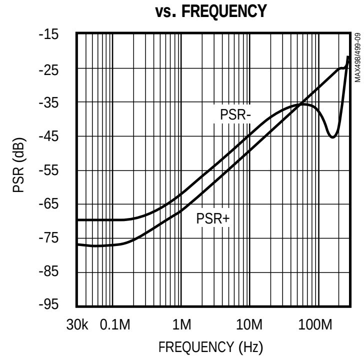
OFF-ISOLATION vs. FREQUENCY



CROSSTALK vs. FREQUENCY

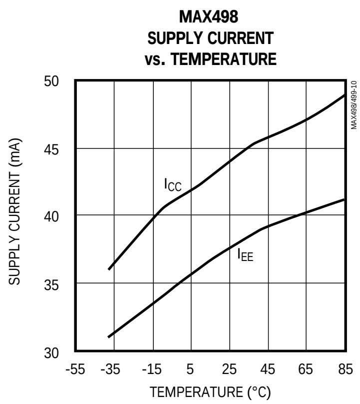


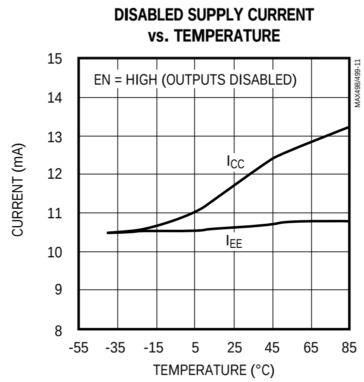
POWER-SUPPLY REJECTION vs. FREQUENCY

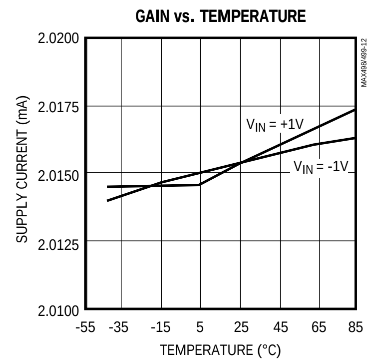


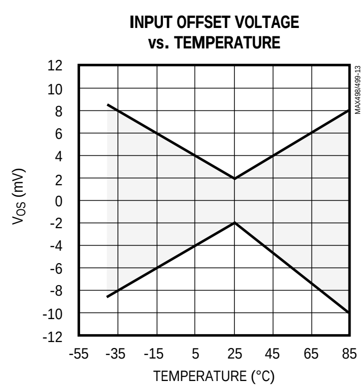
Typical Operating Characteristics (continued)

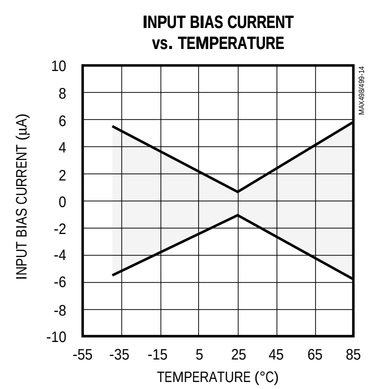
(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

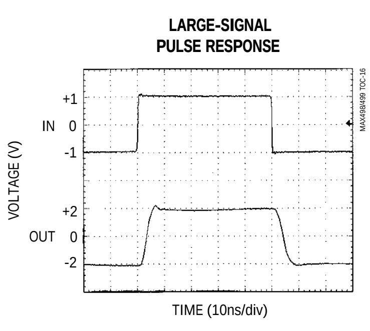


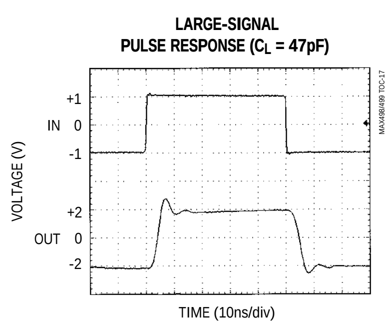


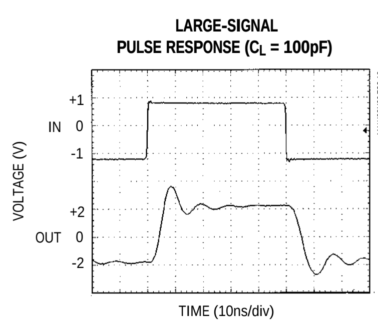










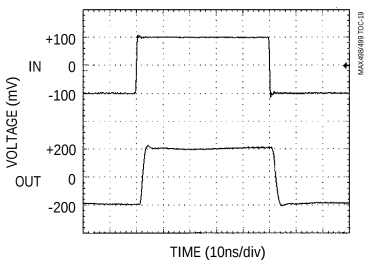


Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

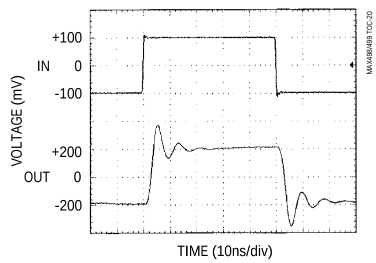
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

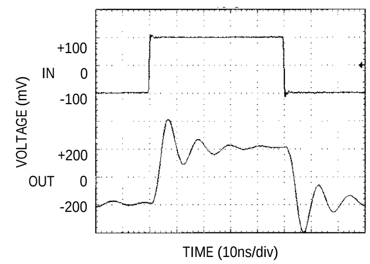
SMALL-SIGNAL PULSE RESPONSE



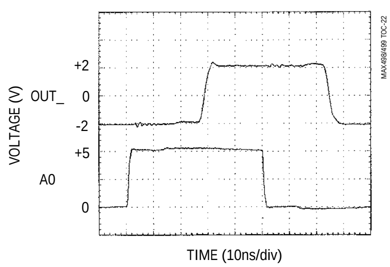
SMALL-SIGNAL PULSE RESPONSE (C_L = 47pF)



SMALL-SIGNAL PULSE RESPONSE (C_L = 100pF)

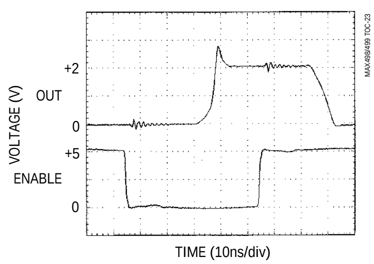


CHANNEL SWITCHING

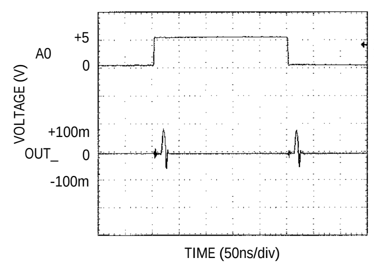


IN_A = -1V
IN_B = +1V

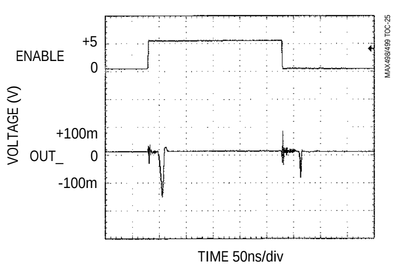
ENABLE/DISABLE SWITCHING



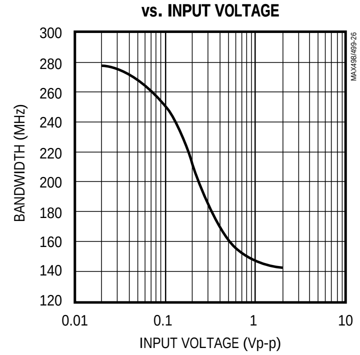
CHANNEL-SWITCHING TRANSIENT



ENABLE/DISABLE SWITCHING TRANSIENT



BANDWIDTH vs. INPUT VOLTAGE



Pin Description

PIN		NAME	FUNCTION
MAX498	MAX499		
1, 3, 5, 11, 13, 19	2, 4, 9, 11, 24	GND	Analog Ground. All ground pins are internally connected. Connect all ground pins externally to ground to minimize impedance.
2	1	IN1A	Signal Input 1, Channel A
4	3	IN2A	Signal Input 2, Channel A
6	5	IN3A	Signal Input 3, Channel A
7, 22	6, 18	V_{CC}	Positive Power-Supply Voltage. Connect V_{CC} to +5V. V_{CC} pins are internally connected. Connect both pins externally to +5V to minimize supply impedance. Bypass each pin to ground with a 0.1µF ceramic capacitor.
8	—	IN0B	Signal Input 0, Channel B
9, 21	7, 17	V_{EE}	Negative Power-Supply Voltage. Connect V_{EE} to -5V. V_{EE} pins are internally connected. Connect both pins to -5V externally to minimize supply impedance. Bypass each pin to ground with a 0.1µF ceramic capacitor.
10	8	IN1B	Signal Input 1, Channel B
12	10	IN2B	Signal Input 2, Channel B
14	12	IN3B	Signal Input 3, Channel B
15, 17	13, 15	N.C.	No Connect. Not internally connected; connect to GND.
16	14	OUT3	Output 3
18	16	OUT2	Output 2
20	19	OUT1	Output 1
23	—	OUT0	Output 0
24	20	$\overline{CS}$	Chip-Select Input. When $\overline{CS}$ is low, the A0 and $\overline{EN}$ latches are transparent. The data present at A0 is latched when $\overline{CS}$ goes high. LE's status determines whether $\overline{EN}$ is latched along with A0, or if the $\overline{EN}$ latch remains transparent independently of $\overline{CS}$.
25	21	A0	Address Input. A0 = 0 selects channel A, and A0 = 1 selects channel B if $\overline{CS}$ is low. A0 is latched on $\overline{CS}$'s low-to-high transition.
26	22	$\overline{EN}$	Output Buffer-Enable Input. $\overline{EN}$ = 0 enables the output buffer amplifiers, and $\overline{EN}$ = 1 disables the output buffers if $\overline{CS}$ is low. $\overline{EN}$ is latched during $\overline{CS}$'s low-to-high transition if LE is high. $\overline{EN}$ is not latched if LE is low.
27	23	LE	Latch-Enable Input. With LE = 1, $\overline{EN}$ is latched along with A0 when $\overline{CS}$ goes high. When LE = 0, the $\overline{EN}$ latch is transparent independently of $\overline{CS}$'s state.
28	—	IN0A	Signal Input 0, Channel A

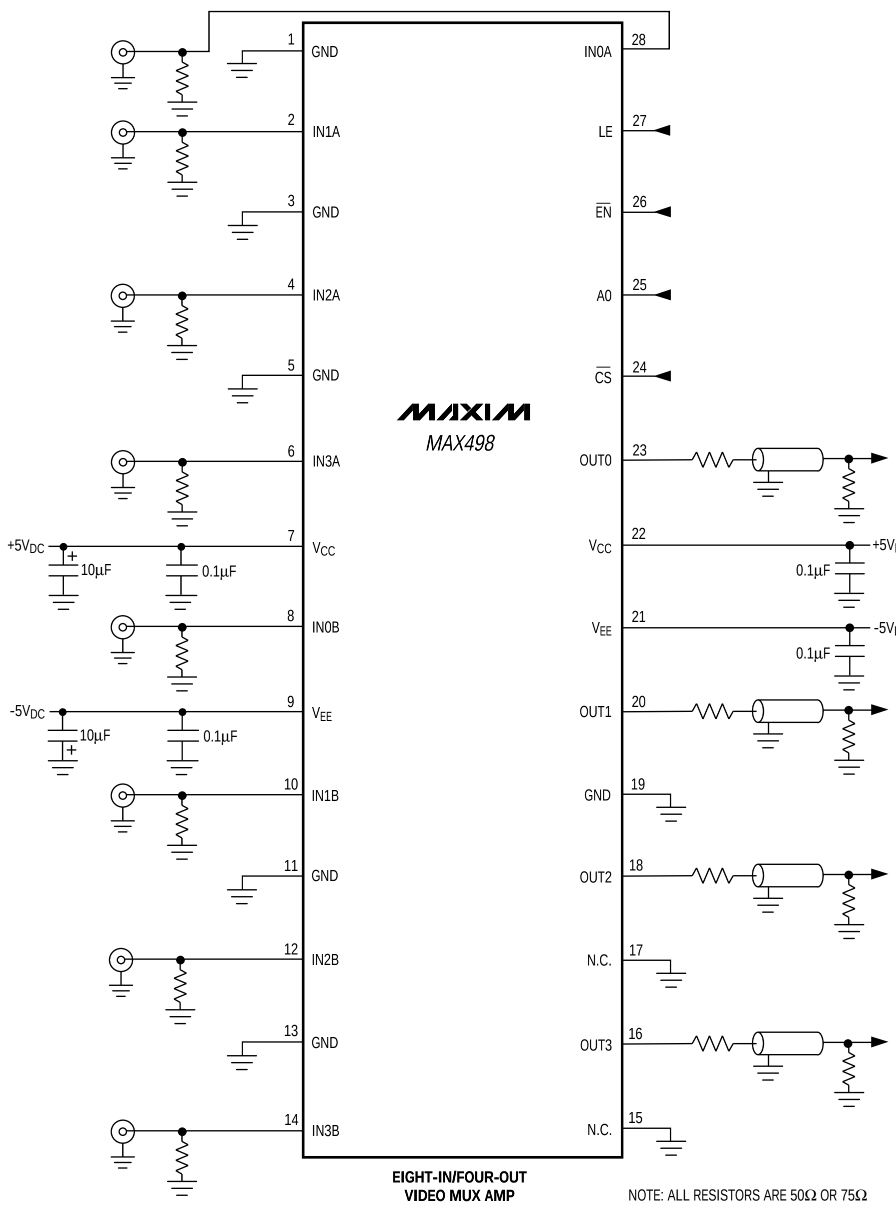


Figure 1a. MAX498 Typical Application Circuit

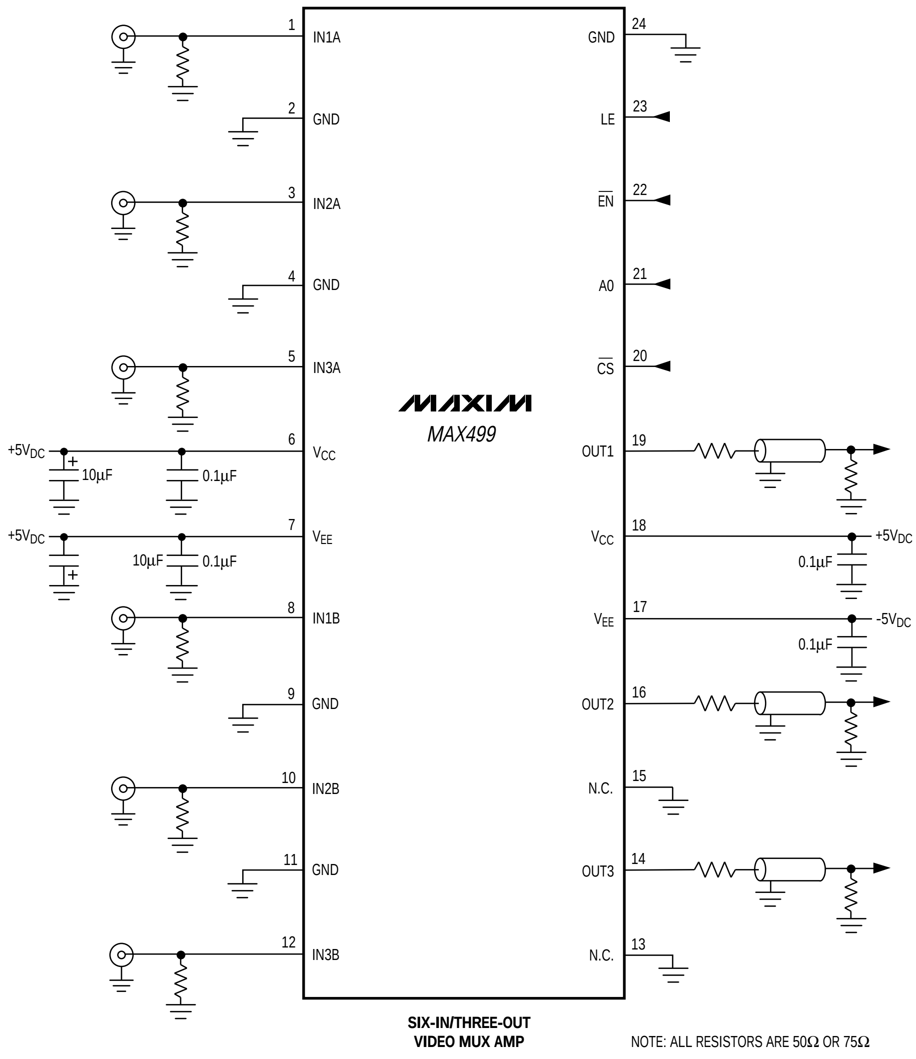


Figure 1b. MAX499 Typical Application Circuit

Detailed Description

The MAX498/MAX499 are quad/triple video switches with high-speed, closed-loop, voltage-feedback amplifiers set to a 2V/V gain. Figure 1 shows typical application circuits. The amplifiers use a unique two-stage, voltage-feedback architecture that combines the benefits of conventional voltage-feedback and current-feedback topologies to achieve wide bandwidths and high slew rates while maintaining precision.

Figure 2 is a simplified block diagram of the MAX498/MAX499. All four amplifier/switch blocks are identical to that shown for Ch_0. A common control logic block accepts external logic inputs A0, $\overline{EN}$, $\overline{CS}$, and LE, and controls the status of switches S1, S2, and S3 of each amplifier in parallel, as described in the *Digital Interface* section.

S3 is open in the enabled state, and if Ch_A is selected, S1 is connected to IN_A and S2 is connected to GND. If Ch_B is selected, S1 is connected to GND and S2 is connected to IN_B. Connecting the deselected GM_ block to GND ensures minimum feedthrough.

S3 is closed in the disabled state, and both S1 and S2 are connected to GND. Disconnecting both inputs and connecting the amplifier's inputs to GND significantly improves off-isolation.

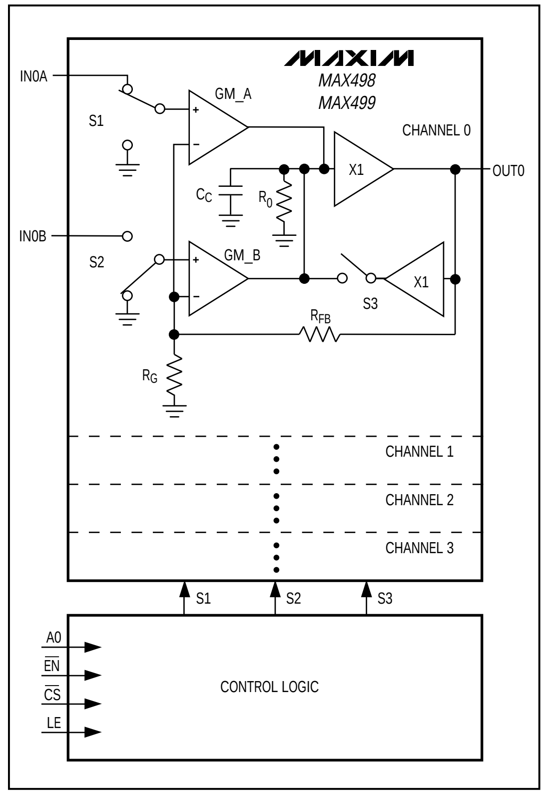


Figure 2. Block Diagram

Applications Information

Power Dissipation

The MAX498/MAX499's maximum output current is limited by the package's maximum allowable power dissipation. The maximum junction temperature should not exceed +150°C. Power dissipation increases with load, and this increase can be approximated by one of the following equations:

For $V_{OUT} > 0V$: $|V_{CC} - V_{OUT}| \, I_{LOAD}$

OR

For $V_{OUT} < 0V$: $|V_{EE} - V_{OUT}| \, I_{LOAD}$.

These devices can drive 100Ω loads connected to each of the outputs over the entire rated output swing and temperature range. While the output is short-circuit protected to 120mA, this does not necessarily guarantee that under all conditions, the maximum junction temperature will not be exceeded. Do not exceed the derating values given in the *Absolute Maximum Ratings* section.

Total Noise

The MAX498/MAX499's low $2.6pA/\sqrt{Hz}$ input current noise and $7.8nV/\sqrt{Hz}$ voltage noise provide for lower total noise compared to typical current-mode feedback amplifiers, which usually have significantly higher input current noise. The input current noise multiplied by the feedback resistor is the dominant noise source of current-mode feedback amplifiers.

Differential Gain and Phase Errors

Differential gain and phase errors are critical specifications for a buffer in composite (NTSC, PAL, SECAM) video applications, because these errors correspond directly to color changes in the displayed picture of composite video systems. The MAX498/MAX499's low differential gain and phase errors (0.03%/0.06°) make them ideal in broadcast-quality, composite video applications.

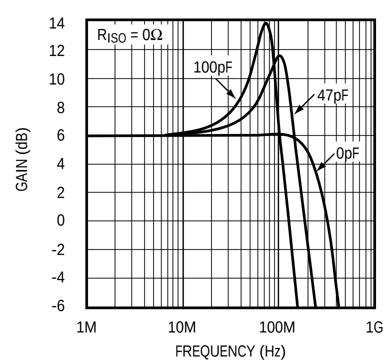


Figure 3a. Small-Signal Gain vs. Frequency and Load Capacitor (R_L = 100Ω, R_{ISO} = 0Ω)

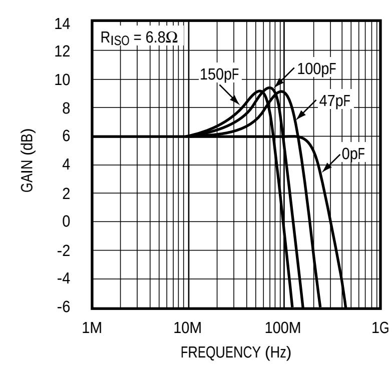


Figure 3b. Small-Signal Gain vs. Frequency and Load Capacitor (R_L = 100Ω, R_{ISO} = 6.8Ω)

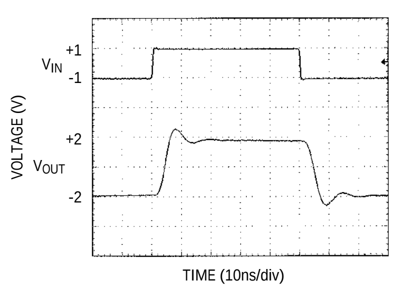


Figure 4a. Large-Signal Pulse Response with C_L = 100pF and R_{ISO} = 5.1Ω

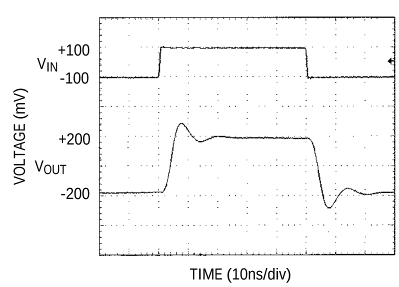


Figure 4b. Small-Signal Pulse Response with C_L = 100pF and R_{ISO} = 5.1Ω

Coaxial Cable Drivers

High-speed performance, excellent output current capability, and an internally fixed gain of +2 make the MAX498/MAX499 ideal for driving back-terminated 50Ω or 75Ω coaxial cables to ±2.5V.

In a typical application, the MAX498/MAX499 drive a back-terminated cable (Figure 1). The back-termination resistor, at the output, matches the impedance of the cable's driven end to the cable's impedance, eliminating signal reflections. This resistor, along with the load-termination resistor, forms a voltage divider with the load impedance, which attenuates the signal at the cable's output by one-half. The MAX498/MAX499 operate with an internal +2V/V closed-loop gain to provide unity gain at the cable's output.

Capacitive-Load Driving

In most amplifier circuits, driving large capacitive loads increases the likelihood of oscillation. This is especially true for circuits with high loop gains, such as voltage followers. The amplifier's output resistance and the capacitive load form an RC filter that adds a pole to the loop response. If the pole frequency is low enough (as when driving a large capacitive load), the circuit-phase margin is degraded and oscillation may occur.

The MAX498/MAX499 drive capacitive loads up to 100pF without sustained oscillation, although some peaking may occur (Figures 3a and 3b). When driving larger capacitive loads, or to reduce peaking, add an isolation resistor (R_{ISO}) between the output and the capacitive load (Figures 4a, 4b, and 5).

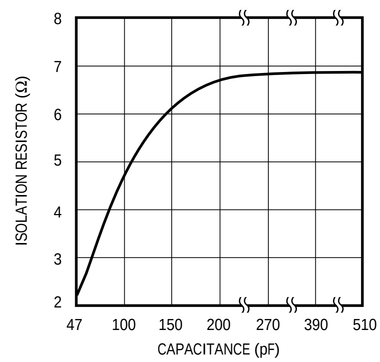


Figure 5. Isolation Resistor vs. Capacitive Load

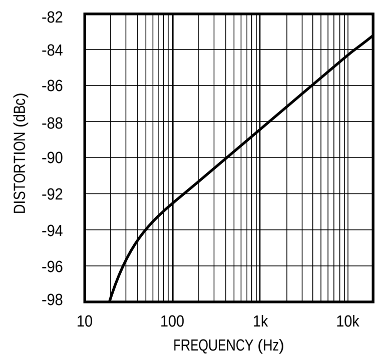


Figure 6. Total Harmonic Distortion (Audio) vs. Frequency

Switching Audio Signals (Audio-Distortion Measurement)

When switching audio signals, distortion is the prime consideration in performance. Figure 6 shows total harmonic distortion vs. frequency, in the audio range, for the MAX498/MAX499.

Large Switch Arrays

Large crosspoint switch arrays are possible with the MAX498/MAX499 using the enable function $\overline{EN}$. When the amplifiers are disabled, output impedance is typically 1.2kΩ, due to the feedback and gain resistors. This limits the number of outputs that can be paralleled without a buffer. Since each output can drive 100Ω, eight outputs can typically be connected together. If additional outputs must be connected in parallel, a MAX4178 (single), MAX496 (quad), or equivalent unity-gain buffer can be used.

Whether enabled or disabled, each input represents more than 200kΩ of resistance. Capacitance is the prime consideration limiting the number of inputs that can be connected to a single output. Since each output can drive 100pF of capacitance without an isolation resistor, 50 inputs (C_{IN} = 2pF, typical) can be driven by a single output. However, peaking will occur as inputs are added (Figure 3), which reduces the 0.1dB bandwidth.

Digital Interface

The MAX498/MAX499 multiplexer architecture ensures that no input channels are ever connected together. Select a channel by changing A0's state (A0 = 0 for channel A, and A0 = 1 for channel B) and pulsing $\overline{CS}$ low (see Tables 1a and 1b). Figure 7 shows the logic timing diagram.

When the enable input ($\overline{EN}$) is driven to a TTL low state, it enables the MAX498/MAX499 amplifier outputs. When $\overline{EN}$ is driven high, it disables the amplifier outputs. When disabled, the MAX498/MAX499 exhibit a 1.2kΩ disabled output resistance due to their internal feedback resistors.

LE determines whether $\overline{EN}$ is latched by $\overline{CS}$ or operates independently. When the latch-enable input (LE) is connected to V+, $\overline{CS}$ becomes the latch control for the $\overline{EN}$ input register. If $\overline{CS}$ is low, both the $\overline{EN}$ and A0 latches are transparent; once $\overline{CS}$ returns high, both A0 and $\overline{EN}$ are latched.

When LE is connected to ground, the $\overline{EN}$ latch is transparent and independent of $\overline{CS}$. This allows all MAX498/MAX499 devices to be shut down simultaneously, regardless of $\overline{CS}$'s input state. Simply connect LE to ground and connect all $\overline{EN}$ inputs together (Figure 8a). Hard wire LE to V+ or ground (rather than driving LE with a gate) to prevent crosstalk from the digital inputs to IN0A.

Another option for output disable is to connect LE to V+, parallel the outputs of several MAX498/MAX499s, and use EN to individually disable all devices but the one in use (Figure 8b).

When the outputs are disabled, off-isolation from the analog inputs to the amplifier outputs is typically 81dB at 10MHz.

Grounding and Layout

The MAX498/MAX499 bandwidths are in the RF frequency range. Depending on the size of the PC board used and the frequency of operation, it may be necessary to use Micro-strip or Stripline techniques.

To realize the full AC performance of these high-speed buffers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers (wire-wrap boards are too inductive, and bread boards are too capacitive), with one side a signal layer and the other a large, low-impedance ground plane. With multilayer boards, locate the ground plane on the layer that is not dedicated to a specific signal trace. The ground plane should be as free from voids as possible. Connect all ground pins to the ground plane.

Connect both positive power-supply pins together and bypass with a 0.10µF ceramic capacitor at each power-supply pin, as close to the device as possible. Repeat for the negative power-supply pins. The capacitor lead lengths should be as short as possible to minimize lead inductance; surface-mount chip capacitors are ideal. A large-value (10µF or greater) tantalum or electrolytic bypass capacitor on each supply may be required for high-current loads. The location of this capacitor is not critical.

The MAX498/MAX499's analog input pins are isolated with ground pins to minimize parasitic coupling, which can degrade crosstalk and/or amplifier stability. Keep signal paths as short as possible to minimize inductance. Ensure that all input channel traces are the same length, to maintain the phase relationship between the four channels. To further reduce crosstalk, connect the coaxial-cable shield to the ground side of the 75Ω terminating resistor at the ground plane, and terminate all unused inputs to ground and outputs with a 100Ω or 150Ω resistor to ground.

Table 1a. Amplifier and Channel Selection with LE = V+

$\overline{CS}$	$\overline{EN}$	A0	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
0	0	1	Enables amplifier outputs. Selects channel B.
0	1	X	Disables amplifiers. Outputs high-Z.
1	X	X	Latches A0, $\overline{EN}$. Outputs unchanged.

Table 1b. Amplifier and Channel Selection with LE = GND

$\overline{CE}$	$\overline{EN}$	$\overline{A0}$	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
1	0	X	Enables amplifier outputs. Latches A0 to output A or B, according to A0's state at $\overline{CS}$'s last edge.
X	1	X	Disables amplifiers. Outputs high-Z. A0 latch = channel A.
0	0	1	Enables amplifier outputs. Selects channel B.

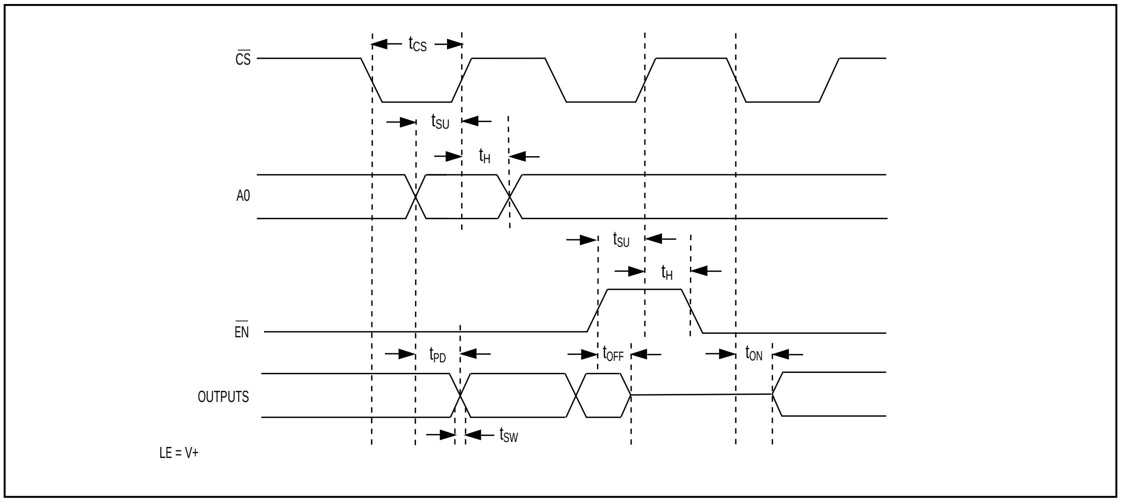


Figure 7. Logic Timing Diagram

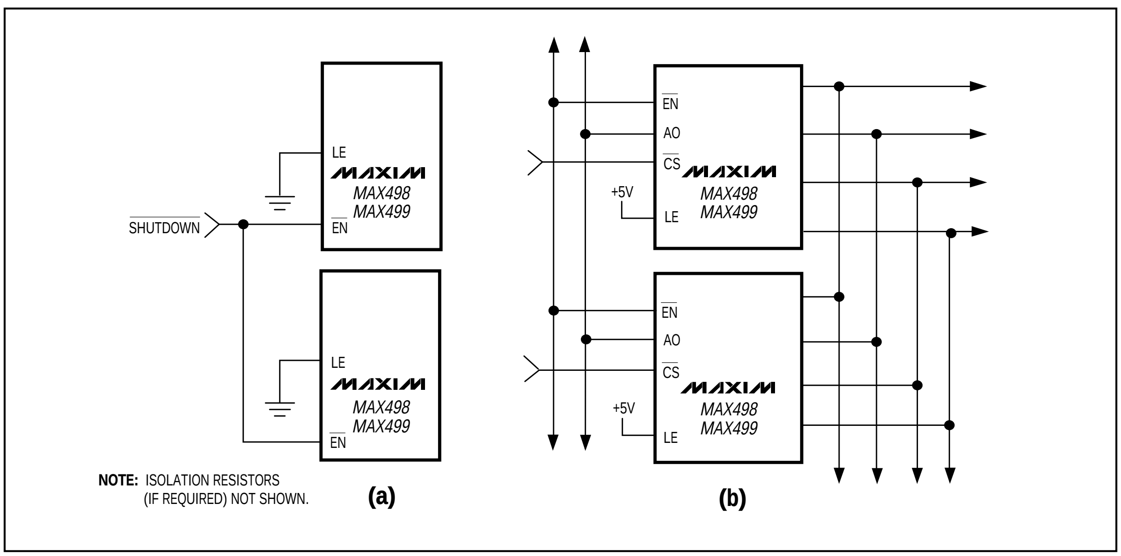


Figure 8. (a) Simultaneous Shutdown of all MAX498/MAX499s; (b) Enable (EN) Register Latched by CS

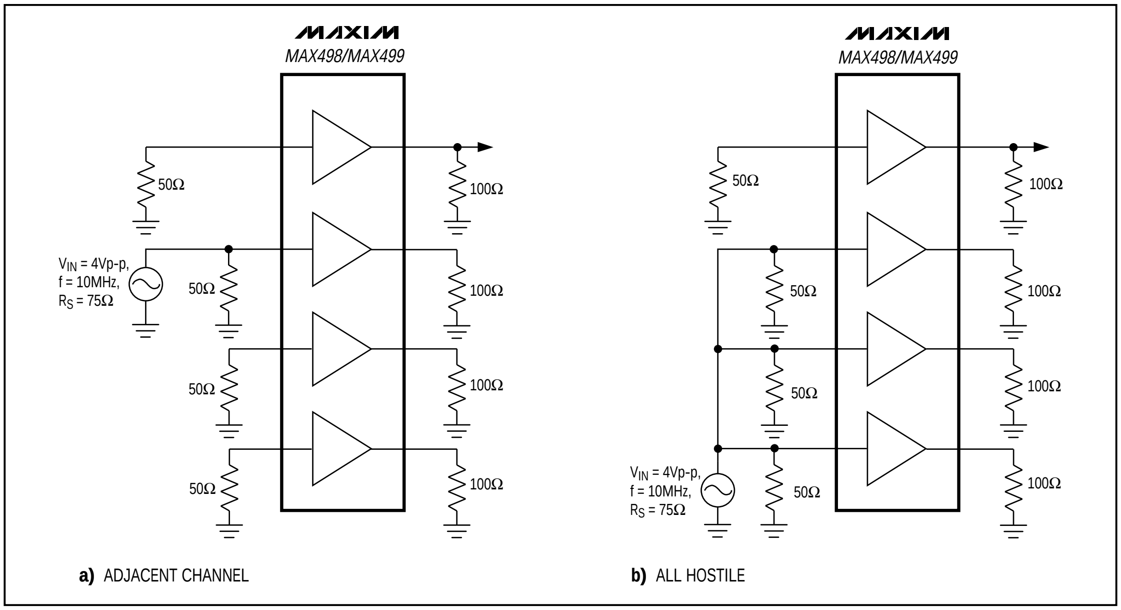


Figure 9. Test Circuits for Measuring Crosstalk: a) Adjacent Channel; b) All Hostile

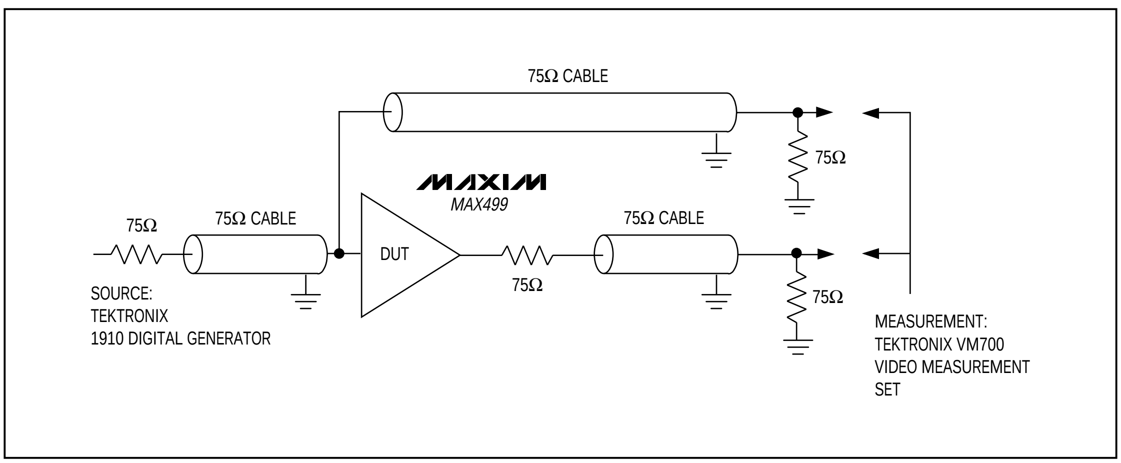
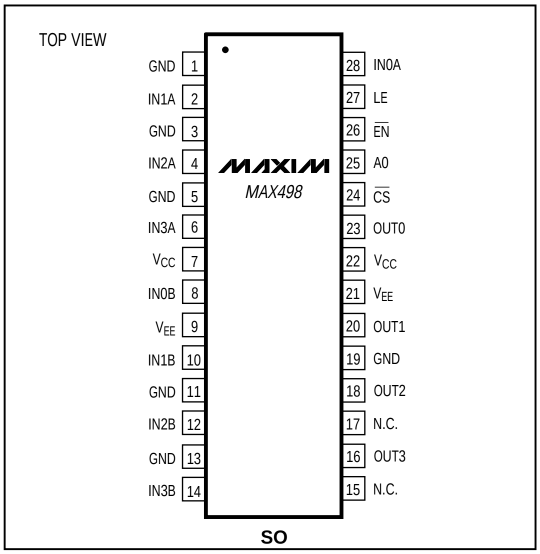


Figure 10. Differential Phase and Gain Error Test Circuit

Quad/Triple, SPDT, RGB Switches with 250MHz Video Buffer Amplifiers

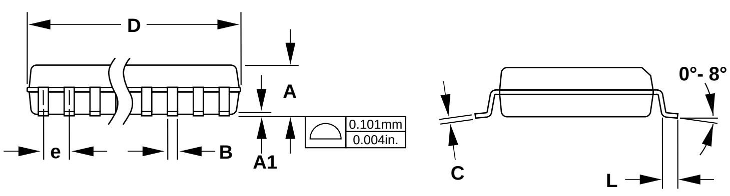
Pin Configurations (continued)

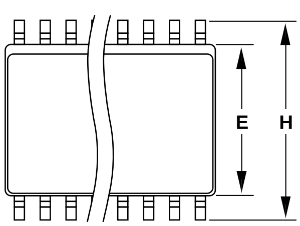


Chip Information

SUBSTRATE CONNECTED TO: V_{EE}
TRANSISTOR COUNT: 813

Package Information





Wide SO SMALL-OUTLINE PACKAGE (0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

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