19-1560; Rev 1; 7/05

+2.7V to +5.5V, Low-Power, Triple, Parallel 8-Bit DAC with Rail-to-Rail Voltage Outputs

MAX5101

General Description

The MAX5101 parallel-input, voltage-output, triple 8-bit digital-to-analog converter (DAC) operates from a single +2.7V to +5.5V supply and comes in a space-saving 16-pin TSSOP package. Internal precision buffers swing rail-to-rail. For all three DACs, the internal reference voltage is tied to V_{DD}.

The MAX5101 has separate input latches for each of its three DACs. Data is transferred to the input latches from a common 8-bit input port. The DACs are individually selected through address inputs A0 and A1 and are updated by bringing $\overline{WR}$ low.

The MAX5101 features a 1µA software shutdown mode, as well as a power-on reset mode that resets all registers to code 00 hex on power-up.

Features

- ♦ +2.7V to +5.5V Single-Supply Operation
- ♦ Ultra-Low Supply Current
  - 0.3mA while Operating
  - 1µA in Software Shutdown Mode
- ♦ Ultra-Small 16-Pin TSSOP Package
- ♦ Output Buffer Amplifiers Swing Rail-to-Rail
- ♦ Power-On Reset Sets All Registers to Zero

Applications

Digital Gain and Offset Adjustment

Programmable Attenuators

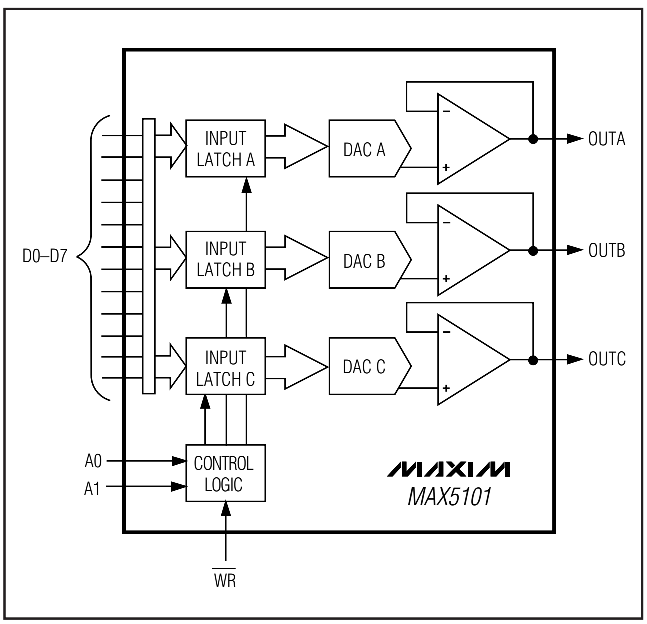
Portable Instruments

Power-Amp Bias Control

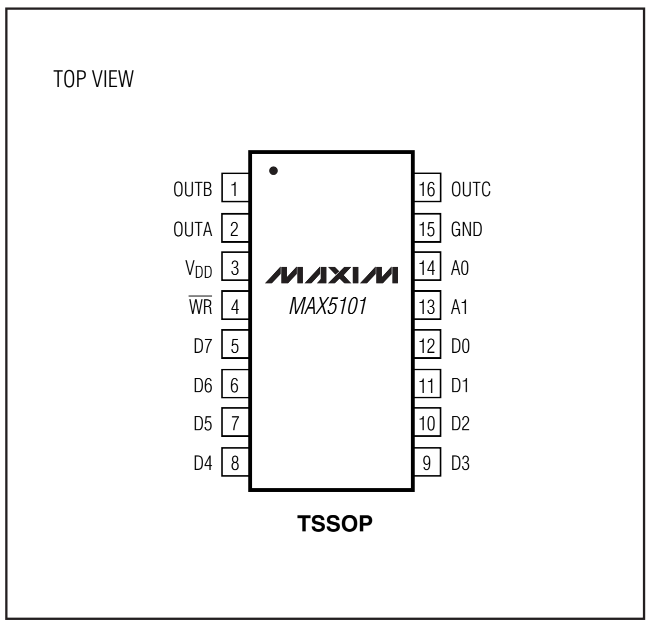
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX5101AEUE	-40°C to +85°C	16 TSSOP	±1
MAX5101BEUE	-40°C to +85°C	16 TSSOP	±2

Functional Diagram



Pin Configuration



+2.7V to +5.5V, Low-Power, Triple, Parallel 8-Bit DAC with Rail-to-Rail Voltage Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6V
D_, A_, $\overline{WR}$ to GND ....-0.3V to +6V
OUT_ to GND ....-0.3V to V_{DD}
Maximum Current into Any Pin ....±50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 5.7mW/°C above +70°C) 457mW

Operating Temperature Range
MAX5101_EUE ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution					8	Bits
Integral Nonlinearity (Note 1)	INL	MAX5101A			±1	LSB
		MAX5101B			±2	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic			±1	LSB
Zero-Code Error	ZCE	Code = 00 hex			±20	mV
Zero-Code-Error Supply Rejection		Code = 00 hex, V_{DD} = 2.7V to 5.5V			10	mV
Zero-Code Temperature Coefficient		Code = 00 hex		±10		µV/°C
Gain Error (Note 2)		Code = F0 hex			±1	%
Gain-Error Temperature Coefficient		Code = F0 hex		±0.001		LSB/°C
DAC OUTPUTS						
Output Voltage Range		R_L = ∞	0		V_{DD}	V
DIGITAL INPUTS						
Input High Voltage	V_{IH}	V_{DD} = 2.7V to 3.6V	2			V
		V_{DD} = 3.6V to 5.5V	3			
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = V_{DD} or GND			±1.0	µA
Input Capacitance	C_{IN}			10		pF
DYNAMIC PERFORMANCE						
Output Voltage Slew Rate		From code 00 to code F0 hex		0.6		V/µs
Output Settling Time (Note 3)		To 1/2LSB, from code 10 to code F0 hex		6		µs
Channel-to-Channel Isolation (Note 4)		Code 00 to code FF hex		500		nVs
Digital Feedthrough (Note 5)		Code 00 to code FF hex		0.5		nVs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital-to-Analog Glitch Impulse		Code 80 hex to code 7F hex		90		nVs
Wideband Amplifier Noise				60		μV_{RMS}
Shutdown Recovery Time	t_{SDR}	To ±1/2LSB of final value of V_{OUT}		13		µs
Time to Shutdown	t_{SDN}	I_{DD} < 5µA		20		µs
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		2.7		5.5	V
Supply Current (Note 6)	I_{DD}			280	520	µA
Shutdown Current				1	3	µA
DIGITAL TIMING (Figure 1) (Note 7)						
Address to $\overline{WR}$ Setup	t_{AS}		5			ns
Address to $\overline{WR}$ Hold	t_{AH}		0			ns
Data to $\overline{WR}$ Setup	t_{DS}		25			ns
Data to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{WR}$ Pulse Width	t_{WR}		20			ns

Note 1: Reduced digital code range (code 00 hex to code F0 hex) due to swing limitations when the output amplifier is loaded.
Note 2: Gain error is: [100 ($V_{F0,meas}$ - ZCE - $V_{F0,ideal}$) / V_{DD}]. Where $V_{F0,meas}$ is the DAC output voltage with input code F0 hex, and $V_{F0,ideal}$ is the ideal DAC output voltage with input code F0 hex (i.e., $V_{DD} \cdot 240 / 256$).
Note 3: Output settling time is measured from the 50% point of the falling edge of $\overline{WR}$ to ±1/2LSB of V_{OUT}'s final value.
Note 4: Channel-to-Channel Isolation is defined as the glitch energy at a DAC output in response to a full-scale step change on any other DAC output. The measured channel has a fixed code of 80 hex.
Note 5: Digital Feedthrough is defined as the glitch energy at any DAC output in response to a full-scale step change on all eight data inputs with $\overline{WR}$ at V_{DD}.
Note 6: $R_L = \infty$, digital inputs at GND or V_{DD}.
Note 7: Timing measurement reference level is (V_{IH} + V_{IL}) / 2.

+2.7V to +5.5V, Low-Power, Triple, Parallel 8-Bit DAC with Rail-to-Rail Voltage Outputs

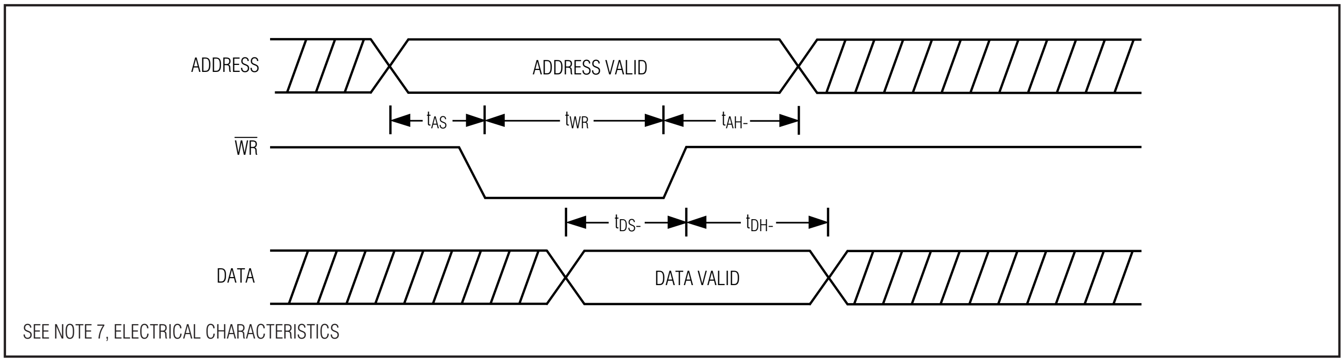
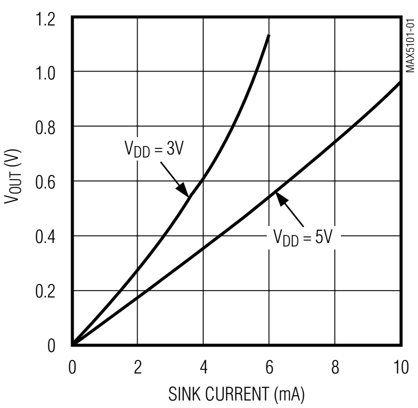


Figure 1. Timing Diagram

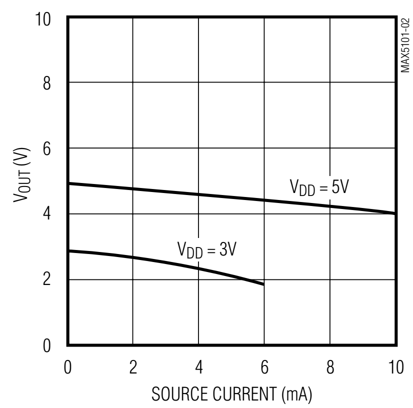
Typical Operating Characteristics

(V_{DD} = +3V, R_L = 10kΩ, C_L = 100pF, code = FF hex, T_A = +25°C, unless otherwise noted.)

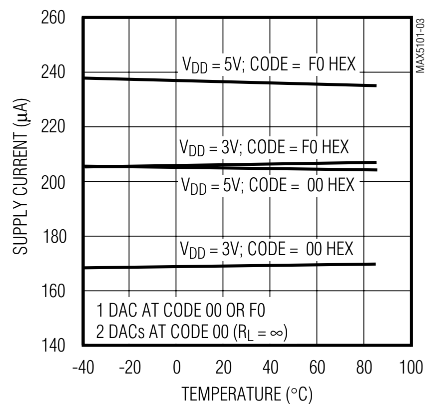
DAC ZERO-CODE OUTPUT VOLTAGE vs. SINK CURRENT



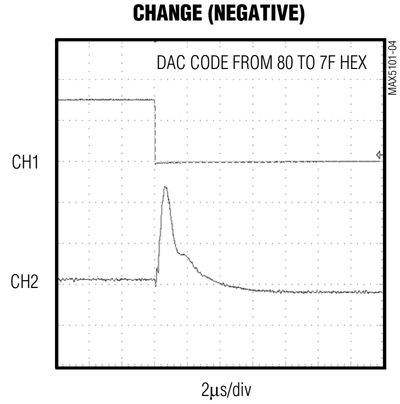
DAC FULL-SCALE OUTPUT VOLTAGE vs. SOURCE CURRENT



SUPPLY CURRENT vs. TEMPERATURE

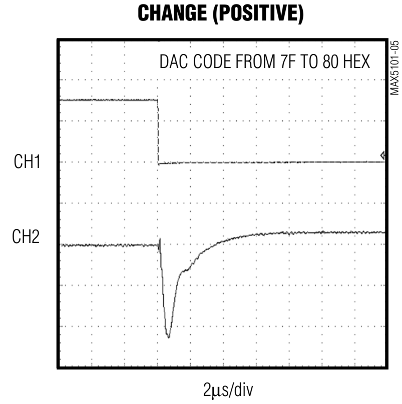


WORST-CASE 1LSB DIGITAL STEP CHANGE (NEGATIVE)



CH1 = $\overline{WR}$, 2V/div
CH2 = V_{OUTA}, 50mV/div, AC-COUPLED

WORST-CASE 1LSB DIGITAL STEP CHANGE (POSITIVE)

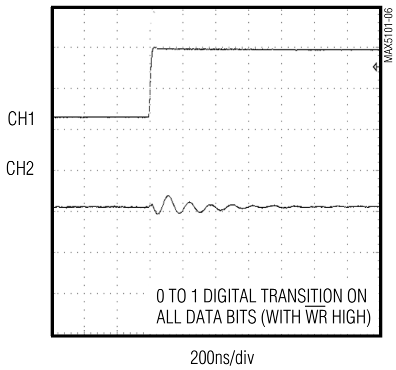


CH1 = $\overline{WR}$, 2V/div
CH2 = V_{OUTA}, 50mV/div, AC-COUPLED

Typical Operating Characteristics (continued)

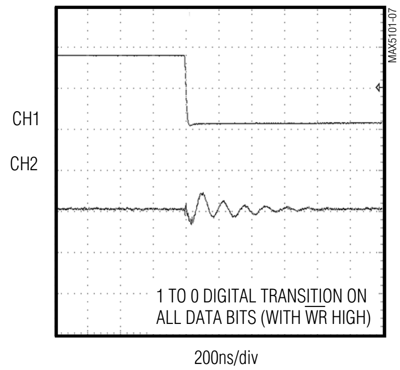
(V_{DD} = +3V, R_L = 10kΩ, C_L = 100pF, code = FF hex, T_A = +25°C, unless otherwise noted.)

DIGITAL FEEDTHROUGH GLITCH IMPULSE (0 TO 1 DIGITAL TRANSMISSION)



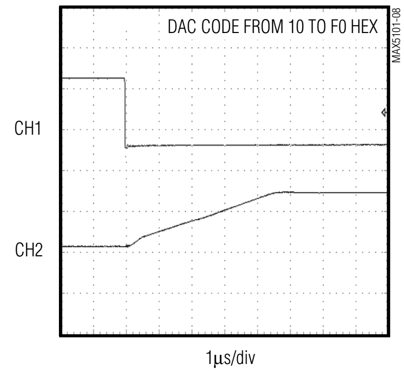
CH1 = D7, 2V/div
CH2 = V_{OUTA}, 1mV/div, AC-COUPLED

DIGITAL FEEDTHROUGH GLITCH IMPULSE (1 TO 0 DIGITAL TRANSMISSION)



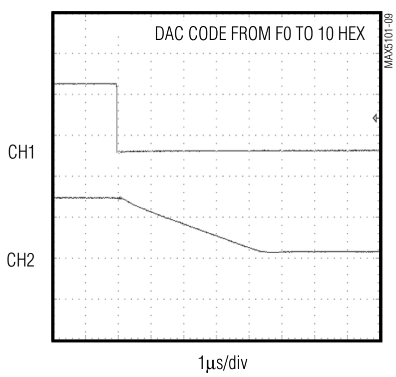
CH1 = D7, 2V/div
CH2 = V_{OUTB}, 1mV/div, AC-COUPLED

POSITIVE SETTLING TIME



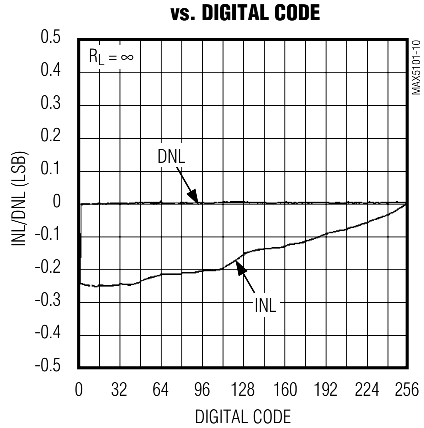
CH1 = $\overline{WR}$, 2V/div
CH2 = V_{OUTA}, 2V/div

NEGATIVE SETTLING TIME



CH1 = $\overline{WR}$, 2V/div
CH2 = V_{OUTA}, 2V/div

INTEGRAL AND DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



+2.7V to +5.5V, Low-Power, Triple, Parallel 8-Bit DAC with Rail-to-Rail Voltage Outputs

Pin Description

PIN	NAME	FUNCTION
1	OUTB	DAC B Voltage Output
2	OUTA	DAC A Voltage Output
3	V_{DD}	Positive Supply Voltage. Bypass V_{DD} to GND using a 0.1µF capacitor.
4	$\overline{WR}$	Write Input (active low). Use $\overline{WR}$ to load data into the DAC input latch selected by A0 and A1.
5–12	D7–D0	Data Inputs 7–0
13	A1	DAC Address Select Bit (MSB)
14	A0	DAC Address Select Bit (LSB)
15	GND	Ground
16	OUTC	DAC C Voltage Output

Detailed Description

Digital-to-Analog Section

The MAX5101 uses a matrix decoding architecture for the digital-to-analog converters (DACs). The internal reference voltage is connected to V_{DD} and divided down by a resistor string placed in a matrix fashion. Row and column decoders select the appropriate tab from the resistor string to provide the needed analog voltages. The resistor network converts the 8-bit digital input into an equivalent analog output voltage in proportion to the supply voltage (V_{DD}). The resistor string presents a code-independent input impedance to the supply and guarantees a monotonic output.

The voltages are buffered by rail-to-rail op amps connected in a follower configuration to provide a rail-to-rail output (see *Functional Diagram*).

Output Buffer Amplifiers

The DAC outputs are internally buffered by a precision amplifier with a typical slew rate of 0.6V/µs. The typical settling time to ±1/2LSB at the output is 6µs when loaded with 10kΩ in parallel with 100pF.

DAC Reference Voltage

The MAX5101's reference is internally tied to V_{DD}. The output voltage (V_{OUT}) for any DAC is represented by a digitally programmable voltage source as follows:

$$V_{OUT} = (N_B \cdot V_{DD}) / 256$$

where N_B is the numeric value of the DAC binary input code.

Digital Inputs and Interface Logic

In the MAX5101, address lines A0 and A1 select the DAC that receives data from D0–D7, as shown in Table 1. When $\overline{WR}$ is low, the addressed DAC's input latch is transparent. Data is latched when $\overline{WR}$ is high. The DAC outputs (OUTA, OUTB) represent the data held in the three 8-bit input latches. To avoid output glitches in the MAX5101, ensure that data is valid before $\overline{WR}$ goes low.

Low-Power Shutdown Mode

The MAX5101 features a software shutdown mode. A write performed to address A1 = H and A0 = H causes the device to shut down. A subsequent write to any of the other three addresses disables shutdown and turns the analog circuitry on. As the MAX5101 comes out of shutdown, all registers retain their digital values prior to shutdown. However, when the device powers up (i.e., V_{DD} ramps up), all latches are internally preset with code 00 hex. In shutdown, the output amplifiers enter a high-impedance state. When bringing the device out of shutdown, allow 13µs for the output to stabilize.

Power-Supply Bypassing and Ground Management

Digital or AC transient signals on GND can create noise at the analog output. Return GND to the highest-quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and GND as possible.

Careful PC board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

Table 1. MAX5101 Addressing Table (partial)

$\overline{WR}$	A1	A0	OPERATION
H	X	X	Input data latched
L	L	L	DAC A input latch transparent
L	L	H	DAC B input latch transparent
L	H	L	DAC C input latch transparent
L	H	H	Enter shutdown mode

H = high state, L = low state, X = don't care

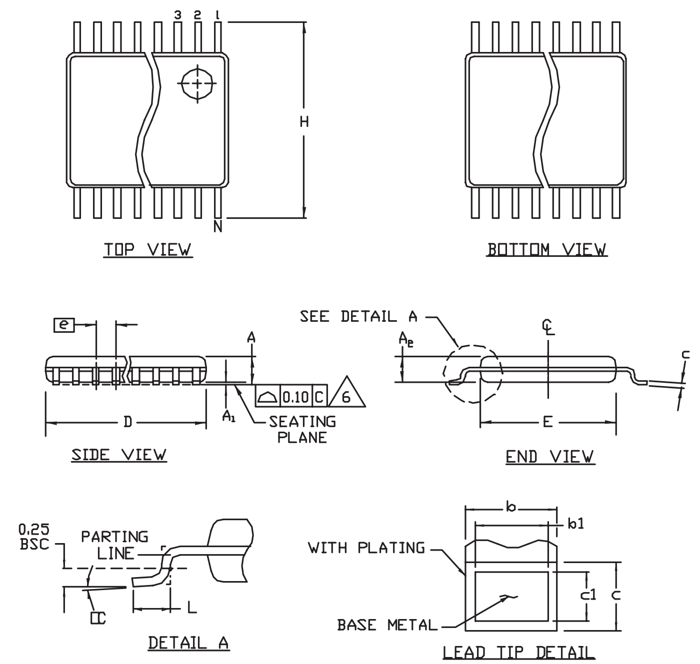
Chip Information

TRANSISTOR COUNT: 6848

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY			
APPROVAL	DOCUMENT CONTROL NO. 21-0066	REV. G	1/1