19-1080; Rev 0; 6/96

MAXIM

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

General Description

The MAX533 serial-input, voltage-output, 8-bit quad digital-to-analog converter (DAC) operates from a single +2.7V to +3.6V supply. Internal precision buffers swing rail to rail, and the reference input range includes both ground and the positive rail. The MAX533 features a 1µA shutdown mode.

The serial interface is double buffered: a 12-bit input shift register is followed by four 8-bit buffer registers and four 8-bit DAC registers. The 12-bit serial word consists of eight data bits and four control bits (for DAC selection and special programming commands). Both the input and DAC registers can be updated independently or simultaneously with a single software command. Two additional asynchronous control pins, $\overline{LDAC}$ and $\overline{CLR}$, provide simultaneous updating or clearing of the input and DAC registers.

The interface is compatible with SPI™, QSPI™ (CPOL = CPHA = 0 or CPOL = CPHA = 1), and Microwire™. A buffered data output allows daisy chaining of serial devices.

In addition to 16-pin DIP and CERDIP packages, the MAX533 is available in a 16-pin QSOP that occupies the same area as an 8-pin SO.

Applications

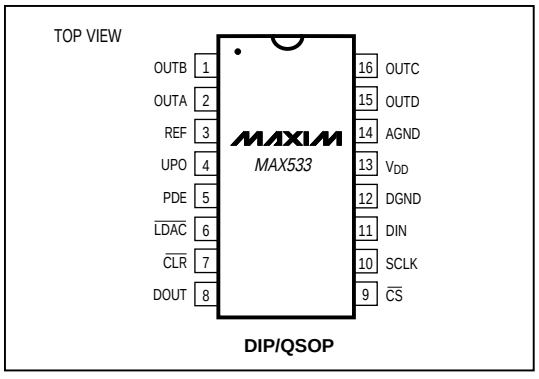
Digital Gain and Offset Adjustments

Programmable Attenuators

Programmable Current Sources

Portable Instruments

Pin Configuration



DIP/QSOP

Features

- ♦ **+2.7V to +3.6V Single-Supply Operation**
- ♦ **Ultra-Low Supply Current:**
  0.7mA while Operating
  1µA in Shutdown Mode
- ♦ **Ultra-Small 16-Pin QSOP Package**
- ♦ **Ground to V_{DD} Reference Input Range**
- ♦ **Output Buffer Amplifiers Swing Rail to Rail**
- ♦ **10MHz Serial Interface, Compatible with SPI, QSPI (CPOL = CPHA = 0 or CPOL = CPHA = 1), and Microwire**
- ♦ **Double-Buffered Registers for Synchronous Updating**
- ♦ **Serial Data Output for Daisy Chaining**
- ♦ **Power-On Reset Clears Serial Interface and Sets All Registers to Zero**
- ♦ **Software Shutdown**
- ♦ **Software-Programmable Logic Output**
- ♦ **Asynchronous Hardware Clear Resets All Internal Registers to Zero**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX533ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX533BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX533ACEE	0°C to +70°C	16 QSOP	±1
MAX533BCEE	0°C to +70°C	16 QSOP	±2
MAX533BC/D	0°C to +70°C	Dice*	±2
MAX533AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX533BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX533AEEE	-40°C to +85°C	16 QSOP	±1
MAX533BEEE	-40°C to +85°C	16 QSOP	±2
MAX533AMJE	-55°C to +125°C	16 CERDIP**	±1
MAX533BMJE	-55°C to +125°C	16 CERDIP**	±2

**Dice are tested at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram appears at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V, +6V
V_{DD} to AGND.....-0.3V, +6V
Digital Input Voltage to DGND .....-0.3V, +6V
Digital Output Voltage to DGND.....-0.3V, (V_{DD} + 0.3V)
AGND to DGND .....±0.3V
REF.....-0.3V, (V_{DD} + 0.3V)
OUT_ .....-0.3V, V_{DD}
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.3mW/°C above +70°C).....667mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX533 _ C_ E .....0°C to +70°C
MAX533 _ E_ E .....-40°C to +85°C
MAX533 _ MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution					8	Bits
Integral Nonlinearity (Note 1)	INL	MAX533A			±1	LSB
		MAX533B			±2	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic (all codes)			±1.0	LSB
Zero-Code Error	ZCE	Code = 00 hex			±20	mV
Zero-Code-Error Supply Rejection		Code = 00 hex, V_{DD} = 2.7V to 3.6V			1	LSB
Zero-Code Temperature Coefficient		Code = 00 hex		±10		µV/°C
Full-Scale Error		Code = FF hex			±30	mV
Full-Scale Error Supply Rejection		Code = FF hex, V_{DD} = 2.7V to 3.6V			1	LSB
Full-Scale Temperature Coefficient		Code = FF hex		±10		µV/°C
REFERENCE INPUTS						
Input Voltage Range			0		V_{DD}	V
Input Resistance			322	460	598	kΩ
Input Capacitance				10		pF
Channel-to-Channel Isolation		(Note 2)		-60		dB
AC Feedthrough		(Note 3)		-70		dB
DAC OUTPUTS						
Output Voltage Range		R_L = open	0		V_{REF}	V
Load Regulation		Code = FF hex, R_L from 10kΩ to ∞			0.25	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7V_{DD}			V
Input Low Voltage	V_{IL}				0.3V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1.0	µA
Input Capacitance	C_{IN}	(Note 4)			10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = TBDmA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate		CODE = FF hex		0.6		V/µs
Output Settling Time		To 1/2LSB, from code 00 to code FF hex (Note 5)		6		µs
Digital Feedthrough and Crosstalk		VREF = 0V, code 00 to code FF hex (Note 6)		5		nV-s
Digital-to-Analog Glitch Impulse		Code 80 hex to code 7F hex		50		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 2.5Vp-p at 1kHz, V_{DD} = 3V, code = FF hex		-70		dB
		V_{REF} = 2.5Vp-p at 10kHz		-62		
Multiplying Bandwidth		V_{REF} = 0.5Vp-p, 3dB bandwidth		380		kHz
Wideband Amplifier Noise				60		µV_{RMS}
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		2.7		3.6	V
Supply Current	I_{DD}	MAX533C/E		0.68	1.3	mA
		MAX533M		0.68	1.5	
Shutdown Current				1	10	µA

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Rise to $\overline{CS}$ Fall Setup Time (Note 4)	t_{VDCS}	MAX533C/E			50	µs
		MAX533M			60	
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}	MAX533C/E	40	20		ns
		MAX533M	50	25		
$\overline{CS}$ Rise to $\overline{LDAC}$ Fall Setup Time (Note 7)	t_{CLL}	MAX533C/E	40			ns
		MAX533M	50			
$\overline{CLR}$ Pulse Width Low	t_{CLW}	MAX533C/E	40	20		ns
		MAX533M	50	25		
$\overline{CS}$ Pulse Width High	t_{CSW}	MAX533C/E	90			ns
		MAX533M	100			

TIMING CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, AGND = DGND = 0V, C_{DOUT} = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

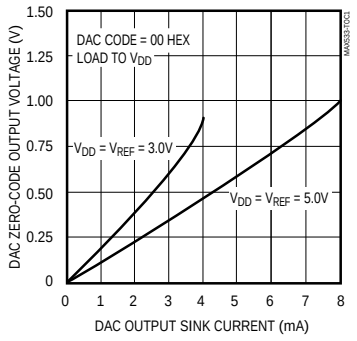
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-INTERFACE TIMING						
SCLK Clock Frequency (Note 8)	f_{CLK}	MAX533C/E			10	MHz
		MAX533M			8.3	
SCLK Pulse Width High	t_{CH}	MAX533C/E	40			ns
		MAX533M	50			
SCLK Pulse Width Low	t_{CL}	MAX533C/E	40			ns
		MAX533M	50			
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}	MAX533C/E	40			ns
		MAX533M	50			
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN to SCLK Rise to Setup Time	t_{DS}	MAX533C/E	40			
		MAX533M	50			
DIN to SCLK Rise to Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay (Note 9)	t_{DO1}	MAX533C/E			200	ns
		MAX533M			230	
SCLK Fall to DOUT Valid Propagation Delay (Note 10)	t_{DO2}	MAX533C/E			210	ns
		MAX533M			250	
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	MAX533C/E	40			ns
		MAX533M	50			
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CS1}	MAX533C/E	40			ns
		MAX533M	50			

Note 1: INL and DNL are measured with R_L referenced to ground. Nonlinearity is measured from the first code that is greater than or equal to the maximum offset specification to code FF hex (full scale). See *DAC Linearity and Voltage Offset* section.
Note 2: V_{REF} = 2.5Vp-p, 10kHz. Channel-to-channel isolation is measured by setting one DAC's code to FF hex and setting all other DAC's codes to 00 hex.
Note 3: V_{REF} = 2.5Vp-p, 10kHz. DAC code = 00 hex.
Note 4: Guaranteed by design, not production tested.
Note 5: Output settling time is measured from the 50% point of the rising edge of $\overline{CS}$ to 1/2LSB of V_{OUT}'s final value.
Note 6: Digital crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other DAC.
Note 7: If $\overline{LDAC}$ is activated prior to $\overline{CS}$'s rising edge, it must stay low for t_{LDAC} or longer after $\overline{CS}$ goes high.
Note 8: When DOUT is not used. If DOUT is used, f_{CLK} max is 4MHz, due to the SCLK to DOUT propagation delay.
Note 9: Serial data clocked out at SCLK's rising edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).
Note 10: Serial data clocked out at SCLK's falling edge (measured from 50% of the clock edge to 20% or 80% of V_{DD}).

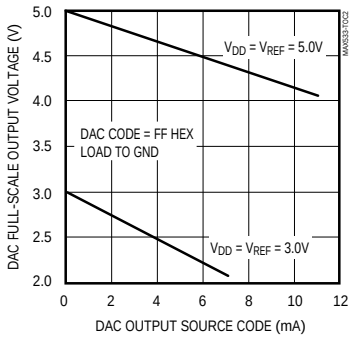
Typical Operating Characteristics

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

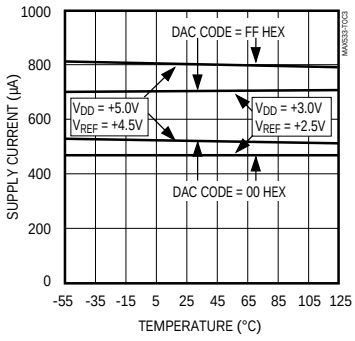
DAC ZERO-CODE OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



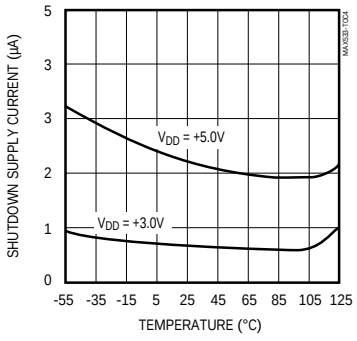
DAC FULL-SCALE OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



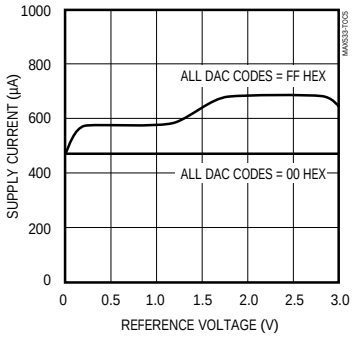
SUPPLY CURRENT vs. TEMPERATURE



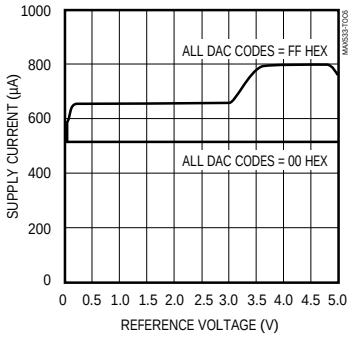
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



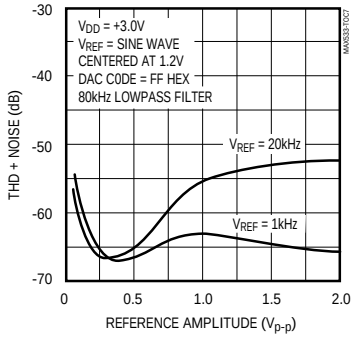
SUPPLY CURRENT vs. REFERENCE VOLTAGE (V_{DD} = +3.0V)



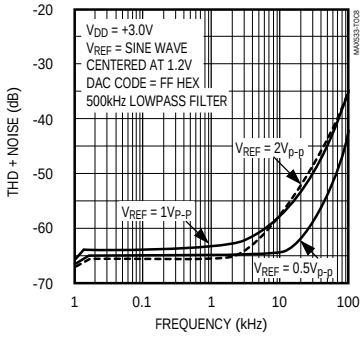
SUPPLY CURRENT vs. REFERENCE VOLTAGE (V_{DD} = +5.0V)



THD + NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY

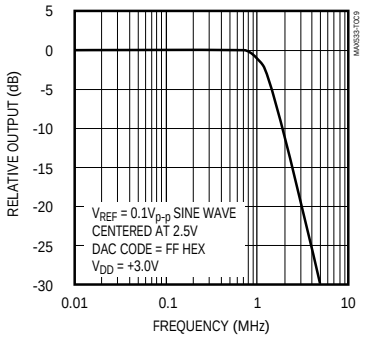


2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

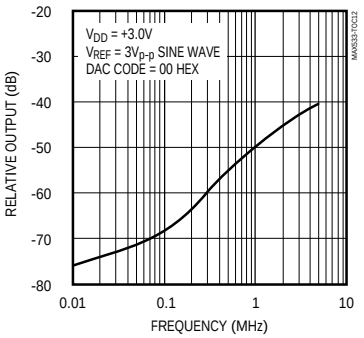
Typical Operating Characteristics (continued)

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

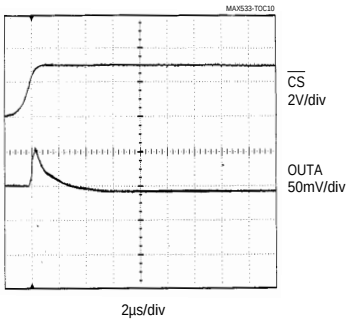
REFERENCE INPUT FREQUENCY RESPONSE



REFERENCE FEEDTHROUGH vs. FREQUENCY



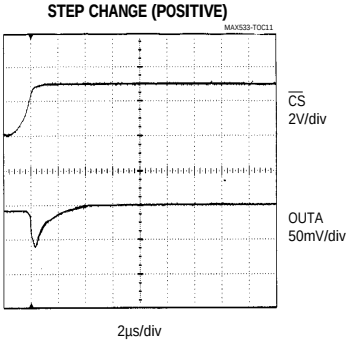
WORST-CASE 1LSB DIGITAL STEP CHANGE (NEGATIVE)



V_{DD} = 3.0V
V_{REF} = 2.5V

DAC CODE = 80 TO 7F hex
NO LOAD

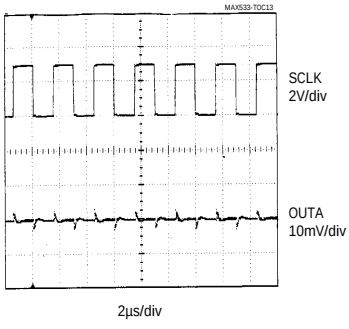
WORST-CASE 1LSB DIGITAL STEP CHANGE (POSITIVE)



V_{DD} = 3.0V
V_{REF} = 2.5V

DAC CODE = 7F TO 80 hex
NO LOAD

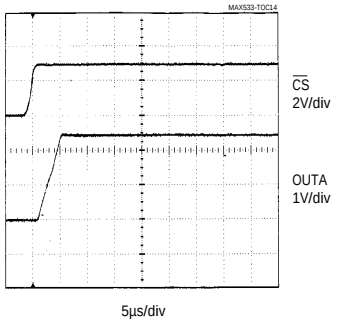
CLOCK FEEDTHROUGH



SCLK = 333kHz
SCLK t_R = t_F = 25ns
V_{DD} = 3.0V

V_{REF} = 2.5V
DAC CODE = 80 hex
NO LOAD

POSITIVE SETTLING TIME



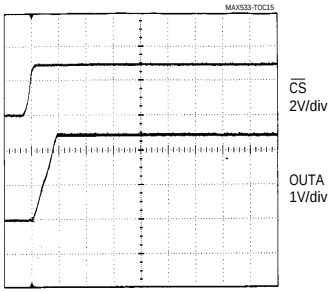
V_{DD} = 3.0V
V_{REF} = 2.5V

DAC CODE = 00 TO FF hex
NO LOAD

Typical Operating Characteristics (continued)

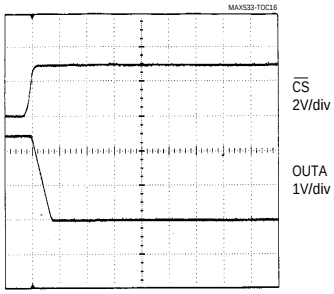
(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

POSITIVE SETTLING TIME



V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = 01 TO FF hex
NO LOAD

NEGATIVE SETTLING TIME



V_{DD} = 3.0V
V_{REF} = 2.5V
DAC CODE = FF TO 00 hex
NO LOAD

Pin Description

PIN	NAME	FUNCTION
1	OUTB	DAC B Voltage Output
2	OUTA	DAC A Voltage Output
3	REF	Reference-Voltage Input
4	UPO	Software-Programmable Logic Output
5	PDE	Power-Down Enable. Must be high to enter software shutdown mode.
6	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low (level sensitive) transfers the contents of each input latch to its respective DAC latch.
7	$\overline{CLR}$	Clear DAC Input (active low). Driving $\overline{CLR}$ low asynchronously clears the input and DAC registers, and sets all DAC outputs to zero.
8	DOUT	Serial Data Output. Sinks and sources current. Data at DOUT can be clocked out on the rising or falling edge of SCLK (Table 1).
9	$\overline{CS}$	Chip-Select Input (active low). Data is shifted in and out when $\overline{CS}$ is low. Programming commands are executed when $\overline{CS}$ returns high.
10	SCLK	Serial Clock Input. Data is clocked in on the rising edge and clocked out on the falling (default) or rising edge (A0 = A1 = 1, see Table 1).
11	DIN	Serial Data Input. Data is clocked in on the rising edge of SCLK.
12	DGND	Digital Ground
13	V_{DD}	Power Supply, +2.7V to +3.6V
14	AGND	Analog Ground
15	OUTD	DAC D Voltage Output
16	OUTC	DAC C Voltage Output

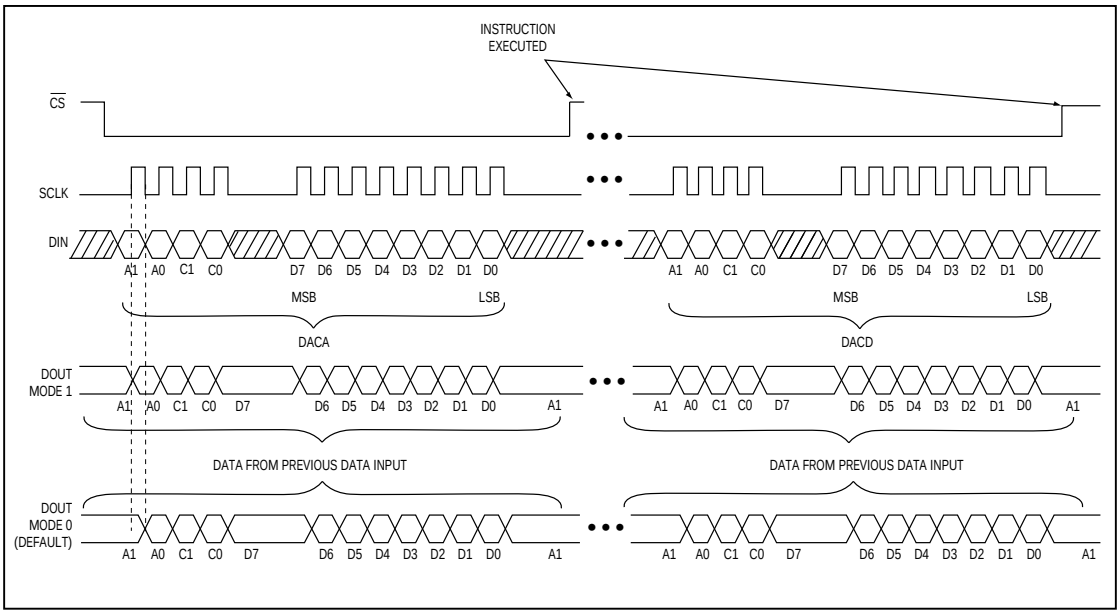


Figure 1. 3-Wire Interface Timing

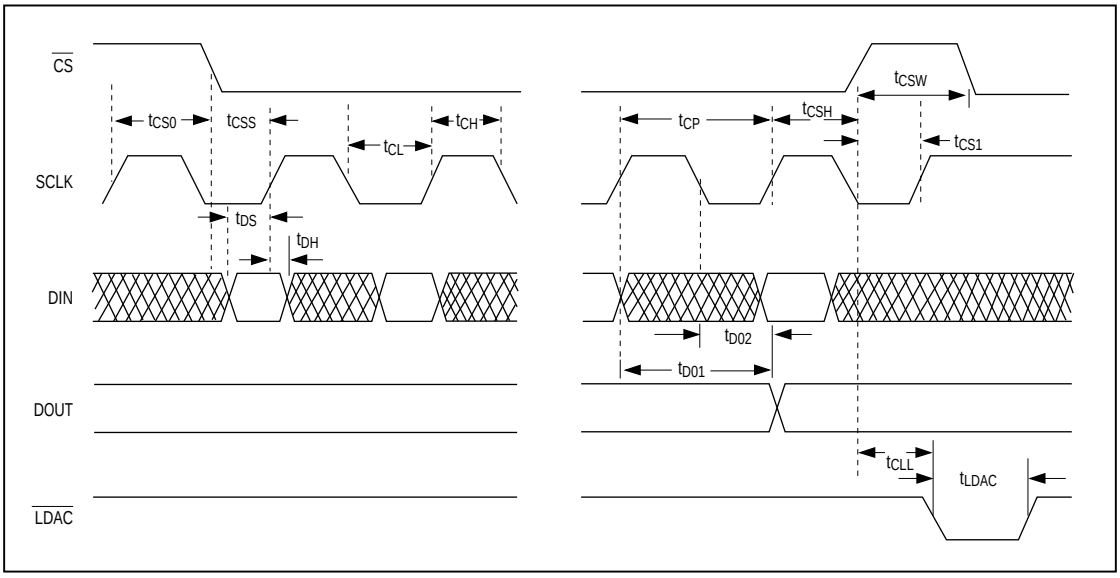


Figure 2. Detailed Serial-Interface Timing Diagram

Detailed Description

Serial Interface

At power-on, the serial interface and all digital-to-analog converters (DACs) are cleared and set to code zero. The serial data output (DOUT) is set to transition on SCLK's falling edge.

The MAX533 communicates with microprocessors through a synchronous, full-duplex, 3-wire interface (Figure 1). Data is sent MSB first and can be transmitted in one 4-bit and one 8-bit (byte) packet or in one 12-bit word. If a 16-bit word is used, the first four bits are ignored. A 4-wire interface adds a line for $\overline{LDAC}$ and allows asynchronous updating. The serial clock (SCLK) synchronizes the data transfer. Data is transmitted and received simultaneously.

Figure 2 shows the detailed serial-interface timing. Please note that the clock should be low if it is stopped between updates. DOUT does not go into a high-impedance state if the clock idles or $\overline{CS}$ is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. Data at DOUT is clocked out 12 clock cycles later, either at SCLK's falling edge (default or mode 0) or rising edge (mode 1).

Chip select ($\overline{CS}$) must be low to enable the DAC. If $\overline{CS}$ is high, the interface is disabled and DOUT remains unchanged. $\overline{CS}$ must go low at least 40ns before the first rising edge of the clock pulse to properly clock in the first bit. With $\overline{CS}$ low, data is clocked into the MAX533's internal shift register on the rising edge of the external serial clock. Always clock in the full 12 bits because each time $\overline{CS}$ goes high the bits currently in the input shift register are interpreted as a command. SCLK can be driven at rates up to 10MHz.

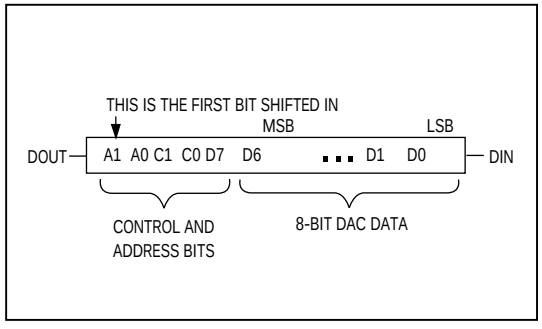


Figure 3. Serial Input Format

Serial Input Data Format and Control Codes

The 12-bit serial input format shown in Figure 3 comprises two DAC address bits (A1, A0), two control bits (C1, C0), and eight bits of data (D7...D0).

The 4-bit address/control code configures the DAC as shown in Table 1.

Load Input Register, DAC Registers Unchanged (Single Update Operation)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		0	1	8-Bit Data							

($\overline{LDAC}$ = H)

When performing a single update operation, A1 and A0 select the respective input register. At the rising edge of $\overline{CS}$, the selected input register is loaded with the current shift-register data. All DAC outputs remain unchanged. This preloads individual data in the input register without changing the DAC outputs.

Load Input and DAC Registers

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		1	1	8-Bit Data							

($\overline{LDAC}$ = H)

This command directly loads the selected DAC register at $\overline{CS}$'s rising edge. A1 and A0 set the DAC address. Current shift-register data is placed in the selected input and DAC registers.

For example, to load all four DAC registers simultaneously with individual settings (DAC A = 0.5V, DAC B = 1V, DAC C = 1.5V, and DAC D = 2V), four commands are required. First, perform three single input register update operations for DACs A, B, and C (C1 = 0). The final command loads input register D and updates all four DAC registers from their respective input registers.

Software "$\overline{LDAC}$" Command

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = 1)

All DAC registers are updated with the contents of their respective input registers at $\overline{CS}$'s rising edge. With the exception of using $\overline{CS}$ to execute, this performs the same function as the asynchronous $\overline{LDAC}$.

12-BIT SERIAL WORD					LDAC	FUNCTION
A1	A0	C1	C0	D7 . . . . . D0		
0	0	0	1	8-bit DAC data	1	Load input register A; all DAC outputs unchanged.
0	1	0	1	8-bit DAC data	1	Load input register B; all DAC outputs unchanged.
1	0	0	1	8-bit DAC data	1	Load input register C; all DAC outputs unchanged.
1	1	0	1	8-bit DAC data	1	Load input register D; all DAC outputs unchanged.
0	0	1	1	8-bit DAC data	1	Load input register A; all DAC outputs updated
0	1	1	1	8-bit DAC data	1	Load input register B; all DAC outputs updated
1	0	1	1	8-bit DAC data	1	Load input register C; all DAC outputs updated
1	1	1	1	8-bit DAC data	1	Load input register D; all DAC outputs updated.
0	1	0	0	X X X X X X X X	1	Software $\overline{LDAC}$ commands. Update all DACs from their respective input registers. Also bring the part out of shutdown mode.
1	0	0	0	8-bit DAC data	X	Load all DACs with shift-register data. Also bring the part out of shutdown mode.
1	1	0	0	X X X X X X X X	X	Software shutdown (provided PDE is high)
0	0	1	0	X X X X X X X X	X	UPO goes low.
0	1	1	0	X X X X X X X X	X	UPO goes high.
0	0	0	0	X X X X X X X X	X	No operation (NOP); shift data in shift registers.
1	1	1	0	X X X X X X X X	X	Set DOUT phase—SCLK rising (mode 1). DOUT clocked out on rising edge of SCLK. All DACs updated from their respective input registers.
1	0	1	0	X X X X X X X X	X	Set DOUT phase—SCLK falling (mode 0). DOUT clocked out on falling edge of SCLK. All DACs updated from their respective registers (default).

Load All DACs with Shift-Register Data

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	8-Bit Data							

($\overline{LDAC}$ = X)

All four DAC registers are updated with shift-register data. This command allows all DACs to be set to any analog value within the reference range. This command can be used to substitute $\overline{CLR}$ if code 00 hex is programmed, which clears all DACs.

Software Shutdown

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = X, PDE = H)

Shuts down all output buffer amplifiers, reducing supply current to 10µA max.

User-Programmable Output (UPO)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	UPO Output
0	0	1	0	x	x	x	x	x	x	x	x	Low
0	1	1	0	x	x	x	x	x	x	x	x	High

($\overline{LDAC}$ = X)

User-programmable logic output for controlling another device across an isolated interface. Example devices are gain control of an amplifier, a 4mA to 20mA amplifier, and a polarity output for a motor speed control.

No Operation (NOP)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = X)

The NOP command (no operation) allows data to be shifted through the MAX533 shift register without affecting the input or DAC registers. This is useful in daisy chaining (also see the *Daisy Chaining Devices* section).

For this command, the data bits are “Don't Cares.” As an example, three MAX533s are daisy chained (A, B, and C), and devices A and C need to be updated. The 36-bit-wide command would consist of one 12-bit word for device C, followed by an NOP instruction for device B and a third 12-bit word with data for device A. At $\overline{CS}$'s rising edge, device B will not change state.

Set DOUT Phase—SCLK Rising (Mode 1)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

Mode 1 resets the serial-output DOUT to transition at SCLK's rising edge. Once this command is issued, DOUT's phase is latched and will not change except on power-up or if the specific command to set the phase to falling edge is issued.

This command also loads all DAC registers with the contents of their respective input registers, and is identical to the “$\overline{LDAC}$” command.

Set DOUT Phase—SCLK Falling (Mode 0, Default)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	x	x	x	x	x	x	x	x

($\overline{LDAC}$ = x)

This command resets DOUT to transition at SCLK's falling edge. The same command also updates all DAC registers with the contents of their respective input registers, identical to the “$\overline{LDAC}$” command.

$\overline{LDAC}$ Operation (Hardware)

$\overline{LDAC}$ is typically used in 4-wire interfaces (Figure 7). This command is level sensitive, and it allows asynchronous hardware control of the DAC outputs. With $\overline{LDAC}$ low, the DAC registers are transparent, and any time an input register is updated, the DAC output immediately follows.

Clear DACs with $\overline{CLR}$

Strobing the $\overline{CLR}$ pin low causes an asynchronous clear of input and DAC registers and sets all DAC outputs to zero. Similar to the $\overline{LDAC}$ pin, $\overline{CLR}$ can be invoked at any time, typically when the device is not selected ($\overline{CS}$ = H). When the DAC data is all zeros, this function is equivalent to the “Update all DACs from Shift Registers” command.

Serial Data Output

DOUT is the internal shift register's output. DOUT can be programmed to clock out data on SCLK's falling edge (mode 0) or rising edge (mode 1). In mode 0, output data lags input data by 12.5 clock cycles, maintaining compatibility with Microwire and SPI. In mode 1, output data lags input data by 12 clock cycles. On power-up, DOUT defaults to mode 0 timing. DOUT never three-states; it always actively drives either high or low and remains unchanged when $\overline{CS}$ is high.

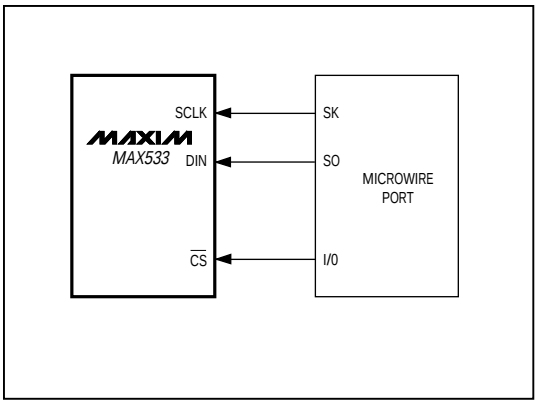


Figure 4. Connections for Microwire

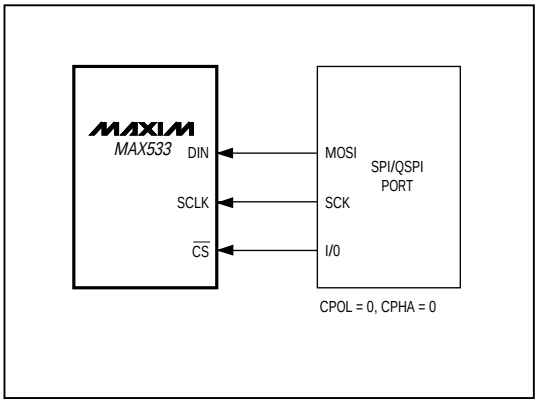


Figure 5. Connections for SPI/QSPI

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Interfacing to the Microprocessor

The MAX533 is Microwire™ and SPI™/QSPI™ compatible. For SPI and QSPI, clear the CPOL and CPHA configuration bits (CPOL = CPHA = 0). The SPI/QSPI CPOL = CPHA = 1 configuration can also be used if the DOUT output is ignored.

The MAX533 can interface with Intel's 80C5X/80C3X family in mode 0 if the SCLK clock polarity is inverted. More universally, if a serial port is not available, three lines from one of the parallel ports can be used for bit manipulation.

Digital feedthrough at the voltage outputs is greatly minimized by operating the serial clock only to update the registers. Also see the Clock Feedthrough photo in the *Typical Operating Characteristics* section. The clock idle state is low.

Daisy-Chaining Devices

Any number of MAX533s can be daisy-chained by connecting DOUT of one device to DIN of the following device in the chain. The NOP instruction (Table 1) allows data to be passed from DIN to DOUT without changing the input or DAC registers of the passing device. A 3-wire interface updates daisy-chained or individual MAX533s simultaneously by bringing $\overline{CS}$ high (Figure 6).

Analog Section

DAC Operation

The MAX533 uses a matrix decoding architecture for the DACs, which saves power in the overall system. The external reference voltage is divided down by a resistor string placed in a matrix fashion. Row and column decoders select the appropriate tab from the resistor string to provide the needed analog voltages. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output. Figure 8 shows a simplified diagram of the four DACs.

Reference Input

The voltage at REF sets the full-scale output voltage for all four DACs. The 460kΩ typical input impedance at REF is code independent. The output voltage for any DAC can be represented by a digitally programmable voltage source as follows:

$$V_{OUT} = (NB \times V_{REF}) / 256$$

where NB is the numerical value of the DAC's binary input code.

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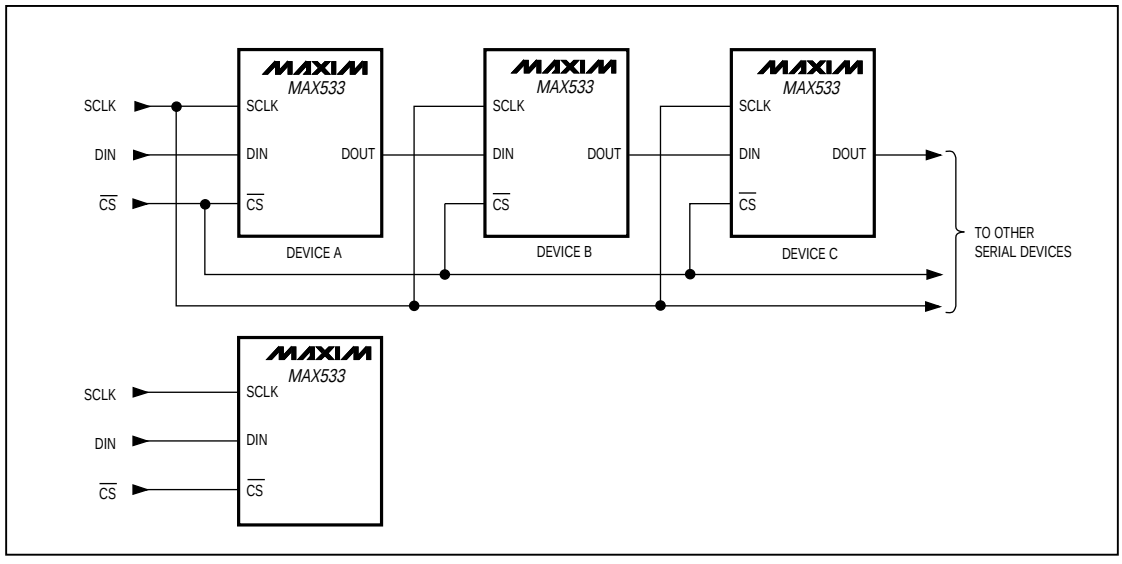


Figure 6. Daisy-chained or individual MAX533s are simultaneously updated by bringing $\overline{CS}$ high. Only three wires are required.

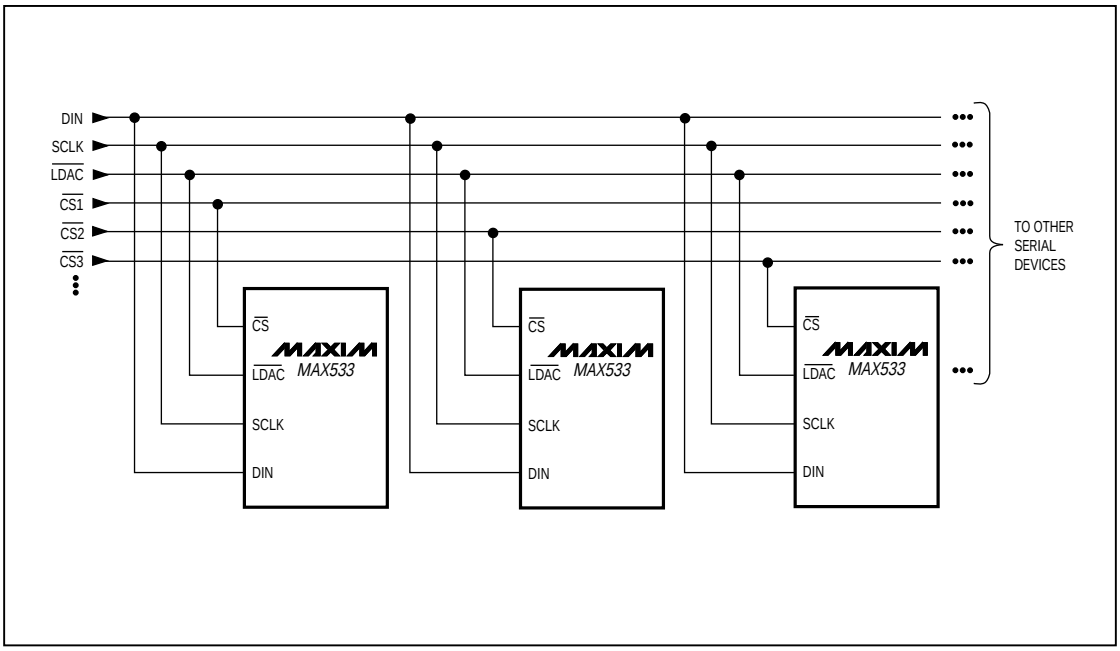


Figure 7. Multiple MAX533s sharing one DIN line. Simultaneously update by strobing LDAC, or specifically update by enabling an individual CS.

Output Buffer Amplifiers

All MAX533 voltage outputs are internally buffered by precision unity-gain followers that slew at about 0.6V/µs. The outputs can swing from GND to V_{DD}. With a 0V to +2.5V (or +2.5V to 0V) output transition, the amplifier outputs will typically settle to 1/2LSB in 6µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive (≥10kΩ) or capacitive loads.

Applications Information

DAC Linearity and Voltage Offset

The output buffer can have a negative input offset voltage that would normally drive the output negative, but since there is no negative supply the output stays at 0V (Figure 9). When linearity is determined using the endpoint method, it is measured between zero code (all inputs 0) and full-scale code (all inputs 1) after offset and gain error are calibrated out. However, in single-supply operation the next code after zero may not change the output (Figure 9), so the lowest code that produces a positive output is the lower endpoint.

2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

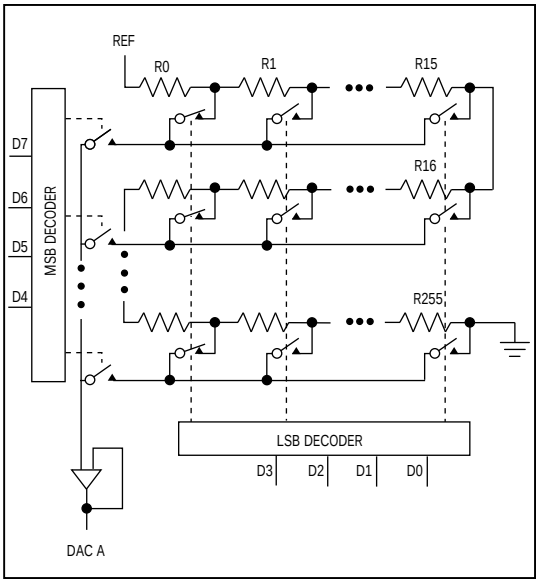


Figure 8. DAC Simplified Circuit Diagram

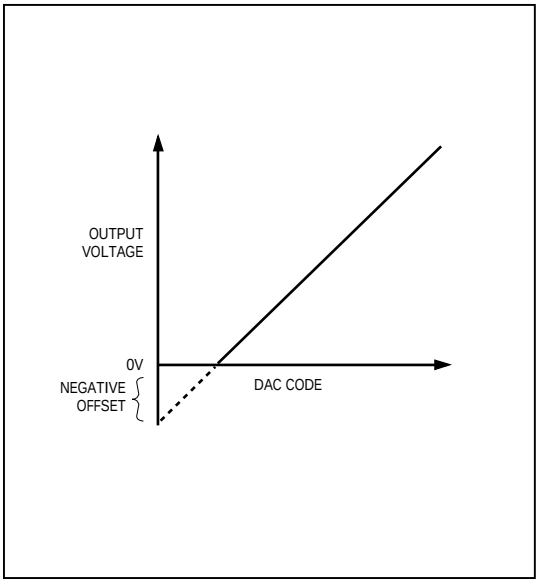


Figure 9. Effect of Negative Offset (Single Supply)

Power Sequencing

The voltage applied to REF should not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REF and V_{DD} to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

Connect AGND and DGND together at the IC. This ground should then return to the highest-quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and DGND as possible.

Careful PC board layout minimizes crosstalk among DAC outputs and digital inputs. Figure 10 shows suggested circuit board layout to minimize crosstalk.

Unipolar-Output, Two-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input are the same polarity. Figure 11 shows the MAX533 unipolar configuration, and Table 2 shows the unipolar code.

Table 2. Unipolar Code Table

DAC CONTENTS		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

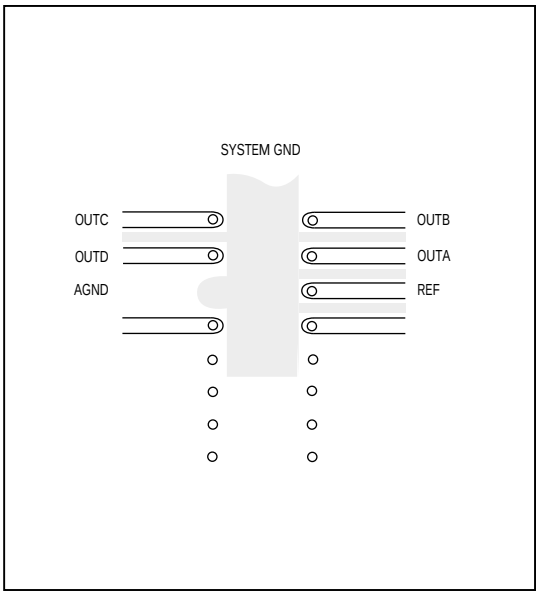


Figure 10. Suggested PC Board Layout for Minimizing Crosstalk (Bottom View)

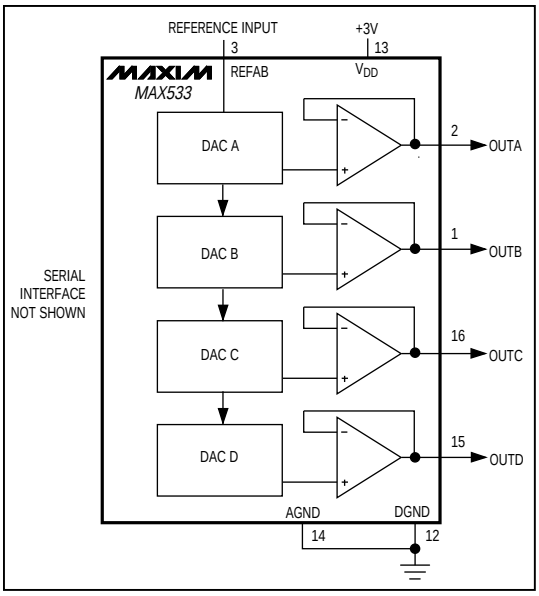
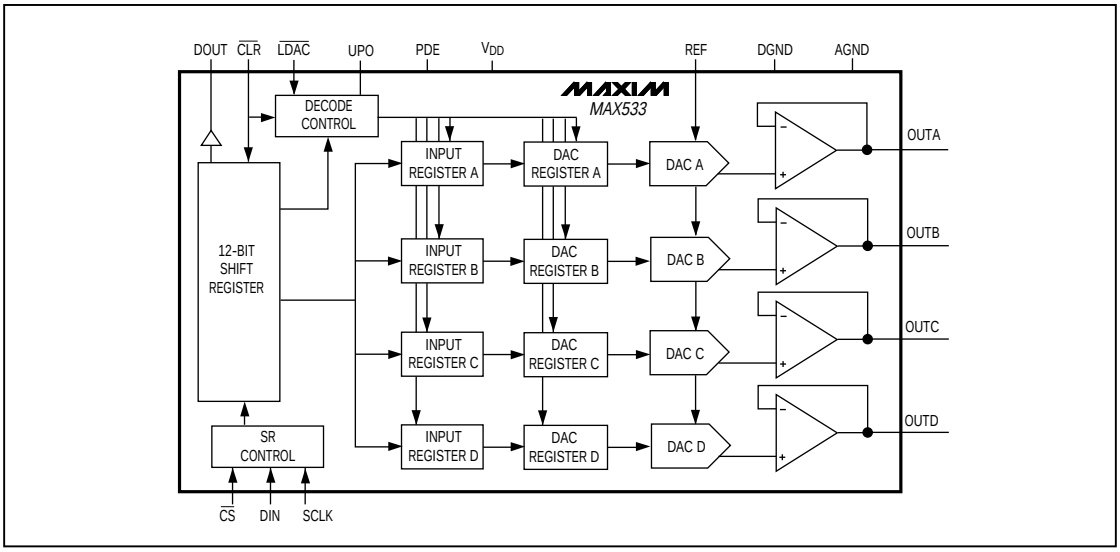


Figure 11. Unipolar Output Circuit

Functional Diagram

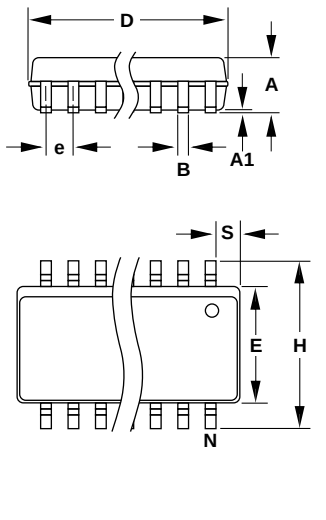


2.7V, Low-Power, 8-Bit Quad DAC with Rail-to-Rail Output Buffers

Chip Information

TRANSISTOR COUNT: 6821

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.127	0.25
A2	0.055	0.061	1.40	1.55
B	0.008	0.012	0.20	0.31
C	0.0075	0.0098	0.19	0.25
D	SEE VARIATIONS			
E	0.150	0.157	3.81	3.99
e	0.25 BSC		0.635 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.189	0.196	4.80	4.98
S	16	0.0020	0.0070	0.05	0.18
D	20	0.337	0.344	8.56	8.74
S	20	0.0500	0.0550	1.27	1.40
D	24	0.337	0.344	8.56	8.74
S	24	0.0250	0.0300	0.64	0.76
D	28	0.386	0.393	9.80	9.98
S	28	0.0250	0.0300	0.64	0.76

21-0055A

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