



+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

MAX531/MAX538/MAX539

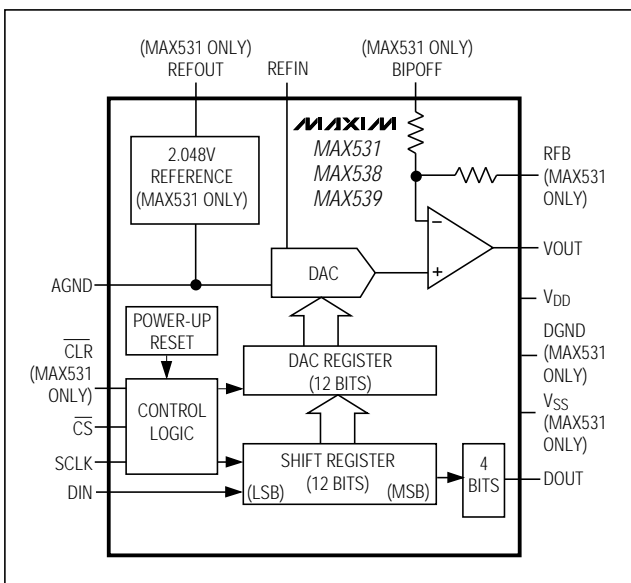
General Description

The MAX531/MAX538/MAX539 are low-power, voltage-output, 12-bit digital-to-analog converters (DACs) specified for single +5V power-supply operation. The MAX531 can also be operated with $\pm 5V$ supplies. The MAX538/MAX539 draw only 140 μA , and the MAX531 (with internal reference) draws only 260 μA . The MAX538/MAX539 come in 8-pin DIP and SO packages, while the MAX531 comes in 14-pin DIP and SO packages. All parts have been trimmed for offset voltage, gain, and linearity, so no further adjustment is necessary. The MAX538's buffer is fixed at a gain of +1 and the MAX539's buffer at a gain of +2. The MAX531's internal op amp may be configured for a gain of +1 or +2, as well as for unipolar or bipolar output voltages. The MAX531 can also be used as a four-quadrant multiplier without external resistors or op amps. For parallel data inputs, see the MAX530 data sheet.

Applications

- Battery-Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery-Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

Functional Diagram



Features

- ◆ Operate from Single +5V Supply
- ◆ Buffered Voltage Output
- ◆ Internal 2.048V Reference (MAX531)
- ◆ 140 μA Supply Current (MAX538/MAX539)
- ◆ INL = $\pm 1/2$ LSB (max)
- ◆ Guaranteed Monotonic over Temperature
- ◆ Flexible Output Ranges:
 - 0V to V_{DD} (MAX531/MAX539)
 - V_{SS} to V_{DD} (MAX531)
 - 0V to 2.6V (MAX531/MAX538)
- ◆ 8-Pin SO/DIP (MAX538/MAX539)
- ◆ Power-On Reset
- ◆ Serial Data Output for Daisy-Chaining

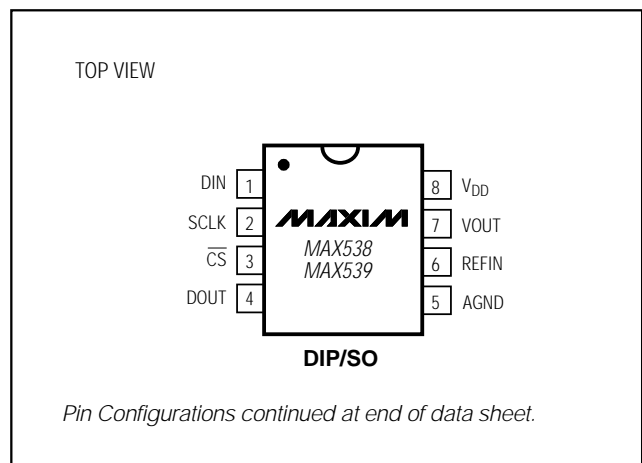
Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | ERROR (LSB) |
|------------|--------------|----------------|-------------|
| MAX531ACPD | 0°C to +70°C | 14 Plastic DIP | $\pm 1/2$ |
| MAX531BCPD | 0°C to +70°C | 14 Plastic DIP | ± 1 |
| MAX531ACSD | 0°C to +70°C | 14 SO | $\pm 1/2$ |
| MAX531BCSD | 0°C to +70°C | 14 SO | ± 1 |
| MAX531BC/D | 0°C to +70°C | Dice* | ± 1 |

Ordering Information continued at end of data sheet.

*Dice are specified at $T_A = +25^\circ C$ only.

Pin Configurations



Pin Configurations continued at end of data sheet.



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ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| V _{DD} to DGND and V _{DD} to AGND | -0.3V, +6V |
| V _{SS} to DGND and V _{SS} to AGND | -6V, +0.3V |
| V _{DD} to V _{SS} | -0.3V, +12V |
| AGND to DGND | -0.3V, +0.3V |
| Digital Input Voltage to DGND | -0.3V, (V _{DD} + 0.3V) |
| REFIN | (V _{SS} - 0.3V), (V _{DD} + 0.3V) |
| REFOUT to AGND | -0.3V, (V _{DD} + 0.3V) |
| RFB | (V _{SS} - 0.3V), (V _{DD} + 0.3V) |
| BIPOFF | (V _{SS} - 0.3V), (V _{DD} + 0.3V) |
| V _{OUT} (Note 1) | V _{SS} , V _{DD} |
| Continuous Current, Any Pin | -20mA, +20mA |

| | |
|---|-----------------|
| Continuous Power Dissipation (T _A = +70°C) | |
| 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) | 727mW |
| 8-Pin SO (derate 5.88mW/°C above +70°C) | 471mW |
| 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) | 800mW |
| 14-Pin SO (derate 8.33mW/°C above +70°C) | 667mW |
| Operating Temperature Ranges | |
| MAX53_C_ | 0°C to +70°C |
| MAX53_E_ | -40°C to +85°C |
| Storage Temperature Range | -65°C to +165°C |
| Lead Temperature (soldering, 10sec) | +300°C |

Note 1: The output may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation limit is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = +5V ±10%, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = V_{OUT} (MAX531), C_{REFOUT} = 33μF (MAX531), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|---|-----|-----|-----------------------|--------|
| STATIC PERFORMANCE | | | | | | |
| Resolution | N | | 12 | | | Bits |
| Relative Accuracy (Note 2) | INL | MAX53_AC/E | | | ±0.5 | LSB |
| | | MAX53_BC/E | | | ±1 | |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | ±1 | LSB |
| Unipolar Offset Error | V _{OS} | MAX53_C/E | 0 | | 8 | LSB |
| Unipolar Offset Tempco | TCV _{OS} | | | 3 | | ppm/°C |
| Gain Error (Note 2) | GE | MAX53_C/E | | | ±1 | LSB |
| Gain-Error Tempco | | | | 1 | | ppm/°C |
| Power-Supply Rejection Ratio (Note 3) | PSRR | 4.5V ≤ V _{DD} ≤ 5.5V | | 0.4 | 1 | LSB/V |
| VOLTAGE OUTPUT (V_{OUT}) | | | | | | |
| Output Voltage Range | | MAX531 (G = +1), MAX538 | 0 | | V _{DD} - 2 | V |
| | | MAX531 (G = +2), MAX539 | 0 | | V _{DD} - 0.4 | |
| Output Load Regulation | | V _{OUT} = 2V, R _L = 2kΩ | | | 1 | LSB |
| Short-Circuit Current | I _{SC} | | | 12 | | mA |
| REFERENCE INPUT (REFIN) | | | | | | |
| Voltage Range | | | 0 | | V _{DD} - 2 | V |
| Input Resistance | | Code dependent, minimum at code 555 hex | 40 | | | kΩ |
| Input Capacitance | | Code dependent (Note 4) | 10 | | 50 | pF |
| AC Feedthrough | | REFIN = 1kHz, 2Vp-p | | -80 | | dB |

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MAX531/MAX538/MAX539

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

($V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$, $AGND = DGND = 0V$, $REFIN = 2.048V$ (external), $RFB = BIPOFF = V_{OUT}$ (MAX531), $C_{REFOUT} = 33\mu F$ (MAX531), $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|---------------|---|---------------------|-------|---------|-----------------|---|
| REFERENCE OUTPUT (REFOUT—MAX531 only) | | | | | | | |
| Reference Output Voltage | | $V_{DD} = 5.0V$ | $T_A = +25^\circ C$ | 2.024 | 2.048 | 2.072 | V |
| | | | MAX531BC | 2.017 | | 2.079 | |
| | | | MAX531BE | 2.013 | | 2.083 | |
| Temperature Coefficient | $T_{CREFOUT}$ | MAX531AC/AE/AM/BM | | 30 | 50 | ppm/ $^\circ C$ | |
| | | MAX531BC/BE | | 30 | | | |
| Resistance | R_{REFOUT} | (Note 5) | | 0.5 | 2 | Ω | |
| Power-Supply Rejection Ratio | PSRR | $4.5V \leq V_{DD} \leq 5.5V$ | | | 300 | $\mu V/V$ | |
| Noise Voltage | e_n | 0.1Hz to 10kHz | | 400 | | μV_{p-p} | |
| Minimum Required External Capacitor | C_{MIN} | | 3.3 | | | μF | |
| DIGITAL INPUTS (DIN, SCLK, \overline{CS}, CLR) | | | | | | | |
| Input High | V_{IH} | | 2.4 | | | V | |
| Input Low | V_{IL} | | | | 0.8 | V | |
| Input Current | I_{IN} | $V_{IN} = 0V$ or V_{DD} | | | ± 1 | μA | |
| Input Capacitance | C_{IN} | | | 8 | | pF | |
| DIGITAL OUTPUT (DOUT) | | | | | | | |
| Output High | V_{OH} | $I_{SOURCE} = 2mA$ | $V_{DD} - 1$ | | | V | |
| Output Low | V_{OL} | $I_{SINK} = 2mA$ | | | 0.4 | V | |
| DYNAMIC PERFORMANCE | | | | | | | |
| Voltage-Output Slew Rate | SR | $T_A = +25^\circ C$ | 0.15 | 0.25 | | V/ μs | |
| Voltage-Output Settling Time | | $T_o \pm 1/2LSB$, $V_{OUT} = 2V$ | | 25 | | μs | |
| Digital Feedthrough | | $\overline{CS} = V_{DD}$, $DIN = 100kHz$ | | 5 | | nV-s | |
| Signal-to-Noise plus Distortion | SINAD | $REFIN = 1kHz$, $2V_{p-p}$ ($G = +1$ or $+2$), code = FFF hex | | 68 | | dB | |
| POWER SUPPLY | | | | | | | |
| Positive Supply Voltage | V_{DD} | | 4.5 | | 5.5 | V | |
| Power-Supply Current | I_{DD} | All inputs = 0V or V_{DD} , output = no load | MAX531 | 260 | 400 | μA | |
| | | | MAX538, MAX539 | 140 | 300 | | |
| SWITCHING CHARACTERISTICS | | | | | | | |
| \overline{CS} Setup Time | t_{CSS} | | 20 | | | ns | |
| SCLK Fall to \overline{CS} Fall Hold Time | t_{CSH0} | | 15 | | | ns | |
| SCLK Fall to \overline{CS} Rise Hold Time | t_{CSH1} | | 0 | | | ns | |
| SCLK High Width | t_{CH} | | 35 | | | ns | |
| SCLK Low Width | t_{CL} | | 35 | | | ns | |
| DIN Setup Time | t_{DS} | | 45 | | | ns | |
| DIN Hold Time | t_{DH} | | 0 | | | ns | |
| DOUT Valid Propagation Delay | t_{DO} | $C_L = 50pF$ | | | 80 | ns | |
| \overline{CS} High Pulse Width | t_{CSW} | | 20 | | | ns | |
| CLR Pulse Width | t_{CLR} | | 25 | | | ns | |
| \overline{CS} Rise to SCLK Rise Setup Time | t_{CS1} | | 50 | | | ns | |

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MAX531/MAX538/MAX539

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only)

($V_{DD} = +5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $AGND = DGND = 0V$, $REFIN = 2.048V$ (external), $RFB = BIPOFF = VOUT$, $C_{REFOUT} = 33\mu F$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|---------------|---|----------------------|-------|--------------|------------------|---|
| Resolution | N | | 12 | | | Bits | |
| Relative Accuracy | INL | Tested at $V_{DD} = 5V$, $V_{SS} = -5V$ | | | ± 0.5 | LSB | |
| | | | MAX531AC/E | | ± 1 | | |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | ± 1 | LSB | |
| Bipolar Offset Error | V_{OS} | BIPOFF = REFIN, MAX531_C/E | | | ± 8 | LSB | |
| Bipolar Offset Tempco | TCV_{OS} | BIPOFF = REFIN | | 3 | | ppm/ $^{\circ}C$ | |
| Gain Error (Unipolar or Bipolar) | GEU | MAX531_C/E | | | ± 1 | LSB | |
| Gain-Error Tempco | | | | 1 | | ppm/ $^{\circ}C$ | |
| Power-Supply Rejection Ratio (Note 3) | PSRR | $4.5V \leq V_{DD} \leq 5.5V$, $-5.5V \leq V_{SS} \leq -4.5V$ | | 0.4 | 1 | LSB/V | |
| REFERENCE INPUT (REFIN) | | | | | | | |
| Voltage Range | | | $V_{SS} + 2$ | | $V_{DD} - 2$ | V | |
| Input Resistance | | Code dependent, minimum at code 555 hex | 40 | | | k Ω | |
| Input Capacitance | | Code dependent (Note 4) | 10 | | 50 | pF | |
| AC Feedthrough | | REFIN = 1kHz, 2.0Vp-p | | -80 | | dB | |
| REFERENCE OUTPUT (REFOUT—MAX531 only) | | | | | | | |
| Reference Output Voltage | | $V_{DD} = 5.0V$ | $T_A = +25^{\circ}C$ | 2.024 | 2.048 | 2.072 | V |
| | | | MAX531BC | 2.017 | | 2.079 | |
| | | | MAX531BE | 2.013 | | 2.083 | |
| Temperature Coefficient | TC_{REFOUT} | MAX531AC/AE/AM/BM | | 30 | 50 | ppm/ $^{\circ}C$ | |
| | | MAX531BC/BE | | 30 | | | |
| Resistance | R_{REFOUT} | (Note 5) | | 0.5 | 2 | Ω | |
| Power-Supply Rejection Ratio | PSRR | $4.5V \leq V_{DD} \leq 5.5V$ | | | 300 | $\mu V/V$ | |
| Noise Voltage | e_n | 0.1Hz to 10kHz | | 400 | | $\mu Vp-p$ | |
| Minimum Required External Capacitor | C_{MIN} | | 3.3 | | | μF | |
| DIGITAL INPUTS (DIN, SCLK, \overline{CS}) | | | | | | | |
| Input High | V_{IH} | | 2.4 | | | V | |
| Input Low | V_{IL} | | | | 0.8 | V | |
| Input Current | I_{IN} | $V_{IN} = 0V$ or V_{DD} | | | ± 1 | μA | |
| Input Capacitance | C_{IN} | | | 8 | | pF | |
| DIGITAL OUTPUT (DOUT) | | | | | | | |
| Output High | V_{OH} | $I_{SOURCE} = 2mA$ | $V_{DD} - 1$ | | | V | |
| Output Low | V_{OL} | $I_{SINK} = 2mA$ | | | 0.4 | V | |

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MAX531/MAX538/MAX539

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only) (continued)

($V_{DD} = +5V \pm 10\%$, $V_{SS} = -5V \pm 10\%$, $AGND = DGND = 0V$, $REFIN = 2.048V$ (external), $RFB = BIPOFF = VOUT$, $C_{REFOUT} = 33\mu F$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|---------------------------------------|----------------|----------------|------|------------|
| VOLTAGE OUTPUT (VOUT) | | | | | | |
| Output Voltage Range | | MAX531 (G = +1) | $V_{SS} + 2$ | $V_{DD} - 2$ | | V |
| | | MAX531 (G = +2) | $V_{SS} + 0.4$ | $V_{DD} - 0.4$ | | |
| Output Load Regulation | | $VOUT = 2V$, $R_L = 2k\Omega$ | | | 1 | LSB |
| Short-Circuit Current | I_{SC} | | | 12 | | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Voltage-Output Slew Rate | SR | | 0.15 | 0.25 | | V/ μs |
| Voltage-Output Settling Time | | To $\pm 1/2$ LSB, $VOUT = 2V$ | | 25 | | μs |
| Digital Feedthrough | | Step 000 hex to FFF hex | | 5 | | nV-s |
| Signal-to-Noise plus Distortion | SINAD | REFIN = 1kHz, 2Vp-p, (G = +1) | | 68 | | dB |
| | | REFIN = 1kHz, 2Vp-p, (G = +2) | | 68 | | |
| POWER SUPPLY | | | | | | |
| Positive Supply Voltage | V_{DD} | | 4.5 | | 5.5 | V |
| Negative Supply Voltage | V_{SS} | | -5.5 | | 0 | V |
| Positive Supply Current | I_{DD} | All inputs = 0V or V_{DD} , no load | | 260 | 400 | μA |
| Negative Supply Current | I_{SS} | All inputs = 0V or V_{DD} , no load | | -120 | -200 | μA |
| SWITCHING CHARACTERISTICS | | | | | | |
| \overline{CS} Setup Time | t_{CSS} | | 20 | | | ns |
| SCLK Fall to \overline{CS} Fall Hold Time | t_{CSH0} | | 15 | | | ns |
| SCLK Fall to \overline{CS} Rise Hold Time | t_{CSH1} | | 0 | | | ns |
| SCLK High Width | t_{CH} | | 35 | | | ns |
| SCLK Low Width | t_{CL} | | 35 | | | ns |
| DIN Setup Time | t_{DS} | | 45 | | | ns |
| DIN Hold Time | t_{DH} | | 0 | | | ns |
| DOUT Valid Propagation Delay | t_{DO} | $C_L = 50pF$ | | | 80 | ns |
| \overline{CS} High Pulse Width | t_{CSW} | | 20 | | | ns |
| \overline{CLR} Pulse Width | t_{CLR} | | 25 | | | ns |
| \overline{CS} Rise to SCLK Rise Setup Time | t_{CS1} | | 50 | | | ns |

Note 2: In single-supply operation, INL and GE calculated from code 11 to code 4095. Tested at $V_{DD} = +5V$.

Note 3: This specification applies to both gain-error power-supply rejection ratio and offset-error power-supply rejection ratio.

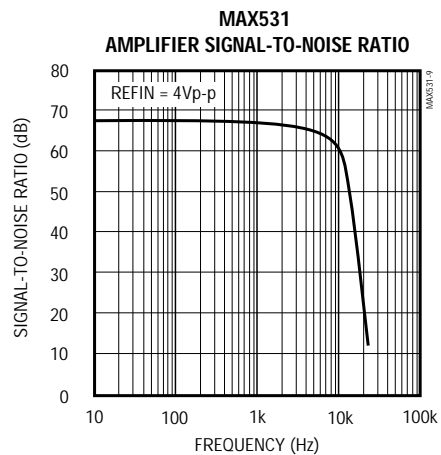
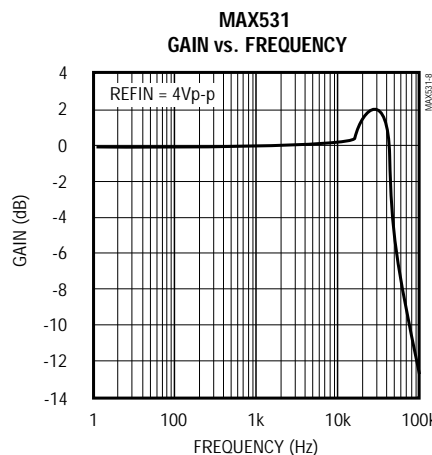
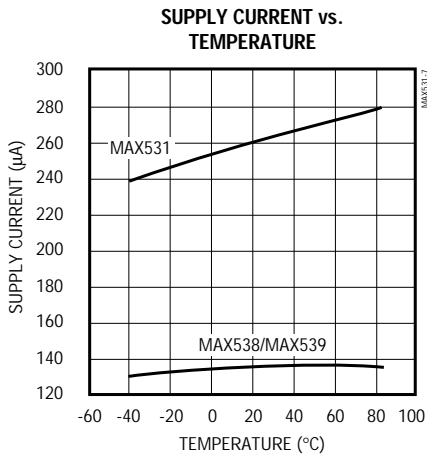
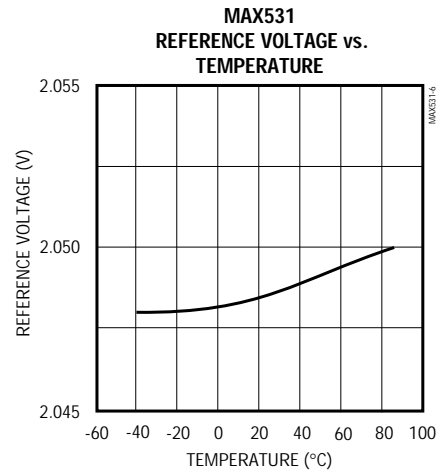
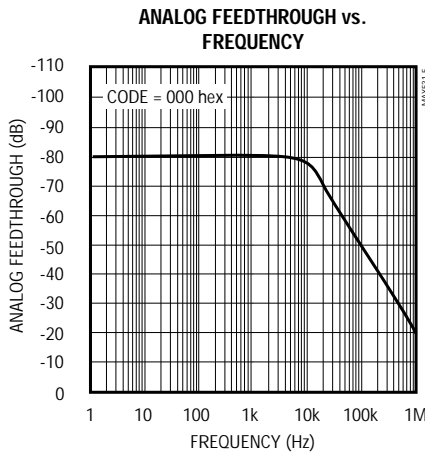
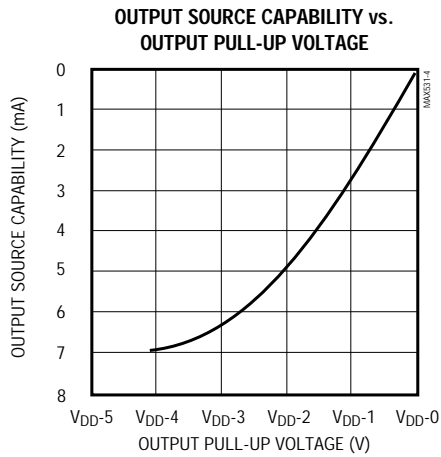
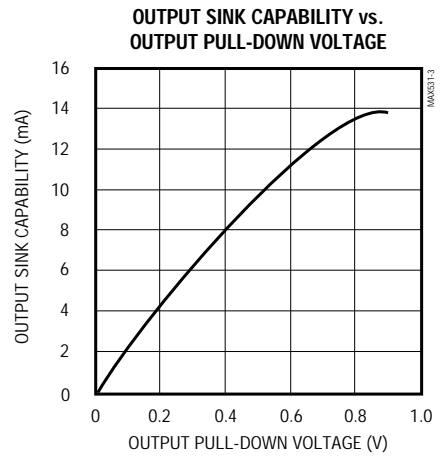
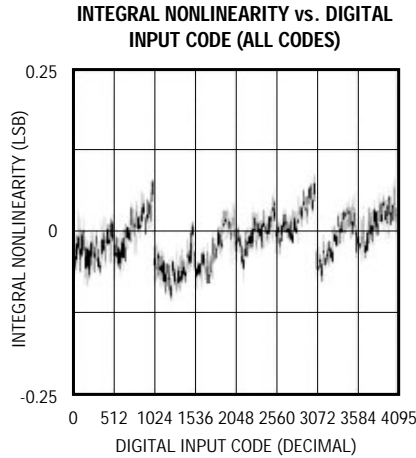
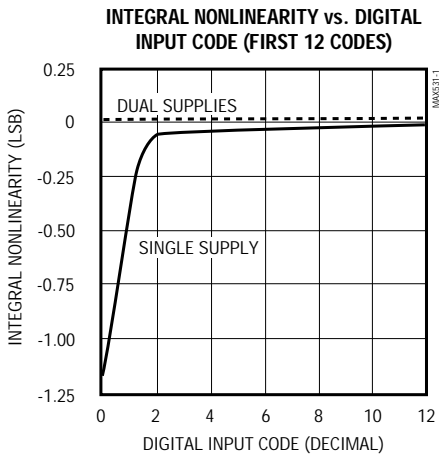
Note 4: Guaranteed by design.

Note 5: Tested at $I_{OUT} = 100\mu A$. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

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Typical Operating Characteristics

($V_{DD} = +5V$, $V_{REFIN} = 2.048V$, $T_A = +25^\circ C$, unless otherwise noted.)

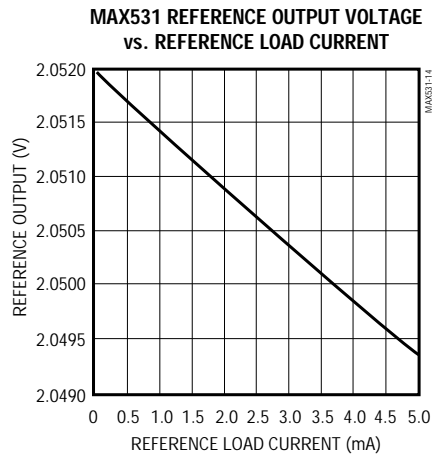
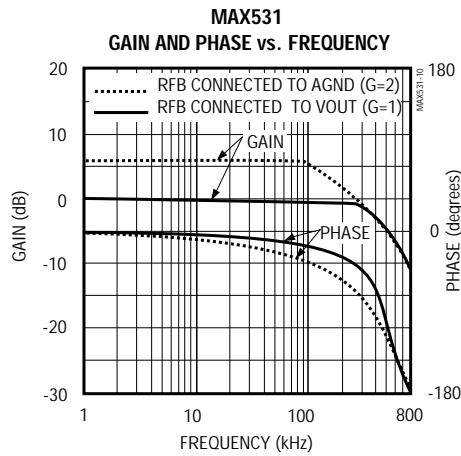


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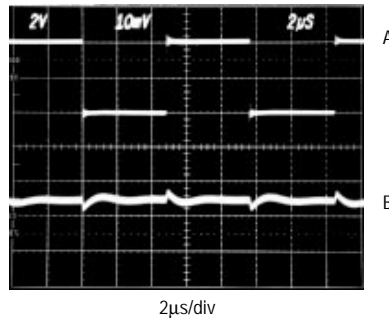
MAX531/MAX538/MAX539

Typical Operating Characteristics (continued)

($V_{DD} = +5V$, $V_{REFIN} = 2.048V$, $T_A = +25^\circ C$, unless otherwise noted.)

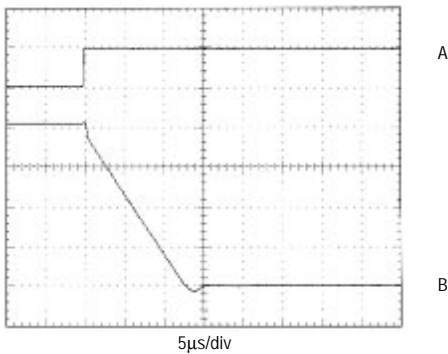


DIGITAL FEEDTHROUGH



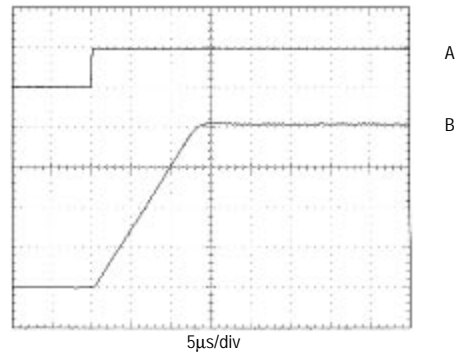
$\overline{CS} = \text{HIGH}$
 A: DIN = 4Vp-p, 100kHz
 B: VOUT, 10mV/div

NEGATIVE SETTLING TIME (MAX531)



$V_{DD} = \pm 5V$, $V_{REFIN} = 2V$, BIPOLAR CONFIGURATION
 A: CS RISING EDGE, 5V/div
 B: VOUT, NO LOAD, 1V/div

POSITIVE SETTLING TIME (MAX531)



$V_{DD} = \pm 5V$, $V_{REFIN} = 2V$, BIPOLAR CONFIGURATION
 A: CS RISING EDGE, 5V/div
 B: VOUT, NO LOAD, 1V/div

+5V, Low-Power, Voltage-Output Serial 12-Bit DACs

Pin Description

| PIN | | NAME | FUNCTION |
|--------|------------------|-------------------------|---|
| MAX531 | MAX538 MAX539 | | |
| 1 | — | BIPOFF | Bipolar Offset/Gain Resistor |
| 2 | 1 | DIN | Serial Data Input |
| 3 | — | $\overline{\text{CLR}}$ | Clear. Asynchronously sets DAC register to 000 hex. |
| 4 | 2 | SCLK | Serial Clock Input |
| 5 | 3 | $\overline{\text{CS}}$ | Chip Select, active low |
| 6 | 4 | DOUT | Serial Data Output for daisy-chaining |
| 7 | — | DGND | Digital Ground |
| 8 | 5 | AGND | Analog Ground |
| 9 | 6 | REFIN | Reference Input |
| 10 | — | REFOUT | Reference Output, 2.048V |
| 11 | — | V _{SS} | Negative Power Supply |
| 12 | 7 | VOUT | DAC Output |
| 13 | 8 | V _{DD} | Positive Power Supply |
| 14 | — | RFB | Feedback Resistor |

Detailed Description

General DAC Discussion

The MAX531/MAX538/MAX539 use an “inverted” R-2R ladder network with a single-supply CMOS op amp to convert 12-bit digital data to analog voltage levels (see *Functional Diagram*). The term “inverted” describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX531/MAX538/MAX539’s topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to 000 hex on power-up. Additionally, a clear $\overline{\text{CLR}}$ pin, when held low, sets the DAC register to 000 hex. $\overline{\text{CLR}}$ operates asynchronously and independently from the chip-select ($\overline{\text{CS}}$) pin.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output, BiCMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 12-bit performance. Settling time is 25 μ s to 0.01% of final value. The settling time is considerably longer when the DAC code is initially set to 000 hex, because at this code the op amp is completely debiased. Start from code 001 hex if necessary. The output is short-circuit protected and can drive a 2k Ω load with more than 100pF load capacitance.

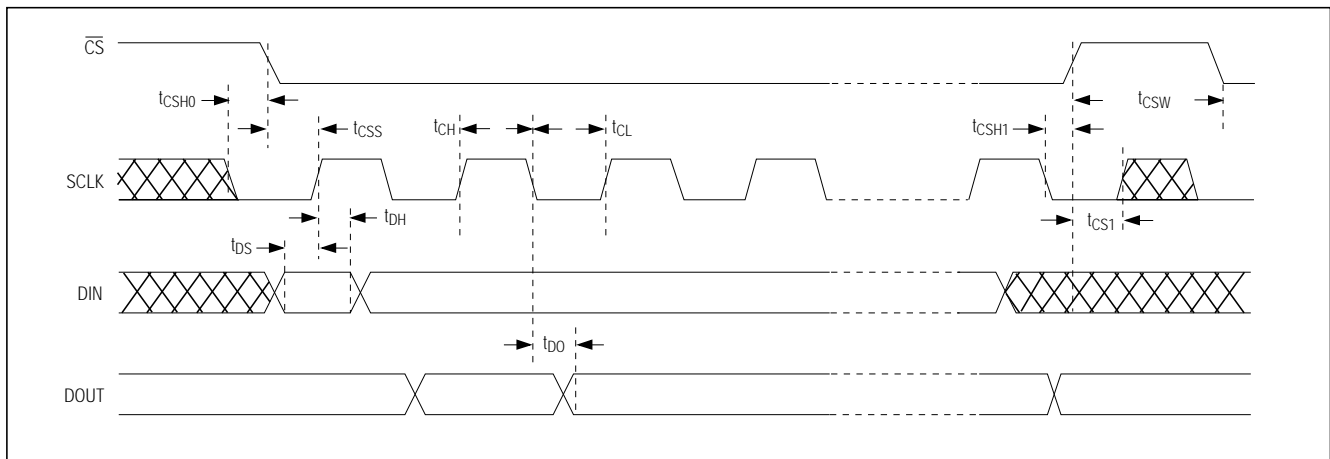


Figure 1. Timing Diagram

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

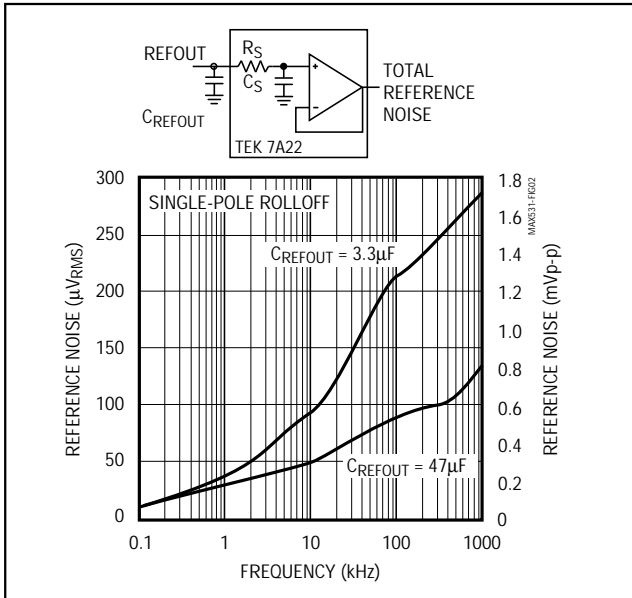


Figure 2. Reference Noise vs. Frequency

Internal Reference (MAX531 only)

The on-chip reference is laser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current, so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typically, source current is 5mA and sink current is 100 μA .

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50 μA maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100 μA to avoid gain errors.

For applications requiring very low-noise performance, connect a 33 μF capacitor from REFOUT to AGND. If noise is not a concern, a lower value capacitor (3.3 μF min) may be used. To reduce noise further, insert a buffered RC filter between REFOUT and REFIN (Figure 2). The reference bypass capacitor, C_{REFOUT} , is still required for reference stability. In applications not requiring the reference, connect REFOUT to V_{DD} or use the MAX538 or MAX539 (no internal reference).

External Reference

An external reference in the range ($V_{\text{SS}} + 2\text{V}$) to ($V_{\text{DD}} - 2\text{V}$) may be used with the MAX531 in dual-supply operation. With the MAX538/MAX539 or the MAX531 in single-supply use, the reference must be positive and may not exceed $V_{\text{DD}} - 2\text{V}$. The reference voltage determines the DAC's full-scale output. The DAC input resistance is code dependent and is minimum (40k Ω) at code 555 hex and virtually infi-

nite at code 000 hex. REFIN's input capacitance is also code dependent and has a 50pF maximum value at several codes. Because of the code-dependent nature of reference input impedances, a high-quality, low-output-impedance amplifier (such as the MAX480 low-power, precision op amp) should be used.

If an upgrade to the internal reference is required, the 2.5V MAX873A is suitable: $\pm 15\text{mV}$ initial accuracy, $\text{TCV}_{\text{OUT}} = 7\text{ppm}/^\circ\text{C}$ (max).

Logic Interface

The MAX531/MAX538/MAX539 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

Figure 1 shows the MAX531/MAX538/MAX539 timing. The maximum serial clock rate is given by $1 / (t_{\text{CH}} + t_{\text{CL}})$, approximately 14MHz. The digital update rate is limited by the chip-select period, which is $16 \times (t_{\text{CH}} + t_{\text{CL}}) + t_{\text{CSW}}$. This equals a 1.14 μs , or 877kHz, update rate. However, the DAC settling time to 12 bits is 25 μs , which may limit the update rate to 40kHz for full-scale step transitions.

Applications Information

Refer to Figures 3a and 3b for typical operating connections.

Serial Interface

The MAX531/MAX538/MAX539 use a three-wire serial interface that is compatible with SPI™, QSPI™ (CPOL = CPHA = 0), and Microwire™ standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the *Functional Diagram*). Sixteen bits of serial data are clocked into the DAC MSB first with the MSB preceded by four fill (dummy) bits. The four dummy bits are not normally needed. They are required **only** when DACs are daisy-chained. Data is clocked in on SCLK's rising edge while $\overline{\text{CS}}$ is low. The serial input data is held in a 16-bit serial shift register. On $\overline{\text{CS}}$'s rising edge, the 12 least significant bits are transferred to the DAC register and update the DAC. With $\overline{\text{CS}}$ high, data cannot be clocked into the MAX531/MAX538/MAX539.

The MAX531/MAX538/MAX539 input data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The QSPI interface allows variable data input from eight to 16 bits, and can be loaded into the DAC in one write cycle.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

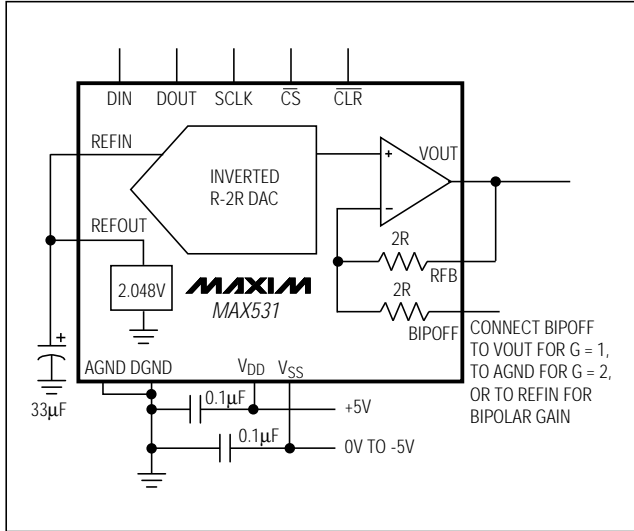


Figure 3a. MAX531 Typical Operating Circuit

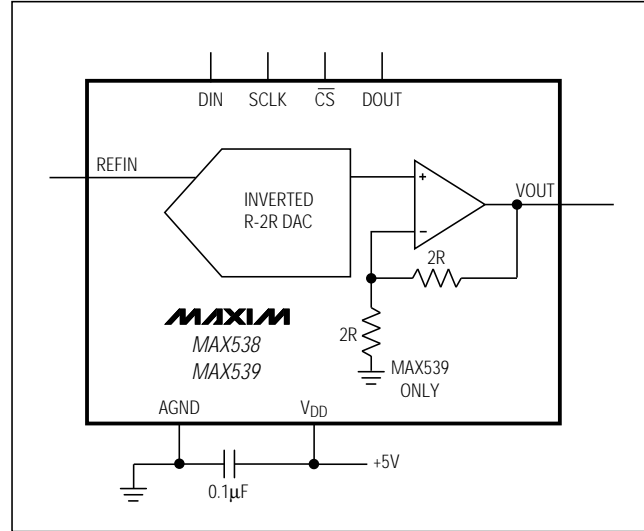


Figure 3b. MAX538/MAX539 Typical Operating Circuit

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. DOUT does **not** go into a high-impedance state when \overline{CS} is high. DOUT changes on SCLK's falling edge when \overline{CS} is low. When \overline{CS} is high, DOUT remains in the state of the last data bit.

Any number of MAX531/MAX538/MAX539 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that t_{CL} (\overline{CS} low to SCLK high) is greater than $t_{DO} + t_{DS}$.

Unipolar Configuration

The MAX531 is configured for a gain of +1 (0V to V_{REFIN} unipolar output) by connecting BIPOFF and RFB to VOUT (Figure 6). The converter operates from either single or dual supplies in this configuration. See Table 1 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, $1\text{LSB} = V_{REFIN} (2^{-12})$. The MAX538 is internally configured for unipolar gain = +1 operation.

A gain of +2 (0V to $2V_{REFIN}$ unipolar output) is set up by connecting BIPOFF to AGND and RFB to VOUT (Figure 7). Table 2 shows the DAC-latch contents vs. VOUT. The MAX531 operates from either single or dual

supplies in this mode. In this range, $1\text{LSB} = (2)(V_{REFIN}) (2^{-12}) = (V_{REFIN})(2^{-11})$. The MAX539 is internally configured for unipolar gain = +2 operation.

Bipolar Configuration

A bipolar range is set up by connecting BIPOFF to REFOUT and RFB to VOUT, and operating from dual ($\pm 5\text{V}$) supplies (Figure 8). Table 3 shows the DAC-latch contents (input) vs. VOUT (output). In this range, $1\text{LSB} = V_{REFIN} (2^{-11})$.

Four-Quadrant Multiplication

The MAX531 can be used as a four-quadrant multiplier by connecting BIPOFF to REFOUT and RFB to VOUT, using (1) an offset binary digital code, (2) bipolar power supplies, using dual power supplies, and (3) a bipolar analog input at REFOUT within the range $V_{SS} + 2\text{V}$ to $V_{DD} - 2\text{V}$, as shown in Figure 9.

In general, a 12-bit DAC's output is $(D)(V_{REFIN})(G)$, where "G" is the gain (+1 or +2) and "D" is the binary representation of the digital input divided by 2^{12} or 4096. This formula is precise for unipolar operation. However, for bipolar, offset binary operation, the MSB is really a polarity bit. No resolution is lost, as there are the same number of steps. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V ($G = +2$) to a range of -2.048V to $+2.048\text{V}$.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. Negative full scale is $-V_{REFIN}$, while positive full scale is $+V_{REFIN} - 1\text{LSB}$.

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

MAX531/MAX538/MAX539

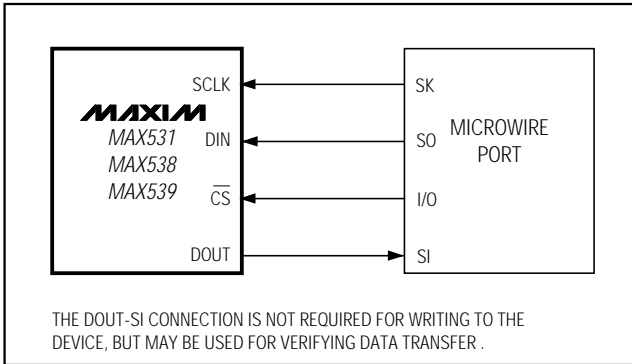


Figure 4. Microwire Connection

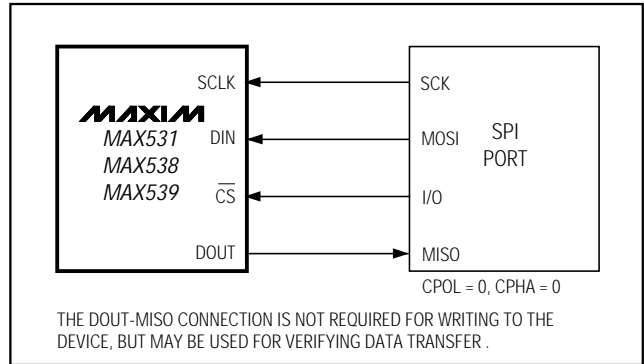


Figure 5. SPI/QSPI Connection

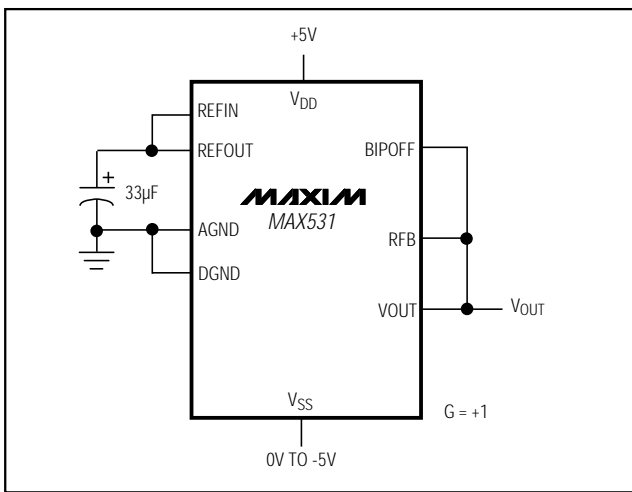


Figure 6. Unipolar Configuration (0V to +2.048V Output)

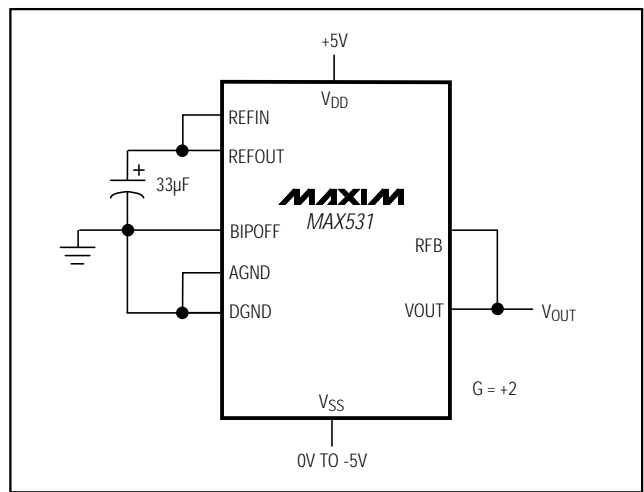


Figure 7. Unipolar Configuration (0V to +4.096V Output)

Table 1. Unipolar Binary Code Table (0V to VREFIN Output), Gain = +1

| INPUT | OUTPUT |
|----------------|--|
| 1111 1111 1111 | $(V_{REFIN}) \frac{4095}{4096}$ |
| 1000 0000 0001 | $(V_{REFIN}) \frac{2049}{4096}$ |
| 1000 0000 0000 | $(V_{REFIN}) \frac{2048}{4096} = +V_{REFIN} / 2$ |
| 0111 1111 1111 | $(V_{REFIN}) \frac{2047}{4096}$ |
| 0000 0000 0001 | $(V_{REFIN}) \frac{1}{4096}$ |
| 0000 0000 0000 | 0V |

Table 2. Unipolar Binary Code Table (0V to 2VREFIN Output), Gain = +2

| INPUT | OUTPUT |
|----------------|---|
| 1111 1111 1111 | $+2 (V_{REFIN}) \frac{4095}{4096}$ |
| 1000 0000 0001 | $+2 (V_{REFIN}) \frac{2049}{4096}$ |
| 1000 0000 0000 | $+2 (V_{REFIN}) \frac{2048}{4096} = +V_{REFIN}$ |
| 0111 1111 1111 | $+2 (V_{REFIN}) \frac{2047}{4096}$ |
| 0000 0000 0001 | $+2 (V_{REFIN}) \frac{1}{4096}$ |
| 0000 0000 0000 | 0V |

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

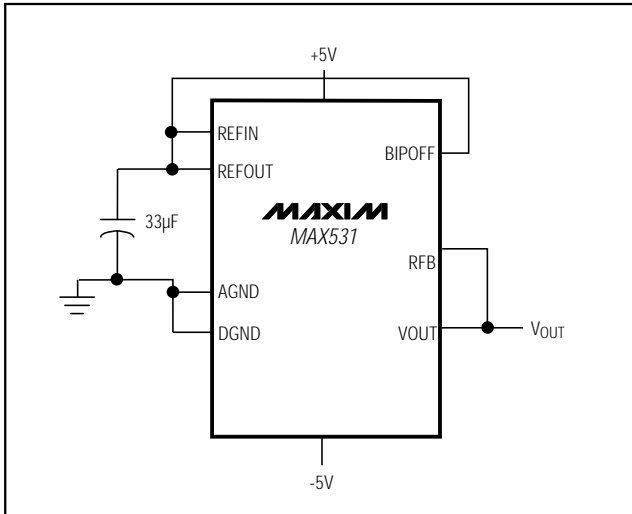


Figure 8. Bipolar Configuration (-2.048V to +2.048V Output)

Single-Supply Linearity

As with any amplifier, the MAX531/MAX538/MAX539's output buffer can be positive or negative. When the offset is positive, it is easily accounted for (Figure 10). However, when the offset is negative, the buffer output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive.

Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinearity near-zero output when operating with a single supply. To account for this nonlinearity in the MAX531/MAX538/MAX539, linearity and gain error are measured from code 11 to code 4095. The output buffer's offset and nonlinear behavior do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 4095.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

Table 3. Bipolar (Offset Binary) Code Table (-VREFIN to +VREFIN Output)

| INPUT | | | OUTPUT |
|-------|------|------|---|
| 1111 | 1111 | 1111 | $(+V_{REFIN}) \frac{2047}{2048}$ |
| 1000 | 0000 | 0001 | $(+V_{REFIN}) \frac{1}{2048}$ |
| 1000 | 0000 | 0000 | 0V |
| 0111 | 1111 | 1111 | $(-V_{REFIN}) \frac{1}{2048}$ |
| 0000 | 0000 | 0001 | $(-V_{REFIN}) \frac{2047}{2048}$ |
| 0000 | 0000 | 0000 | $(-V_{REFIN}) \frac{2048}{2048} = -V_{REFIN}$ |

DGND and AGND should be connected together at the chip. For the MAX531 in single-supply applications, connect VSS to AGND at the chip. The best ground connection may be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass VDD (and VSS in dual-supply mode) with a 0.1µF ceramic capacitor, connected between VDD and AGND (and between VSS and AGND). Mount with short leads close to the device. Ferrite beads may also be used to further isolate the analog and digital power supplies.

Figures 11a and 11b illustrate the grounding and bypassing scheme described.

Saving Power

When the DAC is not being used by the system, minimize power consumption by setting the appropriate code to minimize load current. For example, in bipolar mode, with a resistive load to ground, set the DAC code to mid-scale (Table 3). If there is no output load, minimize internal loading on the reference by setting the DAC to all 0s (on the MAX531, use \overline{CLR}). Under this condition, REFIN is high impedance and the op amp operates at its minimum quiescent current. Due to these low current levels, the output settling time for an input code close to 0 typically increases to 60µs (no more than 100µs).

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

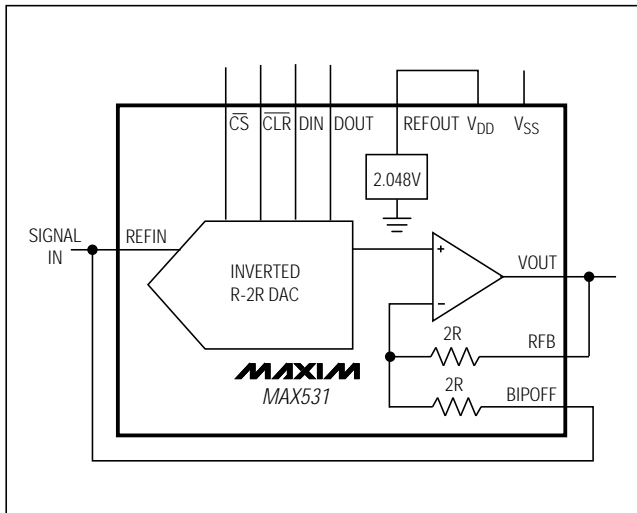


Figure 9. MAX531 Connected as Four-Quadrant Multiplier. The unused REFOUT is connected to V_{DD}.

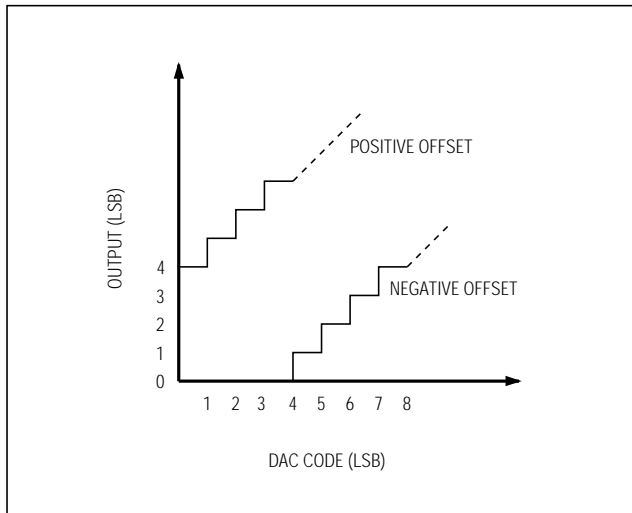


Figure 10. Single-Supply Offset

AC Considerations

Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package and cause internal stray capacitance to appear at the DAC output as noise, even though \overline{CS} is held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding \overline{CS} high, transmitting 555 hex from DIN to DOUT.

Analog Feedthrough

Because of internal stray capacitance, higher frequency analog input signals may couple to the output as shown in the Analog Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. It is tested by holding \overline{CS} high, setting the DAC code to all 0s, and sweeping REF_{IN}.

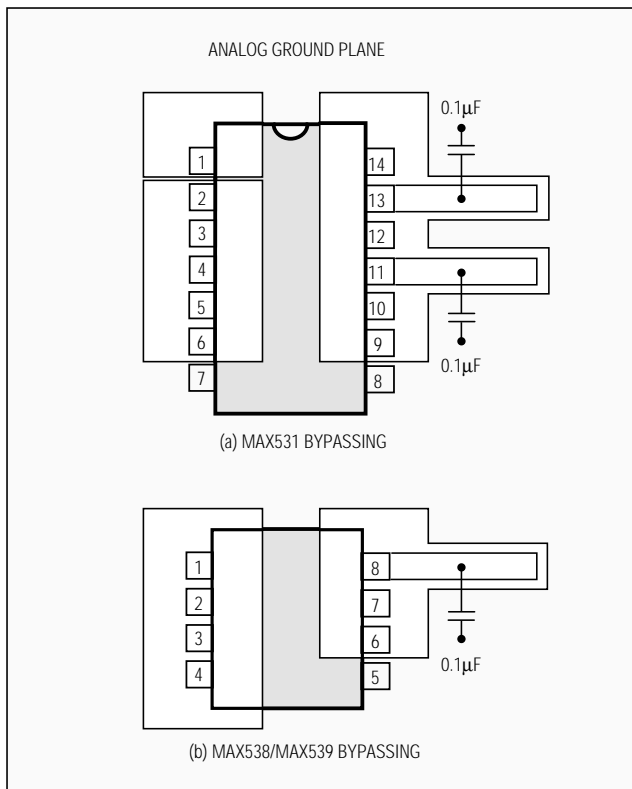


Figure 11. Power-Supply Bypassing

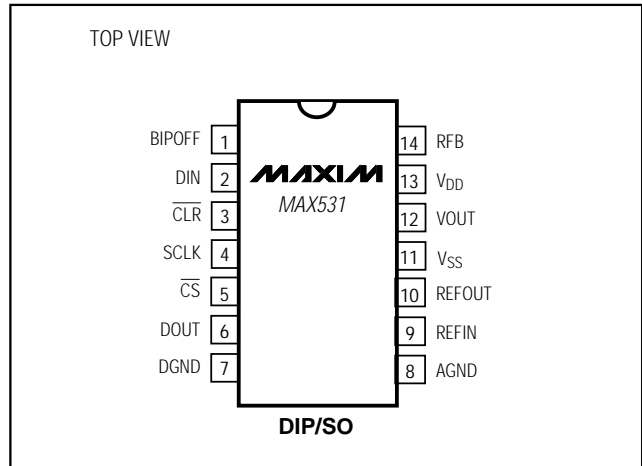
+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

Ordering Information (continued)

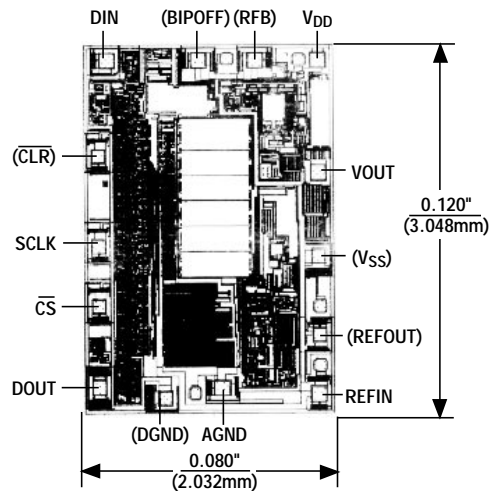
| PART | TEMP. RANGE | PIN-PACKAGE | ERROR (LSB) |
|--------------------|----------------|----------------|-------------|
| MAX531AEPD | -40°C to +85°C | 14 Plastic DIP | ±1/2 |
| MAX531BEPD | -40°C to +85°C | 14 Plastic DIP | ±1 |
| MAX531AESD | -40°C to +85°C | 14 SO | ±1/2 |
| MAX531BESD | -40°C to +85°C | 14 SO | ±1 |
| MAX538 ACPA | 0°C to +70°C | 8 Plastic DIP | ±1/2 |
| MAX538BCPA | 0°C to +70°C | 8 Plastic DIP | ±1 |
| MAX538ACSA | 0°C to +70°C | 8 SO | ±1/2 |
| MAX538BCSA | 0°C to +70°C | 8 SO | ±1 |
| MAX538BC/D | 0°C to +70°C | Dice* | ±1 |
| MAX538AEPD | -40°C to +85°C | 8 Plastic DIP | ±1/2 |
| MAX538BEPD | -40°C to +85°C | 8 Plastic DIP | ±1 |
| MAX538AESD | -40°C to +85°C | 8 SO | ±1/2 |
| MAX538BESD | -40°C to +85°C | 8 SO | ±1 |
| MAX539 ACPA | 0°C to +70°C | 8 Plastic DIP | ±1/2 |
| MAX539BCPA | 0°C to +70°C | 8 Plastic DIP | ±1 |
| MAX539ACSA | 0°C to +70°C | 8 SO | ±1/2 |
| MAX539BCSA | 0°C to +70°C | 8 SO | ±1 |
| MAX539BC/D | 0°C to +70°C | Dice* | ±1 |
| MAX539AEPD | -40°C to +85°C | 8 Plastic DIP | ±1/2 |
| MAX539BEPD | -40°C to +85°C | 8 Plastic DIP | ±1 |
| MAX539AESD | -40°C to +85°C | 8 SO | ±1/2 |
| MAX539BESD | -40°C to +85°C | 8 SO | ±1 |

*Dice are specified at T_A = +25°C only.

Pin Configurations (continued)



Chip Topography



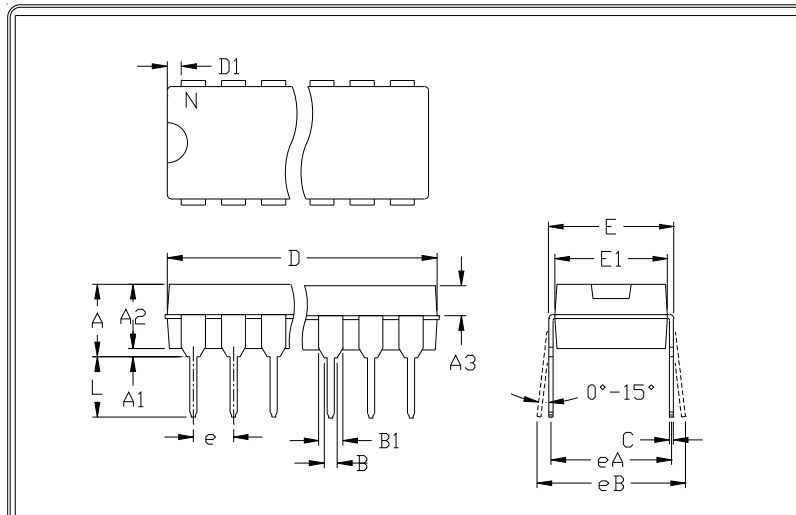
() ARE FOR MAX531 ONLY.

TRANSISTOR COUNT: 922
SUBSTRATE CONNECTED TO V_{DD}

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

Package Information

MAX531/MAX538/MAX539



| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 0.200 | --- | 5.08 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.016 | 0.022 | 0.41 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.012 | 0.20 | 0.30 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 | --- | 2.54 | --- |
| eA | 0.300 | --- | 7.62 | --- |
| eB | --- | 0.400 | --- | 10.16 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |

| | INCHES | | MILLIMETERS | | N | MS001 |
|---|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28.96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

- NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. CONTROLLING DIMENSION: MILLIMETER
 4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
 5. SIMILAR TO JEDEC MO-058AB
 6. N = NUMBER OF PINS



PACKAGE FAMILY OUTLINE: PDIP .300*

1/1

21-0043 A
DOCUMENT CONTROL NUMBER REV

+5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

Package Information (continued)

| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 | | 1.27 | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| h | 0.010 | 0.020 | 0.25 | 0.50 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | N | MS012 |
|---|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | A |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | B |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | C |

NOTES:
 1. D&E DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
 4. CONTROLLING DIMENSION: MILLIMETER
 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
 6. N = NUMBER OF PINS

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TITLE DOCUMENT CONTROL NUMBER REV

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[MCP47FVB04T-E/MQ](#) [MCP48FEB28T-E/MQ](#) [MCP48FVB28T-20E/ST](#) [MCP47FVB28T-20E/ST](#) [MCP47FEB24T-E/MQ](#) [MCP48FVB18T-20E/ST](#) [MCP47FEB14T-E/MQ](#) [MCP47FEB08T-E/MQ](#) [MCP48FVB08T-20E/ST](#) [MCP47FEB04T-E/MQ](#) [MCP47FVB04T-20E/ST](#)
[AD7524JRZ-REEL](#) [LTC1664CGN](#) [LTC1664IGN](#) [LTC7545ACSW](#) [MCP47DA1T-A1E/OT](#) [MCP4921-E/MC](#) [UC3910D](#) [DAC39J84IAAV](#)
[DAC8218SPAG](#) [DAC8562TDGSR](#) [MAX545BCPD+](#) [DAC7641YB/250](#) [DAC7611PB](#) [DAC0800LCM](#) [TLV5638CDR](#) [TLC5615IDR](#)
[DAC900TPWRQ1](#)