19-0741; Rev 1; 5/09

MAXIM

Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

General Description

The MAX5661 single 16-bit DAC with precision high-voltage amplifiers provides a complete solution for programmable current and voltage-output applications. The output amplifiers swing to industry-standard levels of ±10V (voltage output) or source from 0mA (or from 4mA) to 20mA (current output). The voltage output (OUTV) drives resistive loads greater than 2kΩ and capacitive loads of up to 1.2µF. Voltage-output force-sense connections compensate for series protection resistors and field-wiring resistance. Short-circuit protection on the voltage output limits output current to 10mA (typ) sourcing or -11.5mA (typ) sinking. The current output (OUTI) drives resistive loads up to 37.5V (max) and inductive loads up to 1H.

The MAX5661 provides either a current output or a voltage output. Only one output is active at any given time, regardless of the configuration. The MAX5661 voltage output operates with ±13.48V to ±15.75V supplies (V_{DDV}, V_{SSV}) and the current output operates with a single +13.48V to +40V supply (V_{DDI}). A +4.75V to +5.25V digital supply (V_{CC}) powers the rest of the internal circuitry. A buffered reference input accepts an external +4.096V reference voltage.

Update the DAC outputs using software commands or the asynchronous $\overline{LDAC}$ input. An asynchronous $\overline{CLR}$ input sets the DAC outputs to the value stored in the clear register or to zero. The $\overline{FAULT}$ output asserts when the DAC's current output is an open circuit, the DAC's voltage output is a short circuit, or when the $\overline{CLR}$ input is low.

The MAX5661 communicates through a 4-wire 10MHz SPI™-/QSPI™-/MICROWIRE™-compatible serial interface. The DOUT output allows daisy chaining of multiple devices. The MAX5661 is available in a 10mm x 10mm, 64-pin, LQFP package and operates over the -40°C to +105°C temperature range.

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MICROWIRE is a trademark of National Semiconductor Corp.

Applications

Industrial Analog Output Modules

Industrial Instrumentation

Programmable Logic Controls/Distributed Control Systems

Process Control

Features

- **10-Bit Programmable Full-Scale Output Adjustment for Up to ±25% Over Range**
- **Programmable Voltage Output**
  - **Unipolar Range: 0 to +10.24V ±25%**
  - **Bipolar Range: ±10.24V ±25%**
- **Programmable Current Output**
  - **Unipolar Low Range: 0 to 20.45mA**
  - **Unipolar High Range: 3.97mA to 20.45mA**
- **Flexible Analog Supplies (See Table 16)**
  - **±13.48V to ±15.75V for Voltage Output**
  - **+13.48V to +40V for Current Output**
- **Force-Sense Connections (Voltage Output) for Differential Voltage-Output Remote Sensing**
- **Voltage-Output Current Limit**
- **Dropout Detector Senses Out-of-Regulation Current Output**
- **$\overline{CLR}$ and $\overline{LDAC}$ Inputs for Asynchronous DAC Updates**
- **$\overline{CLR}$ Input Resets Output to Programmed Value or Zero Code**
- **$\overline{FAULT}$ Output Indicates Open-Circuited Current Output, Short-Circuited Voltage Output, or Clear State**
- **Temperature Drift**
  - **Voltage Output: ±0.4ppm FSR/°C**
  - **Current Output: ±7.9ppm FSR/°C**
- **Small 64-Pin LQFP Package (10mm x 10mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5661GCB+	-40°C to +105°C	64 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

ABSOLUTE MAXIMUM RATINGS

V_{DDCORE} to V_{SSV} .....-0.3V to +42V
V_{DDI} to AGND.....-0.3V to +42V
V_{DDV} to AGND.....-0.3V to +17V
V_{SSV} to AGND .....-17V to +0.3V
V_{DDI} to V_{SSV} .....-0.3V to +59V
V_{CC} to DGND .....-0.3V to +6V
DGND, DUTGND, DUTGNDS, DACGND, DACGNDS to AGND .....-0.3V to +6V
Digital Inputs ($\overline{CS}$, DIN, SCLK, $\overline{CLR}$, $\overline{LDAC}$, CNF_) to DGND .....-0.3V to (V_{CC} + 0.3V)
Digital Outputs (DOUT, $\overline{FAULT}$) to DGND..... .....-0.3V to the lesser of (V_{CC} + 0.3V) or +6V
REF to AGND.....-0.3V to +6V
OUTV, SVP, SVN, COMPV to V_{SSV}.....-0.3V to (V_{DDV} + 0.3V)
OUTI, COMPI, OUTI4/$\overline{0}$ to AGND.....-0.3V to (V_{DDI} + 0.3V)
Maximum Current into Any Pin .....±100mA
Continuous Power Dissipation (T_A = +70°C)
64-Pin, 10mm x 10mm TQFP (derate 25mW/°C above +70°C)..... 2000mW
Junction-to-Ambient Thermal Resistance in Still Air (θ_{JA}) .....40°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... 8°C/W
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering,10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DUTGND} = V_{DACGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ ll 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				16			Bits
Integral Nonlinearity	INL	V_{OUT}			±0.2	±4	LSB
		I_{OUT}, V_{DDI} = 40V, V_{SSV} = V_{DDV} = 0 (Note 2)	4–20mA		±6		
			0 to 20mA			±10	
		I_{OUT}, V_{DDI} = V_{DDV} = +15V, V_{SSV} = -15V (Note 2)	4–20mA		±2		
			0 to 20mA		±6		
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 3)		-1.0		+1.0	LSB
Zero-Scale Voltage Error	V_{ZSE}	OUTV	Unipolar		±0.01	±3	mV
			Bipolar		±2.0	±10	
Zero-Scale Current (Note 4)		0 to 20mA mode	T_A = +25°C	-45	-30	-15	µA
			T_A = T_{MIN} to T_{MAX}	-60	-30	0	
		4–20mA mode	T_A = +25°C	3.955	3.97	3.985	mA
			T_A = T_{MIN} to T_{MAX}	3.94	3.97	4.00	
Zero-Scale Current Error (Note 4)	I_{ZSE}	0 to 20mA mode	T_A = +25°C	-15	±2.0	+15	µA
			T_A = T_{MIN} to T_{MAX}	-30	±2.0	+30	
		4–20mA mode	T_A = +25°C	-15	±3.0	+15	
			T_A = T_{MIN} to T_{MAX}	-30	±7.0	+30	
Voltage-Offset Error Drift	TCV_{OS}	OUTV	Unipolar		±0.5		ppm of FSR/°C
			Bipolar		±0.2		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DUTGND} = V_{DACGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ ll 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Offset Error Drift	TCI_{OS}	OUTI	0 to 20mA		±4		ppm of FSR/°C
			4–20mA		±4		
Gain Error	GE	OUTV	Unipolar		±2.5	±10	mV
			Bipolar		±4.5	±20	
		OUTI	T_A = +25°C		±8.0	±70	µA
			T_A = T_{MIN} to T_{MAX}		±40	±130	
Gain-Error Drift	TCGE	OUTV	Unipolar		±0.4		ppm of FSR/°C
			Bipolar		±0.4		
		OUTI	0 to 20mA		-7.9		
			4–20mA		-8.6		
Power-Supply Rejection Ratio	PSRR	OUTV, unipolar output, full-scale code, V_{DDV} from +13.48V to +15.75V			20	200	µV/V
		OUTV, bipolar output, zero-scale code, V_{SSV} from -13.48V to -15.75V			20	200	
		OUTI, full-scale code, V_{DDI} from +13.48V to +40V, V_{SSV} = -15.75V, V_{DDV} = +15.75V			0.013	5	µA/V
		OUTI, full-scale code, V_{DDI} from +13.48V to +40V, V_{DDV} = V_{SSV} = 0			0.017	5	
REFERENCE INPUT							
Reference Input Current	I_{REF}				0.050	1	µA
Reference Input Voltage Range	V_{REF}			4.0	4.096	4.2	V
DYNAMIC PERFORMANCE							
Output-Voltage Noise at 10kHz	e_n	Unipolar output, V_{OUTV} = +10.48V			230		nV/√Hz
		Bipolar output, V_{OUTV} = ±10.48V			300		
Output-Current Noise at 10kHz	i_n	0 to 20mA range			132		pA/√Hz
		4–20mA range			120		
Voltage-Output Slew Rate		C_{OUTV} = 100pF, R_{OUTV} = 2kΩ, step = 20V, C_{EXT} = 0nF			0.1		V/µs
Current-Output Slew Rate		L_{OUTI} = 0, R_{OUTI} = 500Ω, step = 20mA			0.15		mA/µs
Major Code Transition Glitch		From code 7FFFh to code 8000h	OUTV		1		µV•s
			OUTI, 0 to 20mA		2.0		nA•s
			OUTI, 4–20mA		2.0		
Digital Feedthrough		Outputs set to zero scale, all digital inputs from 0V to V_{CC} and back to 0V	OUTV		0.1		nV•s
			OUTI, R_L = 500Ω		0.2		pA•s

Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DUTGND} = V_{DACGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ ll 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SETTLING TIME							
Voltage-Output Settling Time		Bipolar output, C_{COMPV} = 3.3nF, to 0.1%	C_{OUTV} = 1nF, R_{OUTV} = 2kΩ		3		ms
			C_{OUTV} = 1.2µF, R_{OUTV} = 2kΩ		5.44		
		Bipolar output, C_{COMPV} = 0nF, to 0.1%	C_{OUTV} = 100pF, R_{OUTV} = 2kΩ		244		µs
		Unipolar output, C_{COMPV} = 3.3nF, to 0.1%	C_{OUTV} = 1nF, R_{OUTV} = 2kΩ		1.8		ms
			C_{OUTV} = 1.2µF, R_{OUTV} = 2kΩ		3.64		
		Unipolar output, C_{COMPV} = 0nF, to 0.1%	C_{OUTV} = 100pF, R_{OUTV} = 2kΩ		130		µs
Current-Output Settling Time		0 to 20.45mA range to 0.1%	R_{OUTI} = 500Ω		1.5		ms
			L_{OUTI} = 1mH		1.66		
			L_{OUTI} = 10mH		1.66		
			L_{OUTI} = 1H		1.97		
		3.97mA to 20.45mA range to 0.1%	R_{OUTI} = 500Ω		1.43		
			L_{OUTI} = 1mH		1.58		
			L_{OUTI} = 10mH		1.58		
			L_{OUTI} = 1H		1.73		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DUTGND} = V_{DACGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ ll 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUTV OUTPUT							
OUTV Linear Output Voltage Range				V_{SSV} + 3.0		V_{DDV} - 3.0	V
Default OUTV Output Voltage Ranges (0V to Full Scale)	V_{OUT}	Unipolar, V_{DDV} = +13.48V, V_{SSV} = -13.48V		0		+10.48	V
		Bipolar, V_{DDV} = +13.48V, V_{SSV} = -13.48V		-10.48		+10.48	
Minimum OUTV Output Voltage Range (FS to ADJ)	V_{OUT}	Unipolar			+7.68		V
		Bipolar			±7.68		
Maximum OUTV Output Voltage Range (FS to ADJ)	V_{OUT}	Unipolar			+12.8		V
		Bipolar			±12.8		
DC Output Impedance					0.1		Ω
OUTV Off-State Leakage Current		OUTV off or disabled, output leakage current from OUTV to AGND			2.5	10	µA
OUTV Short-Circuit Output Current	I_{SC}	Sourcing		7	10	13	mA
		Sinking		-18.0	-11.5	-9.0	
Minimum OUTV Resistive Load	R_{OUTV}	Full-scale code			2		kΩ
Maximum OUTV Capacitive Load	C_{OUTV}	C_{COMPV} = 3.3nF			1.2		µF
		C_{COMPV} = 0nF			1		nF
OUTI OUTPUT							
OUTI Voltage Compliance		Full-scale output, R_{OUTI} = 1500Ω (Note 5)				V_{DDI} - 2.5	V
OUTI Output Current Range		0 to 20mA mode includes FS calibration (Note 4)		0		20.45	mA
		4–20mA mode includes FS calibration		3.97		20.45	
DC Output Impedance		OUTI = full scale			45		MΩ
OUTI Off-State Leakage Current		OUTI off or disabled, 0V < V_{OUTI} < V_{DDI}			0.1	10	µA
Current-Mode Dropout Detection		V_{DDI} - V_{OUTI}, $\overline{FAULT}$ does not assert			1.3		V
FEEDBACK SENSE BUFFER INPUTS							
Input Current		V_{SSV} + 1.7V < SVP, SVN < V_{DDV} - 1.7V			0.05	1	µA
Input Voltage Range		SVP, SVN		V_{SSV} + 1.7		V_{DDV} - 1.7	V
DIGITAL INPUTS							
Input High Voltage	V_{IH}	V_{CC} = 4.75V to 5.25V		2.4			V
Input Low Voltage	V_{IL}	V_{CC} = 4.75V to 5.25V				0.8	V
Input Capacitance	C_{IN}				10		pF
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{CC}		-1		+1	µA
DIGITAL OUTPUTS							
Output High Voltage	V_{OH}	I_{SOURCE} = 400µA, except $\overline{FAULT}$		V_{CC} - 0.5			V
Output Low Voltage	V_{OL}	V_{CC} = 4.75V	I_{SINK} = 1.6mA			0.4	V
			I_{SINK} = 10mA			1	

Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = V_{DUTGND} = V_{DACGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ ll 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. See the *Typical Operating Circuit*.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Leakage Current		$\overline{FAULT}$ only		0.1	2	µA
Three-State Output Leakage Current		DOUT only		±0.1	±2	µA
POWER SUPPLIES (see Table 16)						
V_{CC} Supply Range	V_{CC}		+4.75		+5.25	V
V_{DDV} Supply Range	V_{DDV}	Only OUTV powered	+13.48		+15.75	V
		Only OUTI powered		AGND		
		Both OUTV and OUTI powered	+13.48		+15.75	
V_{SSV} Supply Range	V_{SSV}	Only OUTV powered	-15.75		-13.48	V
		Only OUTI powered		AGND		
		Both OUTV and OUTI powered	-15.75		-13.48	
V_{DDI} Supply Range	V_{DDI}	Only OUTV powered		V_{DDV}		V
		Only OUTI powered	+13.48		+40.00	
		Both OUTV and OUTI powered	V_{DDV}		+40	
V_{DDCORE} Supply Range	V_{DDCORE}	Only OUTV powered		V_{DDV}		V
		Only OUTI powered		V_{DDI}		
		Both OUTV and OUTI powered		V_{DDV}		
Analog and Digital Supply Currents (OUTV Active)	I_{VDDV} + I_{VDDI} + $I_{VDDCORE}$	OUTV powered, V_{DDV} = V_{DDI} = V_{DDCORE} = +15.75V, V_{SSV} = -15.75V, V_{CC} = +5.25V, OUTV unloaded, all ditgital inputs at V_{CC} or DGND		4.5	6.5	mA
	I_{VSSV}		-5	-2.5		
	I_{AGND}		-3.0	-1.6		
	I_{VCC}			0.03	0.2	
Analog and Digital Supply Currents (OUTI Active), 0 to 20mA Mode	I_{VDDV} + I_{VDDI} + $I_{VDDCORE}$	OUTI powered, V_{DDV} = V_{SSV} = AGND, V_{DDI} = V_{DDCORE} = +12V to +40V, V_{CC} = +5.25V, zero code		2.8	5.5	mA
	I_{VSSV}		-1.0	-0.03		
	I_{AGND}		-4.0	-2.1		
	I_{VCC}			0.03	0.2	
Analog and Digital Supply Currents (OUTI Active), 4–20mA Mode	I_{VDDV} + I_{VDDI} + $I_{VDDCORE}$	OUTI powered, V_{DDV} = V_{SSV} = AGND, V_{DDI} = V_{DDCORE} = +12V to +40V, V_{CC} = +5.25V, zero code		6.8	9.5	mA
	I_{VSSV}		-1.0	-0.03		
	I_{AGND}		-4.0	-2.1		
	I_{VCC}			0.03	0.2	
Analog and Digital Supply Currents (Either OUTV or OUTI Active)	I_{VDDV} + $I_{VDDCORE}$	Both OUTV and OUTI powered, V_{DDV} = V_{DDCORE} = +15.75V, V_{SSV} = -15.75V, V_{DDI} = +40V, V_{CC} = +5.25V, OUTV unloaded at zero code, all ditgital inputs at V_{CC} or DGND		4.2	6	mA
	I_{VSSV}		-4.0	2.6		
	I_{AGND}		-4.0	-2.0		
	I_{VCC}			0.03	0.2	
	I_{VDDI}	0 to 20mA at zero code		1.3	2	
	I_{VDDI}	4–20mA at zero code		5.3	6.5	

TIMING CHARACTERISTICS

(V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, AGND = DGND = DUTGND = DACGND = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ ll 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C. See Figure 1.) (Notes 1, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rise or Fall to $\overline{CS}$ Fall Setup Time	t_{CSO}		45			ns
$\overline{CS}$ Fall to SCLK Rise or Fall Setup Time	t_{CSS}		40			ns
SCLK Pulse-Width High	t_{CH}		45			ns
SCLK Pulse-Width Low	t_{CL}		45			ns
DIN to SCLK High Setup Time	t_{DS}		40			ns
DIN to SCLK High Hold Time	t_{DH}		0			ns
SCLK Period	t_{CP}		100			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		100			ns
$\overline{CS}$ High to SCLK High or Low Setup Time	t_{CS1}		45			ns
SCLK High to $\overline{CS}$ Hold Time	t_{CSH}		45			ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO}	C_{DOUT} = 100pF			100	ns
$\overline{CS}$ Transitions to DOUT Enable/Disable Delay	t_{DV}	C_{DOUT} = 100pF			100	ns
SCLK Fall or Rise to $\overline{CS}$ Rise Time	t_{SCS}		15			ns
$\overline{LDAC}$ Pulse-Width Low	t_{LDL}		40			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Rise Time	t_{CSLD}		80			ns

Note 1: Devices are 100% production tested at T_A = +25°C and +105°C. Operation to -40°C is guaranteed by design.
Note 2: I_{OUT} INL 100% production tested from 0 to 20mA only.
Note 3: I_{OUT} DNL guaranteed by V_{OUT} DNL.
Note 4: 0 to 20mA zero-scale current extrapolated by interpolation from full scale and code 192. See the *Measuring Zero-Code Current (0 to 20mA Mode)* section.
Note 5: OUTI voltage compliance measured at V_{DDI} = +33.22V.
Note 6: When updating the DAC registers, allow 5µs before sending the next command.

Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

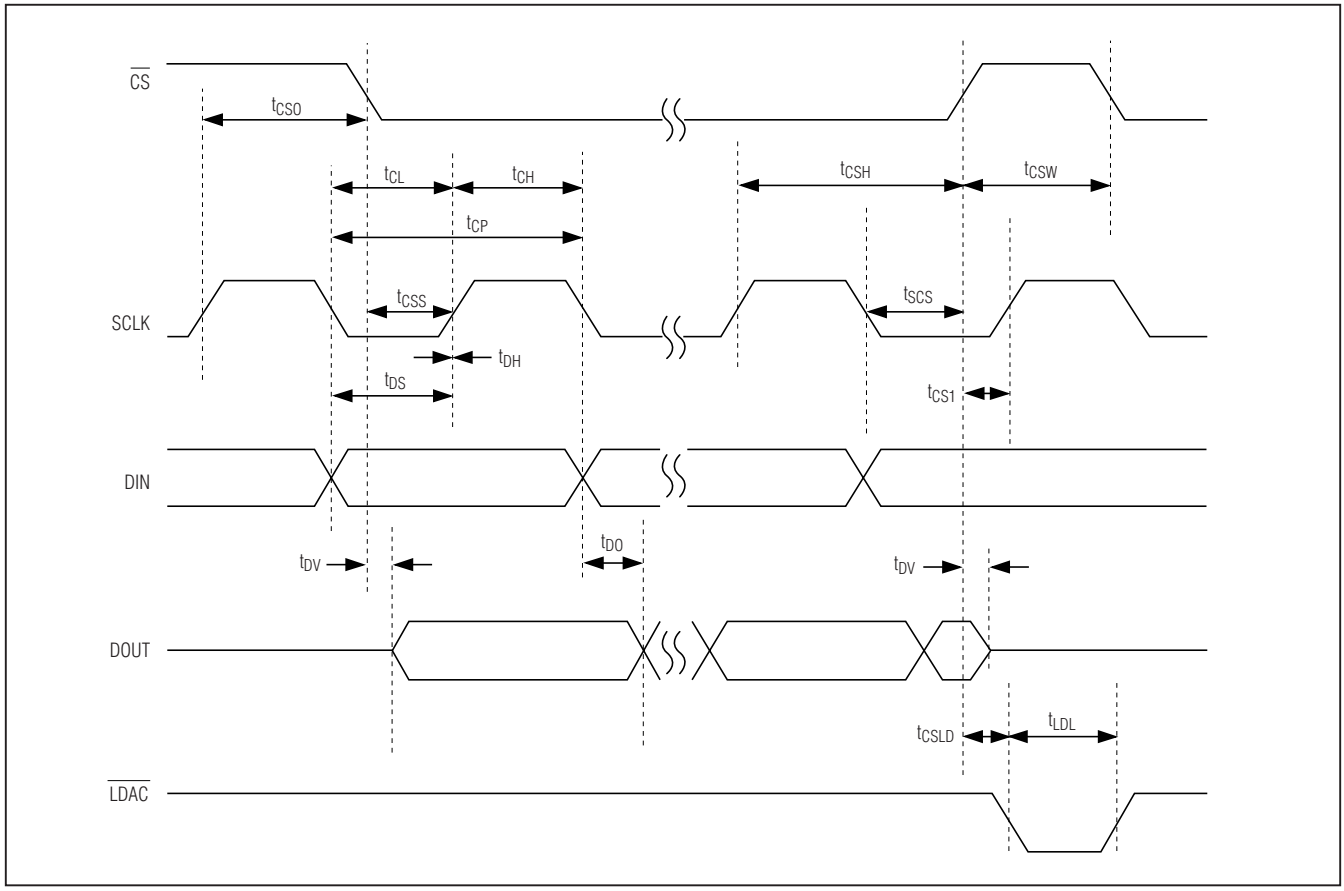
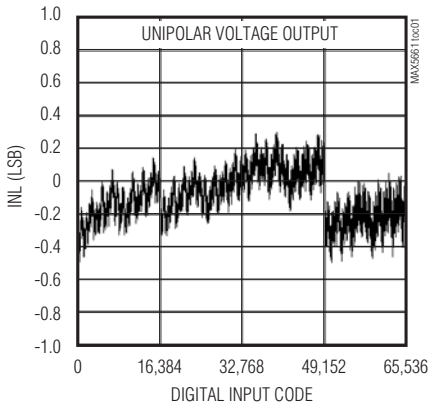


Figure 1. Serial-Interface Timing Diagram

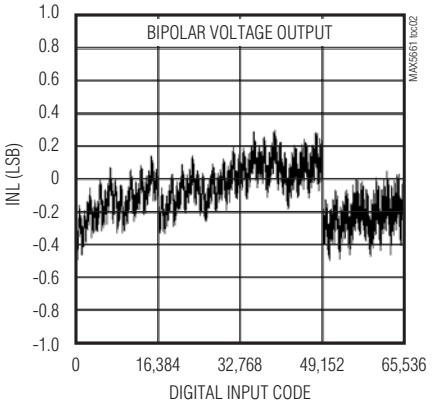
Typical Operating Characteristics

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

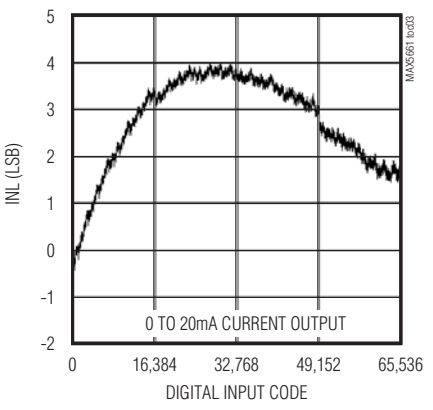
INL vs. DIGITAL INPUT CODE



INL vs. DIGITAL INPUT CODE



INL vs. DIGITAL INPUT CODE

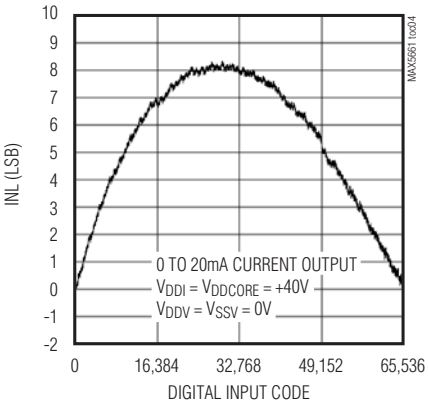


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

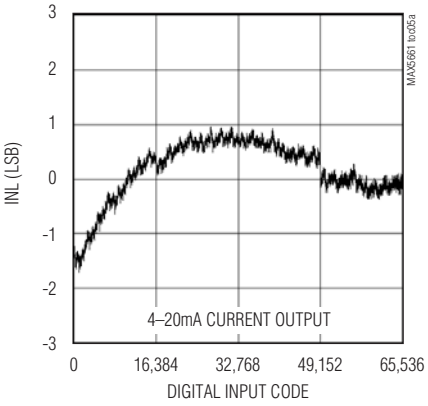
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

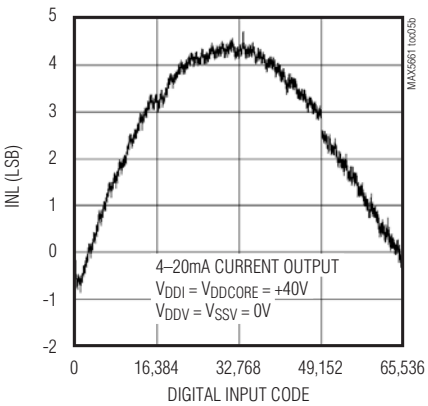
INL vs. DIGITAL INPUT CODE



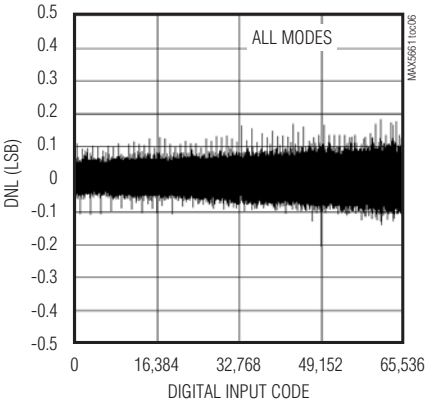
INL vs. DIGITAL INPUT CODE



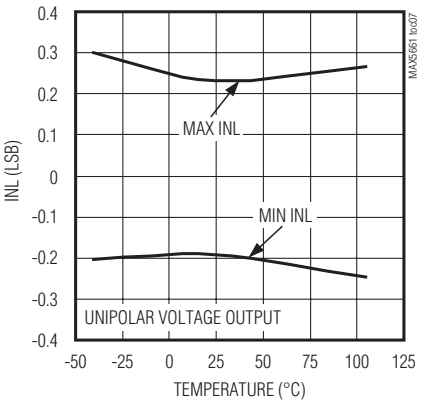
INL vs. DIGITAL INPUT CODE



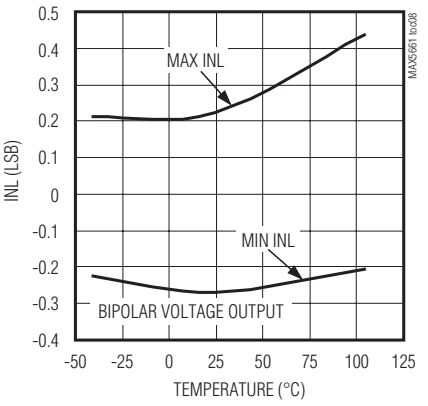
DNL vs. DIGITAL INPUT CODE



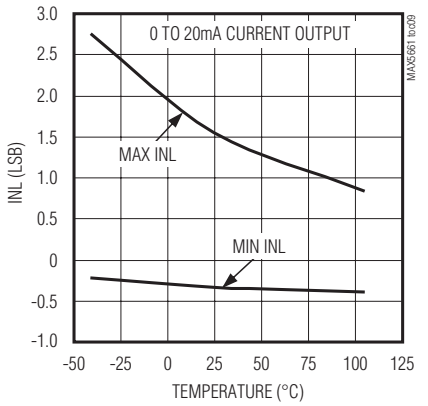
INL vs. TEMPERATURE



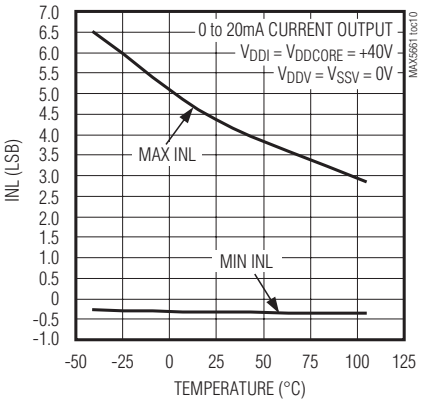
INL vs. TEMPERATURE



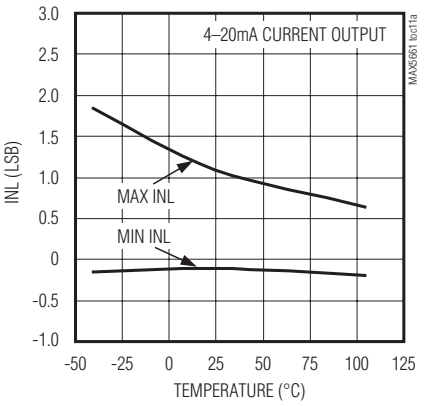
INL vs. TEMPERATURE



INL vs. TEMPERATURE



INL vs. TEMPERATURE

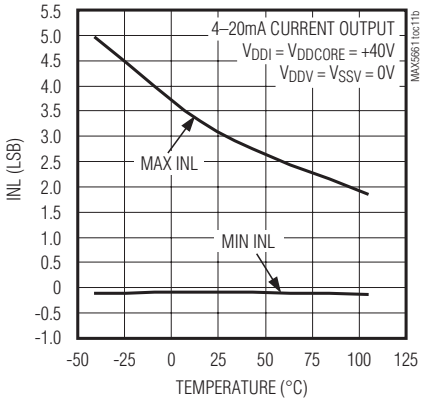


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

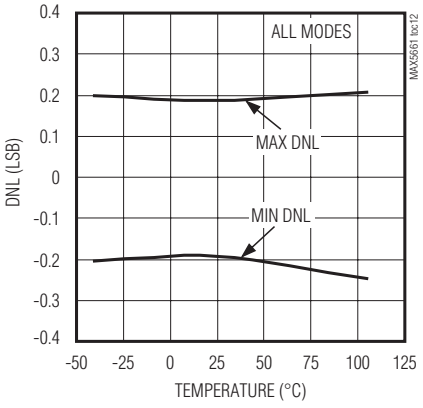
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

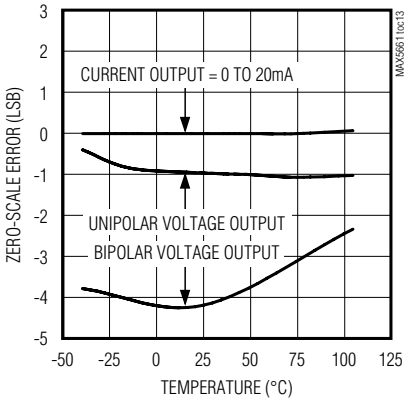
INL vs. TEMPERATURE



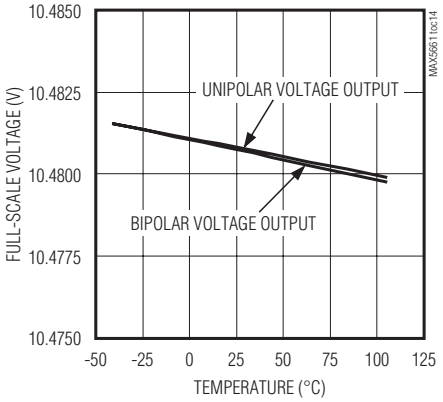
DNL vs. TEMPERATURE



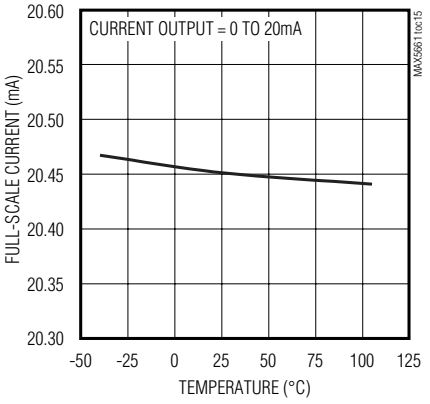
ZERO-SCALE ERROR vs. TEMPERATURE



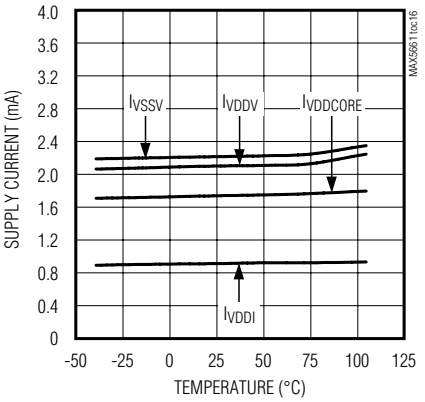
VOLTAGE-OUTPUT FULL-SCALE VOLTAGE vs. TEMPERATURE



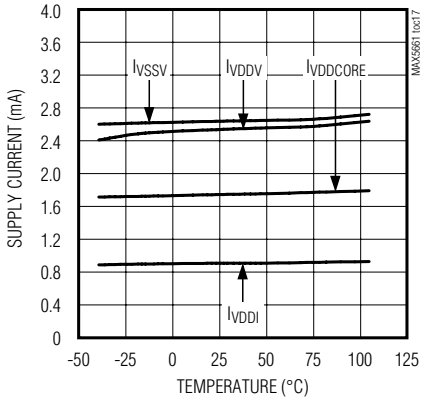
CURRENT-OUTPUT FULL-SCALE CURRENT vs. TEMPERATURE



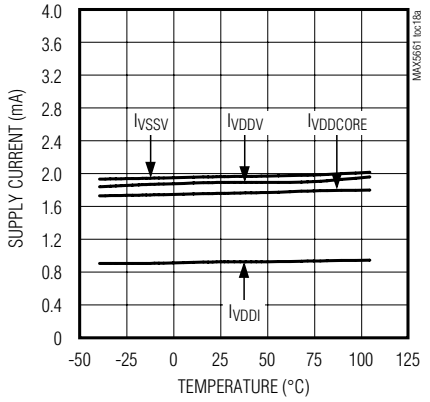
SUPPLY CURRENT vs. TEMPERATURE (UNIPOLAR VOLTAGE OUTPUT)



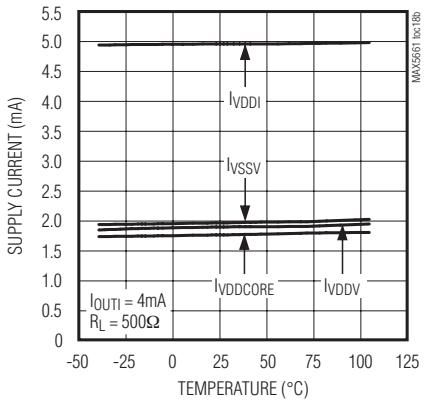
SUPPLY CURRENT vs. TEMPERATURE (BIPOLAR VOLTAGE OUTPUT)



SUPPLY CURRENT vs. TEMPERATURE (0 TO 20mA CURRENT OUTPUT)



SUPPLY CURRENT vs. TEMPERATURE (4–20mA CURRENT OUTPUT)

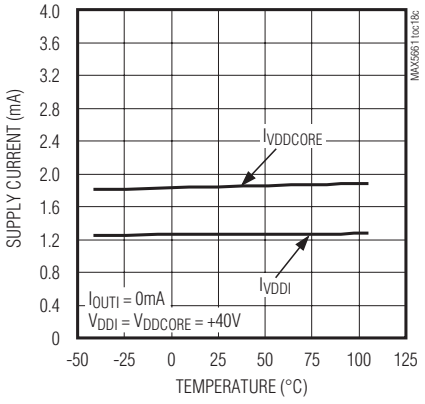


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

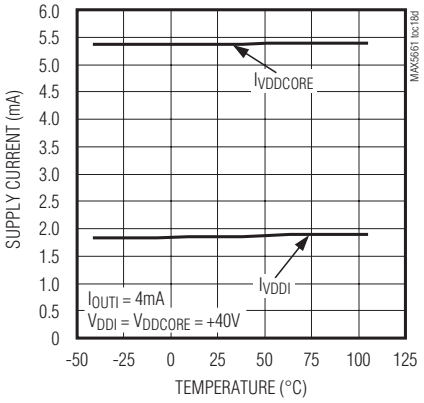
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

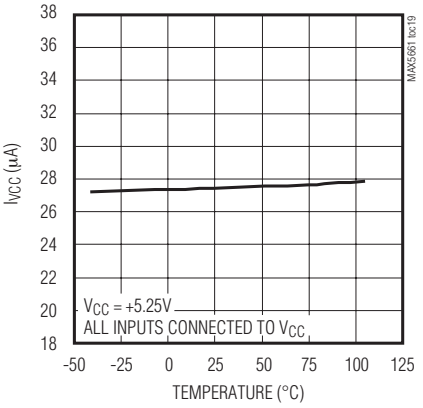
SUPPLY CURRENT vs. TEMPERATURE (0 TO 20mA CURRENT OUTPUT)



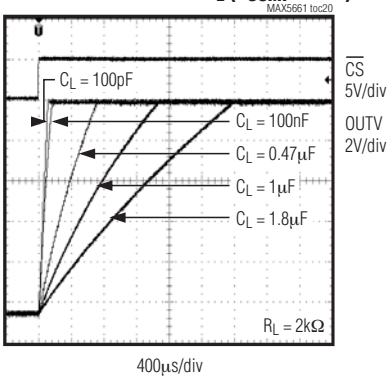
SUPPLY CURRENT vs. TEMPERATURE (4–20mA CURRENT OUTPUT)



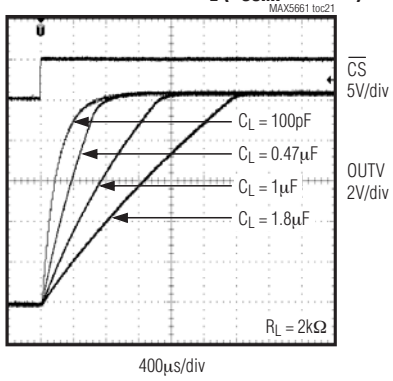
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



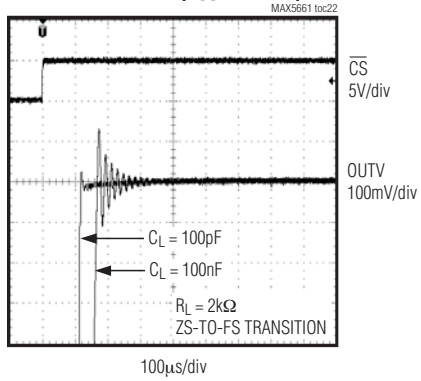
UNIPOLAR VOLTAGE-OUTPUT, ZS-TO-FS TRANSITION vs. C_L (C_{COMP} = 0nF)



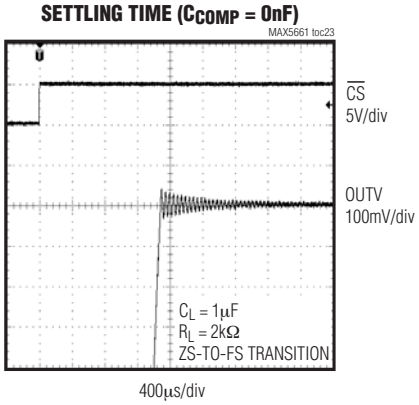
UNIPOLAR VOLTAGE-OUTPUT, ZS-TO-FS TRANSITION vs. C_L (C_{COMP} = 3.3nF)



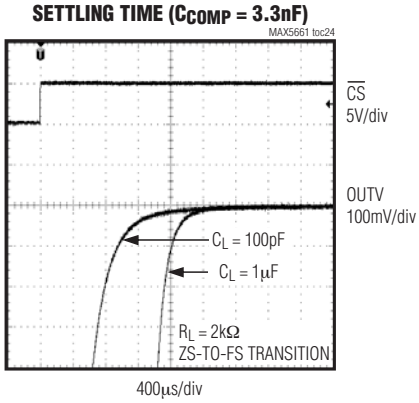
UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)



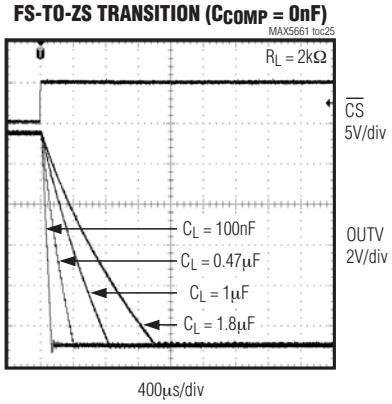
UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)



UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 3.3nF)



UNIPOLAR VOLTAGE-OUTPUT, FS-TO-ZS TRANSITION (C_{COMP} = 0nF)

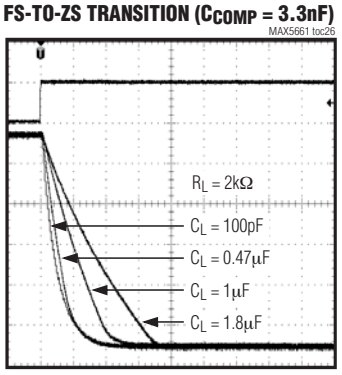


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

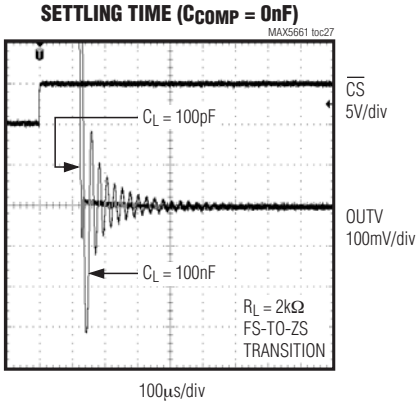
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

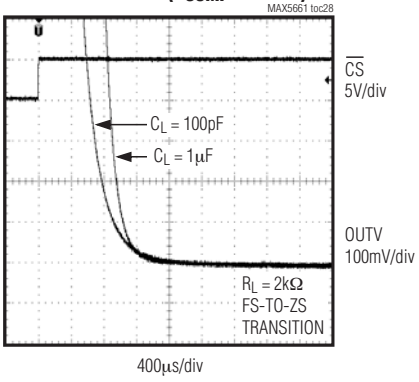
UNIPOLAR VOLTAGE-OUTPUT, FS-TO-ZS TRANSITION (C_{COMP} = 3.3nF)



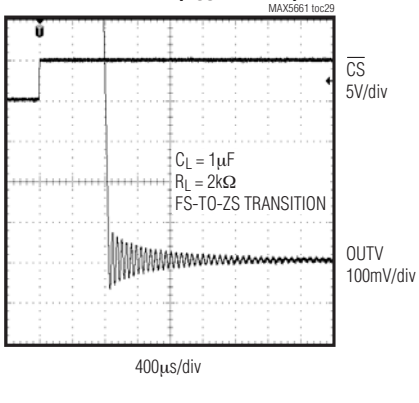
UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)



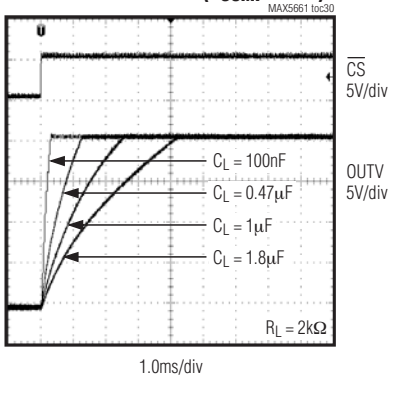
UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 3.3nF)



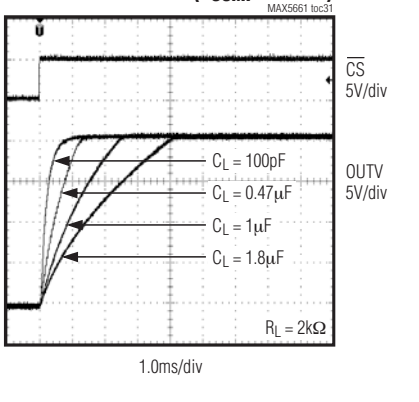
UNIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)



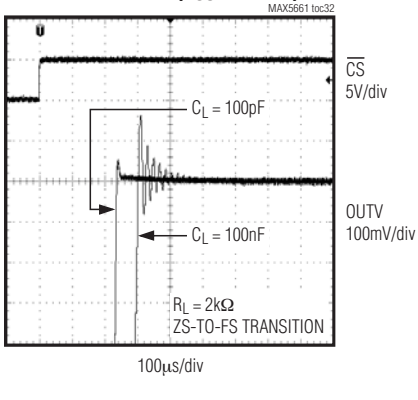
BIPOLAR VOLTAGE-OUTPUT, ZS-TO-FS TRANSITION (C_{COMP} = 0nF)



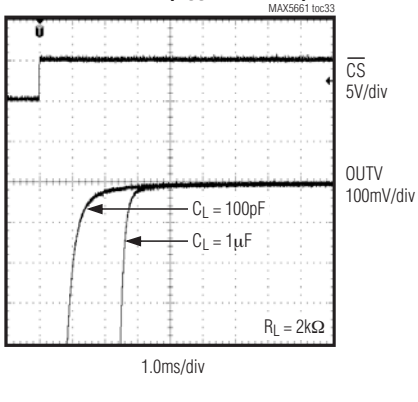
BIPOLAR VOLTAGE-OUTPUT, ZS-TO-FS TRANSITION (C_{COMP} = 3.3nF)



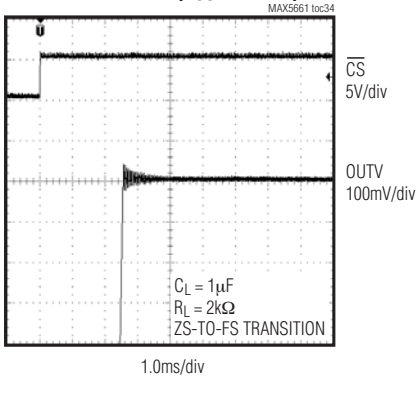
BIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)



BIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 3.3nF)



BIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)

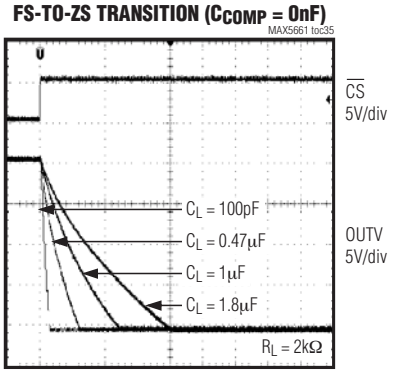


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

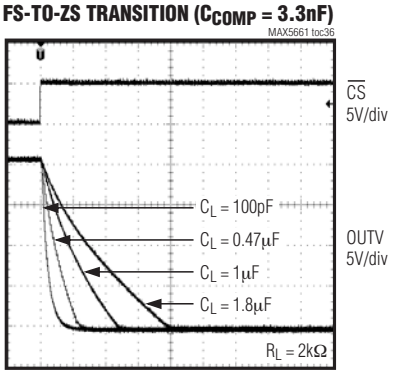
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

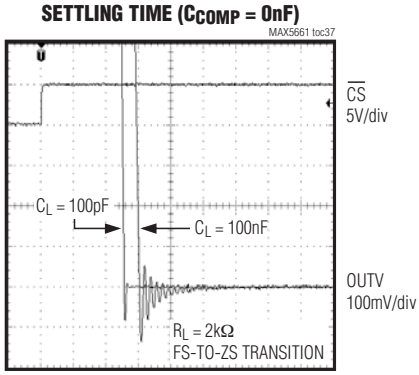
BIPOLAR VOLTAGE-OUTPUT, FS-TO-ZS TRANSITION (C_{COMP} = 0nF)



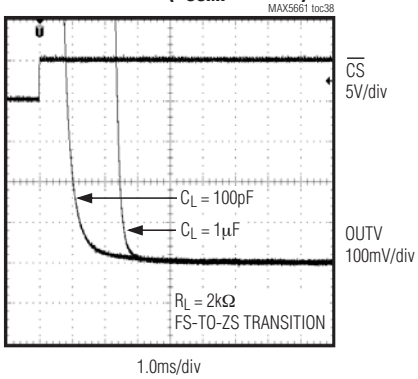
BIPOLAR VOLTAGE-OUTPUT, FS-TO-ZS TRANSITION (C_{COMP} = 3.3nF)



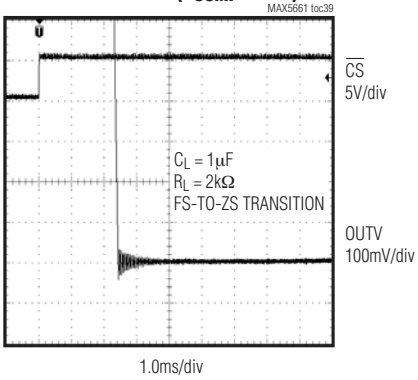
BIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)



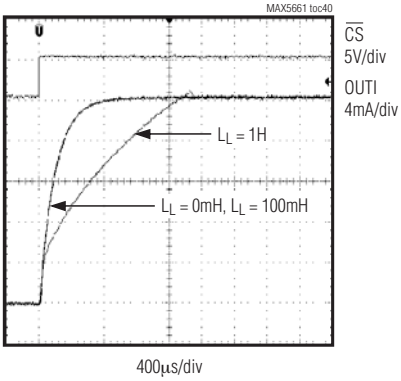
BIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 3.3nF)



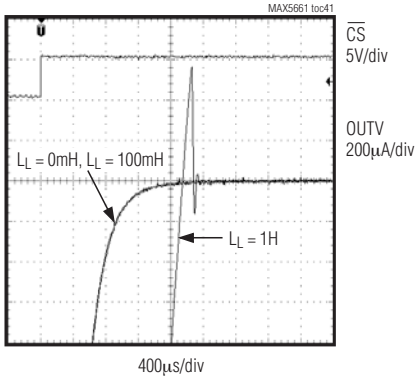
BIPOLAR VOLTAGE-OUTPUT SETTLING TIME (C_{COMP} = 0nF)



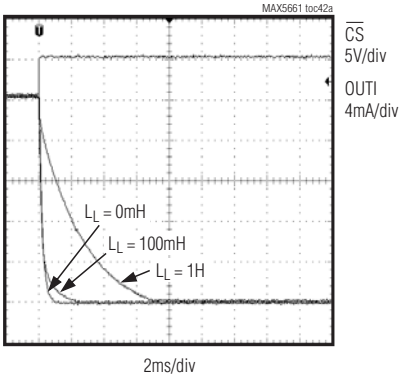
0 TO 20mA CURRENT-OUTPUT, ZS-TO-FS TRANSITION vs. INDUCTIVE LOAD



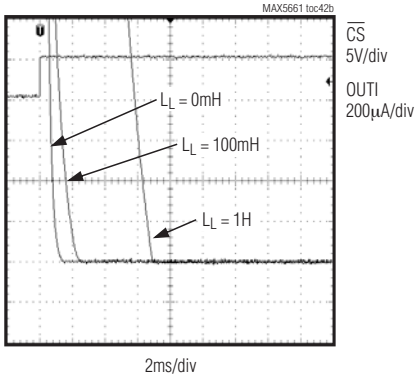
0 TO 20mA CURRENT-OUTPUT, ZS-TO-FS SETTLING TIME



0 TO 20mA CURRENT-OUTPUT, FS-TO-ZS TRANSITION vs. INDUCTIVE LOAD



0 TO 20mA CURRENT-OUTPUT, FS-TO-ZS SETTLING TIME

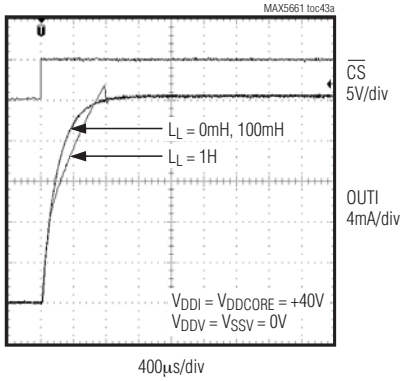


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

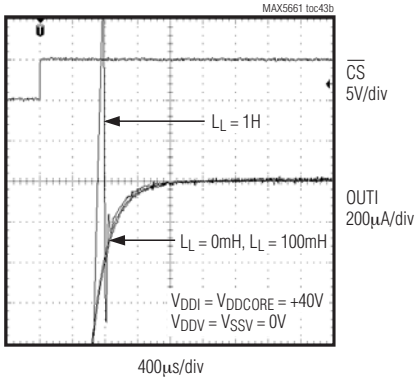
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

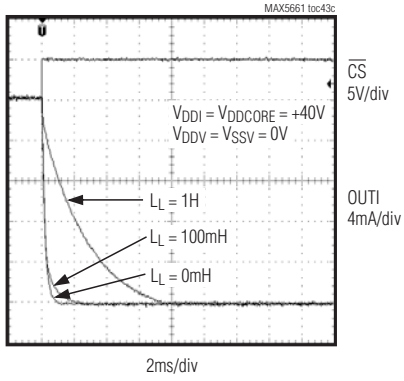
0 TO 20mA CURRENT-OUTPUT, ZS-TO-FS TRANSITION vs. INDUCTIVE LOAD



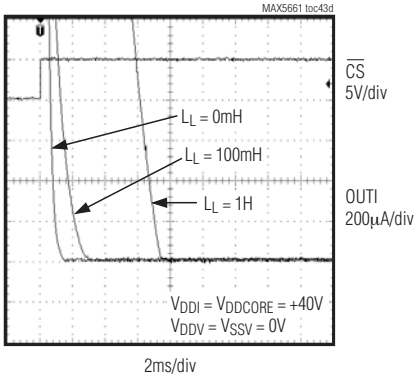
0 TO 20mA CURRENT-OUTPUT, ZS-TO-FS SETTLING TIME



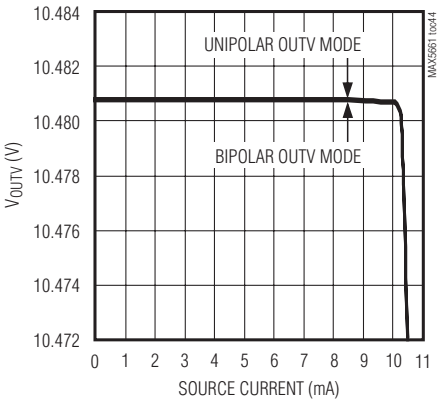
0 TO 20mA CURRENT-OUTPUT, FS-TO-ZS TRANSITION vs. INDUCTIVE LOAD



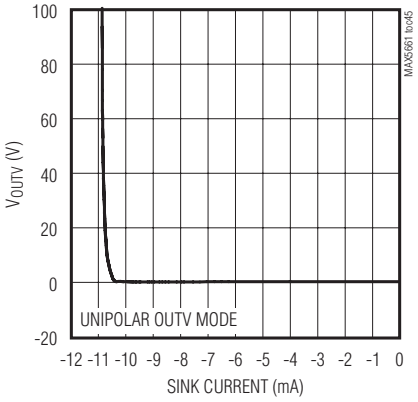
0 TO 20mA CURRENT-OUTPUT, FS-TO-ZS SETTLING TIME



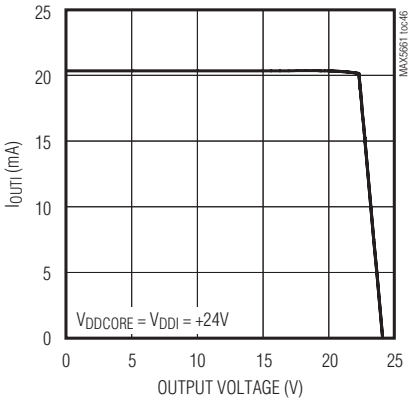
OUTV OUTPUT VOLTAGE vs. LOAD CURRENT (SOURCING)



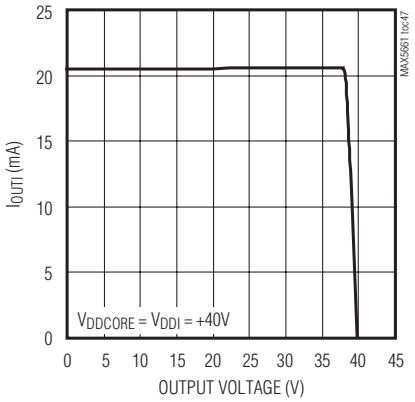
OUTV OUTPUT VOLTAGE vs. LOAD CURRENT (SINKING)



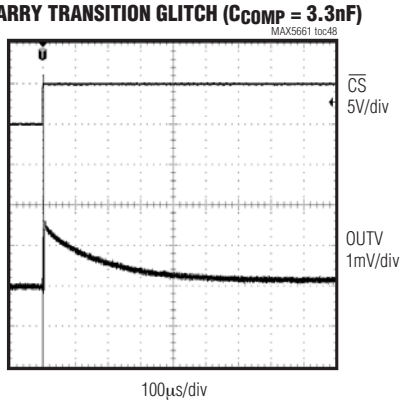
OUTI OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTI OUTPUT CURRENT vs. OUTPUT VOLTAGE



UNIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 3.3nF)

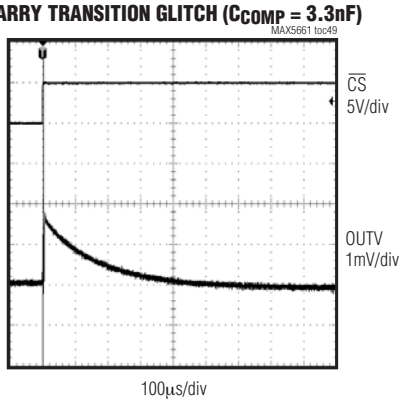


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

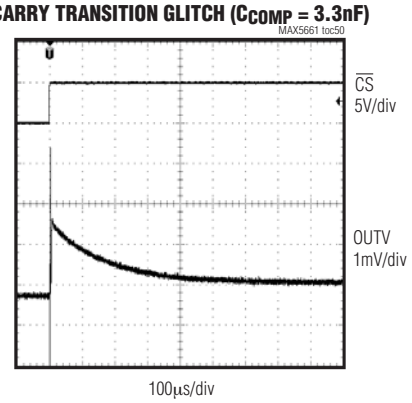
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

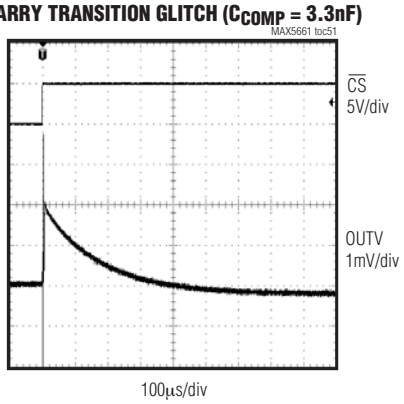
UNIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 3.3nF)



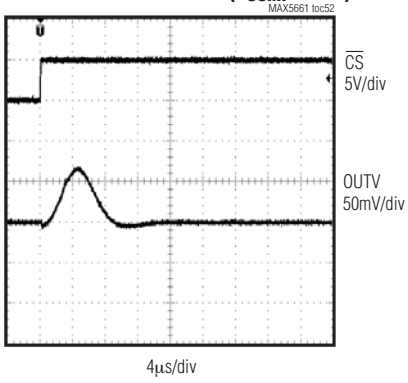
BIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 3.3nF)



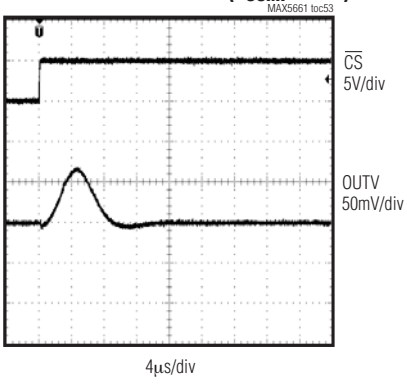
BIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 3.3nF)



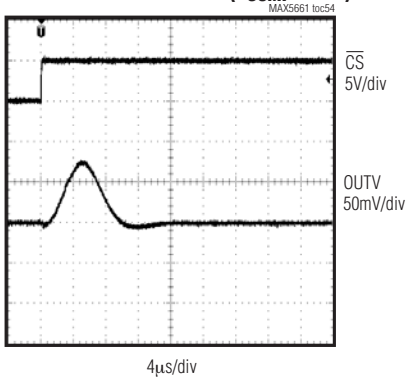
UNIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 0nF)



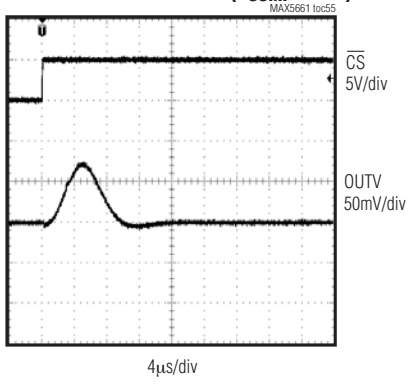
UNIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 0nF)



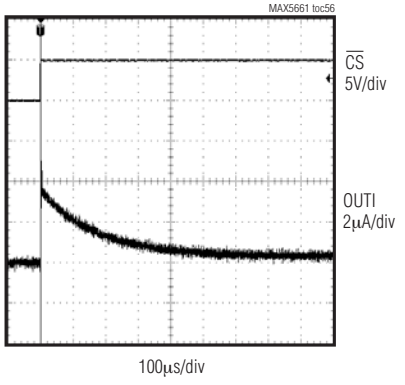
BIPOLAR VOLTAGE-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 0nF)



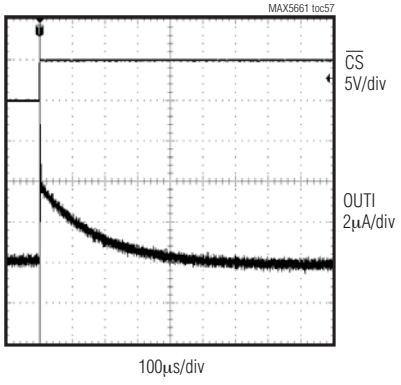
BIPOLAR VOLTAGE-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH (C_{COMP} = 0nF)



0 TO 20mA CURRENT-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH



0 TO 20mA CURRENT-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH

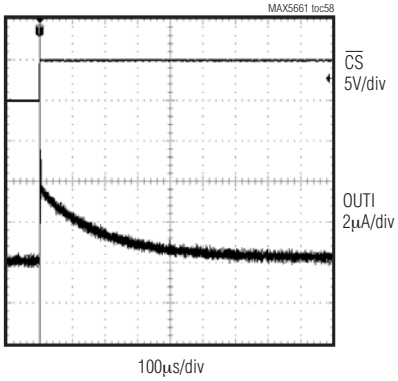


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

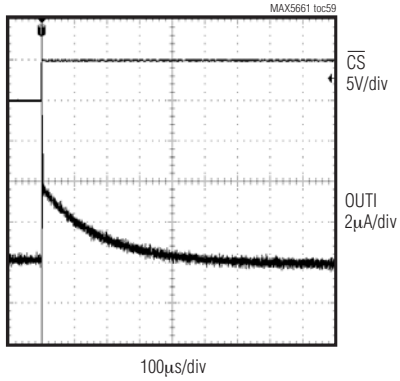
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

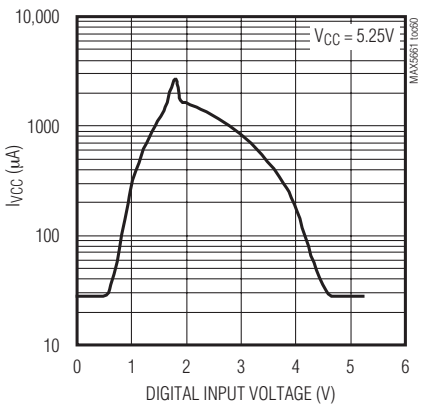
4–20mA CURRENT-OUTPUT, POSITIVE MAJOR CARRY TRANSITION GLITCH



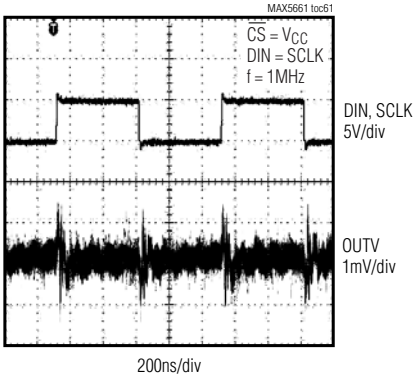
4–20mA CURRENT-OUTPUT, NEGATIVE MAJOR CARRY TRANSITION GLITCH



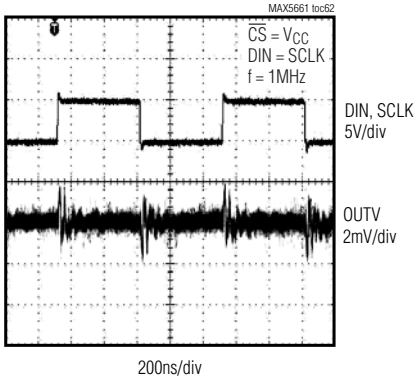
V_{CC} SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



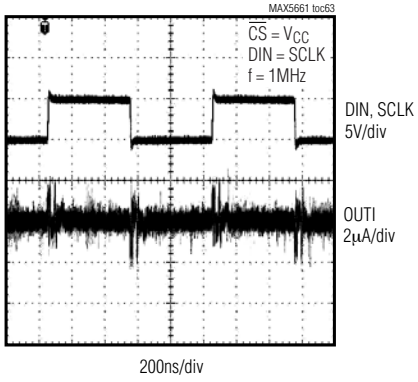
UNIPOLAR VOLTAGE-OUTPUT DIGITAL FEEDTHROUGH



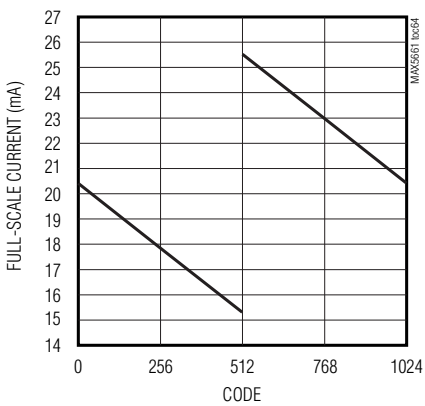
BIPOLAR VOLTAGE-OUTPUT DIGITAL FEEDTHROUGH



CURRENT-OUTPUT DIGITAL FEEDTHROUGH



FULL-SCALE CURRENT vs. FULL-SCALE OUTPUT CURRENT TRIM CODE

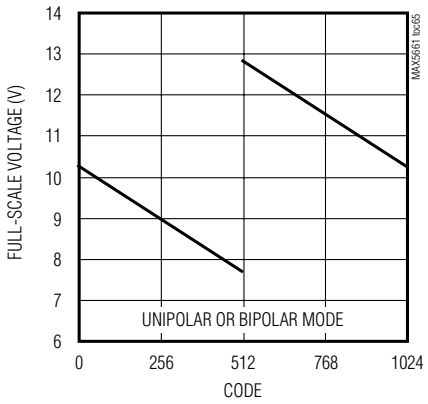


Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

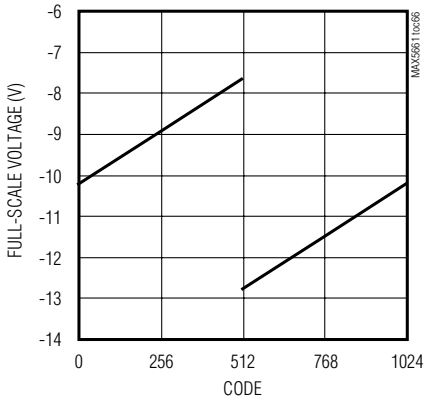
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{CC} = +5V, C_{COMPI} = 22nF, V_{DDV} = V_{DDCORE} = +15V, V_{SSV} = -15V, V_{DDI} = +24V, V_{REF} = +4.096V, V_{AGND} = V_{DGND} = 0V, R_{SERIES} = 47Ω, OUTV loaded with 2kΩ II 100pF to AGND, OUTI loaded with 500Ω to AGND, T_A = +25°C.)

POSITIVE FULL-SCALE VOLTAGE vs. FULL-SCALE OUTPUT TRIM CODE



NEGATIVE FULL-SCALE VOLTAGE vs. FULL-SCALE OUTPUT TRIM CODE



Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7, 8, 10, 15–20, 29–34, 36, 38, 42, 44, 46–52, 58, 61–64	N.C.	No Connection. Not internally connected.
2	OUTI	DAC Current-Source Output. OUTI sources either from 0 to 20mA or from 4–20mA.
4	V_{DDI}	DAC Current-Output Positive Supply. Connect V_{DDI} to a power supply between +13.48V and +40V to power the DAC current-output (OUTI) buffer. Bypass V_{DDI} with a 0.1µF capacitor to AGND, as close as possible to the device.
6	COMPI	OUTI Noise-Limiting Capacitor Connection. Connect a 22nF capacitor from COMPI to V_{DDI} to reduce transient noise at OUTI.
9	OUTI4/$\overline{0}$	Current-Output Range Selection Input. Connect OUTI4/$\overline{0}$ to AGND to select the 0 to 20mA OUTI current-output range. Connect OUTI4/$\overline{0}$ to V_{DDI} to select the 4–20mA OUTI current-output range. The OUTI current range can also be set by software. When using software to set the OUTI current range, connect OUTI4/$\overline{0}$ to AGND.
11	REF	Buffered Voltage Reference Input. Connect an external +4.096V voltage reference to REF. Bypass REF with a 0.1µF capacitor to DACGND, as close as possible to the device. Use a 1kΩ resistor in series to the reference input for optimum performance.
12	DACGND	DAC Analog Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
13	DACGNDS	DAC Analog Sense Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
14	CNF1	Voltage/Current Configuration Input. CNF1 and CNF0 control the OUTV and OUTI outputs. See Tables 13 and 14.
21	CNF0	Voltage/Current Configuration Input. CNF0 and CNF1 control the OUTV and OUTI outputs. See Tables 13 and 14.

Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

Pin Description (continued)

PIN	NAME	FUNCTION
22	DIN	Serial-Data Input. Data is clocked into the serial interface on the rising edge of SCLK.
23	SCLK	Serial-Clock Input
24	$\overline{CS}$	Active-Low Chip-Select Input. Drive $\overline{CS}$ low to enable the serial interface. Drive $\overline{CS}$ high to disable the serial interface. DOUT is high impedance when $\overline{CS}$ is high.
25	DGND	Digital Ground
26	V_{CC}	Digital Power Supply. Connect V_{CC} to a power supply between +4.75V and +5.25V. Bypass V_{CC} with a 0.1µF capacitor to DGND, as close as possible to the device.
27	$\overline{LDAC}$	Active-Low Asynchronous Load DAC Input. Drive $\overline{LDAC}$ low to transfer the contents of the input register to the DAC register to immediately update the output. Connect $\overline{LDAC}$ to V_{CC} if unused.
28	$\overline{FAULT}$	Active-Low Open-Drain Fault Output. $\overline{FAULT}$ asserts low for an OUTI open-circuit condition, an OUTV short-circuit condition, or when the $\overline{CLR}$ input is low (see Table 12 and Figure 9). Ignore the $\overline{FAULT}$ pin function in single supply mode.
35	DOUT	Serial Data Output. Data transitions at DOUT on SCLK's falling edge. DOUT is high impedance when $\overline{CS}$ is high. Use DOUT to read the shift register contents or for daisy chaining multiple MAX5661 devices.
37	$\overline{CLR}$	Active-Low Clear Input. Drive $\overline{CLR}$ low to set the DAC code to the value stored in the clear register, to 0V in voltage mode, or 0mA/4mA depending on the output current mode. Program the contents of the clear register through the serial interface. Enable and disable the $\overline{CLR}$ input through the control register's $\overline{CLREN}$ bit (see Table 4).
39	V_{DDCORE}	DAC Core Positive Supply. Connect V_{DDCORE} to V_{DDI} or V_{DDV} (see Table 16). Bypass V_{DDCORE} with a 0.1µF capacitor to AGND, as close as possible to the device.
40	DUTGNDS	DUT Analog Sense Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
41	DUTGND	DUT Analog Ground. Connect DACGND, DACGNDS, DUTGND, and DUTGNDS together on a low-noise ground plane with a star connection.
43	COMPV	OUTV Amplifier Compensation Feedback Node. Connect a 3.3nF capacitor from OUTV to COMPV when OUTV drives capacitive loads of up to 1.2µF. Leave COMPV open for faster response time.
45	AGND	Analog Ground
53	SVP	Remote Ground Sense Input. Connect SVP to the bottom terminal of R_{OUTV}. See the *Typical Operating Circuit*.
54, 59	I.C.	Internal Connection. Leave unconnected.
55	V_{SSV}	DAC Voltage-Output Negative Power Supply. Always connect V_{SSV} to a power supply between -13.48V and -15.75V. Bypass V_{SSV} with a 0.1µF capacitor to AGND, as close as possible to the device.
56	OUTV	DAC Unipolar/Bipolar Voltage Output. OUTV provides 0 to +10.48V in unipolar mode and -10.48V to +10.48V in bipolar mode.
57	V_{DDV}	DAC Voltage-Output Positive Power Supply. Connect V_{DDV} to a power supply between +13.48V and +15.75V. Bypass V_{DDV} with a 0.1µF capacitor to AGND, as close as possible to the device.
60	SVN	Remote Voltage Sense Input. Connect to the top terminal of R_{OUTV}. See the *Typical Operating Circuit*.

Detailed Description

The MAX5661 single 16-bit DAC with precision high-voltage amplifiers provides a complete solution for programmable current and voltage-output applications. The programmable output amplifiers swing to industry-standard voltage levels of ±10V or current levels from 0mA (or from 4mA) to 20mA. The OUTV voltage output drives resistive loads greater than 2kΩ and capacitive loads up to 1.2µF. Force and sense connections on the voltage output compensate for series protection resistors and field wiring resistance. Short-circuit protection on the voltage output limits output current. The OUTI current output drives resistive loads from 0Ω and higher, up to a compliance voltage of (V_{DDI} - 2.5V). The OUTI current output also drives inductive loads up to 1H.

The MAX5661 provides a current output or a voltage output, with only one output active at any given time. The MAX5661 operates with ±13.48V to ±15.75V dual supplies (V_{DDV}, V_{SSV}) for the voltage output and a +13.48V to +40V single supply (V_{DDI}) for the current output (see Table 16). The +4.75V to +5.25V digital supply (V_{CC}) powers the digital circuitry and V_{DDCORE} powers the rest of the internal analog circuitry. A buffered reference input accepts a +4.096V reference voltage.

The $\overline{LDAC}$ and $\overline{CLR}$ inputs asynchronously update the DAC outputs. $\overline{CLR}$ sets the DAC code to the value stored in the clear register (software clear), or to zero scale (hardware clear). The $\overline{FAULT}$ output asserts for an open-circuit current output, a short-circuit voltage output, or a clear state condition when $\overline{CLR}$ is low. The power-on reset circuitry guarantees the outputs remain off at power-up and all register bits are set to zero to ensure a glitchless power-up sequence.

A 10MHz SPI-/QSPI-/MICROWIRE-compatible serial interface programs the DAC outputs and configures the device. The DOUT output allows shift-register reads or daisy chaining of several devices. The double-buffered interface includes an input register and a DAC register. Use software commands or the asynchronous $\overline{LDAC}$ input to transfer the input register contents to the DAC register and update the DAC outputs.

4-Wire SPI-Compatible Serial Interface

The MAX5661 communicates through a serial interface compatible with SPI, QSPI, and MICROWIRE devices. For SPI, ensure that the SPI bus master (typically a microcontroller (µC)) runs in master mode to generate the serial-clock signal. Set the SCLK frequency to 10MHz or less, and set the clock polarity (CPOL) and phase (CPHA) in the µC control registers to the same value. The MAX5661 operates with SCLK idling high or low, and thus operates with CPOL = CPHA = 0 (see Figure 2) or CPOL = CPHA = 1 (see Figure 3). Force $\overline{CS}$ low to input data at DIN on the rising edge of SCLK. Output data at DOUT updates on the falling edge of SCLK (see Figure 1).

A high-to-low transition on $\overline{CS}$ initiates the 24-bit data input cycle. Once $\overline{CS}$ is low, write an 8-bit command byte (MSB first) at DIN to send data to the appropriate internal register (see Tables 1, 2, and 3). C7 is the MSB of the command byte and C0 is the LSB. Following the command byte, write 2 data bytes containing bits D15–D0. D15 is the MSB of the 2 data bytes and D0 is the LSB (see Figure 4 and the *Register Descriptions* section). Data loads into the shift register 1 bit at a time.

Write the data as one continuous 24-bit stream, always keeping $\overline{CS}$ low throughout the entire 24-bit word. The MAX5661 stores the 24 most recent bits received, including bits from previous transmission(s). Ensure SCLK has 24 rising and falling edges between $\overline{CS}$ falling low to $\overline{CS}$ returning high. Data loads into the shift register on the rising edge of SCLK. Once $\overline{CS}$ returns high, data transfers from the shift register into the appropriate internal register.

When reading data, write an 8-bit command byte and 16 data bits at DIN. On the following 24-bit sequence, read out the shift register's contents (command byte and the 16 data bits) at DOUT (see Figure 5). Data transitions at DOUT on the falling edge of SCLK. While reading data at DOUT on the second 24-bit sequence, load another command byte and 2 data bytes at DIN or write a no-operation command. DOUT three-states when $\overline{CS}$ is high. The DAC outputs update on the rising edge of $\overline{CS}$ after writing to the DAC register or by pulling $\overline{LDAC}$ low.

Daisy chain multiple devices by connecting the first DOUT to the second DIN, and so forth. Daisy chaining allows communication with multiple MAX5661 devices using single $\overline{CS}$ and SCLK signals. See the *Daisy Chaining Multiple MAX5661 Devices* section.

Single 16-Bit DAC with Current and Voltage Outputs for Industrial Analog Output Modules

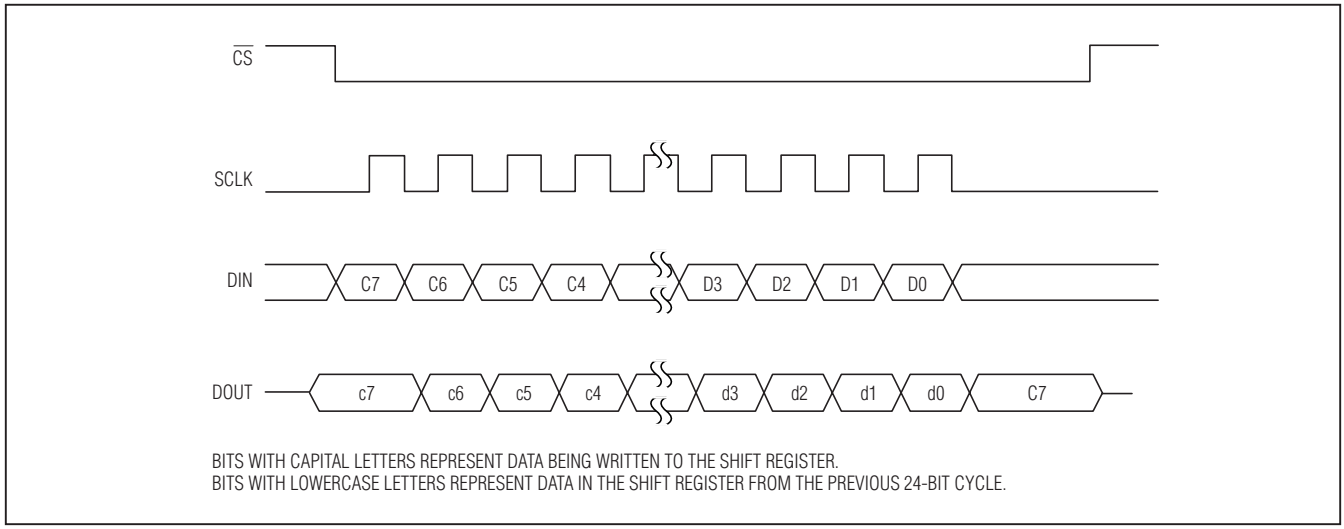


Figure 2. MICROWIRE- or SPI-Interface Timing Diagram (CPOL = CPHA = 0)

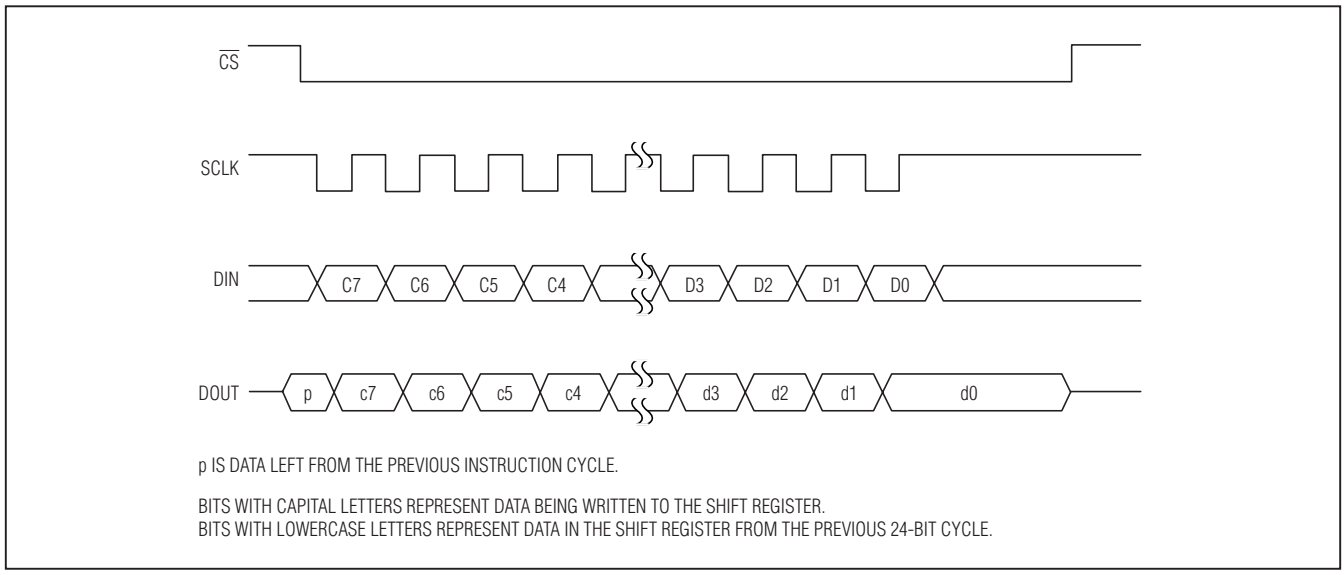


Figure 3. SPI-Interface Timing Diagram (CPOL = CPHA = 1)

Table 1. Input Command Bits

24-BIT SERIAL INPUT WORD																							
COMMAND BYTE								DATA BITS															
MSB																							LSB
C7	C6	C5	C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2. Register Description

COMMAND BITS								OPERATION
C7	C6	C5	C4	C3	C2	C1	C0	
X	X	X	X	0	0	0	0	No operation. Transfer shift register's data to DOUT.
X	X	X	X	0	0	0	1	Write control register.
X	X	X	X	0	0	1	0	Read control register.
X	X	X	X	0	0	1	1	Load input register. DAC register unchanged.
X	X	X	X	0	1	0	0	Load DAC and input register.
X	X	X	X	0	1	0	1	Load DAC register. Transfer input register data to DAC register. DAC outputs update on $\overline{CS}$'s rising edge.
X	X	X	X	0	1	1	0	Write clear register.
X	X	X	X	0	1	1	1	Read input register.
X	X	X	X	1	0	0	0	Read DAC register.
X	X	X	X	1	0	0	1	Read clear register.
X	X	X	X	1	1	1	1	No operation. Transfer shift register's data to DOUT.

X = Don't care. All other commands are reserved for factory use. Do not use.

Register Descriptions

The MAX5661 communicates between its internal registers and the external bus lines through the 4-wire SPI-/QSPI-/MICROWIRE-compatible serial interface. Table 1 details the command bits (C7–C0) and the data bits (D15–D0) of the serial input word. Tables 2 and 3 detail the command byte and the subsequent register accessed. Tables 4–8 detail the various read/write internal registers and their power-on reset states. **When updating the DAC register, allow 5µs before sending the next command.**

Control Register (Read/Write)

Write to the control register to enable the current or voltage output, set the voltage output for unipolar or bipolar mode, and set the current-output range. The control register also initializes the clear and fault modes. Set the command byte to 0x01 to write to the control register. Set the command byte to 0x02 to read from the control register. Write or read data bits D15–D5. D4–D0 are don't-care bits for a write operation. D4, D3, and D2 are read-only bits. D1 and D0 are don't-care bits for a read operation (see Table 4).

Set the OUTVON bit (D15) to 1 to enable the OUTV DAC voltage output. Set the OUTION bit (D14) to 1 to enable the OUTI DAC current output. Always set bit D13 to 0. Set the $\overline{B}$/U bit (D12) to determine whether the OUTV output operates in bipolar mode ($\overline{B}$/U = 0) or unipolar mode ($\overline{B}$/U = 1).

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Table 3. Register Bit Descriptions

OPERATION	DESCRIPTION	COMMAND BYTE								1ST DATA BYTE								2ND DATA BYTE							
		C7	C6	C5	C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
No operation. Transfer shift-register data to DOUT.	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
No operation. Transfer shift-register data to DOUT.	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Write control register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	0	0	1	OUTVON	OUTION	0	B/U	OUTI4/0 EN	14 to 20 BIT	CLREN	CLRMODE	RCLR	FAULTEN	CLRFLAGEN	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Read control register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above.								OUTVON	OUTION	0	B/U	OUTI4/0 EN	14 to 20 BIT	CLREN	CLRMODE	RCLR	FAULTEN	CLRFLAGEN	FAULTV	FAULTI	CLEARST	X	X
Load input register from shift register. DAC register unchanged.	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	0	1	1	MSB <-- 16-Bit DAC Data --> LSB															
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Load input register and DAC register from shift register.	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	1	0	0	MSB <-- 16-Bit DAC Data --> LSB															
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Load DAC register from input register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Write clear register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	1	1	0	MSB <-- 16-Bit Clear-Register Data --> LSB															
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above. Shift-register data not changed by this operation.																							
Read input register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above.								MSB <-- 16-Bit Input-Register Data --> LSB															
Read DAC register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above.								MSB <-- 16-Bit DAC-Register Data --> LSB															
Read clear register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above.								MSB <-- 16-Bit DAC Clear Register Data --> LSB															
Write full-scale output trim register	Data in shift register before $\overline{CS}$ driven high and command executed	X	X	X	X	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Data in shift register after $\overline{CS}$ driven high and command executed	Same as line above.								FS_EN	X	X	X	X	X	FS_ BIT 9 (MSB)	FS_ BIT 8	FS_ BIT 7	FS_ BIT 6	FS_ BIT 5	FS_ BIT 4	FS_ BIT 3	FS_ BIT 2	FS_ BIT 1	FS_ BIT 0 (LSB)

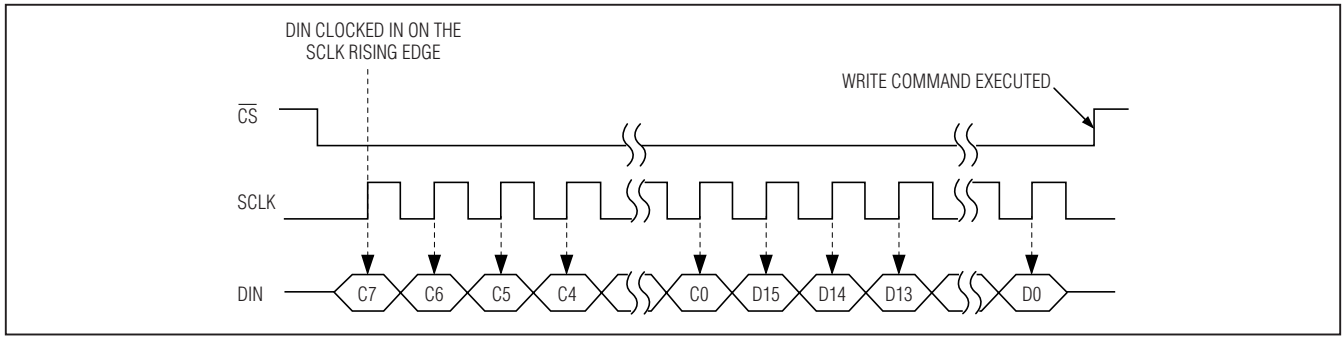

Figure 4. Write Timing

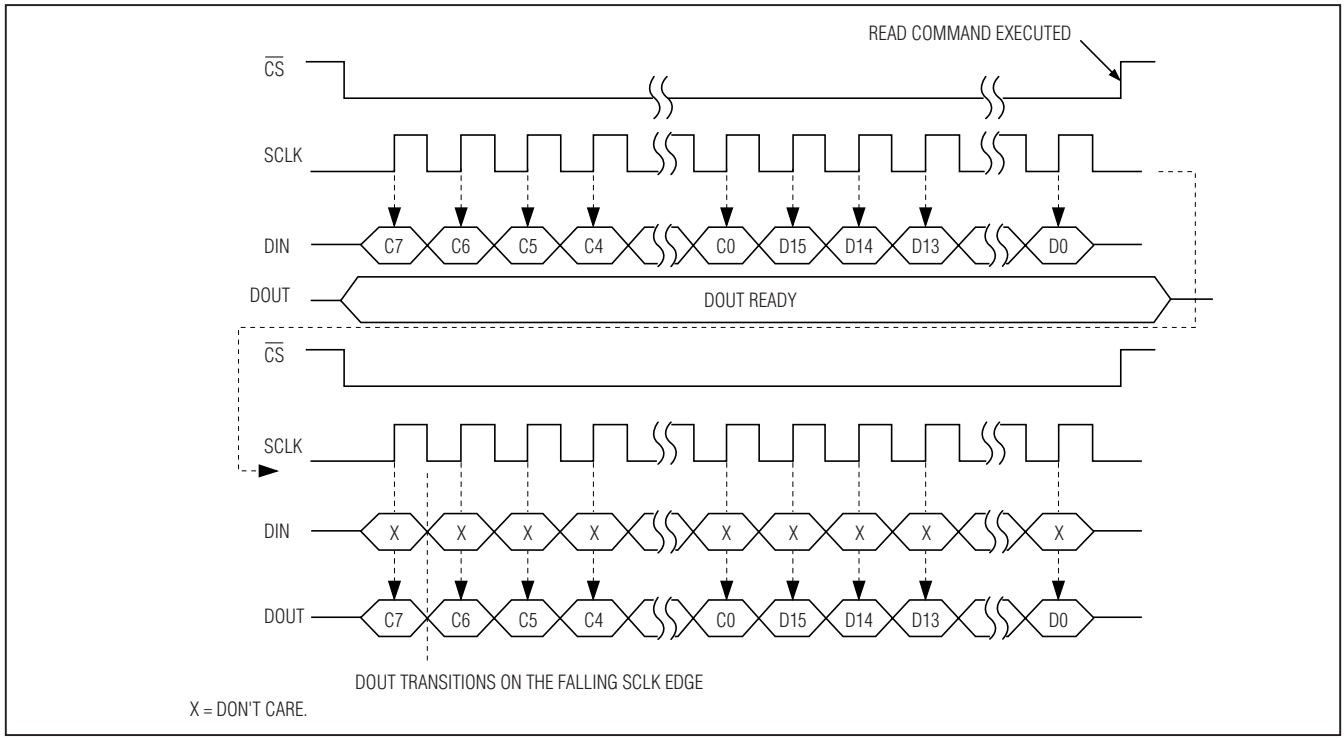

Figure 5. Read Timing

Set the OUTI4/$\overline{0}$EN bit (D11) low to enable the OUTI4/$\overline{0}$ hardware input. Set the I4TO20BIT bit (D10) high to select the current-output range through the software. Set the $\overline{CLREN}$ bit (D9) low to enable the $\overline{CLR}$ hardware input. Set the CLRMODE bit (D8) high to force the output to the value in the clear register or the zero state when the $\overline{CLR}$ hardware input is pulled low. Set the RCLR bit (D7) high to remain in the clear state. Set the FAULTEN bit (D6) high to enable the $\overline{FAULT}$ output functionality. Set the CLRFLAGEN bit (D5) high to activate the $\overline{FAULT}$ output when the MAX5661 is in the clear state.

Bits D4, D3, and D2 are read-only bits. The FAULTV bit (D4) is set to 1 when OUTV is short circuited. The FAULTI bit (D3) is set to 1 when OUTI is open circuited. The CLEARST bit (D2) is set to 1 when the MAX5661 is in the clear state.

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Table 4. Control Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
OUTVON	D15	0	DAC OUTV output enable bit. Set to 1 to enable the OUTV output.
OUTION	D14	0	DAC OUTI output enable bit. Set to 1 to enable the OUTI output.
—	D13	0	Reserved. Always set to 0.
$\overline{B}$/U	D12	0	Voltage-output unipolar/bipolar mode select bit. Set to 0 (default power-up state) to select the bipolar output range (±10.48V). Set to 1 to select the unipolar output range (0 to +10.48V).
OUTI4/$\overline{0}$EN	D11	0	OUTI4/$\overline{0}$ enable bit. Set to 0 (default power-up state) to enable the OUTI4/$\overline{0}$ hardware input. Set to 1 to disable the OUTI4/$\overline{0}$ hardware input, thereby controlling the current-output range through software commands.
I4TO20BIT	D10	0	OUTI current range bit. Set to 0 to set the OUTI current range from 0 to 20mA. Set to 1 to set the OUTI current range from 4–20mA.
$\overline{CLREN}$	D9	0	Clear enable bit. Set to 0 to enable the external $\overline{CLR}$ input. Set to 1 to disable the external $\overline{CLR}$ input.
CLRMODE	D8	0	Clear mode bit. Set to 1 and drive the external $\overline{CLR}$ input low to force the DAC output to the value stored in the clear register. Set to 0 and drive the external $\overline{CLR}$ input low to force the DAC output to 0V in voltage mode or 0mA/4mA depending on output-current mode.
RCLR	D7	0	Remain in clear bit. Set to 1 to remain in the clear state. The RCLR bit determines the steps required to exit the clear state. See the *$\overline{CLR}$ Input* section.
FAULTEN	D6	0	Fault output enable. Set to 1 to enable the $\overline{FAULT}$ output functionality. Set to 0 to disable the $\overline{FAULT}$ output functionality. In single supply mode, set to 0 to disable the $\overline{FAULT}$ pin function.
CLRFLAGEN	D5	0	Clear flag enable. Set to 1 to enable the $\overline{FAULT}$ output to report when the device is in the clear state.
FAULTV	D4	0	Output voltage fault bit (read only). The FAULTV bit is set to 1 when $\overline{FAULT}$ triggers due to an OUTV short-circuit condition. The FAULTV bit is a don't-care bit for control-register write commands. In single supply mode, FAULTV = 1 must be ignored.
FAULTI	D3	0	Output-current fault bit (read only). The FAULTI bit is set to 1 when $\overline{FAULT}$ triggers due to an OUTI open-circuit condition. The FAULTI bit is a don't-care bit for the control register write commands. In single supply mode, monitor the FAULTI bit for any FAULTI condition.
CLEARST	D2	0	Clear state bit (read only). The CLEARST bit is set to 1 when $\overline{CLR}$ is low and CLREN = 0. The CLRST bit is a don't-care bit for control register write commands.
X	D1, D0	0	Not used.

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Input Register (Read/Write)

Write to the input register to store the DAC code. Transfer the value written to the input register to the DAC register by pulling the $\overline{LDAC}$ input low or by writing to the load DAC register (0x05). Set the command byte to 0x03 to write to the input register. Set the command byte to 0x07 to read from the input register. Bits D15–D0 contain the straight binary data (see Table 5).

DAC Register (Read/Write)

Write to the DAC register to update the OUTV and OUTI outputs after $\overline{CS}$ returns high. Set the command byte to 0x04 to write to the DAC register. Set the command byte to 0x08 to read from the DAC register. Bits D15–D0 contain the straight binary data (see Table 6).

Load DAC Register (Write)

Write to the load DAC register to transfer the input register data to the DAC register and update the DAC output. Set the command byte to 0x05 to write to the load DAC register. Bits D15–D0 are don't-care bits.

Clear Register (Read/Write)

Write to the clear register to set the DAC output value when the $\overline{CLR}$ hardware input is pulled low (forcing the MAX5661 into the clear state). Set the command byte to 0x06 to write to the clear register. Set the command byte to 0x09 to read the clear register. Bits D15–D0 contain the straight binary data (see Table 7).

No Operation

Set the command byte to 0x0F or 0x00 to perform a no-operation command. After writing the command byte and 2 data bytes (16 don't-care bits), read out the shift register's contents on the following 24-bit cycle.

Table 5. Input Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
IN15–IN0	D15–D0	0000 0000 0000 0000 (unipolar/current) 1000 0000 0000 0000 (bipolar)	IN15 is the MSB and IN0 is the LSB. Data format is straight binary.

Table 6. DAC Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
DAC15–DAC0	D15–D0	0000 0000 0000 0000 (unipolar/current) 0000 0000 0000 0000 (bipolar)	DAC15 is the MSB and DAC0 is the LSB. Data format is straight binary.

Table 7. Clear Register (Read/Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
CLR15–CLR0	D15–D0	0000 0000 0000 0000 (unipolar/current) 1000 0000 0000 0000 (bipolar)	CLR15 is the MSB and CLR0 is the LSB. Data format is straight binary.

Table 8. Full-Scale Output Trim Register (Write)

BIT NAME	DATA BIT	RESET STATE	FUNCTION
FS_EN + FS_BIT9–FS_BIT0	D9–D0	0000 0000 0000 0000	FS_EN (D15) enables the full-scale output adjustment feature. D9 is the MSB and D0 is the LSB. D9 is straight binary, D8–D0 are inverted binary.

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Full-Scale Output Current Trim Register (Write)

Write to the full-scale output trim register to adjust the output voltage or current ±25%. Set command bits to 0x06 to write to the output trim register. Bit 15 enables the output trim register. Bits D9–D0 program the 10-bit trim DAC (Table 8).

Table 9. N to D: Full-Scale Output Trim Register Bits Map

N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
D9	$\overline{D8}$	$\overline{D7}$	$\overline{D6}$	$\overline{D5}$	$\overline{D4}$	$\overline{D3}$	$\overline{D2}$	$\overline{D1}$	$\overline{D0}$

Table 10. Full-Scale Output Variation vs. N and B

DECIMAL VALUE (N)	BIT DECIMAL VALUE (B)	% CHANGE
0	511	-25
256	255	-12.5
511	0	0^-
512	1023	0^+
767	768	+12.5
1023	512	+25

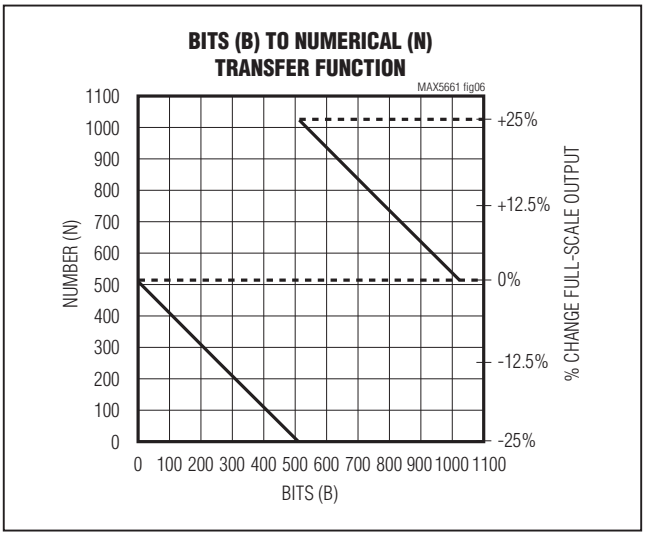

Figure 6. Transfer Function of Bits (B) to Numerical (N) Representation

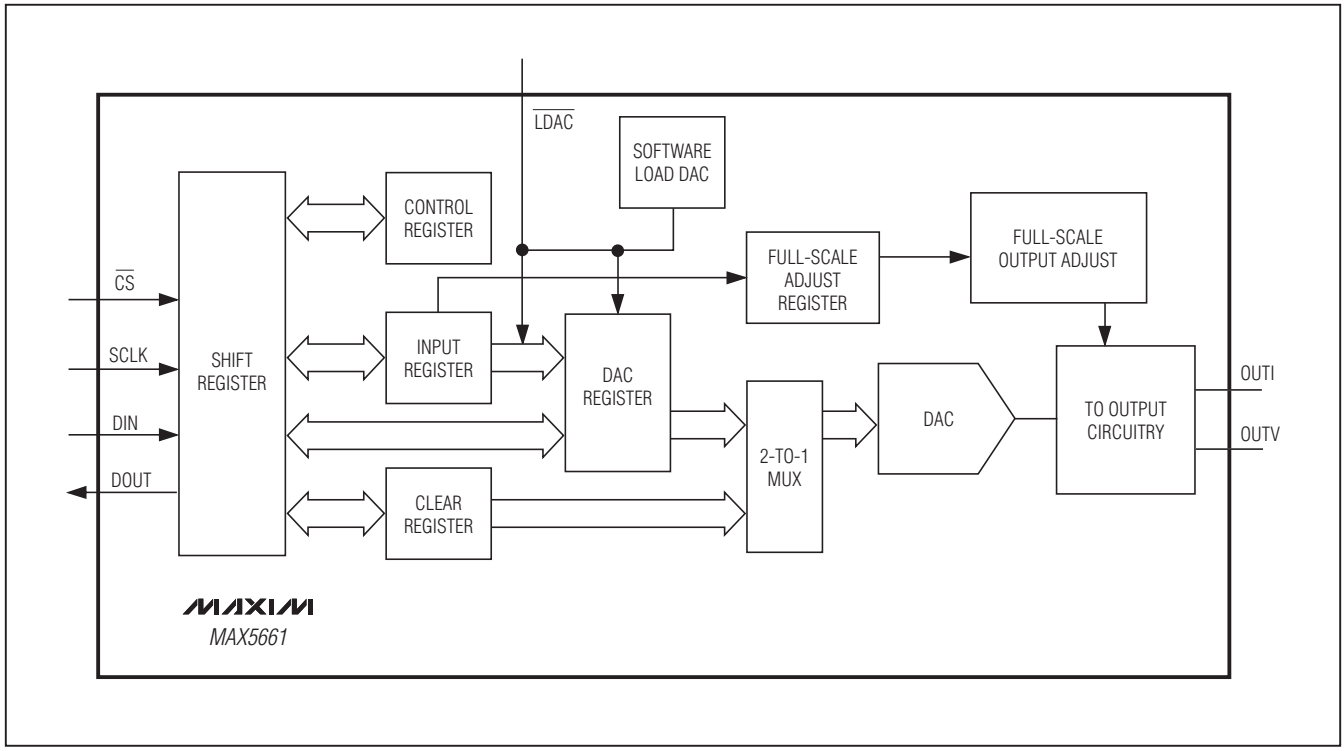

Figure 7. Functional Diagram

Reference Input

Connect an external voltage reference in the +4V to +4.2V range through a 1kΩ series resistor to the buffered REF input. Use a high-accuracy, low-noise +4.096V voltage reference such as the MAX6126AASA41 (3ppm/°C temperature drift and 0.02% initial accuracy) for best 16-bit static accuracy. REF does not accept AC signals. See Table 17 for a listing of +4.096V references.

$\overline{\text{LDAC}}$ Input

The MAX5661 features an active-low load DAC ($\overline{\text{LDAC}}$) logic input that allows asynchronous updates to the DAC outputs. Drive $\overline{\text{LDAC}}$ high to V_{CC} during normal operation while controlling the MAX5661 using only the serial interface. Drive $\overline{\text{LDAC}}$ low to update the DAC output with the input register data. Hold $\overline{\text{LDAC}}$ low to make the input register transparent and immediately update the DAC output with the input register data. Figure 8 shows the $\overline{\text{LDAC}}$ timing with respect to OUT_.

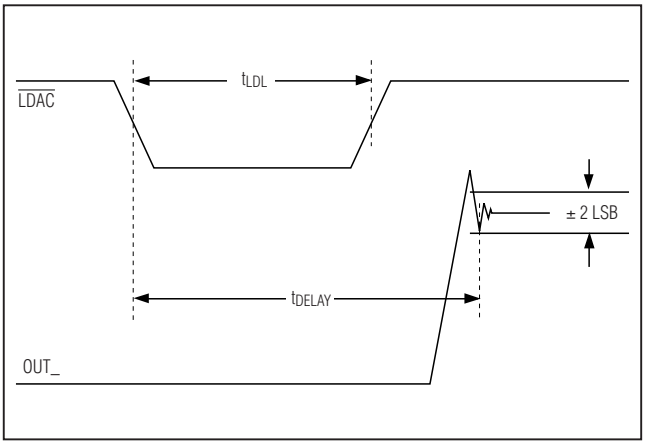

Figure 8. $\overline{\text{LDAC}}$ Timing

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$\overline{CLR}$ Input

The active-low external $\overline{CLR}$ input asynchronously sets the DAC code to the value in the clear register (software clear) or to the zero state (hardware clear), depending on the control register's CLRMODE bit setting (see Tables 4 and 11). Set the CLRMODE bit to 1 and drive external $\overline{CLR}$ low to force the output to the value stored in the clear register. Set the CLRMODE bit to 0 and drive the external $\overline{CLR}$ input low to force the output to the zero state. The zero state value is 0mA in 0 to 20mA current mode, 3.97mA in 4–20mA current mode, or 0V in voltage mode (unipolar or bipolar).

Disable the external $\overline{CLR}$ input functionality by setting the control register's $\overline{CLREN}$ bit to 1. Set the $\overline{CLREN}$ bit to 0 to enable the external $\overline{CLR}$ input functionality.

After setting the $\overline{CLREN}$ bit to 0, force the external $\overline{CLR}$ input low to set the MAX5661 into the clear state. The control register's read-only CLEARST bit is set to 1 while in the clear state. The RCLR (remain in clear) bit determines the steps required to exit the clear state.

With the RCLR bit set to 1, exit the clear state in one of three ways:

1) Pull the external $\overline{CLR}$ input high and then write to the DAC register (0x04) or the load DAC register (0x05) or force $\overline{LDAC}$ low.
2) Pull the external $\overline{CLR}$ input high and set the RCLR bit low.
3) Initiate a power-on reset (POR) to reset the RCLR bit to 0.

With the RCLR bit set to 0, exit the clear state one of three ways:

1) Set the $\overline{CLREN}$ bit high.
2) Pull the external $\overline{CLR}$ input high.
3) Initiate a power-on reset (POR).

$\overline{FAULT}$ Output

The open-drain active-low $\overline{FAULT}$ output asserts low for a current-output open circuit or dropout condition, for a voltage-output short circuit, or when the MAX5661 is in the clear state (see the *$\overline{CLR}$ Input* section).

Enable and disable the $\overline{FAULT}$ output with the control register's FAULTEN and CLRFLAGEN bits (see Tables 4, 12, and Figure 9). Set the FAULTEN bit to 1 to enable the $\overline{FAULT}$ output to report fault conditions on OUTV and OUTI. Set FAULTEN to 0 to disable the $\overline{FAULT}$ output for fault conditions on OUTV and OUTI. Set the CLRFLAGEN bit to 1 to enable the $\overline{FAULT}$ output to report when the device is in the clear state. Set CLRFLAGEN to 0 to disable a hardware indication of the clear state. The $\overline{FAULT}$ output asserts low if CLRFLAGEN = 1 and CLEARST = 1.

Read the control register to determine the source of a $\overline{FAULT}$ output condition. The FAULTV read-only bit is set to 1 when the voltage output (OUTV) is short-circuited. The FAULTI bit is set to 1 when the current output (OUTI) is open circuited or in a dropout condition (V_{DDI} - V_{OUTI} at 1.3V typ). The $\overline{FAULT}$ output asserts low if FAULTEN is set to 1 and either the FAULTV bit or FAULTI bit is set to 1.

Table 11. Hardware-Clear and Software-Clear Truth Table

CLEARST BIT (READ)	CLRMODE BIT (READ/WRITE)	HARDWARE CLEAR	SOFTWARE CLEAR
0 (not in clear state)	X	X	X
1 (in clear state)	0	DAC code set to zero state*	—
1 (in clear state)	1	—	DAC code set by clear register data

X = Don't care.

**Zero state is 0V in unipolar voltage mode, -10.48V in bipolar voltage mode, and 0mA/4mA depending on output-current mode.*

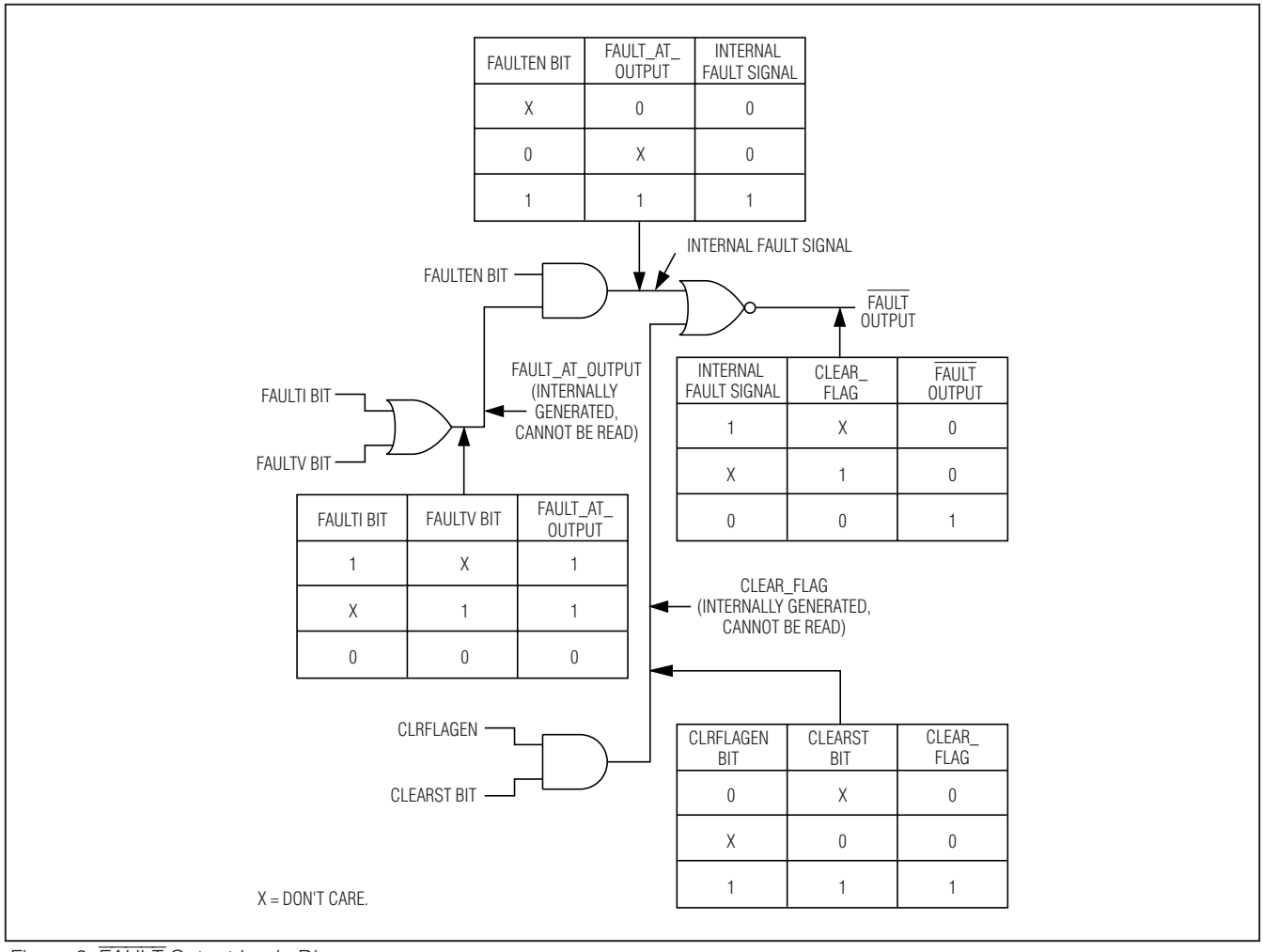

Figure 9. FAULT Output Logic Diagram

Table 12. FAULT Output Truth Table

OUTV SHORT CIRCUITED	OUTI OPEN CIRCUITED OR IN DROPOUT	CLEARST BIT	FAULTEN BIT	CLRFLAGEN BIT	FAULT OUTPUT
No	No	0	X	X	High
No	No	X	X	0	High
X	X	1	X	1	Low
X	X	0	0	X	High
No	Yes	X	1	X	Low
X	X	X	0	0	High
Yes	No	X	1	X	Low

X = Don't care. Only one output (OUTV or OUTI) is active at a time.

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Output Configurations

The CNF0, CNF1, and OUTI4/$\overline{0}$ hardware inputs determine whether the hardware or software controls the MAX5661 DAC outputs (see Table 13). The CNF0 and CNF1 inputs enable and disable the DAC outputs or allow software control of the outputs (see Table 14). The OUTI4/$\overline{0}$ input sets the current range of the OUTI output. Hardware inputs take precedence over the software commands.

The V_{CC} digital supply powers the CNF1, CNF0, and OUTI4/$\overline{0}$ inputs. If V_{CC} = 0V, the DAC outputs enter the zero state and all register bits are set to 0. The zero state of the voltage output (OUTV) is 0V. The zero state of the current output (OUTI) is 0mA when OUTI4/$\overline{0}$ = AGND or 4mA when OUTI4/$\overline{0}$ = V_{DDI}.

Table 13. Output Configuration

CONTROL SIGNAL	HARDWARE INPUT/SOFTWARE BIT	DESCRIPTION	DETAILS
CNF1	Hardware input	Enables/disables the DAC OUTV and OUTI outputs.	CNF1, CNF0: 00 = both outputs disabled 01 = OUTI active, set to 0 to 20mA range 10 = OUTV active, set to bipolar mode 11 = outputs controlled by serial interface
CNF0	Hardware input		
OUTI4/$\overline{0}$	Hardware input	Sets the OUTI current range.	Set the OUTI4/$\overline{0}$EN bit to 0 (default power-up state) to enable the OUTI4/$\overline{0}$ hardware input. Connect the OUTI4/$\overline{0}$ hardware input to AGND to set the OUTI current range to 0 to 20mA. Connect the OUTI4/$\overline{0}$ hardware input to V_{DDI} to set the OUTI current range to 4–20mA. Set the OUTI4/$\overline{0}$EN bit to 1 to disable the OUT14/$\overline{0}$ hardware input. Connect OUTI4/$\overline{0}$ to AGND when controlling the current output through software.
OUTI4/$\overline{0}$EN	Software bit	Enables and disables the OUTI4/$\overline{0}$ input.	Set the OUTI4/$\overline{0}$EN bit to 0 (default power-up state) to enable the OUTI4/$\overline{0}$ hardware input. Set to 1 to disable the OUTI4/$\overline{0}$ hardware input.
OUTVON	Software bit	Enables and disables the DAC OUTV and OUTI outputs.	When the CNF1 and CNF0 hardware inputs are high, the OUTION and OUTVON bits control the DAC output OUTI and OUTV settings. OUTVON, OUTION: 00 = both outputs powered down 01 = OUTI active 10 = OUTV active 11 = both outputs powered down
OUTION	Software bit		
$\overline{B}$/U	Software bit	Sets the voltage output to unipolar mode or bipolar mode.	Set $\overline{B}$/U to 0 to set the OUTV output to bipolar mode (±10.48V). Set $\overline{B}$/U to 1 to set the OUTV output to unipolar mode (0 to +10.48V).
I4TO20BIT	Software bit	Sets the OUTI current range through software.	Set I4TO20BIT to 0 to set the OUTI current range from 0 to 20mA. Set I4TO20BIT to 1 to set the OUTI current range from 4–20mA.

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CNF0/CNF1 Hardware Inputs

The CNF0 and CNF1 inputs enable the DAC's voltage (OUTV) or current (OUTI) outputs. Drive CNF0 and CNF1 low to disable both the OUTV and OUTI outputs. Drive CNF0 high and CNF1 low to enable the OUTI output. Drive CNF0 low and CNF1 high to enable the OUTV output. Drive CNF0 and CNF1 high to control the OUTV and OUTI outputs through the serial interface. Table 14 summarizes the output behavior when programmed by the CNF0/CNF1 hardware inputs.

OUTI Current-Output Configuration

Drive CNF0 high and CNF1 low to enable the OUTI output through the hardware. Alternatively, drive CNF0 and CNF1 high to control OUTI with the serial interface. With CNF1 and CNF0 high, the control register's OUTION bit enables the OUTI output. Set OUTION to 1 to enable the OUTI output. Set OUTION to 0 (default power-up state) to disable the OUTI output.

The OUTI current output derives power from V_{DDI} and V_{DDCORE} (+13.48V to +40V). Connect V_{DDCORE} to V_{DDI} when using the OUTI output.

The control register's OUTI4/$\overline{0}$EN bit (see Tables 4 and 13) determines whether the OUTI4/$\overline{0}$ hardware input or the control register's I4TO20BIT bit controls the OUTI current range. Set the OUTI4/$\overline{0}$EN bit to 0 (default power-up state) to control the current range through the OUTI4/$\overline{0}$ hardware input. Connect the OUTI4/$\overline{0}$ hardware input to AGND to select the 0 to 20mA mode. Connect the OUTI4/$\overline{0}$ hardware input to V_{DDI} to select the 4–20mA mode.

Set the OUTI4/$\overline{0}$EN bit to 1 to allow software control of the OUTI current range through the I4TO20BIT bit (see Table 13). Set I4TO20BIT to 0 to select the 0 to 20mA mode. Set I4TO20BIT to 1 to select the 4–20mA mode.

OUTV Voltage-Output Configuration

Drive CNF0 low and CNF1 high to enable the OUTV output through the hardware (see Table 14). Alternatively, drive CNF0 and CNF1 high to control OUTV with the serial interface. With CNF1 and CNF0 high, the control register's OUTVON bit enables the OUTV output. Set OUTVON to 1 to enable the OUTV output. Set OUTVON to 0 (default power-up state) to disable the OUTV output.

The OUTV output derives power from V_{DDV}, V_{SSV}, and V_{DDCORE}. Connect V_{DDCORE} to V_{DDV} (+13.48V to +15.75V) when using the OUTV output. Always connect a negative supply to V_{SSV} (-13.48V to -15.75V) (see Table 16).

The control register's $\overline{B}$/U bit sets OUTV for bipolar or unipolar mode. Set $\overline{B}$/U to 0 (default power-up state) to select the bipolar output range (±10.48V). Set $\overline{B}$/U to 1 to select the unipolar output range (0 to +10.48V).

Output Transfer Functions

The DAC output voltage/current is a function of the various hardware control inputs and digital inputs in the control register (see Table 13). The transfer functions below assume that the outputs are on, and a reference voltage of +4.096V is applied to the reference input. For the voltage output, the sense input is at the same potential as the DAC output (OUTV = SVP and AGND = SVN). Table 15a details the bipolar output voltage transfer function. Table 15b details the unipolar output voltage transfer function. Table 15c details the 0 to 20mA current-range transfer function. Table 15d details the 4mA to 20mA current-range transfer function.

Table 14. CNF1/CNF0 Hardware Settings

CNF1	CNF0	OUTV, OUTI SETTING
DGND	DGND	Both DAC outputs disabled.
DGND	V_{CC}	OUTI enabled. OUTV disabled.
V_{CC}	DGND	OUTV enabled. OUTI disabled.
V_{CC}	V_{CC}	DAC outputs controlled by the serial interface.

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Table 15a. Bipolar Voltage Output

DAC CODE (DECIMAL VALUE)	OUTPUT VOLTAGE (V)	RANGE
65535	10.47984	Overrange
64769	10.23485	Overrange
64768	10.23453	Nominal range
64767	10.23421	Nominal range
48769	5.117585	Nominal range
48768	5.117266	Nominal range
48767	5.116946	Nominal range
35969	1.023773	Nominal range
35968	1.023453	Nominal range
35967	1.023133	Nominal range
32769	0.00032	Nominal range
32768	0	Nominal range
32767	-0.00032	Nominal range
29569	-1.02313	Nominal range
29568	-1.02345	Nominal range
29567	-1.02377	Nominal range
16769	-5.11695	Nominal range
16768	-5.11727	Nominal range
16767	-5.11759	Nominal range
769	-10.2342	Nominal range
768	-10.2345	Nominal range
767	-10.2349	Underrange
0	-10.4802	Underrange

Table 15b. Unipolar Voltage Output

DAC CODE (DECIMAL VALUE)	OUTPUT VOLTAGE (V)	RANGE
65535	10.48	Overrange
64001	10.23469	Overrange
64000	10.23453	Nominal range
32001	5.117425	Nominal range
32000	5.117266	Nominal range
31999	5.117106	Nominal range
6401	1.023613	Nominal range
6400	1.023453	Nominal range
6399	1.023293	Nominal range
1	0.00016	Nominal range
0	0	Nominal range

Table 15c. 0 to 20mA Current Output

DAC CODE (DECIMAL)	ACTUAL OUTPUT CURRENT (mA)	RANGE	EXTENSION OF OUTPUT CURRENT LINEAR RANGE (mA)
65535	20.449688	Overrange	20.449688
64001	19.970313	Overrange	19.970313
64000	19.970000	Nominal range	19.970000
63999	19.969688	Nominal range	19.969688
32001	9.970313	Nominal range	9.970313
32000	9.970000	Nominal range	9.970000
31999	9.969688	Nominal range	9.969688
12801	3.970313	Nominal range	3.970313
12800	3.970000	Nominal range	3.970000
12799	3.969688	Nominal range	3.969688
97	0.000313	Nominal range	0.000313
96	0.000000	Nominal range	0.000000
95	0.000000	Underrange	-0.000313
80	0.000000	Underrange	-0.005000
60	0.000000	Underrange	-0.011250
40	0.000000	Underrange	-0.017500
30	0.000000	Underrange	-0.020625
0	0.000000	Underrange	-0.030000

Table 15d. 4–20mA Current Output

DAC CODE (DECIMAL)	OUTPUT CURRENT (mA)	RANGE
65535	20.449688	Overrange
64000	20.063690	Overrange
63634	19.971655	Nominal range
60000	19.057835	Nominal range
50000	16.543196	Nominal range
40000	14.028556	Nominal range
30000	11.513917	Nominal range
20000	8.999278	Nominal range
16000	7.993423	Nominal range
5000	5.227320	Nominal range
500	4.095732	Nominal range
238	4.029848	Nominal range
200	4.020293	Underrange
100	3.970000	Underrange
80	3.970000	Underrange
60	3.970000	Underrange
30	3.970000	Underrange
0	3.970000	Underrange

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Measuring Zero-Code Current (0 to 20mA Mode)

After setting the MAX5661 for 0 to 20mA current-range mode, determine the LSB size as follows:

1) Measure I_{OUT} at full scale (FS).

2) Measure I_{OUT} at code 192.

3) Measure I_{OUT} at code 193:

$$I_{LSB} = \frac{I_{OUT}\ \text{at FS} - I_{OUT}\ \text{at 192}}{(2^{16} - 1) - 192}$$

If I_{OUT} (code 193) - I_{OUT} (code 192) > 0.5 I_{LSB}, I_{OUT} (code 192) is inside the linear region of the I_{OUT} transfer curve.

Obtain the straight-line equation from I_{OUT} (FS) and I_{OUT} (192) and substituting code 0 for I_{OUT} (zero scale) in the equation:

$$(I - I_{OUT}\ \text{at 192}) = \left(\frac{I_{OUT}\ \text{at FS} - I_{OUT}\ \text{at 192}}{65535 - 192}\right) \times (\text{code} - 192)$$

$$I_{OUT}\ \text{at ZS} = (I_{OUT}\ \text{at 192} - I_{OUT}\ \text{at FS}) \times 0.0029383 + I_{OUT}\ \text{at 192}$$

The expected current is -30µA (typ).

Applications Information

Power-Supply Sequencing and Bypassing

After connecting all ground inputs, apply the analog supply voltages V_{SSV} first followed by the most positive supply, the second most positive supply, etc. Before applying power, connect the V_{DDCORE} supply to either V_{DDV} or V_{DDI}, as shown in Table 16, depending on whether the current output or voltage output is used. Do not apply V_{DDCORE} separate from the main supply (V_{DDV}/V_{SSV} or V_{DDI}) in the preferred configuration (Table 16). Ensure that there are no unconnected power-supply connections when powering the MAX5661. If V_{SSV} cannot be powered first, connect a Schottky diode between V_{SSV} and AGND.

Daisy Chaining Multiple MAX5661 Devices

In standard SPI-/QSPI-/MICROWIRE-compatible systems, a microcontroller (µC) communicates with its slave devices through a 3- or 4-wire serial interface. The typical interface includes a chip select signal ($\overline{CS}$), a serial clock (SCLK), a data input signal (DIN), and sometimes a data signal output (DOUT). In this system, the µC allots an independent chip-select signal to each slave device so that they can be addressed individually (see Figure 10). Only the slaves with their $\overline{CS}$ inputs asserted low acknowledge and respond to the activity on the serial clock and data lines. This is simple to implement when there are very few slave devices in the system. An alternative programming method is daisy chaining. Daisy chaining, in serial-interface applications, is a method of propagating commands through multiple devices connected in series (see Figure 11). Daisy chaining reduces $\overline{CS}$ and DIN line routing, and saves board space when using the MAX5661.

Daisy chain multiple MAX5661 devices by connecting the DOUT of one device to the DIN of the next. Connect the SCLK of all devices to a common clock and connect the $\overline{CS}$ from all devices to a common chip-select line. Data shifts out of DOUT 24.5 clock cycles after it is shifted into DIN on the falling edge of SCLK. Hold $\overline{CS}$ low until each slave in the chain receives its 24-bit word (8 command bits and 16 data bits). In this configuration, the µC only needs three signals ($\overline{CS}$, SCLK, and DIN) to control all the slaves in the network. The SPI-/QSPI-/MICROWIRE-compatible serial interface normally works at up to 10MHz, but must be slowed to 6MHz if daisy chaining. DOUT is high impedance when $\overline{CS}$ is high.

Figure 10 details a method of controlling multiple MAX5661 devices using separate $\overline{CS}$ lines. This method allows writes to and reads from each device without shifting data through the other device's shift register. Figure 10 shows the $\overline{FAULT}$ outputs shorted together. This configuration requires a read from each device to determine which one has the fault condition and saves an optocoupler in isolated applications. It is not necessary to short the $\overline{FAULT}$ outputs together.

Table 16. Application Modes and Supply-Voltage Limits

APPLICATION MODE	V_{DDV}	V_{SSV}	V_{DDI}	V_{DDCORE}
Voltage from OUTV	+13.48V to +15.75V	-13.48V to -15.75V	V_{DDV}	V_{DDV}
Current from OUTI (Single Supply)	AGND	AGND	+13.48V to +40V	V_{DDI}
Voltage from OUTV and Current from OUTI*	+13.48V to +15.75V	-13.48V to -15.75V	V_{DDV} to +40V	V_{DDV}

**On-the-fly switching. Only one output is active at a time.*

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Figure 11 shows a method of daisy chaining multiple MAX5661 devices using a single $\overline{CS}$ and SCLK line with the $\overline{FAULT}$ outputs shorted together. Connect DOUT from IC1 to DIN of IC2, and DOUT from IC2 to DIN of IC3. Hold $\overline{CS}$ low for three 24-bit write cycles to load data into all three devices. Due to the latency of reading and writing to the different devices, using separate lines for each $\overline{FAULT}$ output does not save time.

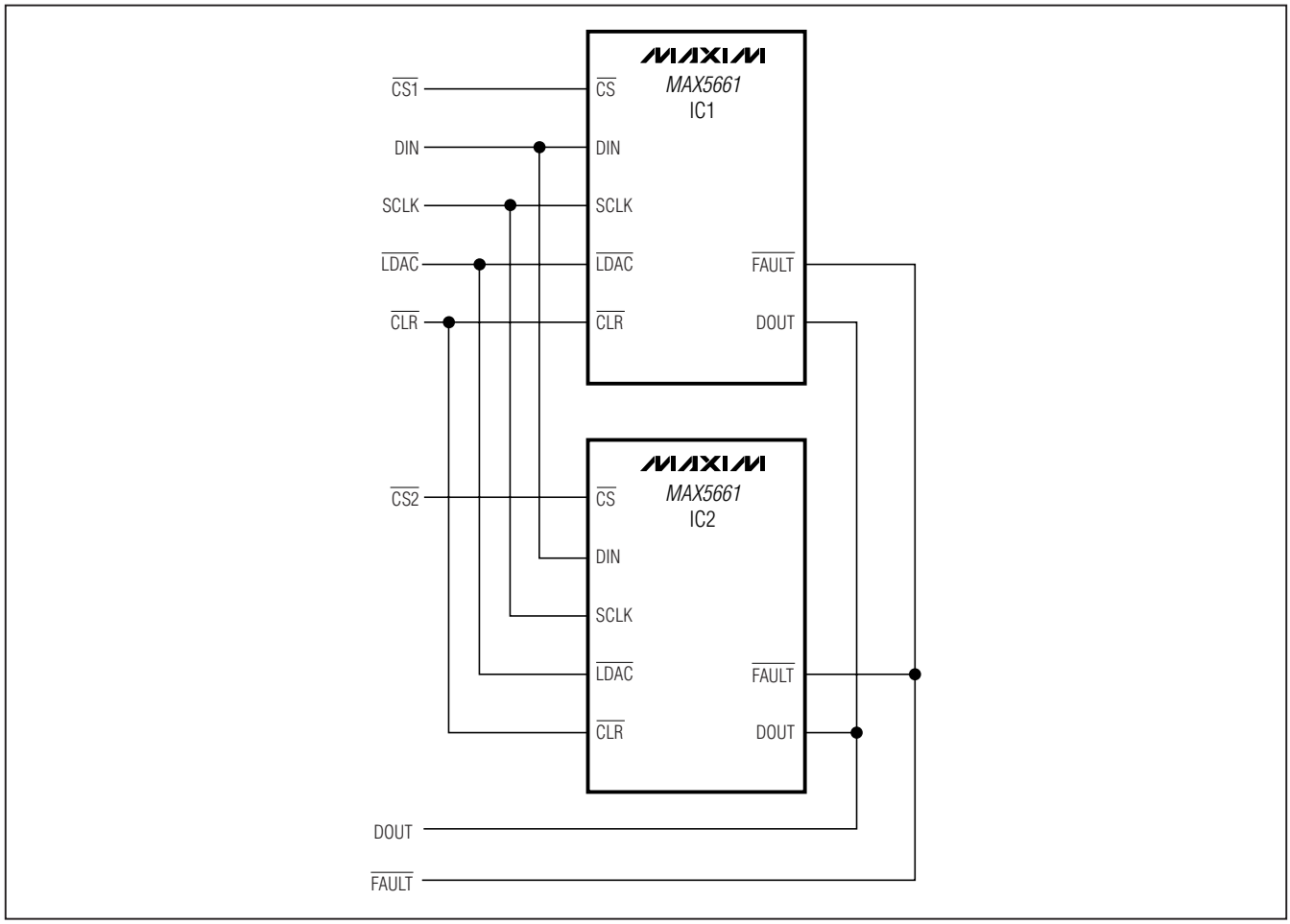

Figure 10. Address Two MAX5661 Devices Through Separate $\overline{CS}$ Lines

Driving Inductive Loads from I_{OUT}

When driving inductive loads > 275µH with the current output (I_{OUT}), connect a 1nF capacitor between V_{DDI} and I_{OUT} for optimal performance.

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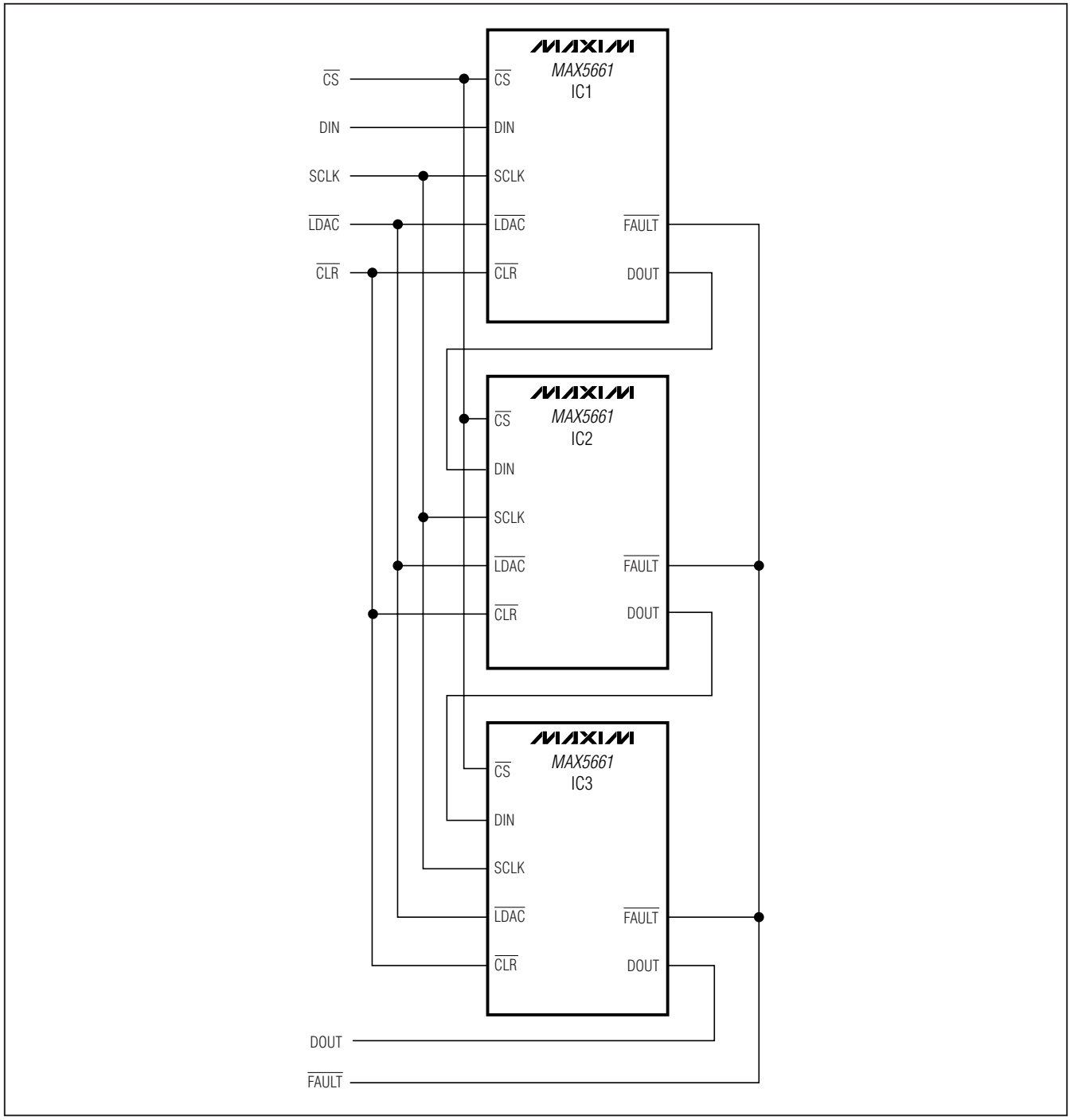

Figure 11. Address Three MAX5661 Devices Through Separate $\overline{CS}$ Lines

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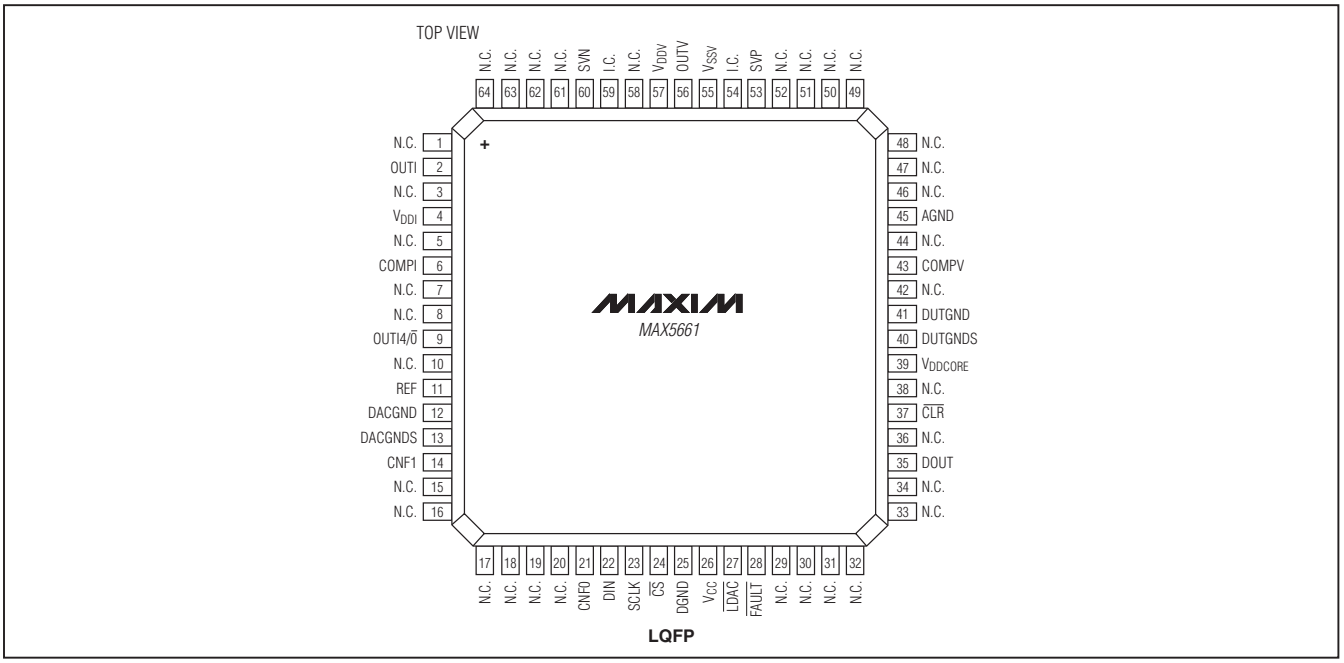
Table 17. +4.096V Reference Selector Guide

PART	SUPPLY VOLTAGE RANGE (V)	TEMPERATURE DRIFT (ppm/°C max)	INITIAL ACCURACY (%)	FEATURES
MAX6341	+8 to +36	1	0.02	Ultra-low drift, 2.4µV_{P-P} output noise
MAX6241	+8 to +36	3	0.02	Low drift, 2.4µV_{P-P} output noise
MAX6174	+4.3 to +40	3	0.06	High-precision reference with temperature sensor
MAX6133_41	+4.3 to +12.6	3	0.04	Ultra-low drift, µMAX®
MAX6126_41	+4.3 to +12.6	3	0.02	Ultra-low noise, µMAX
MAX6043_41	+6 to +40	3	0.05	High voltage, low drift
MAX6143_41	+6 to +40	8	0.1	High precision
MAX6033_41	+4.3 to +12.6	10	0.04	10mA output current, ultra-low drift, SOT23
MAX6041	+4.3 to +12.6	20	0.2	Low power, low drift, low dropout
MAX6064	+4.3 to +12.6	20	0.2	5mA current output, precision SOT23
MAX6220	+8 to +40	20	0.1	-40°C to +125°C, 15mA output
MAX6037_41	+4.3 to +5.5	25	0.2	SOT23 with shutdown
MAX6034_41	+4.3 to +5.5	30	0.2	Low supply current in SC70
MAX6029	+4.3 to +12.6	30	0.15	Ultra-low supply current, SOT23

Chip Information

PROCESS: BiCMOS

Pin Configuration



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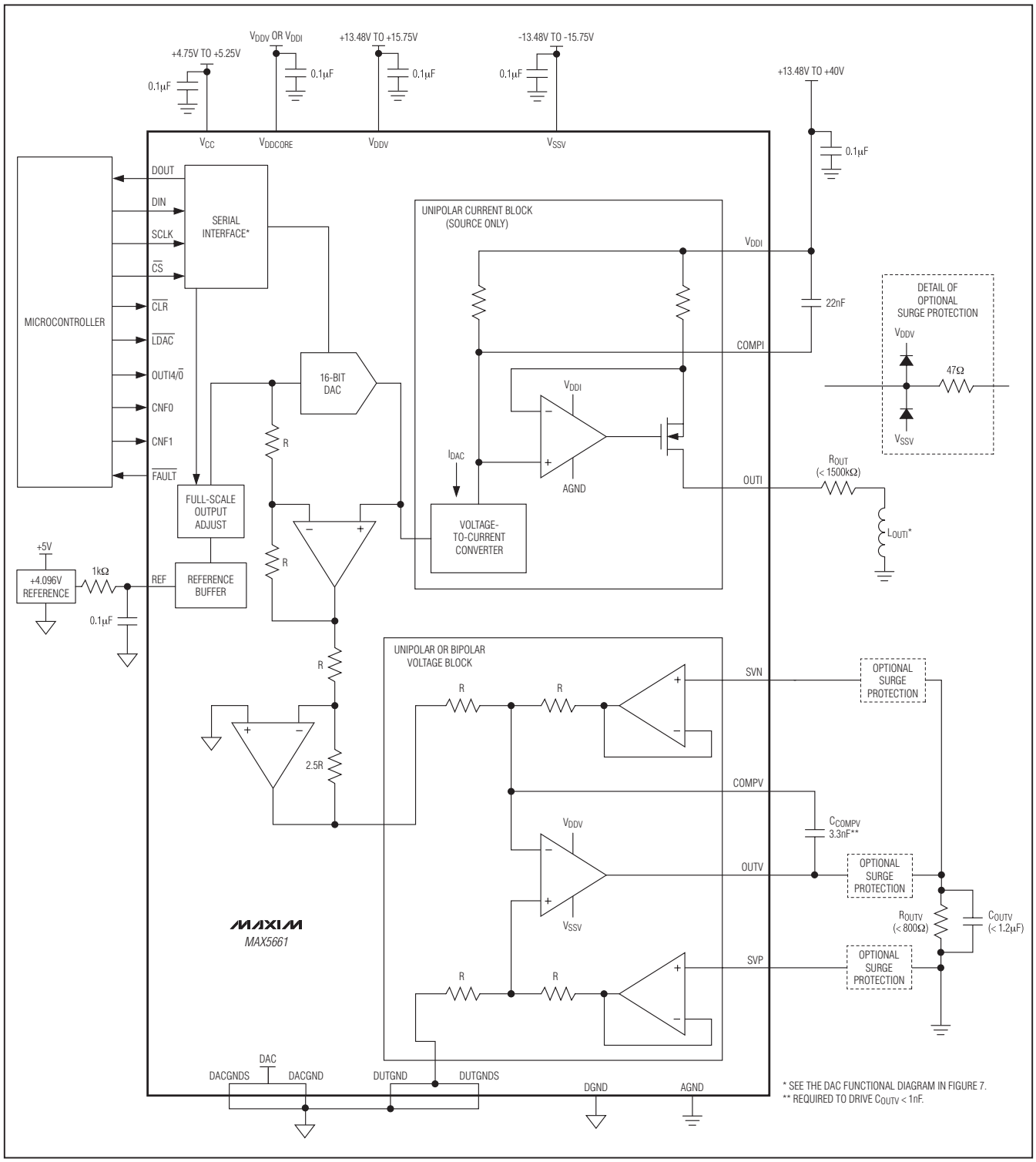
Typical Operating Circuit



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
64 LQFP	C64-8	**21-0083**

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/08	Initial release	—
1	5/09	Clarified how the part operates in single supply mode	18, 24

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