19-2124; Rev 2; 7/03

12-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

General Description

The MAX5722 dual,12-bit, low-power, buffered voltage-output, digital-to-analog converter (DAC) is packaged in a space-saving 8-pin µMAX package (5mm × 3mm). The wide supply voltage range of +2.7V to +5.5V and 112µA supply current accommodates low-power and low-voltage applications. DAC outputs employ on-chip precision output amplifiers that swing Rail-to-Rail®. The MAX5722's reference input accepts a voltage range from 0 to V_{DD}. In power-down, the reference input is high impedance, further reducing the system's total power consumption.

The 20MHz, 3-wire SPI™, QSPI™, MICROWIRE™, and DSP-compatible serial interface save board space and reduce the complexity of opto- and transformer-isolated applications. The MAX5722 on-chip power-on reset (POR) circuit resets the DAC outputs to zero and loads the output with a 100kΩ resistor to ground. This provides additional safety for applications that drive valves or other transducers that need to be off on power-up. The MAX5722's software-controlled power-down reduces supply current to less than 0.3µA and provides software-selectable output loads (1kΩ, 100kΩ, or high impedance) while in power-down. The MAX5722 is specified over the -40°C to +125°C automotive temperature range.

Applications

Automatic Tuning

Gain and Offset Adjustment

Power Amplifier Control

Process Control I/O Boards

Battery-Powered Instruments

VCO Control

Functional Diagram appears at end of data sheet.

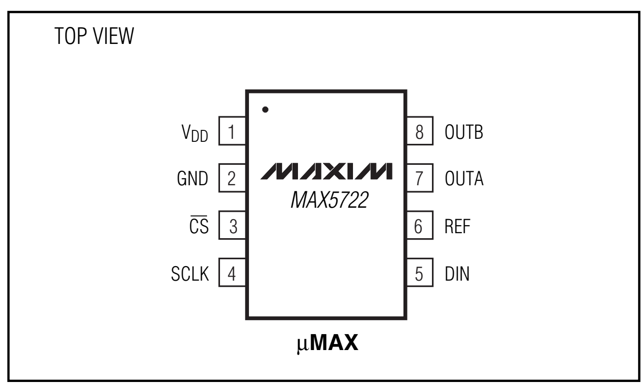
Features

- **Ultra-Low Power Consumption**
  112µA at V_{DD} = +3.6V
  135µA at V_{DD} = +5.5V
- **Wide +2.7V to +5.5V Single-Supply Range**
- **8-Pin µMAX Package**
- **0.3µA Power-Down Current**
- **Guaranteed 12-Bit Monotonicity (±1LSB DNL)**
- **Safe Power-Up Reset to Zero Volts at DAC Output**
- **Three Software-Selectable Power-Down Impedances (100kΩ, 1kΩ, Hi-Z)**
- **Fast 20MHz, 3-Wire SPI, QSPI, and MICROWIRE-Compatible Serial Interface**
- **Rail-to-Rail Output Buffer Amplifiers**
- **Schmitt-Triggered Logic Inputs for Direct Interfacing to Optocouplers**
- **Wide -40°C to +125°C Operating Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5722EUA	-40°C to +85°C	8 µMAX
MAX5722AUA	-40°C to +125°C	8 µMAX

Pin Configuration



12-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6V
OUT_, SCLK, DIN, $\overline{CS}$, REF to GND ....-0.3 to (V_{DD} + 0.3V)
Maximum Continuous Current Into Any Pin......................±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.6 mW/°C above +70°C) 362mW
Operating Temperature Range ....-40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		12			Bits
Integral Nonlinearity Error	INL	(Note 2)		±2	±16	LSB
Differential Nonlinearity Error	DNL	Guaranteed monotonic (Note 2)			±1	LSB
Zero-Code Error	OE	Code = 000		0.4	1.5	% of FS
Zero-Code Tempco				2.3		ppm/°C
Gain Error	GE	Code = FFF hex			±3	% of FS
Gain-Error Tempco				0.26		ppm/°C
Power-Supply Rejection Ratio	PSRR	Code = FFF hex, ΔV_{DD} = ±10%		58.8		dB
REFERENCE INPUT						
Reference Input Voltage Range	V_{REF}		0		V_{DD}	V
Reference Input Impedance	R_{REF}	In operation	64	90	126	kΩ
		In power-down mode		2		MΩ
Power-Down Reference Current		In power-down mode (Note 3)		1	10	µA
DAC OUTPUT						
Output Voltage Range		No load (Note 4)	0		V_{DD}	V
DC Output Impedance		Code = 800 hex		0.8		Ω
Short-Circuit Current		V_{DD} = +3V		15		mA
		V_{DD} = +5V		48		
Wake-Up Time		V_{DD} = +3V		8		µs
		V_{DD} = +5V		8		
Output Leakage Current		Power-down mode = output high impedance		±18		nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)						
Input High Voltage	V_{IH}	V_{DD} = +3V, +5V	0.7 x V_{DD}			V
Input Low Voltage	V_{IL}	V_{DD} = +3V, +5V			0.3 x V_{DD}	V
Input Leakage Current	I_{IN}	Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Input Capacitance	C_{IN}			5		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.5		V/µs
Voltage-Output Settling Time		400 hex to C00 hex (Note 5)		4	10	µs
Digital Feedthrough		Any digital inputs from 0 to V_{DD}		0.15		nV-s
Digital Analog Glitch Impulse		Major carry transition (code 7FF hex to code 800 hex)		12		nV-s
DAC-to-DAC Crosstalk				2.4		nV-s
POWER REQUIREMENTS						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No Load	I_{DD}	All digital inputs at 0 or V_{DD} = 3.6V		112	205	µA
		All digital inputs at 0 or V_{DD} = 5.5V		135	215	
Power-Down Supply Current	I_{DDPD}	All digital inputs at 0 or V_{DD} = 5.5V		0.29	1	µA

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	f_{SCLK}		0		20	MHz
SCLK Pulse Width High	t_{CH}		25			ns
SCLK Pulse Width Low	t_{CL}		25			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		10			ns
SCLK Fall to $\overline{CS}$ Rise Setup Time	t_{CSH}		10			ns
DIN to SCLK Fall Setup Time	t_{DS}		15			ns
DIN to SCLK Fall Hold Time	t_{DH}		0			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		80			ns

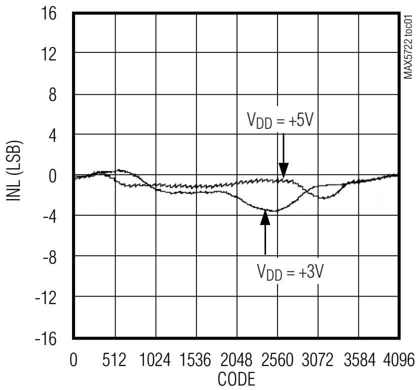
Note 1: DC specifications are tested without output loads.
Note 2: Linearity is guaranteed from code 115 to code 3981.
Note 3: Limited with test conditions.
Note 4: Offset and gain error limit the FSR.
Note 5: Guaranteed by design.

12-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

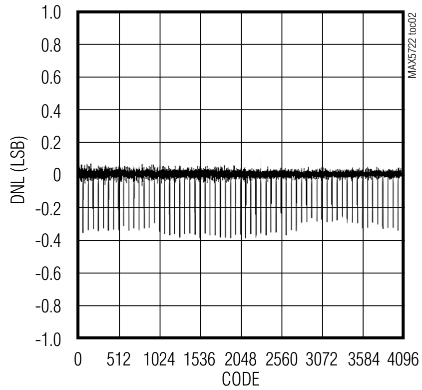
Typical Operating Characteristics

($V_{REF} = V_{DD}$, T_A = +25°C, unless otherwise noted.)

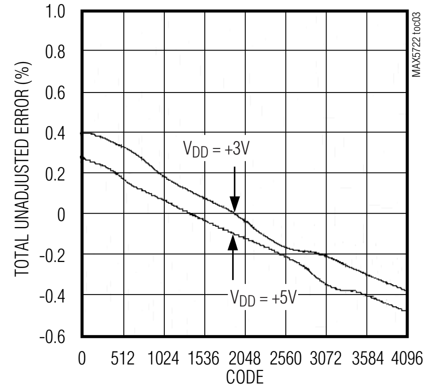
INTEGRAL NONLINEARITY vs. CODE, T_A = +25°C



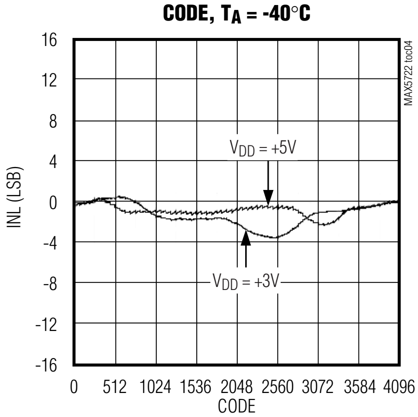
DIFFERENTIAL NONLINEARITY vs. CODE, T_A = +25°C



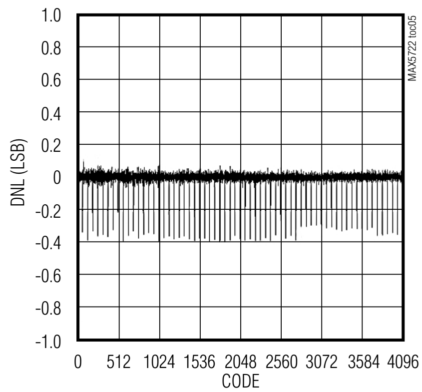
TOTAL UNADJUSTED ERROR vs. CODE, T_A = +25°C



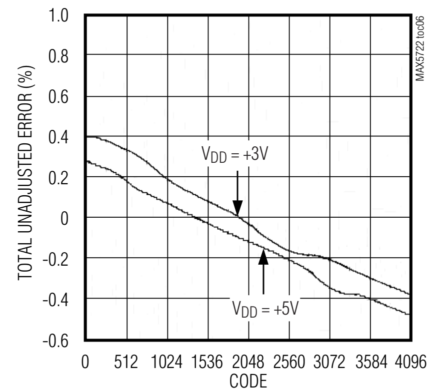
INTEGRAL NONLINEARITY vs. CODE, T_A = -40°C



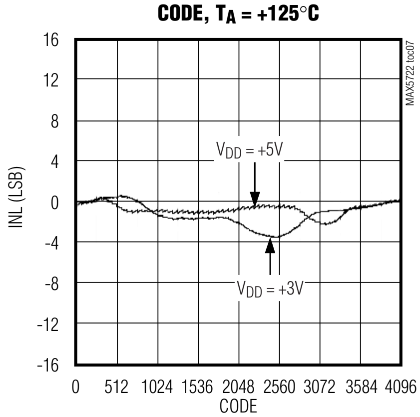
DIFFERENTIAL NONLINEARITY vs. CODE, T_A = -40°C



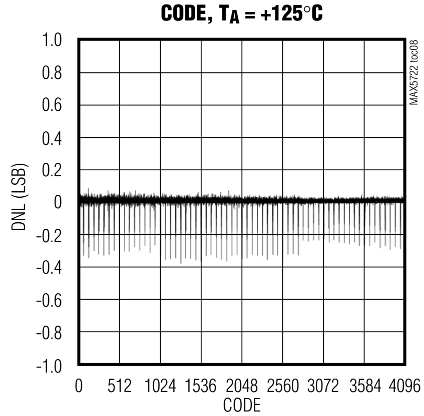
TOTAL UNADJUSTED ERROR vs. CODE, T_A = -40°C



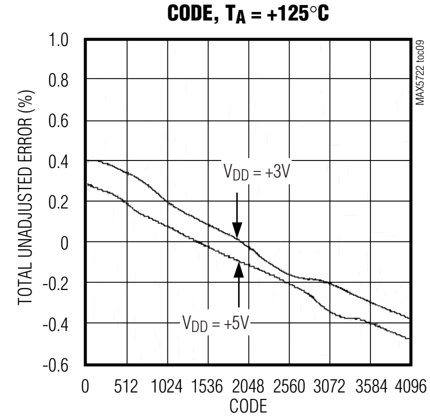
INTEGRAL NONLINEARITY vs. CODE, T_A = +125°C



DIFFERENTIAL NONLINEARITY vs. CODE, T_A = +125°C



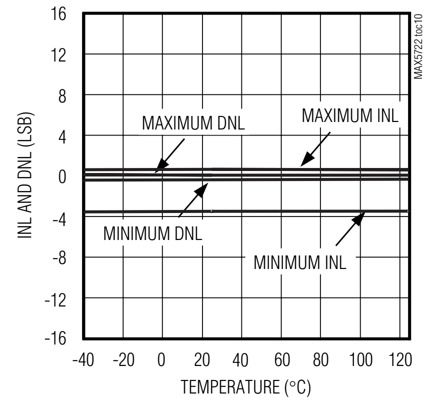
TOTAL UNADJUSTED ERROR vs. CODE, T_A = +125°C



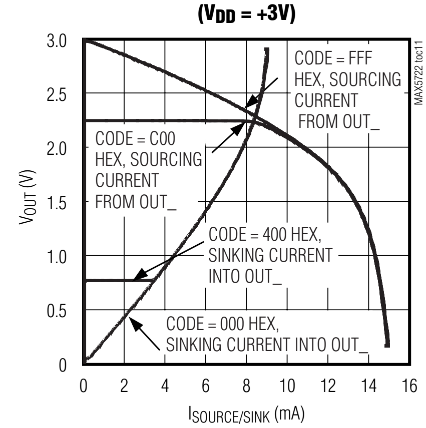
Typical Operating Characteristics (continued)

($V_{REF} = V_{DD}$, $T_A = +25°C$, unless otherwise noted.)

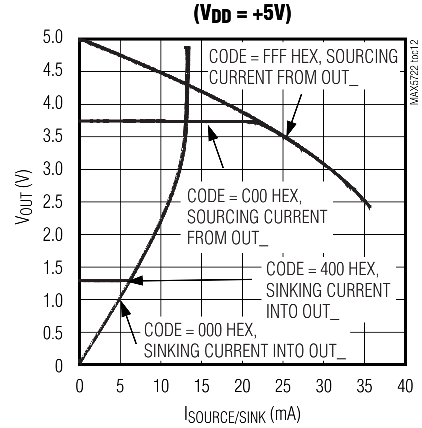
WORST CASE INL AND DNL vs. TEMPERATURE



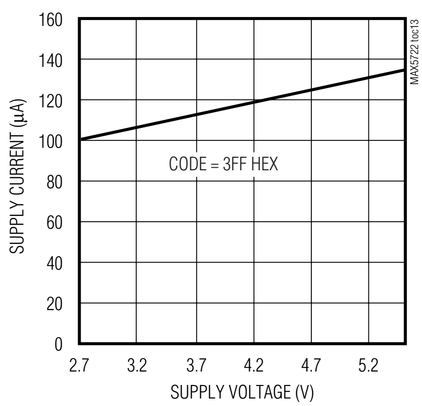
SOURCE-AND-SINK CURRENT CAPABILITY (V_{DD} = +3V)



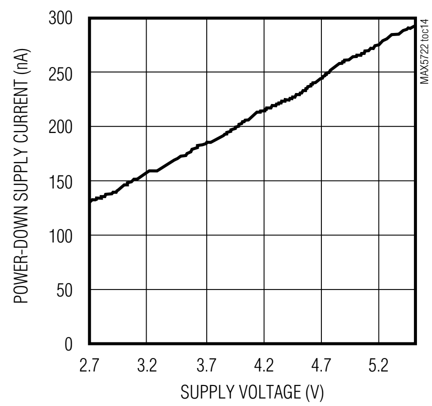
SOURCE-AND-SINK CURRENT CAPABILITY (V_{DD} = +5V)



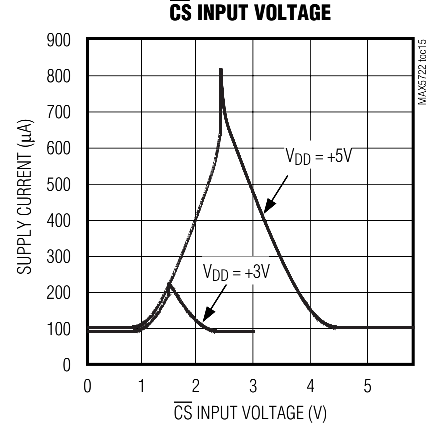
SUPPLY CURRENT vs. SUPPLY VOLTAGE



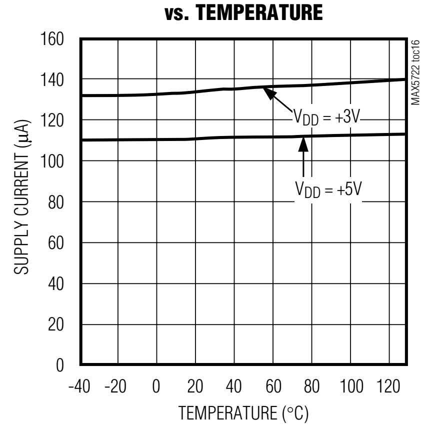
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



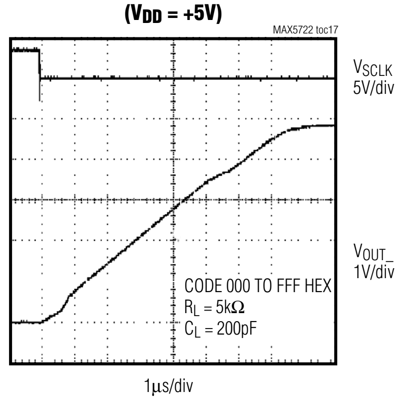
SUPPLY CURRENT vs. $\overline{CS}$ INPUT VOLTAGE



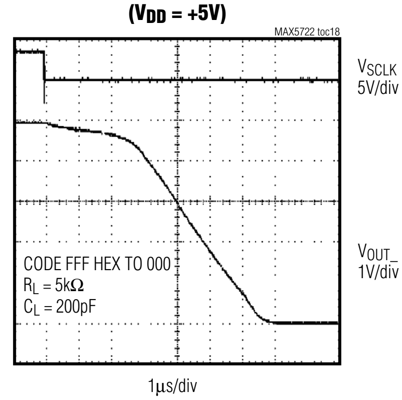
SUPPLY CURRENT vs. TEMPERATURE



FULL-SCALE SETTLING TIME (V_{DD} = +5V)



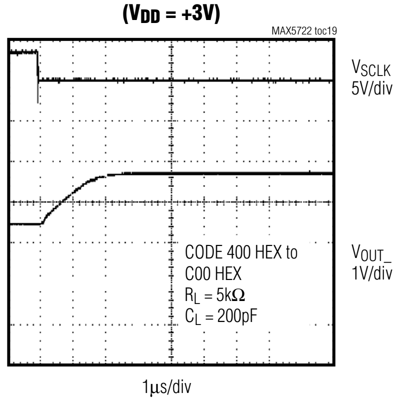
FULL-SCALE SETTLING TIME (V_{DD} = +5V)



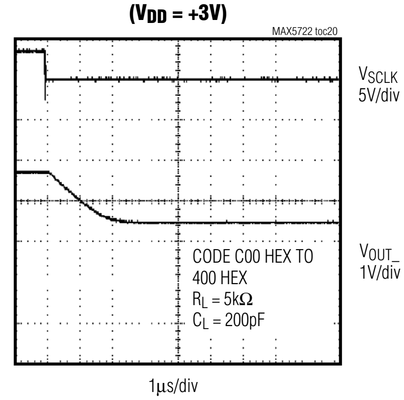
Typical Operating Characteristics (continued)

(V_{REF} = V_{DD}, T_A = +25°C, unless otherwise noted.)

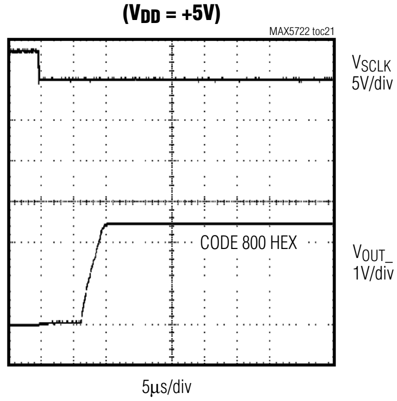
HALF-SCALE SETTLING TIME (V_{DD} = +3V)



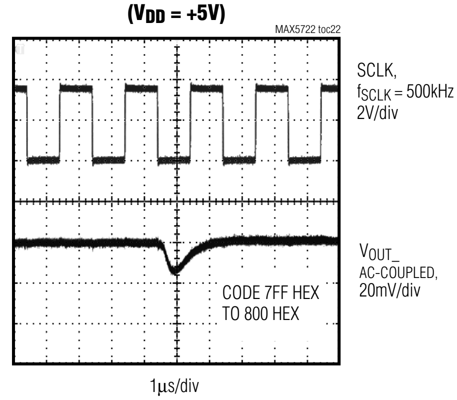
HALF-SCALE SETTLING TIME (V_{DD} = +3V)



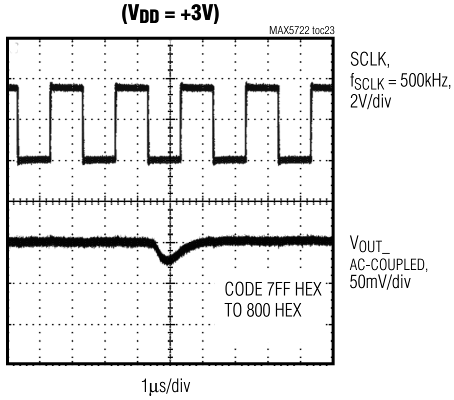
EXITING POWER-DOWN (V_{DD} = +5V)



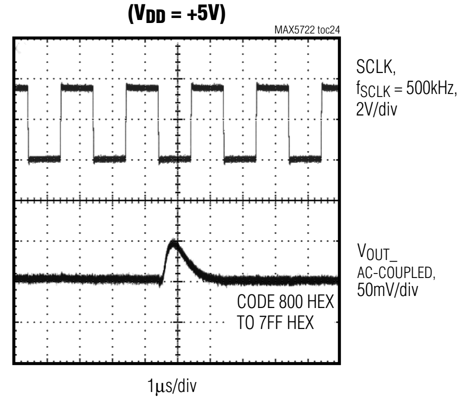
DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +5V)



DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +3V)



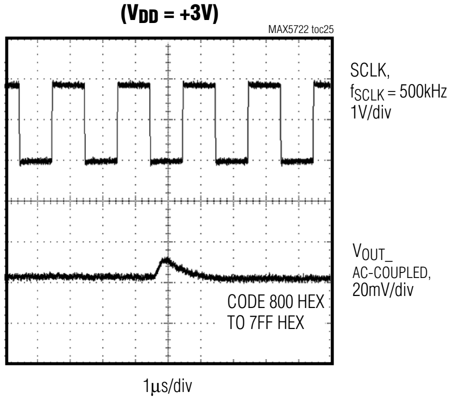
DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +5V)



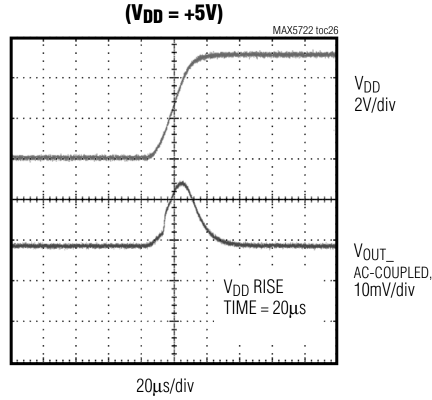
Typical Operating Characteristics (continued)

(V_{REF} = V_{DD}, T_A = +25°C, unless otherwise noted.)

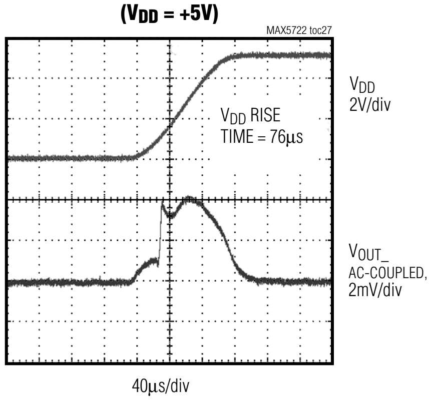
DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +3V)



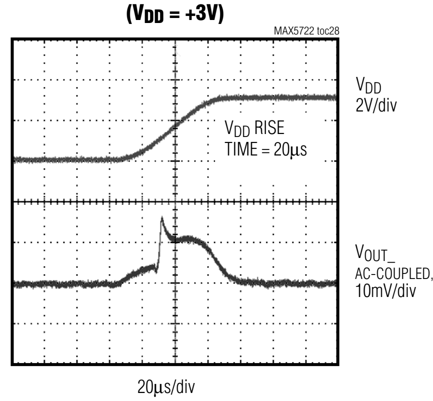
POWER-ON RESET, FAST RISE TIME (V_{DD} = +5V)



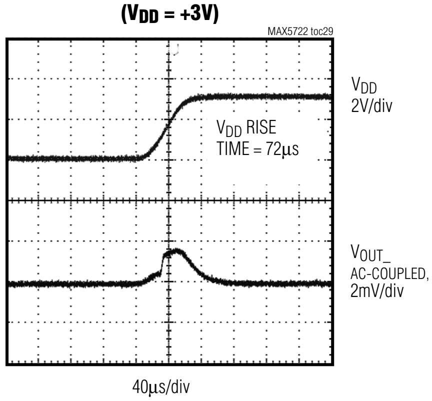
POWER-ON RESET, SLOW RISE TIME (V_{DD} = +5V)



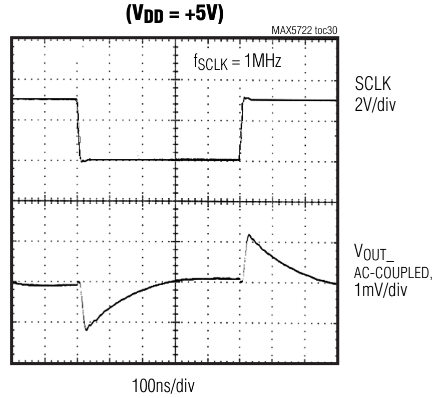
POWER-ON RESET, FAST RISE TIME (V_{DD} = +3V)



POWER-ON RESET, SLOW RISE TIME (V_{DD} = +3V)



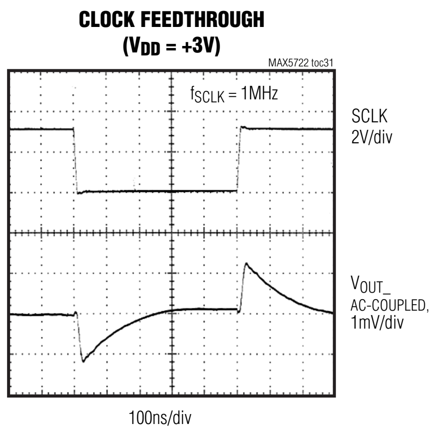
CLOCK FEEDTHROUGH (V_{DD} = +5V)

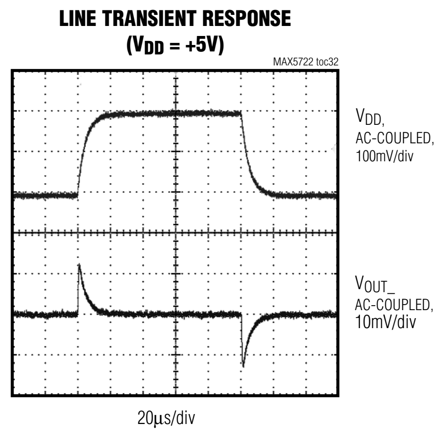


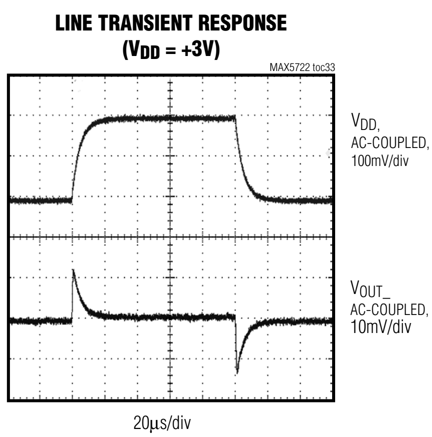
12-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

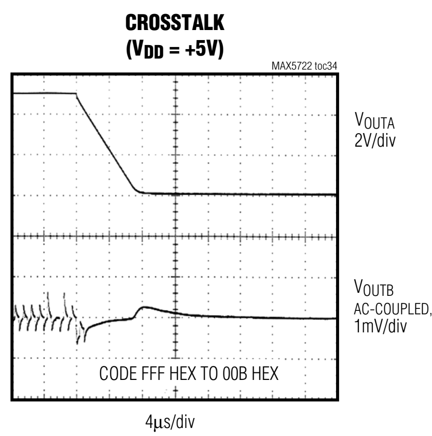
Typical Operating Characteristics (continued)

(V_{REF} = V_{DD}, T_A = +25°C, unless otherwise noted.)









Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power-Supply Input
2	GND	Ground
3	$\overline{CS}$	Chip-Select Input
4	SCLK	Serial-Clock Input
5	DIN	Serial Data Input
6	REF	External Reference Voltage Input
7, 8	OUTA, OUTB	DAC Voltage Outputs. Power-on reset sets DAC register to zero, and internally connects OUT to GND with 100kΩ resistor.

Detailed Description

The MAX5722 contains two 12-bit, voltage-output, low-power, digital-to-analog converters (DACs). Each DAC employs a resistor string architecture that converts a 12-bit digital input word to an equivalent analog output voltage proportional to the applied reference voltage. The MAX5722 shares one reference input (REF) between both DACs. The MAX5722 includes rail-to-rail output buffer amplifiers for each DAC, and input logic for simple microprocessor (µP), and CMOS interfaces. The power-supply range is from +2.7V to +5.5V (*Functional Diagram*). The MAX5722's reference input accepts a voltage range from 0 to V_{DD}. In power-down mode the reference input is high impedance. The MAX5722 is compatible with the 3-wire SPI, QSPI, MICROWIRE, and DSP serial interface with Schmitt-triggered logic inputs.

Reference Input and DAC Output Range

The reference input accepts positive DC and AC signals. The voltage at REF sets the full-scale output voltage of both DACs. The reference input voltage range is 0 to V_{DD}. The impedance at REF is 90kΩ. The voltage at REF can vary from GND to V_{DD}. The output voltages ($V_{OUT\_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times D) / 2^{12}$$

where D is the decimal equivalent of binary DAC input code ranging from 0 to 4095. V_{REF} is the voltage at REF.

Output Buffer Amplifiers

All DACs are internally buffered at the output. The buffer amplifiers have both rail-to-rail common mode and (GND to V_{REF}) output voltage range. The buffers are unity-gain stable with C_L = 200pF and R_L = 5kΩ. Buffer amplifiers are disabled during power-up and individual DAC outputs are shorted to GND through a 100kΩ resistor. Buffer amplifiers can individually or altogether be powered-down by programming the input register control bits. During power-down, contents of the input and DAC registers remain the same. On wake-up, all DAC outputs are restored to their pre-power-down voltage values.

Power-Down Mode

In power-down mode, the DAC outputs are programmed to one of three output states, 1kΩ, 100kΩ, or floating (Table 1). The REF input is high impedance (2MΩ typ), to conserve current drain from the system reference; therefore, the system reference does not have to be powered-down. The DAC outputs return to the values contained in the registers when brought out of power-down. The recovery time, from total power-down to power-up, is 8µs. This extra time is needed to allow the internal bias to wake-up. Power-down mode reduces current consumption to 0.3µA.

3-Wire Serial Interface

The MAX5722 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE/DSP interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at DIN. Immediately following $\overline{CS}$ high-to-low transition, the data is shifted synchronously and latched into the input register on the falling edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial input register, it transfers its contents to the DAC latch. $\overline{CS}$ may then either be held low or brought high. $\overline{CS}$ must be brought high for a minimum of 80ns before the next write sequence, since a write sequence is initiated on a falling edge of $\overline{CS}$. Not

12-Bit, Low-Power, Dual, Voltage-Output DAC with Serial Interface

Table 1. Power-Down Mode Control

EXTENDED CONTROL				DATA BITS						DESCRIPTION	FUNCTION
C3	C2	C1	C0	D11–D5	D4	D3	D2	D1	D0		
1	1	1	1	X	0	X	0	0	0	DAC A	DAC O/P, wake-up
1	1	1	1	X	0	X	0	0	1	DAC A	Floating output
1	1	1	1	X	0	X	0	1	0	DAC A	Output is terminated with 1kΩ
1	1	1	1	X	0	X	0	1	1	DAC A	Output is terminated with 100kΩ
1	1	1	1	X	0	X	1	0	0	DAC B	DAC O/P, wake-up
1	1	1	1	X	0	X	1	0	1	DAC B	Floating output
1	1	1	1	X	0	X	1	1	0	DAC B	Output is terminated with 1kΩ
1	1	1	1	X	0	X	1	1	1	DAC B	Output is terminated with 100kΩ
1	1	1	1	X	1	X	0	0	0	DAC A-B	DAC O/P, wake-up
1	1	1	1	X	1	X	0	0	1	DAC A-B	Floating output
1	1	1	1	X	1	X	0	1	0	DAC A-B	Output is terminated with 1kΩ
1	1	1	1	X	1	X	0	1	1	DAC A-B	Output is terminated with 100kΩ

X = Don't Care

keeping $\overline{CS}$ low during the first 15 SCLK cycles discards input data. The serial clock (SCLK) can idle either high or low between transitions.

The MAX5722 has two internal registers per DAC, the input register and the DAC register. The input register holds the data that is waiting to be shifted to the DAC register. Both input registers can be loaded without updating the output. This function is useful when both outputs need to be updated at the same time. The input register can be made transparent. When the input register is transparent, the data written into DIN loads directly to the DAC register and the output is updated. The DAC output is not updated until data is written to the DAC register. See Table 2 for a list of serial-interface programming commands.

Power-On Reset (POR)

The MAX5722 has an internal POR circuit. At power-up, all DACs are powered-down and OUT_ is terminated to GND through 100kΩ resistors. Contents of input and DAC registers are cleared to all zero. An 8µs recovery time after issuing a wake-up command is needed before writing to the DAC registers. Power-down mode control commands can be applied immediately with no recovery time.

C3-C0 are control bits. The data bits D11 to D0 are in straight binary format. All zeros correspond to zero scale and all ones correspond to full scale.

Digital Inputs

The digital inputs are compatible with CMOS logic. In order to save power and reduce input to output coupling, SCLK and DIN input buffers are powered down immediately after completion of shifting 16 bits into the input shift register. A high to low transition at $\overline{CS}$ powers up SCLK and DIN input buffers.

Applications Information

Unipolar Output

The typical application circuit (Figure 3) shows the MAX5722 configured for a unipolar output, where the output voltages and the reference inputs have the same polarity. Table 3 lists the unipolar output codes.

Bipolar Output

The MAX5722 can be configured for bipolar operation using a dual supply op amp (Figure 4). The transfer function for bipolar operation is:

$$V_{OUT} = V_{REF}\left[\left(\frac{2D}{4096}\right) - 1\right]$$

where D is the decimal value of the DACs binary input code. Table 4 shows digital codes (offset binary) and corresponding output voltages for the circuit in Figure 4.

CONTENTS OF SHIFT REGISTER B15 (MSB)															B0 (LSB)
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 1. 16-Bit Input Word

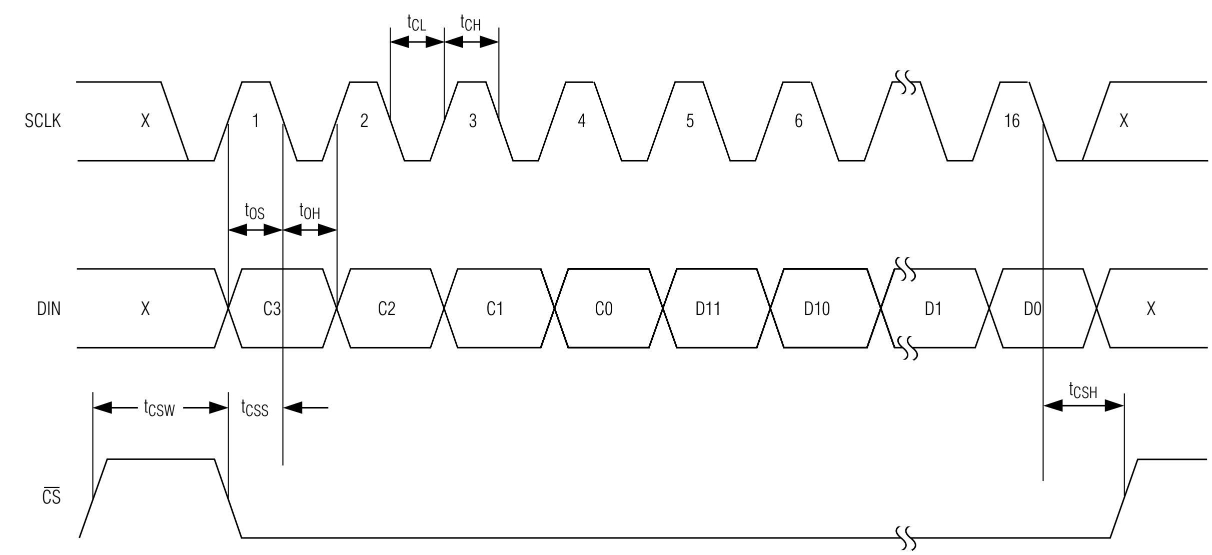


Figure 2. Timing Diagram

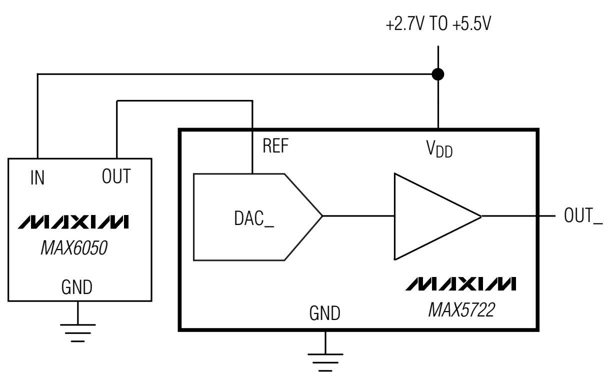


Figure 3. Typical Operating Circuit, Unipolar Output

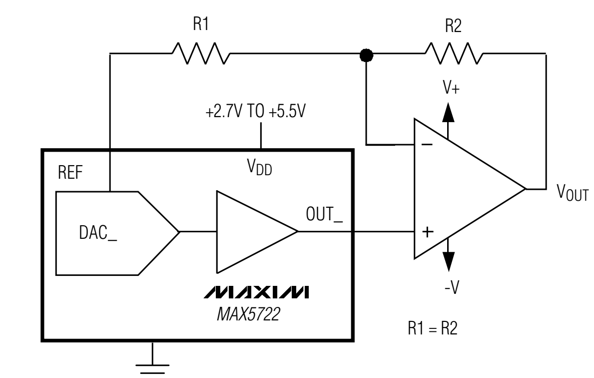


Figure 4. Bipolar Output Circuit

Table 2. Serial-Interface Programming Commands

CONTROL				DATA BITS	DAC	FUNCTION
C3	C2	C1	C0	D11–D0		
0	0	0	0	X	A	Input register transparent, data shifted directly to DAC register, OUTA updated
0	0	0	1	X	B	Input register transparent, data shifted directly to DAC register, OUTB updated
0	1	0	0	X	A	Data shifted to input register, OUTA unchanged
0	1	0	1	X	B	Data shifted to input register, OUTB unchanged
1	0	0	0	X	A	Shift data from input register to DAC register, OUTA updated
1	0	0	1	X	B	Shift data from input register to DAC register, OUTB updated
1	1	0	0	X	A-B	Input registers transparent, data shifted directly to DAC registers, OUTA and OUTB updated
1	1	0	1	X	A-B	Data shifted to input registers, OUTA and OUTB unchanged
1	1	1	0	X	A-B	Shift data from input registers to DAC registers, OUTA and OUTB updated

X = Don't Care

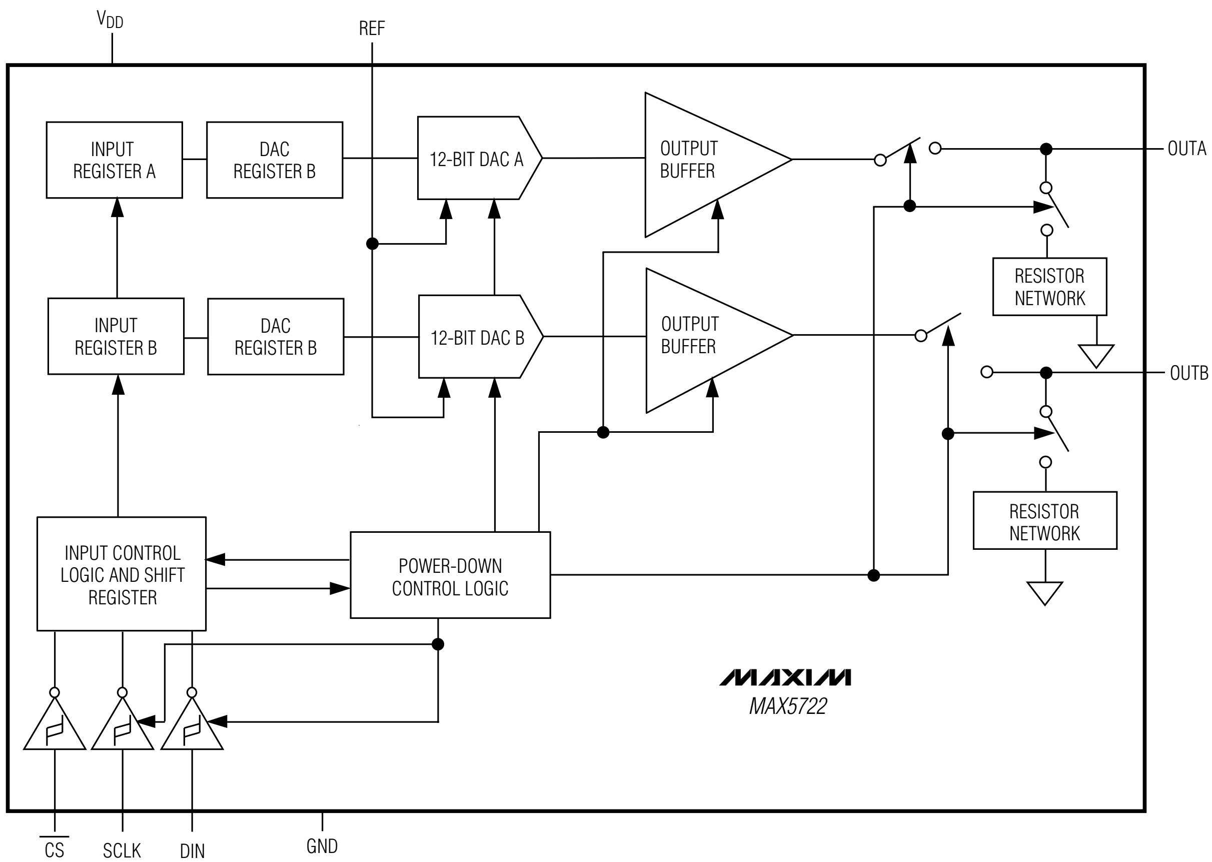
Table 3. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$+\frac{V_{REF}}{2}$
0111 1111 1111	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0

Table 4. Bipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF}$

Functional Diagram



Power Supply and Layout Considerations

Careful PC board layout is important for optimal system performance. To reduce noise injection and digital feedthrough and keep analog and digital signals separate. Ensure that that the return path from GND to the supply ground is short and low impedance. Use a ground plane. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to V_{DD}.

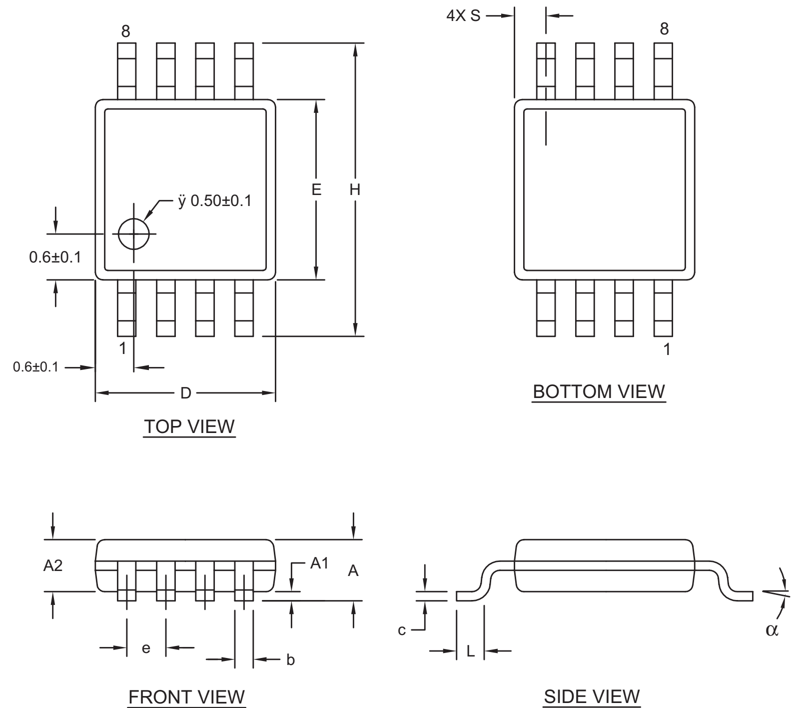
Chip Information

TRANSISTOR COUNT: 7737

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



8LUMAXD.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1