19-6149; Rev 0; 2/12

MAX5816

Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

General Description

The MAX5816 4-channel, low-power, 12-bit, voltage-output digital-to-analog converter (DAC) includes output buffers and an internal reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5816 accepts a wide supply voltage range of 2.7V to 5.5V with extremely low power (3mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a 100kΩ (typ) load to an external reference.

The MAX5816 has an I²C-compatible, 2-wire interface that operates at clock rates up to 400kHz. The DAC output is buffered and has a low supply current of less than 250µA per channel and a low offset error of ±0.5mV (typ). On power-up, the MAX5816 resets the DAC outputs to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The internal reference is initially powered down to allow use of an external reference. The MAX5816 allows simultaneous output updates using software LOAD commands. Multiple devices can simultaneously be updated using software load command in combination with the broadcast ID.

The MAX5816 is available in a 10-pin TDFN package and is specified over the -40°C to +125°C temperature range.

Applications

Programmable Voltage and Current Sources

Gain and Offset Adjustment

Automatic Tuning and Optical Control

Power Amplifier Control and Biasing

Process Control and Servo Loops

Portable Instrumentation

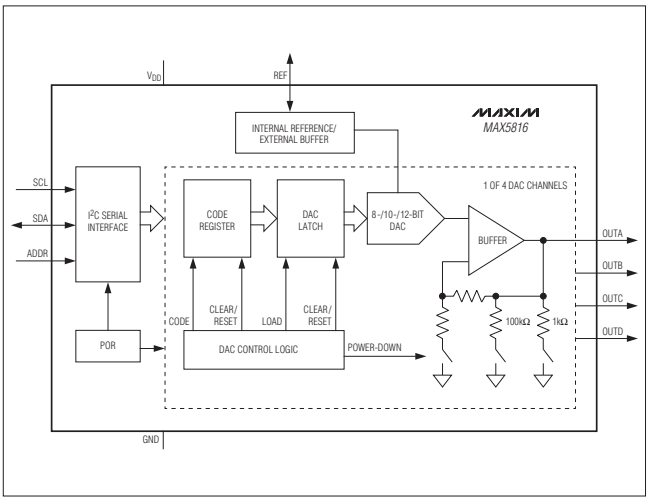
Data Acquisition

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- **Four High-Accuracy DAC Channels**
  - **12-Bit Accuracy Without Adjustment**
  - **±1 LSB INL Buffered Voltage Output**
  - **Guaranteed Monotonic Over All Operating Conditions**
  - **Independent Mode Settings for Each DAC**
- **Three Precision Selectable Internal References**
  - **2.048V, 2.500V, or 4.096V**
- **Internal Output Buffer**
  - **Rail-to-Rail Operation with External Reference**
  - **4.5µs Settling Time**
  - **Outputs Directly Drive 2kΩ Loads**
- **Small 3mm x 3mm 10-Pin TDFN Package**
- **Wide 2.7V to 5.5V Supply Range**
- **Fast 400kHz I²C-Compatible, 2-Wire Serial Interface**
- **Power-On-Reset to Zero-Scale DAC Output**
- **Three Software-Selectable Power-Down Output Impedances**
  - **1kΩ, 100kΩ, or High Impedance**

Functional Diagram



For related parts and recommended products to use with this part, refer to: ***www.maxim-ic.com/MAX5816.related***

Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND.....-0.3V to +6V
OUT_, REF to GND....0.3V to the lower of (V_{DD} + 0.3V) and +6V
SCL, SDA to GND .....-0.3V to +6V
ADDR to GND .....-0.3V to the lower of (V_{DD} + 0.3V) and +6V
Continuous Power Dissipation (T_A = +70°C)
TDFN (derate at 24.4mW/°C above 70°C).....1951.2mW
Maximum Continuous Current into Any Pin ..... ±50mA
Operating Temperature..... -40°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....9°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (Note 3)						
Resolution and Monotonicity	N		12			Bits
Integral Nonlinearity (Note 4)	INL		-1	±0. 5	+1	LSB
Differential Nonlinearity (Note 4)	DNL		-1	±0.2	+1	LSB
Offset Error (Note 5)	OE		-5	±0.5	+5	mV
Offset Error Drift				±10		µV/°C
Gain Error (Note 5)	GE		-1.0	±0.1	+1.0	%FS
Gain Temperature Coefficient		With respect to V_{REF}		±3.0		ppm of FS/°C
Zero-Scale Error			0		10	mV
Full-Scale Error		With respect to V_{REF}	-0.5		+0.5	%FS
DAC OUTPUT CHARACTERISTICS						
Output Voltage Range (Note 6)		No load	0		V_{DD}	V
		2kΩ load to GND	0		V_{DD} - 0.2	
		2kΩ load to V_{DD}	0.2		V_{DD}	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation		$V_{OUT} = V_{FS}/2$	V_{DD} = 3V ±10%, $\|I_{OUT}\| \le$ 5mA		300		µV/mA
			V_{DD} = 5V ±10%, $\|I_{OUT}\| \le$ 10mA		300		
DC Output Impedance		$V_{OUT} = V_{FS}/2$	V_{DD} = 3V ±10%, $\|I_{OUT}\| \le$ 5mA		0.3		Ω
			V_{DD} = 5V ±10%, $\|I_{OUT}\| \le$ 10mA		0.3		
Maximum Capacitive Load Handling	C_L				500		pF
Resistive Load Handling	R_L			2			kΩ
Short-Circuit Output Current		V_{DD} = 5.5V	Sourcing (output shorted to GND)		30		mA
			Sinking (output shorted to V_{DD})		50		
DC Power-Supply Rejection		V_{DD} = 3V ±10% or 5V ±10%			100		µV/V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	Positive and negative			1.0		V/µs
Voltage-Output Settling Time		¼ scale to ¾ scale, to ≤ 1 LSB			4.5		µs
DAC Glitch Impulse		Major code transition			2		nV*s
Channel-to-Channel Feedthrough (Note 7)		External reference			3.5		nV*s
		Internal reference			3.3		
Digital Feedthrough		Code = 0, all digital inputs from 0V to V_{DD}			0.2		nV*s
Power-Up Time		Startup calibration time (Note 8)			200		µs
		From power-down			50		µs
Output Voltage-Noise Density (DAC Output at Midscale)		External reference	f = 1kHz		90		nV/√Hz
			f = 10kHz		82		
		2.048V internal reference	f = 1kHz		112		
			f = 10kHz		102		
		2.5V internal reference	f = 1kHz		125		
			f = 10kHz		110		
		4.096V internal reference	f = 1kHz		160		
			f = 10kHz		145		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Integrated Output Noise (DAC Output at Midscale)		External reference	f = 0.1Hz to 10Hz		12		μV_{P-P}
			f = 0.1Hz to 10kHz		76		
			f = 0.1Hz to 300kHz		385		
		2.048V internal reference	f = 0.1Hz to 10Hz		14		
			f = 0.1Hz to 10kHz		91		
			f = 0.1Hz to 300kHz		450		
		2.5V internal reference	f = 0.1Hz to 10Hz		15		
			f = 0.1Hz to 10kHz		99		
			f = 0.1Hz to 300kHz		470		
		4.096V internal reference	f = 0.1Hz to 10Hz		16		
			f = 0.1Hz to 10kHz		124		
			f = 0.1Hz to 300kHz		490		
Output Voltage-Noise Density (DAC Output at Full Scale)		External reference	f = 1kHz		114		$nV/\sqrt{Hz}$
			f = 10kHz		99		
		2.048V internal reference	f = 1kHz		175		
			f = 10kHz		153		
		2.5V internal reference	f = 1kHz		200		
			f = 10kHz		174		
		4.096V internal reference	f = 1kHz		295		
			f = 10kHz		255		
Integrated Output Noise (DAC Output at Full Scale)		External reference	f = 0.1Hz to 10Hz		13		μV_{P-P}
			f = 0.1Hz to 10kHz		94		
			f = 0.1Hz to 300kHz		540		
		2.048V internal reference	f = 0.1Hz to 10Hz		19		
			f = 0.1Hz to 10kHz		143		
			f = 0.1Hz to 300kHz		685		
		2.5V internal reference	f = 0.1Hz to 10Hz		21		
			f = 0.1Hz to 10kHz		159		
			f = 0.1Hz to 300kHz		705		
		4.096V internal reference	f = 0.1Hz to 10Hz		26		
			f = 0.1Hz to 10kHz		213		
			f = 0.1Hz to 300kHz		750		
REFERENCE INPUT							
Reference Input Range	V_{REF}			1.24		V_{DD}	V
Reference Input Current	I_{REF}	$V_{REF} = V_{DD}$ = 5.5V			55	74	µA
Reference Input Impedance	R_{REF}			75	100		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE OUPUT							
Reference Output Voltage	V_{REF}	V_{REF} = 2.048V, T_A = +25°C		2.043	2.048	2.053	V
		V_{REF} = 2.5V, T_A = +25°C		2.494	2.5	2.506	
		V_{REF} = 4.096V, T_A = +25°C		4.086	4.096	4.106	
Reference Temperature Coefficient					±10	±25	ppm/°C
Reference Drive Capacity		External load			25		kΩ
Reference Capacitive Load					200		pF
Reference Load Regulation		I_{SOURCE} = 0 to 500µA			2		mV/mA
Reference Line Regulation					0.05		mV/V
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	V_{REF} = 4.096V		4.5		5.5	V
		All other options		2.7		5.5	
Supply Current (Note 9)	I_{DD}	Internal reference, V_{DD} = 5.5V	V_{REF} = 2.048V		0.85	1.25	mA
			V_{REF} = 2.5V		0.9	1.25	
			V_{REF} = 4.096V		1.1	1.40	
		External reference	V_{DD} = V_{REF} = 3V		0.65	1.1	
			V_{DD} = V_{REF} = 5V		0.9	1.25	
Power-Down Mode Supply Current	I_{PD}	All DACs off, internal reference ON			140		µA
		All DACs off, internal reference OFF, T_A = -40°C to +85°C			0.5	1	
		All DACs off, internal reference OFF, T_A = +125°C			1.2	2.5	
DIGITAL INPUT CHARACTERISTICS (SCL, SDA, ADDR)							
Input High Voltage	V_{IH}	2.7V < V_{DD} < 5.5V		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}	2.7V < V_{DD} < 5.5V				0.3 x V_{DD}	V
Hysteresis Voltage	V_H				0.15		V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±0.1	±1	µA
Input Capacitance (Note 10)	C_{IN}					10	pF
ADDR Pullup/Pulldown Strength	R_{PU}, R_{PD}	(Note 11)		30	50	90	kΩ
DIGITAL OUTPUT (SDA)							
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.2	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{GND} = 0V, C_L = 200pF, R_L = 2kΩ, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING CHARACTERISTICS (SCL, SDA)						
SCL Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time Repeated for a START Condition	$t_{HD;STA}$		0.6			µs
SCL Pulse Width Low	t_{LOW}		1.3			µs
SCL Pulse Width High	t_{HIGH}		0.6			µs
Setup Time for Repeated START Condition	$t_{SU;STA}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$		0		900	ns
Data Setup Time	$t_{SU;DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_r		20 + C_B/10		300	ns
SDA and SCL Receiving Fall Time	t_f		20 + C_B/10		300	ns
SDA Transmitting Fall Time	t_f		20 + C_B/10		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			µs
Bus Capacitance Allowed	C_B		10		400	pF
Pulse Width of Suppressed Spike	t_{sp}			50		ns

Note 2: Limits are 100% production tested at T_A = +25°C and/or T_A = +125°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are at T_A = +25°C and are not guaranteed.

Note 3: DC Performance is tested without load.

Note 4: Linearity is tested with unloaded outputs to within 20mV of GND and V_{DD}.

Note 5: Gain and offset tested at code 4065 and 30, respectively with V_{REF} = V_{DD}.

Note 6: Subject to zero and full-scale error limits and V_{REF} settings.

Note 7: Measured with all other DAC outputs at midscale with one channel transitioning 0 to full scale.

Note 8: On power-up, the device initiates an internal 200µs (typ) calibration sequence. All commands issued during this time will be ignored.

Note 9: All channels active at V_{FS}, unloaded. Static logic inputs with V_{IL} = V_{GND} and V_{IH} = V_{DD}.

Note 10: Guaranteed by design.

Note 11: An unconnected condition on the ADDR pin is sensed via a resistive pullup and pulldown operation; for proper operation, the ADDR pin should be tied to V_{DD}, GND, or left unconnected with minimal capacitance.

Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

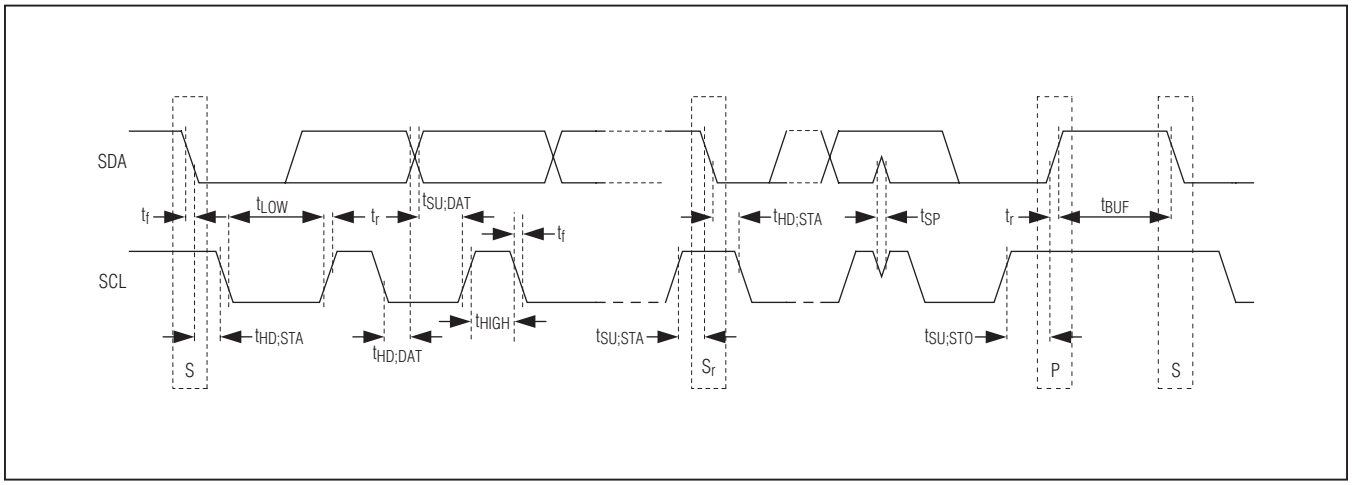
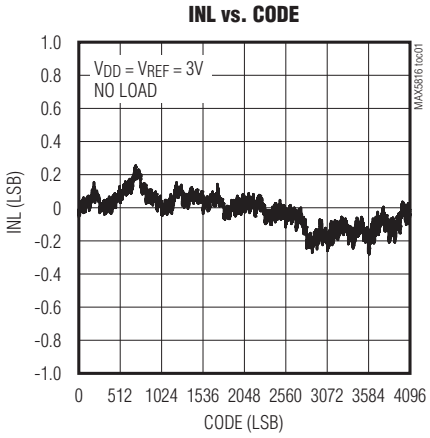
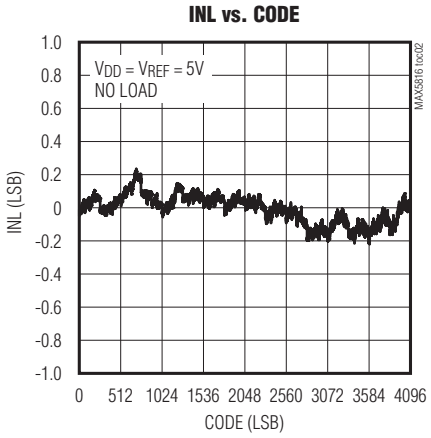


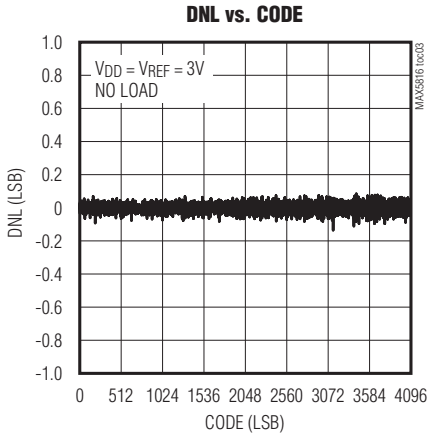
Figure 1. I²C Serial Interface Timing Diagram

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)





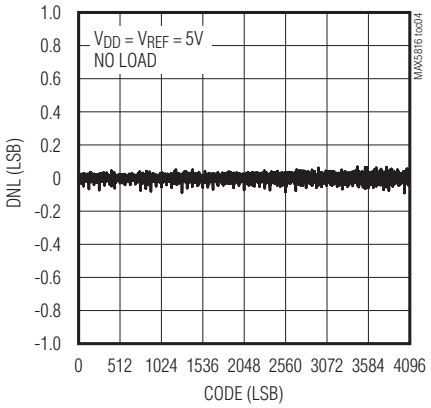


Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

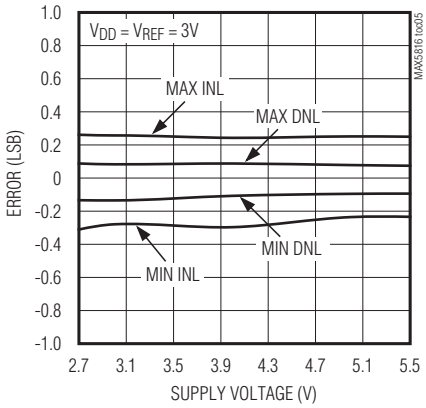
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

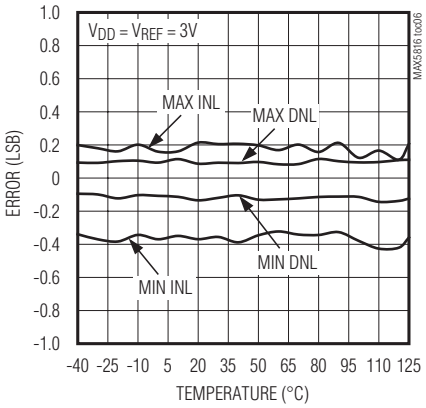
DNL vs. CODE



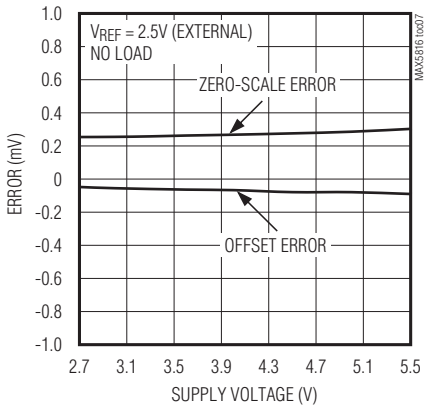
INL AND DNL vs. SUPPLY VOLTAGE



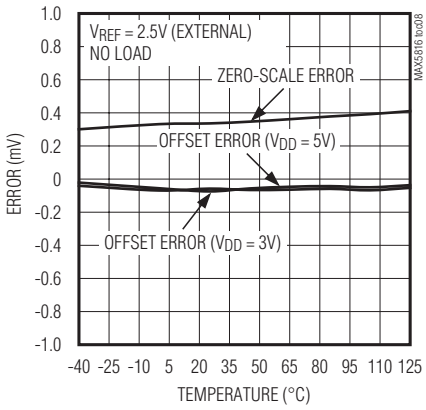
INL AND DNL vs. TEMPERATURE



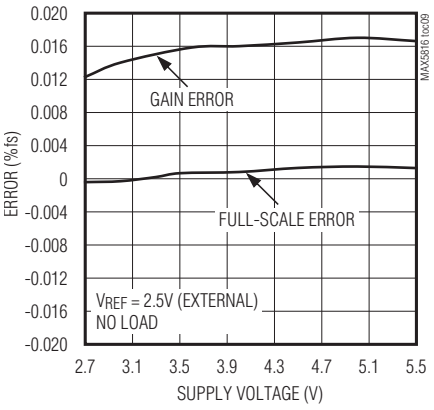
OFFSET AND ZERO-SCALE ERROR vs. SUPPLY VOLTAGE



OFFSET AND ZERO-SCALE ERROR vs. TEMPERATURE



FULL-SCALE ERROR AND GAIN-ERROR vs. SUPPLY VOLTAGE

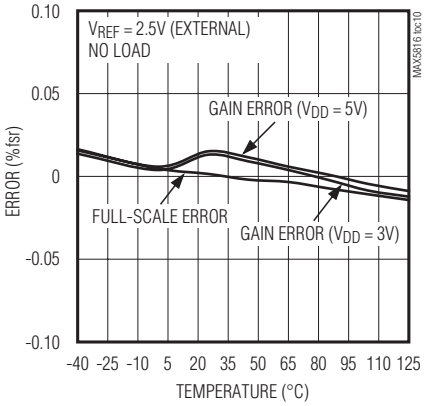


Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

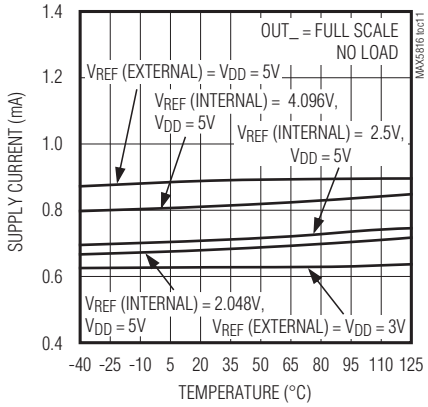
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

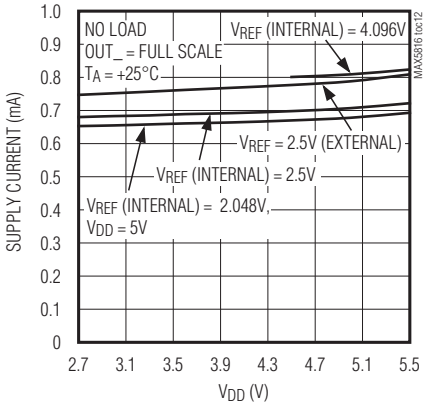
FULL-SCALE ERROR AND GAIN ERROR vs. TEMPERATURE



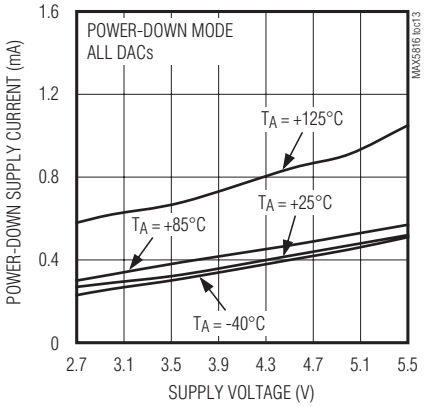
SUPPLY CURRENT vs. TEMPERATURE



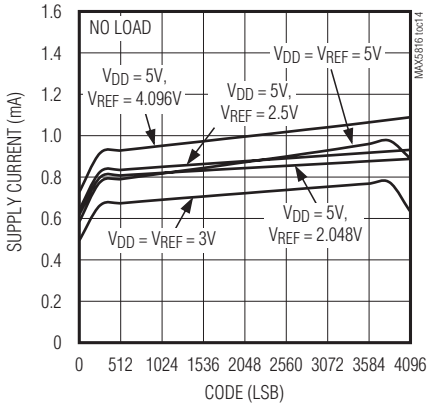
SUPPLY CURRENT vs. SUPPLY VOLTAGE



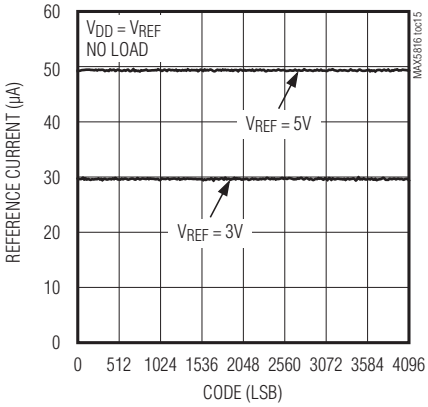
POWER-DOWN MODE SUPPLY CURRENT vs. TEMPERATURE



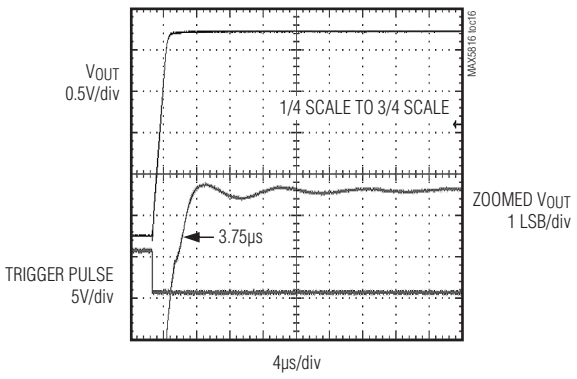
IVDD vs. CODE



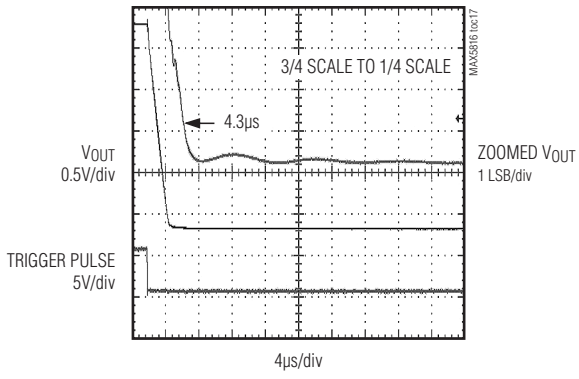
IREF (EXTERNAL) vs. CODE



SETTLING TO ±1 LSB (V_{DD} = V_{REF} = 5V, R_L = 2kΩ, C_L = 200pF)



SETTLING TO ±1 LSB (V_{DD} = V_{REF} = 5V, R_L = 2kΩ, C_L = 200pF)

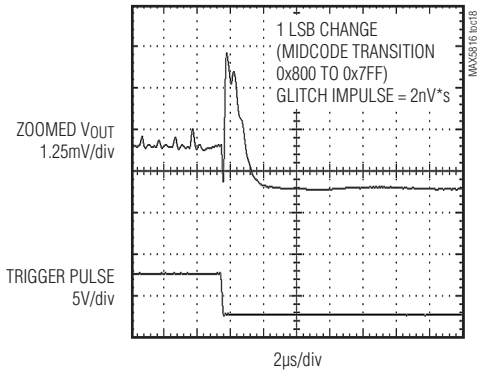


Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

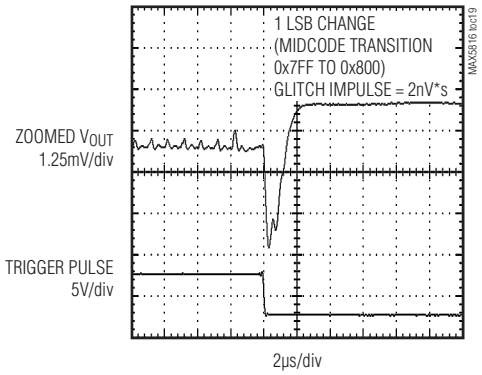
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

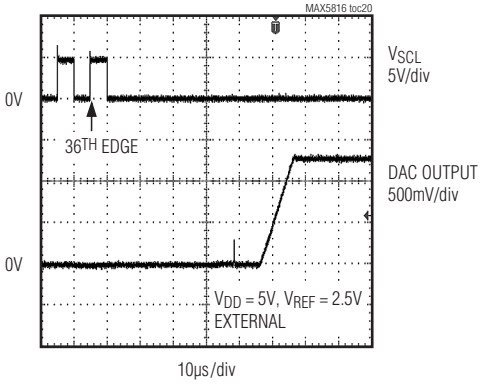
MAJOR CODE TRANSITION GLITCH ENERGY
(V_{DD} = V_{REF} = 5V, R_L = 2kΩ, C_L = 200pF)



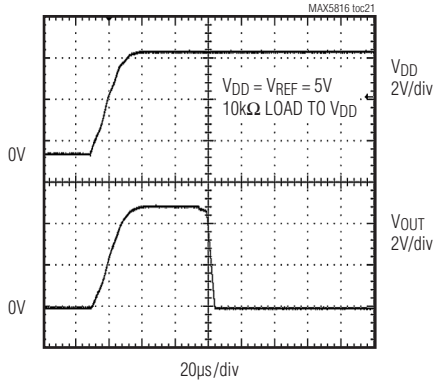
MAJOR CODE TRANSITION GLITCH ENERGY
(V_{DD} = V_{REF} = 5V, R_L = 2kΩ, C_L = 200pF)



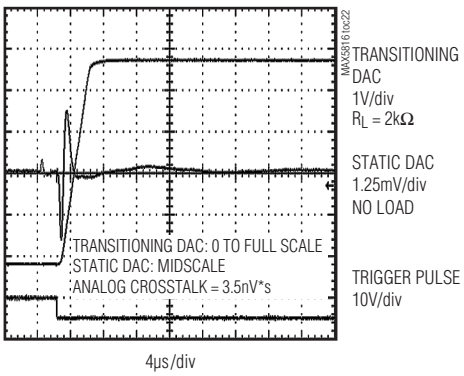
VOUT vs. TIME TRANSIENT EXITING POWER-DOWN



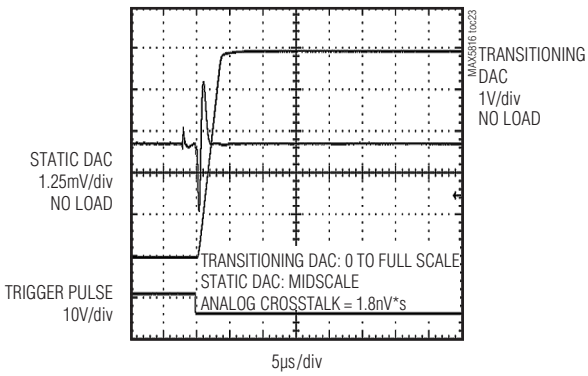
POWER-ON RESET TO 0V



CHANNEL-TO-CHANNEL FEEDTHROUGH
(V_{DD} = V_{REF} = 5V, T_A = +25°C, R_L = 2kΩ, C_L = 200pF)



CHANNEL-TO-CHANNEL FEEDTHROUGH
(V_{DD} = V_{REF} = 5V, T_A = +25°C, NO LOAD)

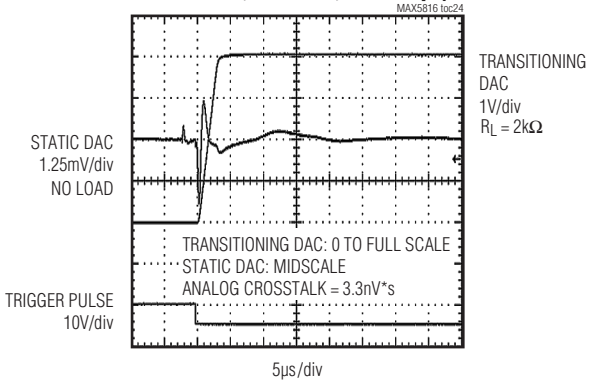


Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

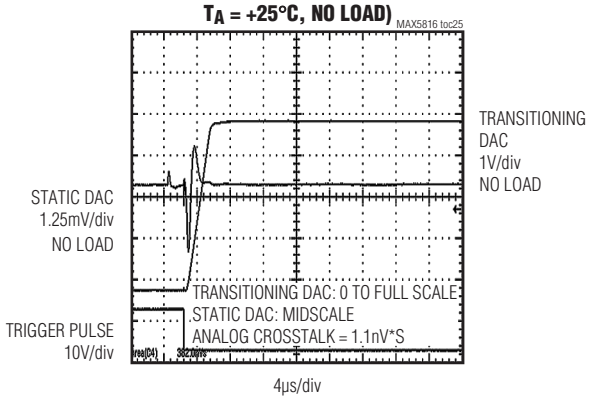
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

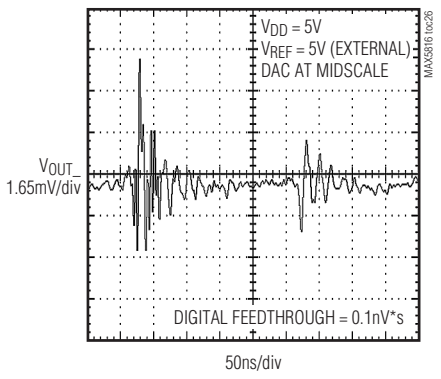
CHANNEL-TO-CHANNEL FEEDTHROUGH (V_{DD} = 5V, V_{REF} = 4.096V (INTERNAL), T_A = +25°C, R_L = 2kΩ, C_L = 200pF)



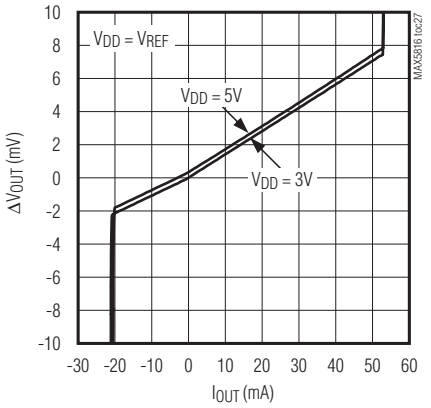
CHANNEL-TO-CHANNEL FEEDTHROUGH (V_{DD} = 5V, V_{REF} = 4.096V (INTERNAL), T_A = +25°C, NO LOAD)



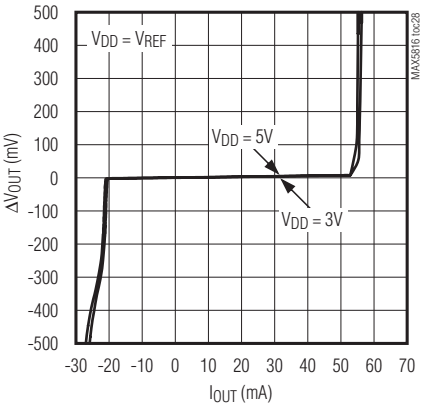
DIGITAL FEEDTHROUGH (V_{DD} = V_{REF} = 5V, R_L = 2kΩ, C_L = 200pF)



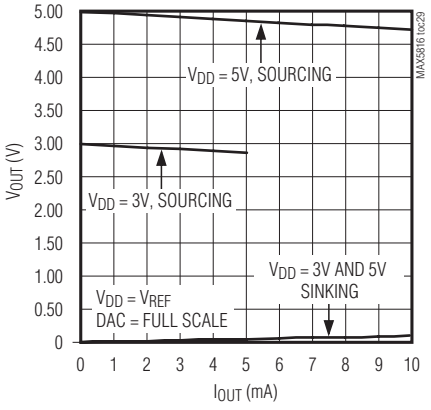
OUTPUT LOAD REGULATION



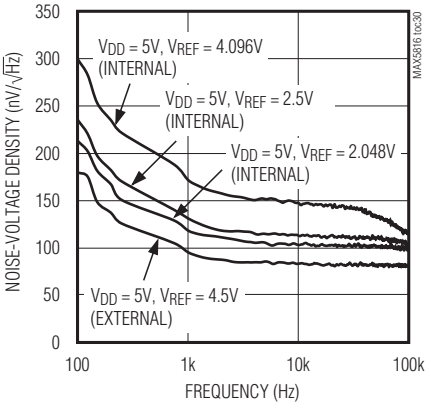
OUTPUT CURRENT LIMITING



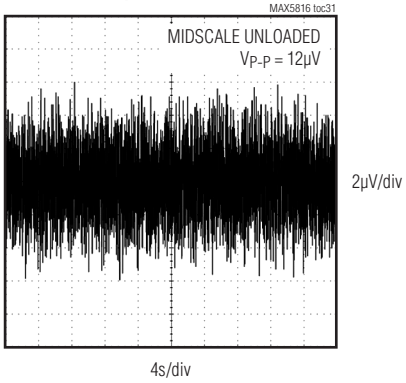
HEADROOM AT RAILS vs. OUTPUT CURRENT



NOISE-VOLTAGE DENSITY VS. FREQUENCY (DAC AT MIDSCALE)



0.1Hz TO 10Hz OUTPUT NOISE, EXTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 4.5V)

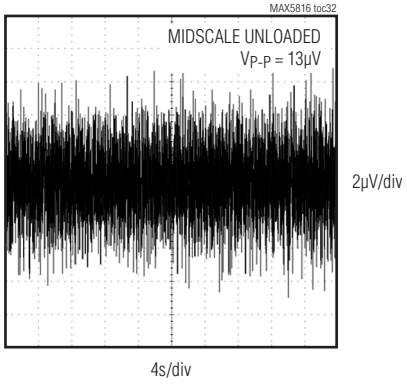


Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

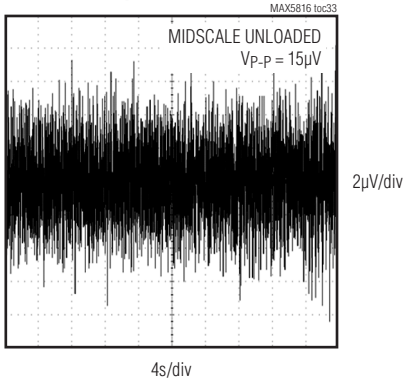
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

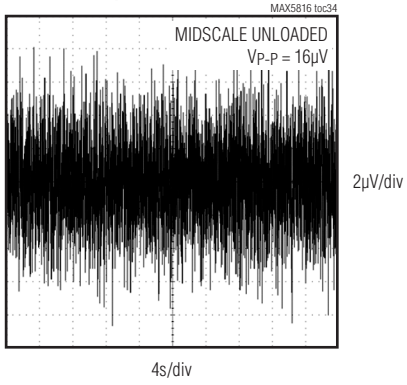
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 2.048V)



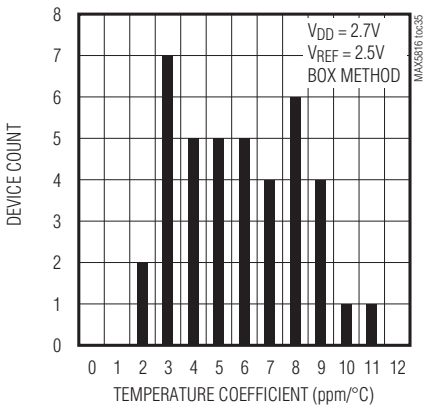
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 2.5V)



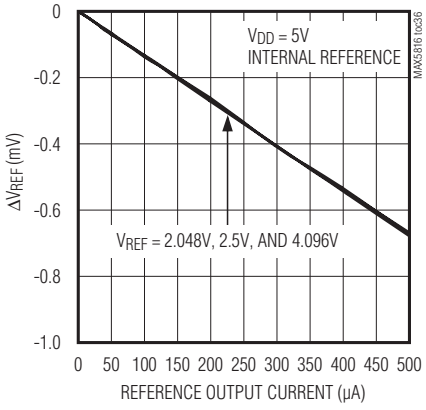
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE (V_{DD} = 5V, V_{REF} = 4.096V)



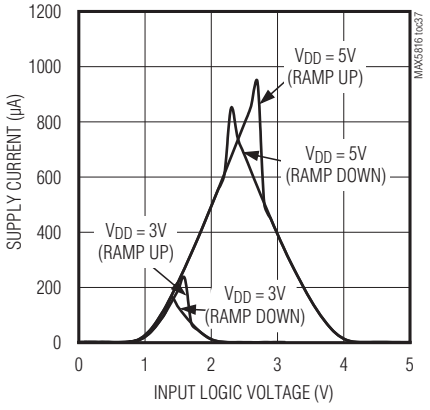
V_{REF} DRIFT vs. TEMPERATURE



REFERENCE LOAD REGULATION

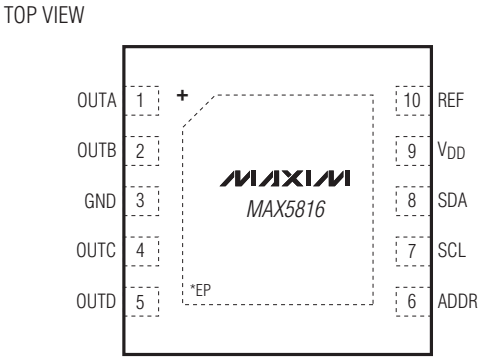


SUPPLY CURRENT vs. INPUT LOGIC VOLTAGE



Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

Pin Configuration



TDFN

Pin Description

PIN	NAME	FUNCTION
1	OUTA	Buffered Channel A DAC Output
2	OUTB	Buffered Channel B DAC Output
3	GND	Ground
4	OUTC	Buffered Channel C DAC Output
5	OUTD	Buffered Channel D DAC Output
6	ADDR	I²C Address Selection Input
7	SCL	Supply Voltage Input. I²C Interface Clock Input
8	SDA	I²C Bidirectional Serial Data
9	V_{DD}	Digital Interface Power-Supply Input. Bypass with a 0.1µF capacitor to GND.
10	REF	Reference Voltage Input/Output
—	EP	Exposed Pad. Connect the exposed pad to ground.

Detailed Description

The MAX5816 is a 4-channel, low-power, 12-bit buffered voltage-output DAC. The 2.7V to 5.5V wide supply voltage range and low-power consumption accommodates most low-power and low-voltage applications. The device presents a 100kΩ load to the external reference. The internal output buffers allow rail-to-rail operation. An internal voltage reference is available with software selectable options of 2.048V, 2.5V, or 4.096V. The device features a fast 400kHz I²C-compatible interface. The MAX5816 includes a serial-in/parallel-out shift register, internal CODE and DAC registers, a power-on-reset (POR) circuit to initialize the DAC outputs to code zero, and control logic.

DAC Outputs (OUT_)

The MAX5816 includes internal buffers on all DAC outputs. The internal output buffers provide improved load regulation for the DAC outputs. The output buffers slew at 1V/µs (typ) and drive up to 2kΩ in parallel with 500pF. Under no-load conditions, the output buffers drive from GND to V_{DD}, subject to offset and gain errors. With a 2kΩ load to GND, the output buffers drive from GND to within 200mV of V_{DD}. With a 2kΩ load to V_{DD}, the output buffers drive to within 200mV of GND and V_{DD}.

The DAC ideal output voltage is defined by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N}$$

where D = code loaded into the DAC register, V_{REF} = reference voltage, N = resolution.

Internal Register Structure

The user interface is separated from the DAC logic to minimize digital feedthrough. Within the serial interface is an input shift register, the contents of which can be routed to control registers, individual, or multiple DACs as determined by the user command.

Within each DAC channel there is a CODE register followed by a DAC latch register (see the *Detailed Functional Diagram*). The contents of the CODE register hold pending DAC output settings which can later be loaded into the DAC registers. The CODE register can be updated using both CODE and CODE_LOAD user commands. The contents of the DAC register hold the current DAC output settings. The DAC register can be updated directly from the serial interface using the CODE_LOAD commands or can upload the current contents of the CODE register using LOAD commands.

The contents of both CODE and DAC registers are maintained during power-down states, so that when the DACs are powered on, they return to their previously stored output settings. Any CODE or LOAD commands issued during power-down states continue to update the register contents. SW_CLEAR and SW_RESET commands (both clear and reset modes) reset the contents of all CODE and DAC registers to their zero-scale defaults.

Internal Reference

The MAX5816 includes an internal precision voltage reference that is software selectable to be 2.048V, 2.500V, or 4.096V. When an internal reference is selected, that voltage is available on the REF pin for other external circuitry (see Figure 9) and can drive a 25kΩ load.

External Reference

The external reference input has a typical input impedance of 100kΩ and accepts an input voltage from +1.24V to V_{DD}. Connect an external voltage supply between REF and GND to apply an external reference. The MAX5816 powers up and resets to external reference mode. Visit **www.maxim-ic.com/products/references** for a list of available external voltage-reference devices.

I²C Serial Interface

The MAX5816 features an I²C-/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL enable communication between the MAX5816 and the master at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX5816 by transmitting the proper slave address followed by the command byte and then the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX5816 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX5816 must transmit the proper slave address followed by a series of nine SCL pulses for each byte of data requested. The MAX5816 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or Repeated START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and

an open-drain output. A pullup resistor, typically 4.7kΩ is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output.

Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX5816 from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals. The MAX5816 can accommodate bus voltages higher than V_{DD} up to a limit of 5.5V; bus voltages lower than V_{DD} are not recommended and may result in significantly increased interface currents.

I²C START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX5816. The master terminates transmission and frees the bus, by issuing a STOP condition. The bus remains active if a Repeated START condition is generated instead of a STOP condition.

I²C Early STOP and Repeated START Conditions

The MAX5816 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. Transmissions ending in an early STOP condition will not impact the internal device settings. If the STOP occurs during a readback byte, the transmission is terminated and a later read mode request will begin transfer of the requested register data from the beginning (this applies to combined format I²C read mode transfers only, interface verification mode transfers will be corrupted). See Figure 2.

I²C Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the R/$\overline{W}$ bit. See Figure 4. The five most significant bits are 00011 with the 2 LSBs determined by ADDR as shown in Table 1. Setting the R/$\overline{W}$ bit to 1 configures the MAX5816 for read mode.

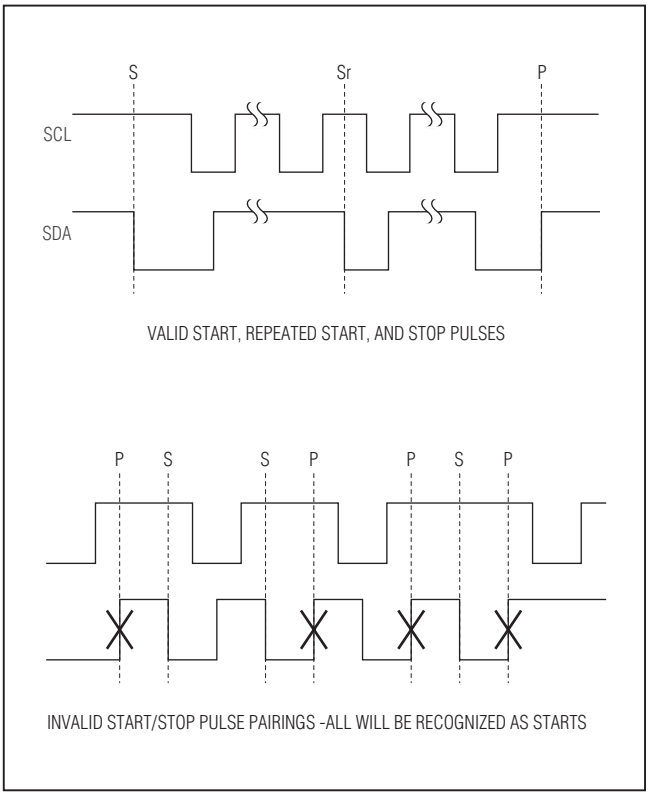


Figure 2. I²C START, Repeated START, and STOP Conditions

Setting the R/$\overline{W}$ bit to 0 configures the MAX5816 for write mode. The slave address is the first byte of information sent to the MAX5816 after the START condition.

The MAX5816 has the ability to detect an unconnected state on the ADDR input for additional address flexibility; if leaving the ADDR input unconnected, be certain to minimize all loading on the pin (i.e. provide a landing for the pin, but do not allow any board traces).

Table 1. I²C Slave Address LSBs for TDFN Package

ADDR	A1	A0
V_{DD}	0	0
N.C.	1	0
GND	1	1

I²C Broadcast Address

A broadcast address is provided for the purpose of updating or configuring all MAX5816 devices on a given I²C bus. All MAX5816 devices acknowledge and respond to the broadcast device address 00010000. The devices will respond to the broadcast address, regardless of the state of the address pins. The broadcast mode is intended for use in write mode only (as indicated by R/$\overline{W}$ = 0 in the address given).

I²C Acknowledge

In write mode, the acknowledge bit (ACK) is a clocked 9th bit that the MAX5816 uses to handshake receipt of each byte of data as shown in Figure 3. The MAX5816 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication.

In read mode, the master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX5816 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX5816, followed by a STOP condition.

I²C Command Byte and Data Bytes

A command byte follows the slave address. A command byte is typically followed by two data bytes unless it is the last byte in the transmission. If data bytes follow the command byte, the command byte indicates the address of the register that is to receive the following two data bytes. The data bytes are stored in a temporary register and then transferred to the appropriate register during the ACK periods between bytes. This avoids any glitching or digital feedthrough to the DACs while the interface is active.

I²C Write Operations (Standard Protocol)

A master device communicates with the MAX5816 by transmitting the proper slave address followed by command and data words. Each transmit sequence is framed by a START or Repeated START condition and a STOP condition as described above. Each word is 8 bits long and is always followed by an acknowledge clock (ACK) pulse as shown in the Figure 4 and Figure 5. The first byte contains the address of the MAX5816 with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the command (or register) to be written and the third and fourth bytes contain the data to be written. By repeating the command plus data byte pairs (Byte #2 through Byte #4 in Figure 4 and Figure 5), the user can execute multiple command writes using a single I²C write sequence. There is no limit as to how many commands the user can execute with a single write sequence. The MAX5816 supports this capability for all user-accessible write mode commands.

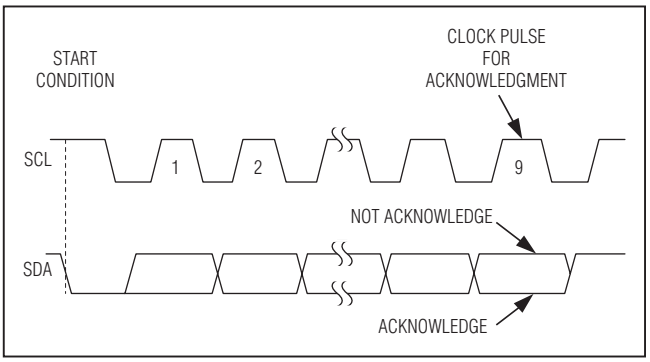


Figure 3. I²C Acknowledge

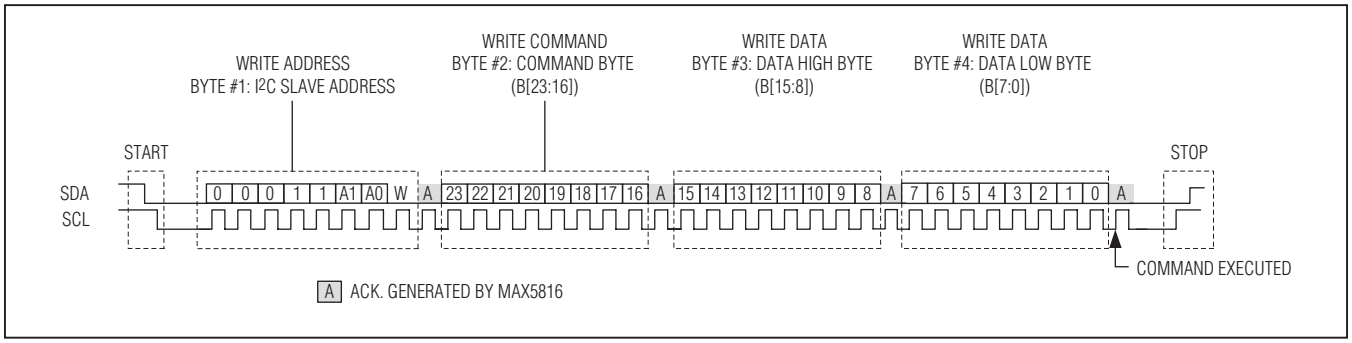


Figure 4. I²C Single Register Write Sequence

I²C Write Operation (Multibyte Operation)

The MAX5816 supports a multibyte transfer protocol for some commands. In multibyte mode, once a command is issued (with multibyte bit = 1), that command is continuously executed based on two byte data blocks for the duration I²C operation. Essentially, bytes 1 to 4 are processed normally, but for every two bytes of data provided after byte 4, the originally requested command is executed again with the latest byte pair provided as input data. Multibyte protocol is enforced until a STOP condition (or repeated START) is encountered, this provides a higher speed transfer mode that is useful in servo DAC applications.

Combined Format I²C Readback Operations

Each readback sequence is framed by a START or Repeated START condition and a STOP condition. Each word is 8 bits long and is followed by an acknowledge clock pulse as shown in Figure 6. The first byte contains the address of the MAX5816 with R/$\overline{W}$ = 0 to indicate a write. The second byte contains the register that is to be read back. There is a Repeated START condition, followed by the device address with R/$\overline{W}$ = 1 to indicate a read and an acknowledge clock. The master has control of the SCL line but the MAX5816 takes over the SDA line. The final two bytes in the frame contain the register data readback followed by a STOP condition. If additional bytes beyond those required to readback the requested data are provided, the MAX5816 will continue to readback ones.

Readback of individual CODE registers is supported for all the user CODE commands. For these commands, which support a DAC address, the requested channel CODE register content will be returned; if all DACs are selected, CODE A content will be returned.

Readback of individual DAC registers is supported for all user LOAD and CODE_LOAD commands. For these commands, which support a DAC address, the requested DAC register content will be returned. If all DACs are selected, DACA content will be returned.

Modified readback of the POWER register is supported for the POWER command. The power status of each DAC is reported in locations B[3:0], with a 1 indicating the DAC is powered down and a zero indicating the DAC is operational (see Table 2).

Readback of all other registers is not directly supported. All requests to read unsupported registers reads back the device's reference status device ID and revision information in the format is shown in Table 2.

Interface Verification I²C Readback Operations

While the MAX5816 supports standard I²C readback of selected registers, it is also capable of functioning in an interface verification mode. This mode is accessed any time a readback operation follows an executed write mode command. In this mode, the last executed three-byte command is read back in its entirety. This behavior allows verification of the interface.

Sample command sequences are shown in Figure 7. The first command transfer is given in write mode with R/$\overline{W}$ = 0 and must be run to completion to qualify for interface verification readback. There is now a STOP/START pair or Repeated START condition required, followed by the readback transfer with R/$\overline{W}$ = 1 to indicate a read and an acknowledge clock from the MAX5816. The master still has control of the SCL line but the MAX5816 takes over the SDA line. The final three bytes in the frame contain the command and register data written in the first transfer presented for readback, followed by a STOP condition. If additional bytes beyond those required to read back the requested data are provided, the MAX5816 will continue to read back ones.

Table 2. Standard I²C User Readback Data

COMMAND BYTE (REQUEST)								READBACK DATA HIGH BYTE								READBACK DATA LOW BYTE							
R7	R6	R5	R4	R3	R2	R1	R0	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	X	0	0	0	A2	A1	A0	CODEn[11:4]								CODEn[3:0]				0	0	0	0
0	X	0	0	1	A2	A1	A0	DACn[11:4]								DACn[3:0]				0	0	0	0
0	X	0	1	0	A2	A1	A0	DACn[11:4]								DACn[3:0]				0	0	0	0
0	X	0	1	1	A2	A1	A0	DACn[11:4]								DACn[3:0]				0	0	0	0
0	X	1	0	0	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	PWD	PWC	PWB	PWA
0	X	1	0	1	X	X	X	1	0	0	0	1	0	0	0	0	1	0	REV_ID [2:0] (010)			REF MODE [1:0]		
0	X	1	1	0	X	X	X																
0	X	1	1	1	X	X	X																

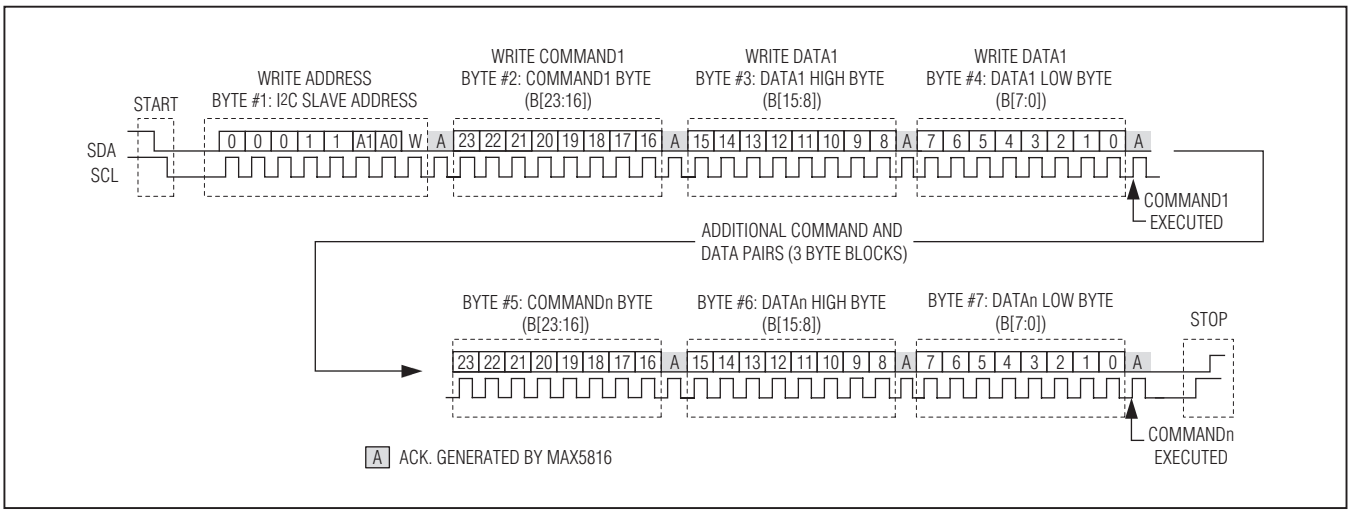


Figure 5. Multiple Register Write Sequence (Standard I²C Protocol)

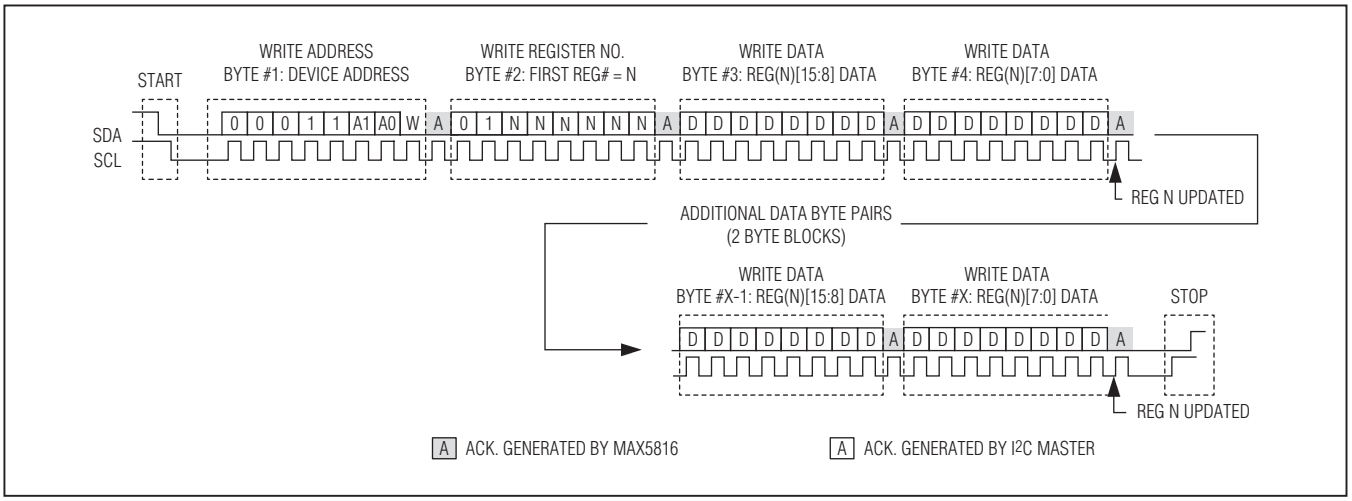


Figure 6. I²C Multibyte Register Write Sequence (Multibyte Protocol)

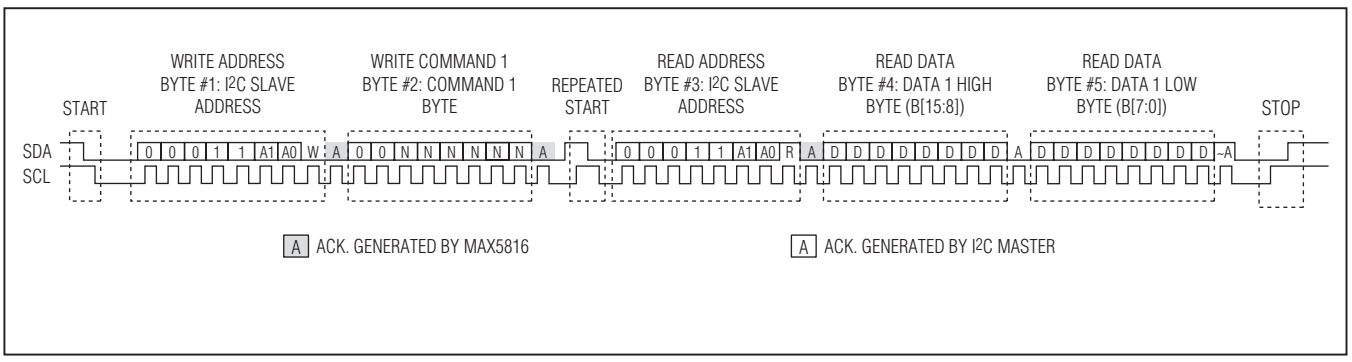


Figure 7. Standard I²C Register Read Sequence

Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

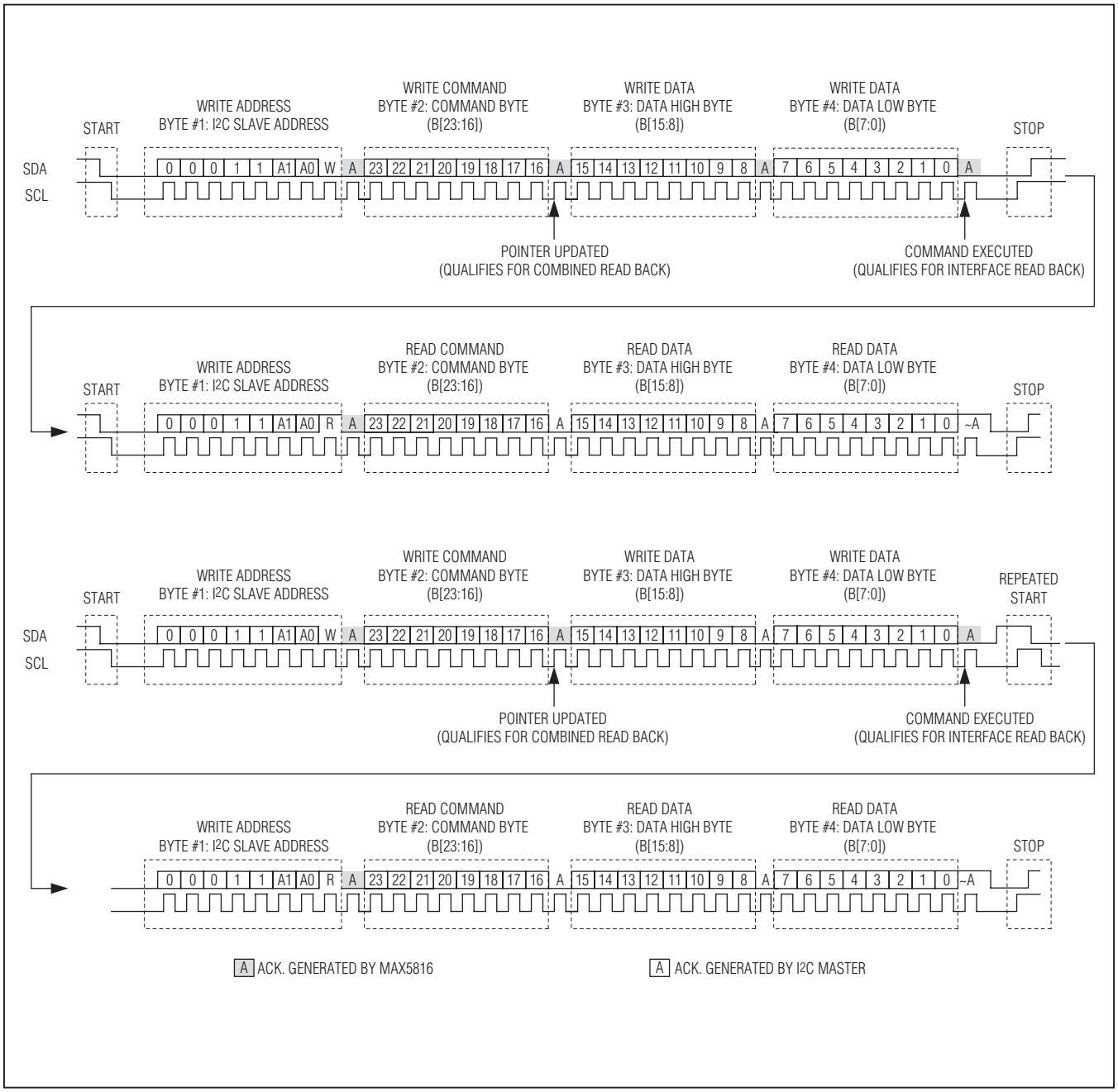


Figure 8. Interface Verification I²C Register Read Sequences

It is not necessary for the write and read mode transfers to occur immediately in sequence. I²C transfers involving other devices do not impact the MAX5816 readback mode. Toggling between readback modes is based on the length of the preceding write mode transfer. Combined format I²C readback operation is resumed if a write command greater than two bytes but less than four bytes is supplied. For commands written using multiple register write sequences, only the last command executed is read back. For each command written, the readback sequence can only be completed one time; partial and/or multiple attempts to readback executed in succession will not yield usable data.

I²C Compatibility

The MAX5816 is fully compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain which pulls the data line low to transmit data or ACK pulses. Figure 9 shows a typical I²C application.

I²C User-Command Register Map

This section lists the user accessible commands and registers for the MAX5816.

Table 3 provides detailed information about the Command Registers.

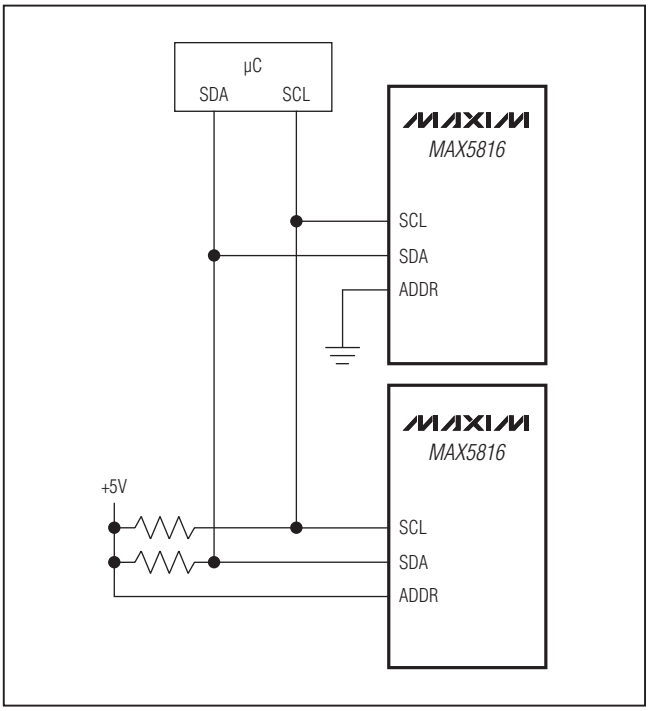


Figure 9. Typical I²C Application Circuit

Table 3. I2C Commands Summary

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION
DAC COMMANDS																									
CODEn	0	0	0	0	0	DAC ADDRESS			CODE REGISTER DATA [11:4]								CODE REGISTER DATA [3:0]				X	X	X	X	Writes data to the selected CODE register(s).
LOADn	0	0	0	0	1	DAC ADDRESS			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Transfers data from the selected CODE registers to the selected DAC register(s).
CODEn_ LOAD_ ALL	0	0	0	1	0	DAC ADDRESS			CODE REGISTER DATA [11:4]								CODE REGISTER DATA [3:0]				X	X	X	X	Simultaneously writes data to the selected CODE register(s) while updating all DAC registers.
CODEn_ LOADn	0	0	0	1	1	DAC ADDRESS			CODE REGISTER DATA [11:4]								CODE REGISTER DATA [3:0]				X	X	X	X	Simultaneously writes data to the selected CODE register(s) while updating selected DAC register(s).

Table 3. I2C Commands Summary (continued)

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION
CONFIGURATION COMMANDS																									
POWER	0	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	Power Mode 00 = Normal 01 = PD 1kΩ 10 = PD 100kΩ 11 = PD Hi-Z		DAC D		DAC C		DAC B	DAC A	Sets the Power Mode of the selected DACs (DACs selected with a 1 in the corresponding DACn bit are updated, DACs with a 0 in the corresponding DACn bit are not impacted).
SW_ RESET or SW_ CLEAR	0	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0 = CLR 1 = RST	Executes a software reset (all registers returned to their default values) or clear (all CODE and DAC registers cleared to their default values).
CONFIG	0	X	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DAC D	DAC C	DAC B	DAC A	Sets the DAC Latch Mode of the corresponding DAC: 0 = DAC latch is LOAD controlled 1 = DAC latch is transparent.
REF	0	X	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	REF Power Mode		REF Mode 00 = EXT 01 = 2.5V 10 = 2.0V 11 = 4.1V	Sets the reference operating mode. REF Power (B2): 0 = Internal reference is only powered if at least one DAC is powered 1 = Internal reference is always powered.

Table 3. I2C Commands Summary (continued)

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION
MULTIBYTE DAC COMMANDS																									
CODEn Multibyte	0	1	0	0	0	DAC ADDRESS			CODE REGISTER DATA[11:4]												CODE REGISTER DATA[3:0]				X	X	X	Writes data to the selected CODE register(s) (multibyte variant).
LOADn Multibyte	0	1	0	0	1	DAC ADDRESS			X	X	X	X					X	X	X	X					X	X	X	Transfers data from the selected CODE registers to the selected DAC register(s) (multibyte variant).
CODEn_ LOAD_ ALL Multibyte	0	1	0	1	0	DAC ADDRESS			CODE REGISTER DATA[11:4]												CODE REGISTER DATA[3:0]				X	X	X	Simultaneously writes data to the selected CODE register(s) while updating all DAC registers (multibyte variant).
CODEn_ LOADn Multibyte	0	1	0	1	1	DAC ADDRESS			CODE REGISTER DATA[11:4]												CODE REGISTER DATA[3:0]				X	X	X	Simultaneously writes data to the selected CODE register(s) while updating selected DAC register(s) (multibyte variant).

Table 4. DAC Selection

B18	B17	B16	DAC SELECTED
0	0	0	DAC A
0	0	1	DAC B
0	1	0	DAC C
0	1	1	DAC D
1	X	X	ALL DACs

CODEn Command

The CODEn command updates the CODE register contents for the selected DAC(s). Changes to the CODE register content based on this command will not affect DAC outputs directly unless the latch has been configured to be transparent (see the CONFIG command). In order to update CODE register content of all DACs, use the CODEn command with DAC selection = 1XX = all DACs. The CODEn command supports the multibyte protocol. See Table 3 and Table 5.

Table 5. CODEn (000) Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	M	0	0	0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
Reserved	Multibyte	CODEn Command			Dac Address			Code Register Data [11:4]								Code Register Data [3:0]				Don't Care			
Data Default Value →								0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
Command Byte								Data High Byte								Data Low Byte							

LOADn Command

The LOADn command (B[23:20] = 0001) updates the DAC register content for the selected DAC(s) by uploading the current contents of the CODE register. The LOADn command can be used with DAC SELECTION = 1XX = ALL DACs to issue a software load for all DACs, which does not alter the existing content of any CODE register (unlike CODEn_LOAD_ALL command). See Table 3 and Table 6. The LOADn command supports the multibyte protocol.

Table 6. LOADn (001) Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	M	0	0	1	A2	A1	A0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Reserved	Multibyte	LOADn Command			DAC Address			Don't Care								Don't Care							
Command Byte								Data High Byte								Data Low Byte							

CODEn_LOAD_ALL Command

The CODEn_LOAD_ALL command updates the CODE register contents for the selected DAC(s) as well as the DAC register content of all DACs. Channels for which the CODE register content has not been modified since the last load to DAC register will not be updated to reduce digital crosstalk. The CODEn_LOAD_ALL command by definition will modify at least one CODE register. To avoid this, use the LOADn command with DAC SELECTION = ALL DACs. The CODEn_LOAD_ALL command supports the multibyte protocol. See Table 3 and Table 7.

Table 7. CODEn_LOAD_ALL (010) Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	M	0	1	0	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
Reserved	Multibyte	CODEn_ LOAD_ ALL Command			DAC Address			Code Register Data[11:4]								Code Register Data [3:0]				Don't Care			
Data Default Value →								0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
Command Byte								Data High Byte								Data Low Byte							

CODEn_LOADn Command

The CODEn_LOADn command updates the CODE register contents for the selected DAC(s) as well as the DAC register content of the selected DAC(s). Channels for which the CODE register content have not been modified since the last load to DAC register will not be updated to reduce digital crosstalk. See Table 3 and Table 8.

Table 8. CODEn_LOADn (011) Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	M	0	1	1	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
Reserved	Multibyte	CODEn_LOADn Command			DAC Address			Code Register Data [11:4]								Code Register Data [3:0]				Don't Care			
Data Default Value →								0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
Command Byte								Data High Byte								Data Low Byte							

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POWER Command

The MAX5816 features a software-controlled power-mode (POWER) command. The POWER command updates the power-mode settings of the selected DACs while the power settings of the remaining of the DACs remain unchanged. The new power setting is determined by bits B[5:4] while the affected DAC(s) are selected by bits B[3:0]. If all DACs are powered down, the device enters a STANDBY mode.

In power-down, the output is disconnected from the buffer and is grounded when one of the two selectable internal resistors or set to high impedance. See Table 9 for the selectable internal resistor values in power-down mode. In STANDBY mode, the DAC register retains its value so that the output is restored when the device powers up. The serial interface remains active in power-down mode.

In powered down mode, the internal reference can be powered down or it can be set to remain powered-on for external use in STANDBY mode, parts using external reference do not load the REF. See Table 9.

Table 9. POWER (100) Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	PD1	PD0	D	C	B	A
Reserved	Don't Care	POWER Command			Don't Care			Don't Care								Don't Care		Power Mode: 00 = Normal mode 01 = 1kΩ 10 = 100kΩ 11 = Hi-Z		DAC Selection			
Data Default Value →								X	X	X	X	X	X	X	X	X	X	0	0	1	1	1	1
Command Byte								Data High Byte								Data Low Byte							

SW_RESET and SW_CLEAR Command

The SW_RESET and SW_CLEAR commands provide a means of issuing a software reset or software clear operation. Set B0 = 0 to issue a software clear operation to return all CODE and DAC registers to the zero-scale value. Set B0 = 1 to reset all CODE, DAC, and configuration registers to their default values. See Table 10.

Table 10. SW_RESET (101) Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R0
Reserved	Don't Care	SW_RESET or SW_CLEAR Command			Don't Care			Don't Care								Don't Care							0 = Clear 1= Reset
Data Default Value →								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
Command Byte								Data High Byte								Data Low Byte							

CONFIG Command

The CONFIG command allows independent configurations of the DAC. In normal mode (0), the DAC latch is operational and responds to LOAD commands. In transparent mode (1), the DAC latch is transparent and CODE register contents are supplied directly to the DAC outputs. See Table 11.

Table 11. CONFIG Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	X	1	1	0	X	X	X	X	X	X	X	D	C	B	A	X	X	X	X	D	C	B	A
Reserved	Don't Care	CONFIG Command			Don't Care			Don't Care								Don't Care				DAC Latch Mode 0 = Operational 1 = Transparent			
Data Default Value →								X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0
Command Byte								Data High Byte								Data Low Byte							

REF Command

The REF command updates the global reference setting used for all DAC channels. Set B[1:0] = 00 to use an external reference for the DACs or set B[1:0] to 01, 10, or 11 to select either the 2.500V, 2.048V, or 4.096V internal reference, respectively.

If RF2 (B2 = 0) is set to zero (default) in the REF command, the reference will be powered down any time all DAC channels are powered down (in STANDBY mode). If RF2 is set to one, the reference will remain powered even if all DAC channels are powered down, allowing continued operation of external circuitry. In this mode the 1µA shutdown state is not available. See Table 12.

Table 12. REF Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	X	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RF2	RF1	RF0
Reserved	Don't Care	REF Command			Don't Care			Don't Care								Don't Care					0 = Default 1 = Always On	REF Mode: 00 = Ext 01 = 2.500V 10 = 2.048V 11 = 4.096V	
Data Default Value →								X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0
Command Byte								Data High Byte								Data Low Byte							

Applications Information

Power-On Reset (POR)

When power is applied to V_{DD}, the DAC output is set to zero scale. To optimize DAC linearity, wait until the supplies have settled and the internal setup and calibration sequence completes (200µs, typ). Note all commands issued during the period will be ignored.

Power Supplies and Bypassing Considerations

Bypass V_{DD} with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect the GND to the analog ground plane.

Layout Considerations

Digital and AC transient signals on GND can create noise at the output. Connect GND to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5816 GND. Carefully layout the traces between channels to reduce AC cross-coupling. Do not use wire-wrapped boards and sockets. Use shielding to minimize noise immunity. Do not run analog and digital signals parallel to one another, especially clock signals. Avoid routing digital lines underneath the MAX5816 package.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a straight line drawn between two codes once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL ≤ 1 LSB, the DAC guarantees no missing codes and is monotonic. If the magnitude of the DNL ≥ 1 LSB, the DAC output may still be monotonic.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. Typically, the point at which the offset error is specified is at or near the zero-scale point of the transfer function.

Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

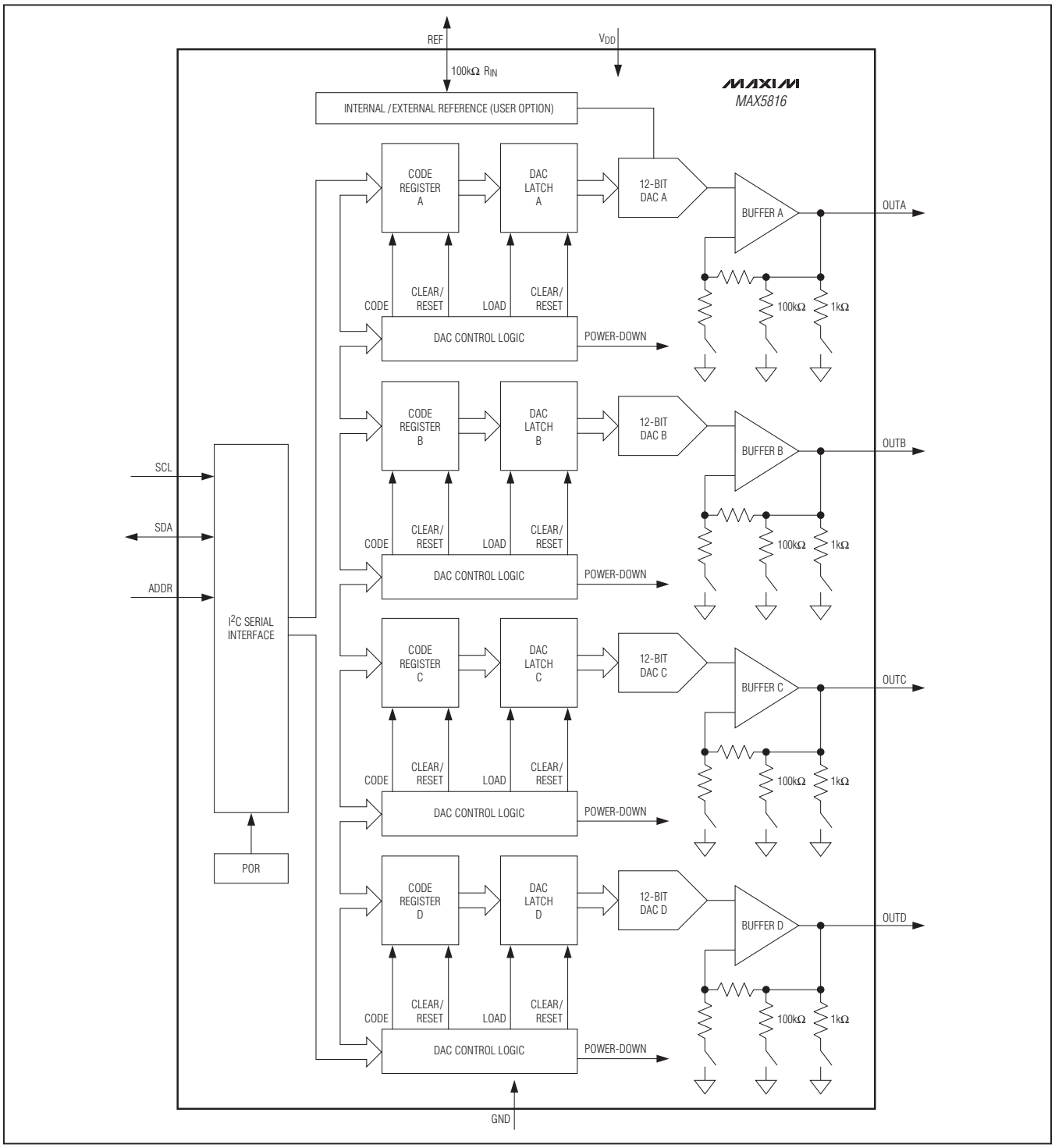
Digital-to-Analog Glitch Impulse

A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

Detailed Functional Diagram



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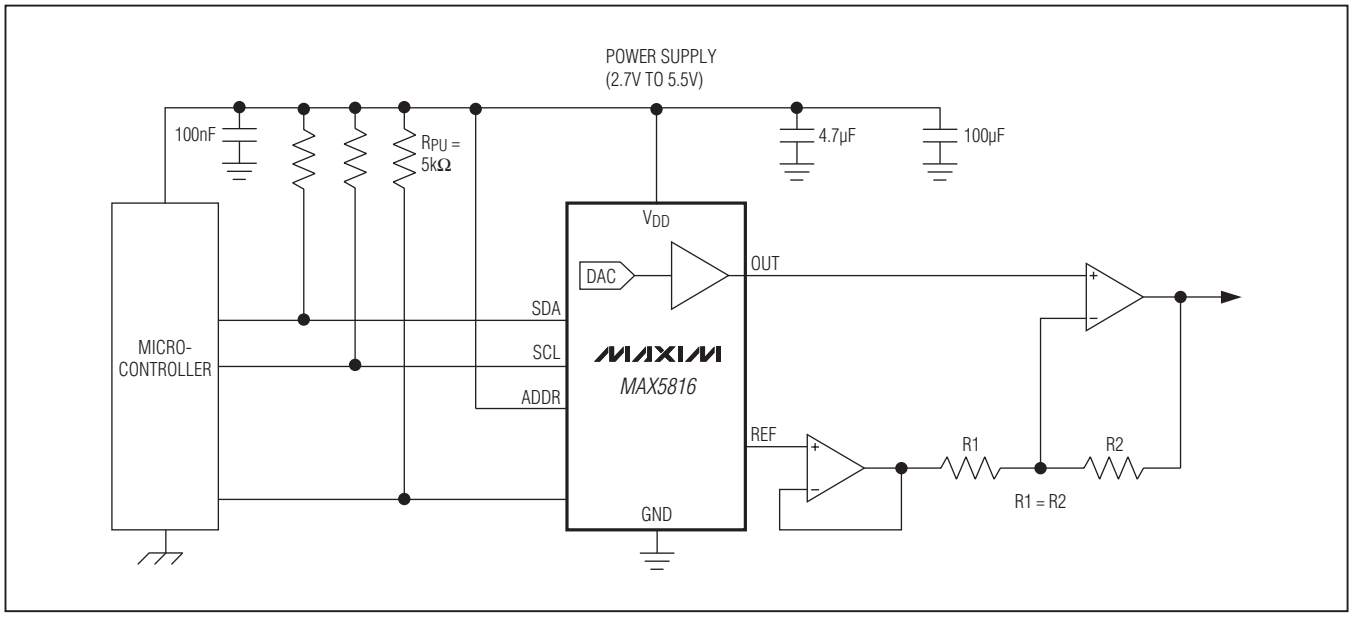
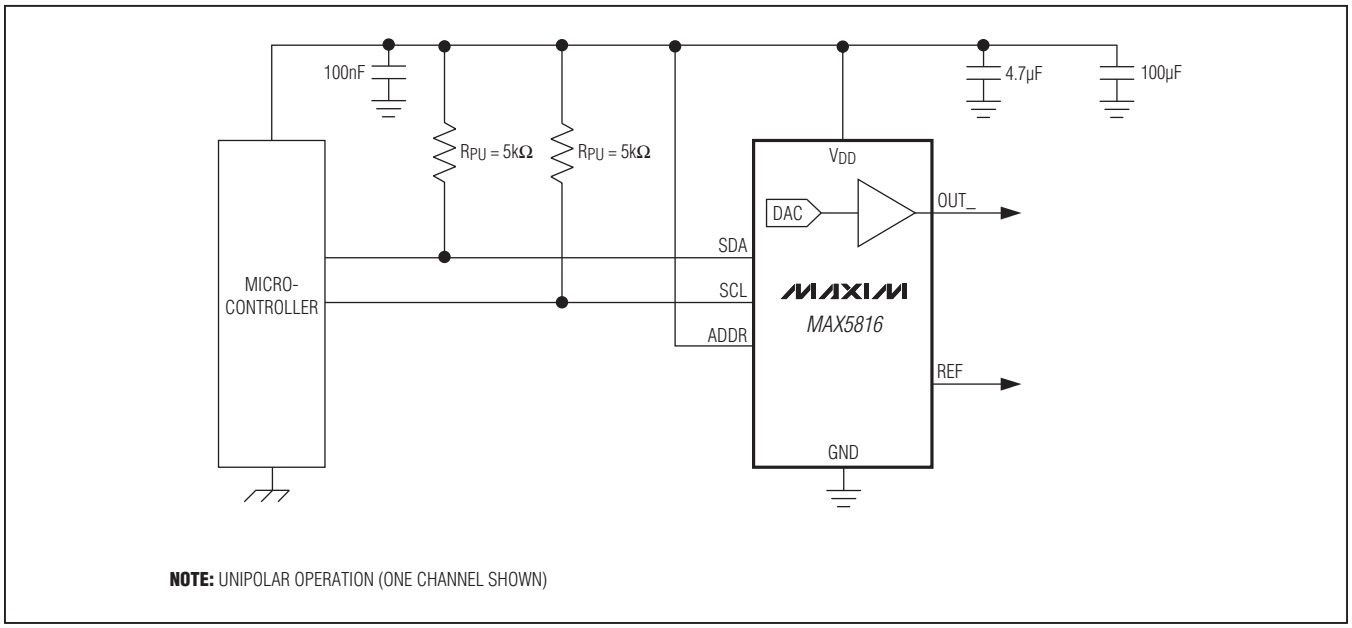


Figure 10. Bipolar Operating Circuit

Typical Operating Circuit



NOTE: UNIPOLAR OPERATION (ONE CHANNEL SHOWN)

Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

Ordering Information

PART	PIN-PACKAGE	RESOLUTION (BIT)	INTERNAL REFERENCE TEMPCO (ppm/°C)
MAX5816ATB+T	10 TDFN-EP*	12	10 (typical)

Note: *The device is specified over the -40°C to +125°C temperature range.*
+Denotes a lead(Pb)–free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP	T1033+1	21-0137	90-0003

Ultra-Small, Quad-Channel, 12-Bit Buffered Output DAC with Internal Reference and I²C Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/12	Initial release	—

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