MAX5868

16-Bit, 5Gsps Interpolating and Modulating RF DAC

General Description

The MAX5868 high-performance interpolating and modulating 16-bit 5Gsps RF DAC can directly synthesize up to 500MHz of instantaneous bandwidth from DC to frequencies greater than 2GHz. The device is optimized for cable and digital video broadcast applications and meets spectral mask requirements for a broad set of communication standards including EPoC, DVB-T, DVB-T2, DVB-C2, ISDB-T, and DOCSIS 3.0/3.1.

The device integrates interpolation filters, a digital quadrature modulator, a numerically controlled oscillator (NCO) and a 14-bit RF DAC core. The user-configurable 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x or 24x, linear phase interpolation filters reduce the input data bandwidth required from an FPGA/ASIC. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis.

The MAX5868 includes a source synchronous 16-bit parallel LVDS data input interface. The input baseband I and Q signals are time interleaved on a single parallel input port configured for double data rate clocking at up to 1240Mwps (620Mwps I and Q each). The device accepts data in word (16 bit), byte (8 bit), or nibble (4 bit) modes. The input data is aligned to the data clock supplied with the data. An input FIFO decouples the timing of the input interface from the DAC update clock domain. In addition, a parity input and parity flag interrupt output are available to ensure data integrity.

The MAX5868 clock input has a flexible clock interface and accepts a differential sine-wave or square-wave input clock signal. The device outputs a divided reference clock to ensure synchronization with the FPGA/ASIC driving its input port. In addition, dedicated input and output signals are provided for synchronizing multiple devices.

The MAX5868 uses a differential current-steering architecture and can produce a 0dBm full-scale output signal level with a 50Ω load. Operating from 1.8V and 1.0V power supplies, the device consumes 1.5W at 5Gsps. The device is offered in a compact 144-pin CSBGA package and is specified for the extended temperature range (-40°C to +85°C).

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX5868.related.

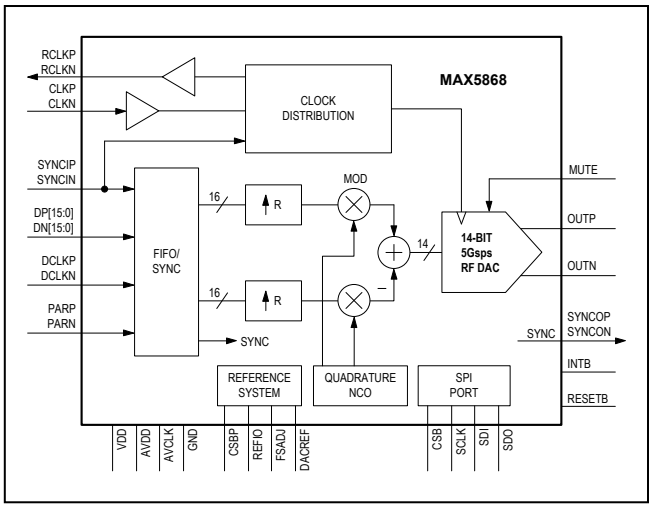
Features and Benefits

- Direct RF Synthesis Solution for Communications
  - 4.96Gsps DAC Output Update Rate
  - High-Performance 14-Bit RF DAC Core
  - Digital Quadrature Modulator and NCO with 1Hz/10Hz/100Hz/1kHz/10kHz Resolution
  - 4x/5x/6x/8x/10x/12x/16x/20x/24x Interpolation
  - 16-Bit 1240Mwps DDR Parallel LVDS Data Bus
- Highly Flexible and Configurable
  - Data Bus with Word, Byte and Nibble Modes
  - Reference Clock Output for FPGA Interface
  - Multiple DAC Synchronization
  - SPI Interface for Device Configuration
- Low Power, Compact Solution
  - 1.5W at f_{CLK} = 5Gsps
  - 10mm x 10mm, 144-Pin CSBGA

Applications

- Ethernet PON over Coax (EPoC)
- Downstream DOCSIS CMTS Modulators
- Digital Video Broadcast
  DVB-T / DVB-T2 / DVB-C2 / ISDB-T Modulators

Simplified Block Diagram



Ordering Information ***appears at end of data sheet.***

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Absolute Maximum Ratings

AVDD2, AVCLK2, V_{DD2}.....-0.3V to +2.1V
OUTP, OUTN..... -0.3V to (V_{AVDD2} + 0.5V)
MUTE, RESETB, CSB, SCLK,
SDO, SDI, INTB..... -0.3V to (V_{DD2} + 0.3V, 2.1V Max)
SINCIP, SYNCIN, SYNCOP, SYNCON, DCLKP, DCLKN,
RCLKP, RCLKN..... -0.3V to (V_{DD2} + 0.3V, 2.1V Max)
DP0, DN0, DP1, DN1, DP2, DN2, DP3, DN3,
DP4, DN4 ..... -0.3V to (V_{DD2} + 0.3V, 2.1V Max)
DP5, DN5, DP6, DN6, DP7, DN7, DP8, DN8,
DP9, DN9 ..... -0.3V to (V_{DD2} + 0.3V, 2.1V Max)
DP10, DN10, DP11, DN11, DP12, DN12, DP13,
DN13..... -0.3V to (V_{DD2} + 0.3V, 2.1V Max)
DP14, DN14, DP15, DN15,
PARP, PARN.....0.3V to (V_{DD2} + 0.3V, 2.1V Max)
AVDD, AVCLK, V_{DD} .....-0.3V to +1.2V
REFIO, DACREF,
FSADJ, CSBP .....0.3V to (V_{AVDD2} + 0.3V, MAX 2.1V)
CLKP, CLKN.....-0.3V to (V_{AVCLK2} + 0.3V, MAX 2.1V)
Continuous Power Dissipation (T_A = +70°C)
CSBGA (derate 38.8mW/°C above +70°C) 3101mW
SDO, INTB Maximum Continuous Current 8mA
Operating Temperature Range
T_A ..... -40°C to +85°C
T_J ..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -60°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

CSBGA
Junction-to-Case Thermal Resistance (θ_{JC}).....12.9°C/W
Junction-to-Board Thermal Resistance (θ_{JB}).....6.23°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....25.8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 10x interpolation, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF. $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +115°C, unless otherwise noted. Typical values are at T_J = +60°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Input Data Word Width				16		Bits
DAC Resolution				14		Bits
Differential Nonlinearity	DNL	Figure 4		±1.5		LSB
Integral Nonlinearity	INL	Figure 4		±3		LSB
Offset Voltage Error	OS			0.003		%FS
Full-Scale Output Current Range	I_{OUTFS}		10		30	mA
Output Voltage Gain Error	GE_{FS}	f_{OUT} = DC, Figure 4		±3		%FS
Output Power	P_{OUT}	f_{OUT} = 100MHz, f_{CLK} = 4.96GHz		0		dBm
Maximum Output Compliance		Typical maximum single-ended output voltage		V_{AVDD2} + 0.4		V
Minimum Output Compliance		Typical minimum single-ended output voltage		V_{AVDD2} - 0.4		V
Output Resistance	R_{OUT}	Differential DAC output resistance		50		Ω

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 10x interpolation, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF. $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +115°C, unless otherwise noted. Typical values are at T_J = +60°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
DAC Clock Frequency	f_{CLK}	(Note 3)				4960	MHz
Adjusted DAC Update Rate	AUR_{DAC}	(Note 4)				1240	Msps
Maximum Data Clock Frequency	$f_{DATACLK}$	(Note 5)			620		MHz
Maximum Input Data Rate	f_{DATA}	DDR interleaved data			1240		Mwps
Out-of-Band Noise and Spurious Eight 6MHz QAM Carriers Average Total Power = -15dBm	ACPR	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)	8x interpolation, f_{OUT} = 575MHz, f_{DATA} = 1152Mwps, f_{CLK} = 4608MHz		-67		dBc
		Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)			-69		
		Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)			-69		
		Noise in any other channel			-67		
		Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)	8x interpolation, f_{OUT} = 975MHz, f_{DATA} = 1152Mwps, f_{CLK} = 4608MHz		-65		
		Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)			-68		
		Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)			-67		
		Noise in any other channel			-64		

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 10x interpolation, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF. $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +115°C, unless otherwise noted. Typical values are at T_J = +60°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Adjacent Channel Power Ratio Thirty-Two 6MHz QAM Carriers 192MHz Wideband Average Total Output Power = -17dBm	ACPR	Adjacent channel (from channel block edge to 192MHz from channel block edge)	f_{OUT} = 1100MHz, f_{DATA} = 1152Mwps, f_{CLK} = 4608MHz		-59		dBc
		Next-adjacent channel (192MHz from channel block edge to 384MHz from channel block edge)			-59		
		Adjacent channel (from channel block edge to 192MHz from channel block edge)	f_{OUT} = 1600MHz, f_{DATA} = 1152Mwps, f_{CLK} = 4608MHz		-57		
		Next-adjacent channel (192MHz from channel block edge to 384MHz from channel block edge)			-57		
Harmonic Distortion Eight 6MHz QAM Carriers Average Total Power = -15dBFS	HD	Second harmonic distortion	f_{OUT} = 400MHz, f_{DATA} = 1152Mwps, f_{CLK} = 4608MHz, 8x interpolation		-66		dBc
		Third harmonic distortion			-67		
Output Settling Time for Full-Scale Input Step (Note 6)		To ±0.024% of output full-scale, 4x interpolation	f_{CLK} = 2460MHz		32		ns
		To ±0.024% of output full-scale, 10x interpolation	f_{CLK} = 4915.2MHz		41		
Output Bandwidth		f_{DAC} = 4915.2MHz, -1dB bandwidth (Note 7)			2250		MHz

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 10x interpolation, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF. $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +115°C, unless otherwise noted. Typical values are at T_J = +60°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERPOLATION FILTERS						
Interpolation Rates	R			4, 5, 6, 8, 10, 12, 16, 20, 24		
Passband Width	PBW	Ripple < 0.01dB		0.407 x f_{DAC}/R		
Stopband Rejection		0.5 x f_{DAC}/R		90		dB
Data Latency		4x interpolation		288		Clock Cycles
		5x interpolation		382		
		6x interpolation		420		
		8x interpolation		496		
		10x interpolation		673		
		12x interpolation		764		
		16x interpolation		864		
		20x interpolation		1137		
		24x interpolation		1317		
NCO						
Maximum Frequency				f_{CLK}/2		Hz
Frequency Control Word Resolution				32		Bits
SNR				86.5		dB
SFDR				92.4		dBc
REFERENCE						
Reference Input Range			1.10		1.30	V
Reference Output Voltage	V_{REFIO}	Internal reference	1.10	1.20	1.30	V
Reference Input Resistance	R_{REFIO}			10		kΩ
Reference Voltage Drift				±65		ppm/°C

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 10x interpolation, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF. $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +115°C, unless otherwise noted. Typical values are at T_J = +60°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS LOGIC INPUTS/OUTPUTS (INTB, RESETB, MUTE, CSB, SCLK, SDI, SDO)							
Input High Voltage	V_{IH}			0.7 x V_{DD2}			V
Input Low Voltage	V_{IL}					0.3 x V_{DD2}	V
Input Current	I_{IN}	Excluding RESETB		-10	±0.1	+10	µA
RESETB Input Current	I_{INRB}			-10		+55	µA
Input Capacitance	C_{IN}				3		pF
Output High Voltage	V_{OH}	I_{LOAD} = 200µA, INTB has a 1kΩ pullup resistor to V_{DD2}		0.8 x V_{DD2}			V
Output Low Voltage	V_{OL}	I_{SINK} = 200µA, INTB has a 1kΩ pullup resistor to V_{DD2}				0.2 x V_{DD2}	V
Output Leakage Current		Three-state			±2.5		µA
Rise/Fall Time		C_{LOAD} = 10pF, 20% to 80%			0.5		ns
LVDS LOGIC INPUT/OUTPUT (DP15–D0P, DN15–DN0, SYNCIP, SYNCIN, SYNCOP, SYNCON, DCLKP, DCLKN, RCLKP, RCLKN, PARP, PARN)							
Differential Input Logic High	V_{IH}					100	mV
Differential Input Logic Low	V_{IL}			-100			mV
Input Common Mode Voltage	V_{ICM}			0.675		1.375	V
Differential Input Resistance	R_{IN}			87.5	100	132.5	Ω
Differential Output Logic High	V_{OH}	R_{LOAD} = 100Ω differential		275		450	mV
Differential Output Logic Low	V_{OL}	R_{LOAD} = 100Ω differential		-450		-275	mV
Output Common Mode Voltage	V_{OCM}			1.125	1.25	1.375	V
Output Maximum Frequency	f_{RCLK}	R_{LOAD} = 100Ω differential, C_{LOAD} = 8pF			620		MHz
CLOCK INPUT (CLKP, CLKN)							
Differential Input Voltage Swing	V_{DIFF}	Sine-wave input			> 0.5		V_{P-P}
Common Mode Voltage	V_{COM}	AC-coupled, internally biased			0.5		V
Differential Input Resistance	R_{CLK}				100		Ω
DATA CLOCK TIMING (8x INTERPOLATION, f_{CLK} = 4.9152GHz) (Note 8)							
Data Setup Time (DATACLK to DATA)	t_S	DATACLK rising edge	+125°C > T_J > +65°C	-680			ps
		DATACLK falling edge		-680			
Data Hold Time (DATACLK to DATA)	t_H	DATACLK rising edge	+125°C > T_J > +65°C	420			ps
		DATACLK falling edge		420			

Electrical Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 10x interpolation, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF. $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +115°C, unless otherwise noted. Typical values are at T_J = +60°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL PORT INTERFACE TIMING						
SCLK Frequency	f_{SCLK}	$1/t_{SCLK}$			50	MHz
SCLK to CSB Setup Time	t_{CSS}			10		ns
SCLK to CSB Hold Time	t_{CSH}			1		ns
SDI to SCLK Hold Time	t_{SDH}	Data-read		1		ns
SDI to SCLK Setup Time	t_{SDS}	Data-read		10		ns
SCLK to SDO Data Delay	t_{SDD}	Data-write		15		ns
POWER SUPPLY						
1.0V Supply Voltage Range	V_{DD}, V_{AVCLK}, V_{AVDD}		0.95	1.0	1.05	V
1.8V Supply Voltage Range	V_{DD2}, V_{AVCLK2}, V_{AVDD2}		1.71	1.8	1.89	V
1.0V Digital Supply Current	I_{VDD}	f_{CLK} = 4915.2MHz, -1dBFS peak input power, 10x interpolation, f_{CENTER} = 2140MHz		520	680	mA
1.8V Digital Supply Current	I_{VDD2}			16	23.5	mA
1.0V Clock Supply Current	I_{AVCLK}			300	442	mA
1.8V Clock Supply Current	I_{AVCLK2}			20	22	mA
1.0V Analog Supply Current	I_{AVDD}			192	280	mA
1.8V Analog Supply Current	I_{AVDD2}			244	290	mA
Total Power Dissipation	P_{TOTAL}			1516	2006	mW

Note 2: All specifications are guaranteed via test at T_J = +60°C and T_J = +115°C to an accuracy of ±10°C, unless otherwise noted. Specifications at T_J < +60°C are guaranteed by design and characterization. Timing specifications are guaranteed by design and characterization.

Note 3: f_{DAC} (DAC update rate) = f_{CLK}.

Note 4: Adjusted DAC update rate is defined as the maximum DAC update rate divided by the smallest interpolating factor. For the MAX5868, the maximum DAC update rate is 4960Msps and the smallest interpolating factor is 4. Adjusted DAC update rate = 4960Msps/4 = 1240Msps. Note this is a mathematically derived specification and is not production tested.

Note 5: $f_{DATACLK}$ = f_{DCLK} = Data Clock Frequency.

Note 6: Settling time is dominated by the interpolation filter step response.

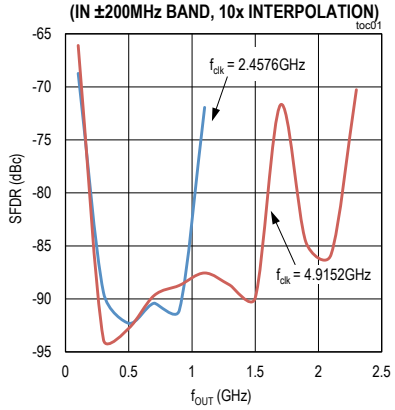
Note 7: Excludes sin(x)/x rolloff.

Note 8: Specification guaranteed by design and characterization, not production tested.

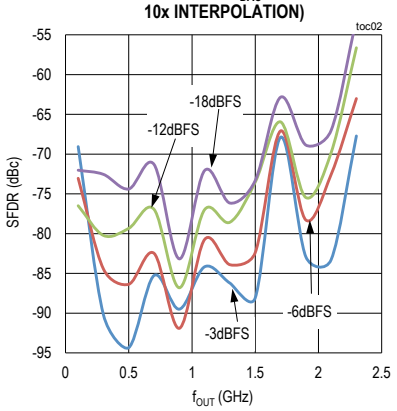
Typical Operating Characteristics

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF, T_A = +25°C, T_J = +65°C, unless otherwise noted.)

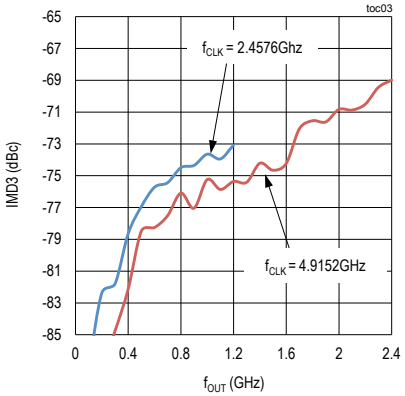
IN-BAND SINGLE TONE SFDR (IN ±200MHz BAND, 10x INTERPOLATION)



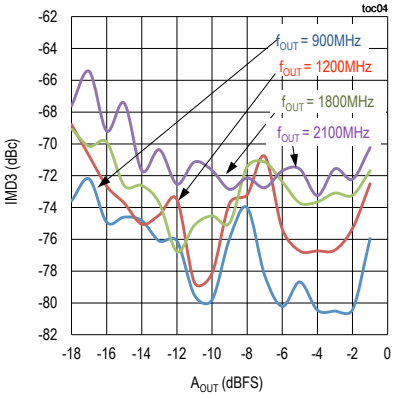
IN-BAND SINGLE-TONE SFDR vs. OUTPUT AMPLITUDE (IN ±200MHz BAND, f_{DAC} = 4.915Gsps, 10x INTERPOLATION)



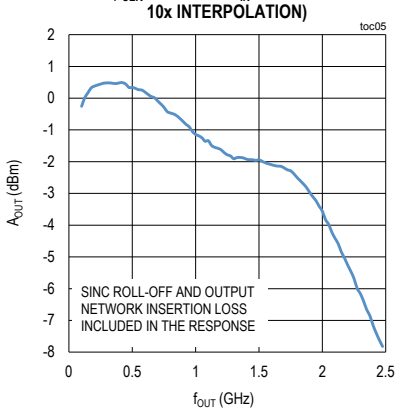
IMD3 vs. OUTPUT FREQUENCY, 600kHz SPACING (10x INTERPOLATION)



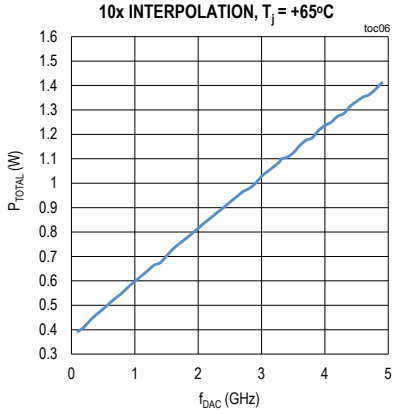
IMD3 vs. OUTPUT AMPLITUDE, 600kHz SPACING (f_{DAC} = 4.915Msps, 10x INTERPOLATION)



DAC OUTPUT FREQUENCY RESPONSE (f_{CLK} = 4.96GHz, A_{IN} = -0.1dBFS, 10x INTERPOLATION)



POWER DISSIPATION vs. DAC UPDATE RATE 10x INTERPOLATION, T_j = +65ºC

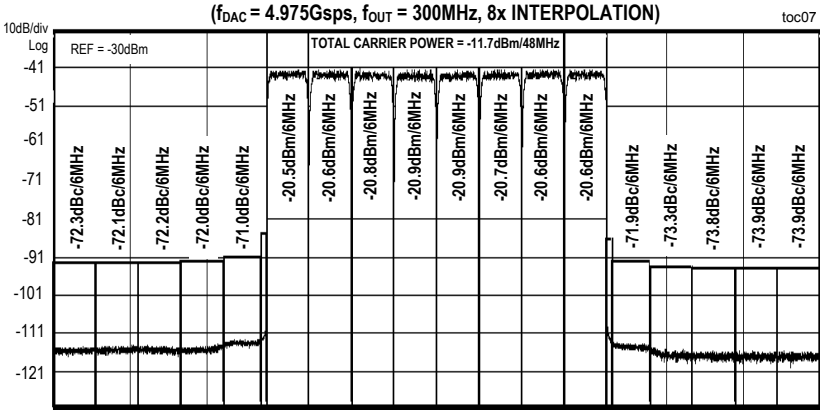


Typical Operating Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF, T_A = +25°C, T_J = +65°C, unless otherwise noted.)

8-CHANNEL 256-QAM (DOCSIS) ACP

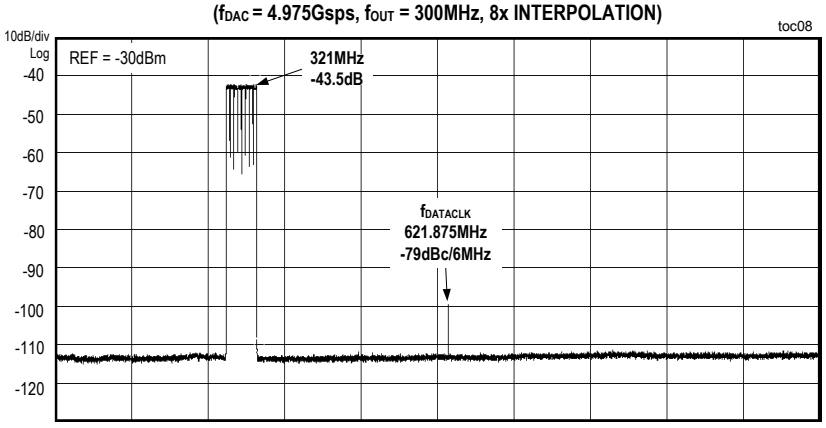
(f_{DAC} = 4.975Gsps, f_{OUT} = 300MHz, 8x INTERPOLATION)



CENTER = 300MHz, SPAN = 108MHz, RBW = 30kHz,
VBW = 3kHz, SWEEP = 2.98s, ATTEN = -2dB

8-CHANNEL 256-QAM (DOCSIS) ACP

(f_{DAC} = 4.975Gsps, f_{OUT} = 300MHz, 8x INTERPOLATION)

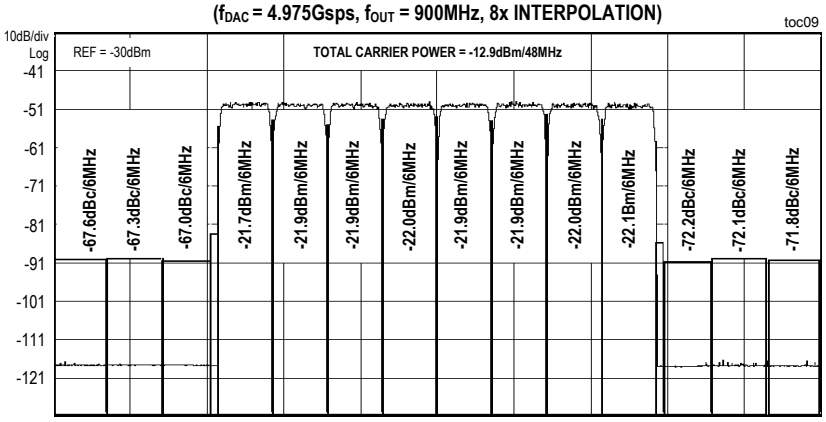


CENTER = 300MHz, SPAN = 1.2GHz, RBW = 30kHz,
VBW = 3kHz, SWEEP = 13.4s, ATTEN = -6dB

Typical Operating Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF, T_A = +25°C, T_J = +65°C, unless otherwise noted.)

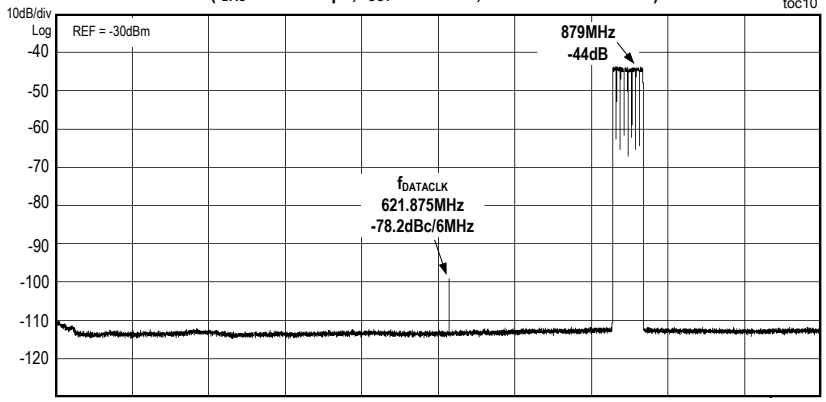
8-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.975Gsps, f_{OUT} = 900MHz, 8x INTERPOLATION)



CENTER = 900MHz, SPAN = 108MHz, RBW = 10kHz,
VBW = 1kHz, SWEEP = 20.9s, ATTEN = -4dB

*SETUP OPTIMIZED FOR GAIN FLATNESS. ADDITIONAL REDUCTION IN NOISE FLOOR POSSIBLE BY DECREASING ATTENUATION.

8-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.975Gsps, f_{OUT} = 900MHz, 8x INTERPOLATION)

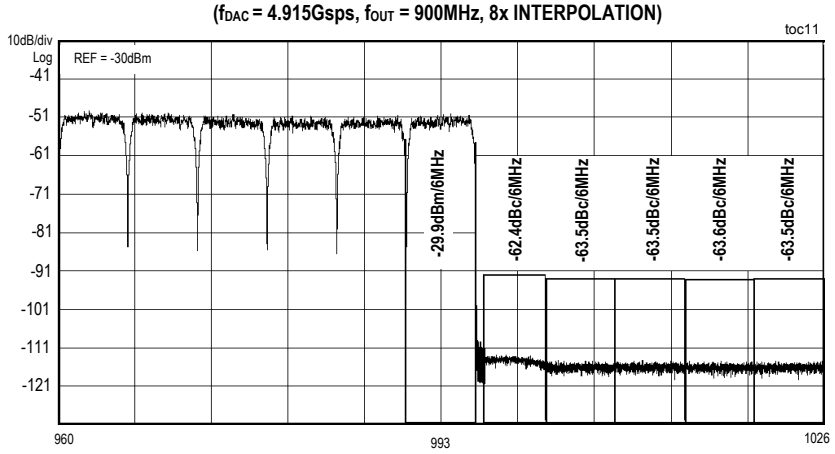


CENTER = 900MHz, SPAN = 1.2GHz, RBW = 30kHz,
VBW = 3kHz, SWEEP = 13.4s, ATTEN = -6dB

Typical Operating Characteristics (continued)

(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF, T_A = +25°C, T_J = +65°C, unless otherwise noted.)

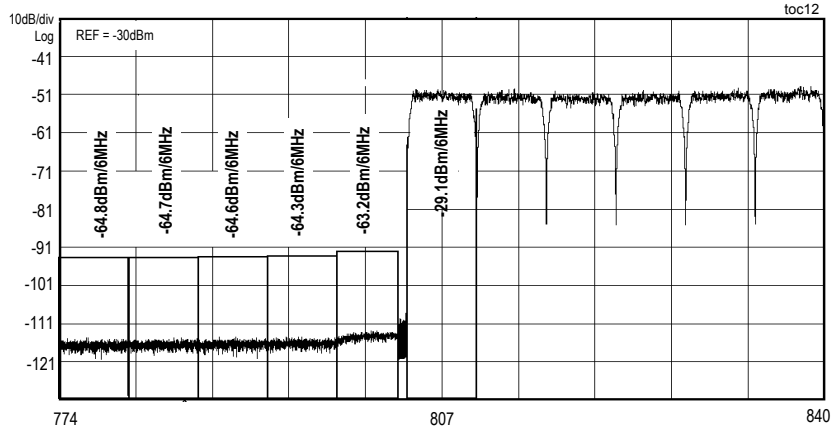
32-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.915Gsps, f_{OUT} = 900MHz, 8x INTERPOLATION)



CENTER = 993MHz, SPAN = 66MHz, RBW = 30kHz,
VBW = 3kHz, SWEEP = 2.98s, ATTEN = -2dB

*SETUP OPTIMIZED FOR NOISE FLOOR. GAIN FLATNESS IS IMPROVED BY INCREASING ATTENUATION.

32-CHANNEL 256-QAM (DOCSIS) ACP
(f_{DAC} = 4.915Gsps, f_{OUT} = 900MHz, 8x INTERPOLATION)



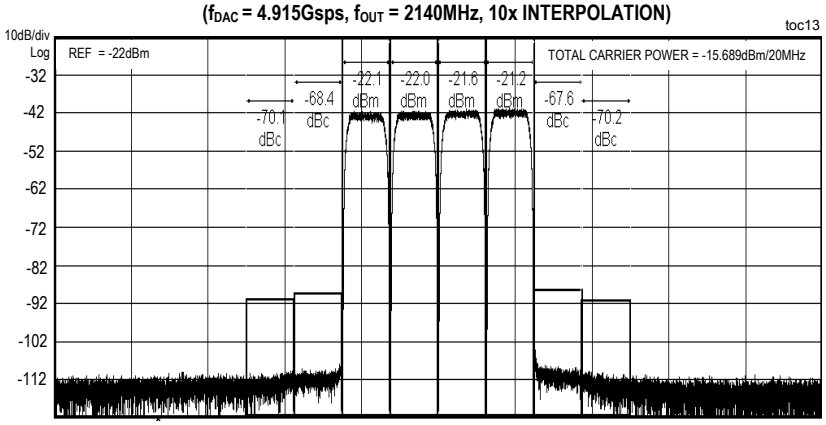
CENTER = 807MHz, SPAN = 66MHz, RBW = 30kHz,
VBW = 3kHz, SWEEP = 2.98s, ATTEN = -2dB

*SETUP OPTIMIZED FOR NOISE FLOOR. GAIN FLATNESS IS IMPROVED BY INCREASING ATTENUATION.

Typical Operating Characteristics (continued)

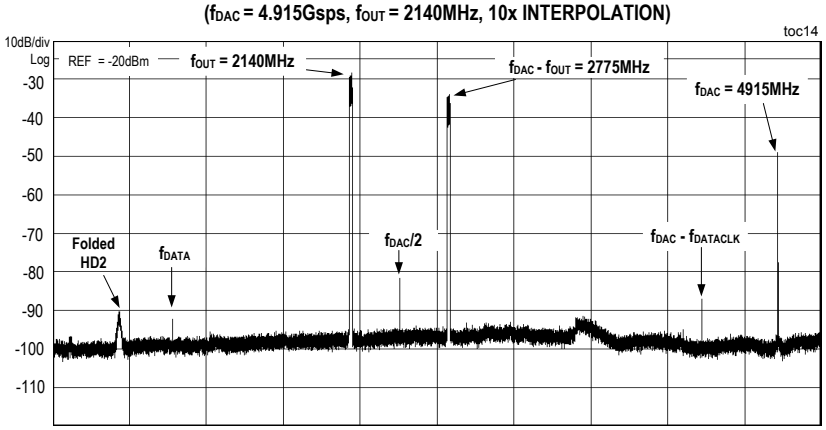
(V_{AVDD} = V_{AVCLK} = V_{DD} = 1.0V, V_{AVDD2} = V_{AVCLK2} = V_{DD2} = 1.8V, P_{CLK} = 0dBm, 16-bit word mode, I_{OUTFS} = 29.5385mA, output is 50Ω double-terminated and transformer coupled, external reference at 1.20V, R_{SET} = 1.3kΩ between FSADJ and DACREF, T_A = +25°C, T_J = +65°C, unless otherwise noted.)

FOUR CARRIER CNR
(f_{DAC} = 4.915Gsps, f_{OUT} = 2140MHz, 10x INTERPOLATION)



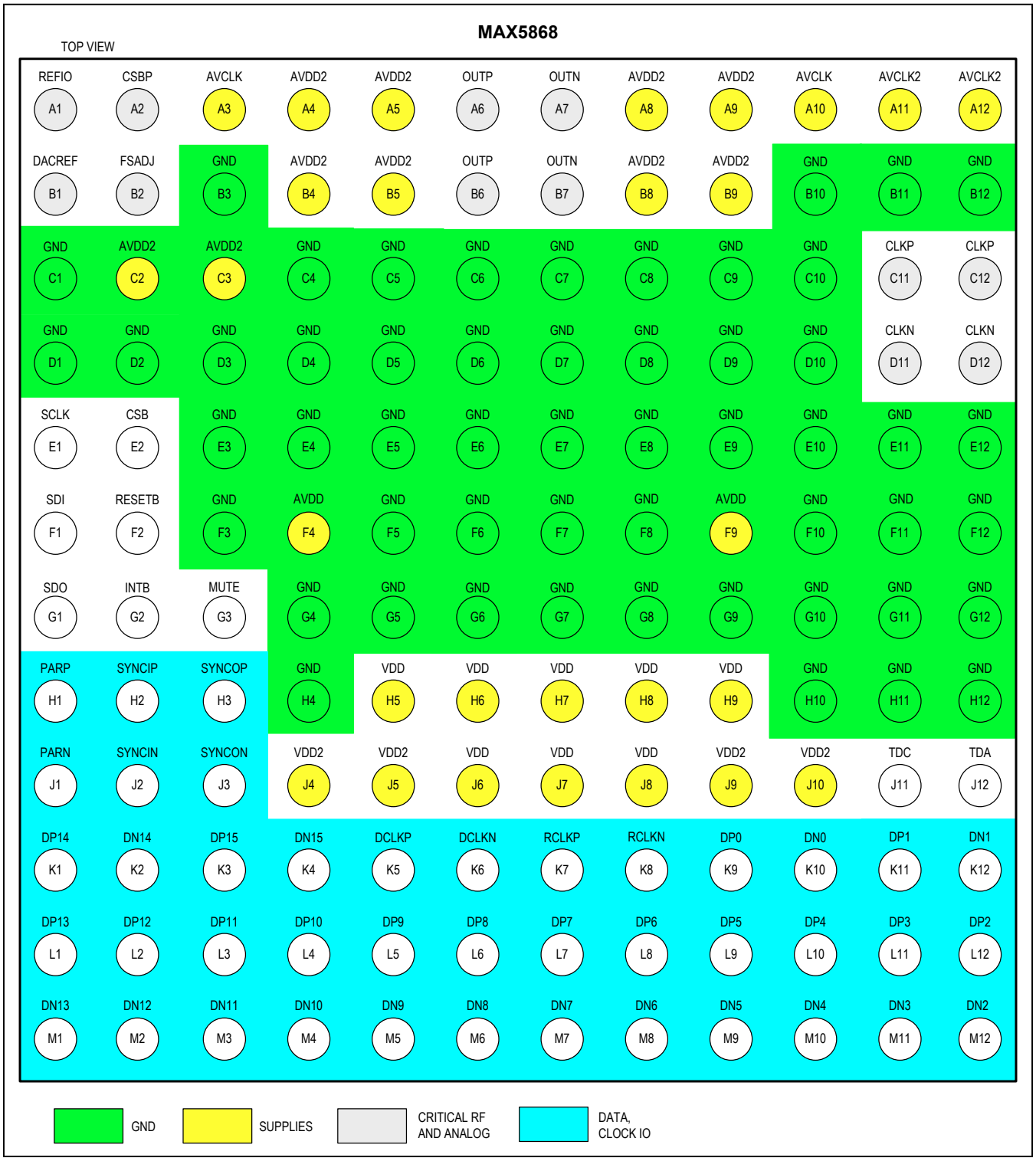
CENTER = 2140MHz, SPAN = 80MHz, RBW = 30kHz,
VBW = 3kHz, SWEEP = 1.104s, ATTEN = 0dB

FOUR CARRIER CNR
(f_{DAC} = 4.915Gsps, f_{OUT} = 2140MHz, 10x INTERPOLATION)



CENTER = 2700MHz, SPAN = 5GHz, RBW = 1MHz,
VBW = 1MHz, SWEEP = 21.3ms, ATTEN= -2dB

Ball Configuration



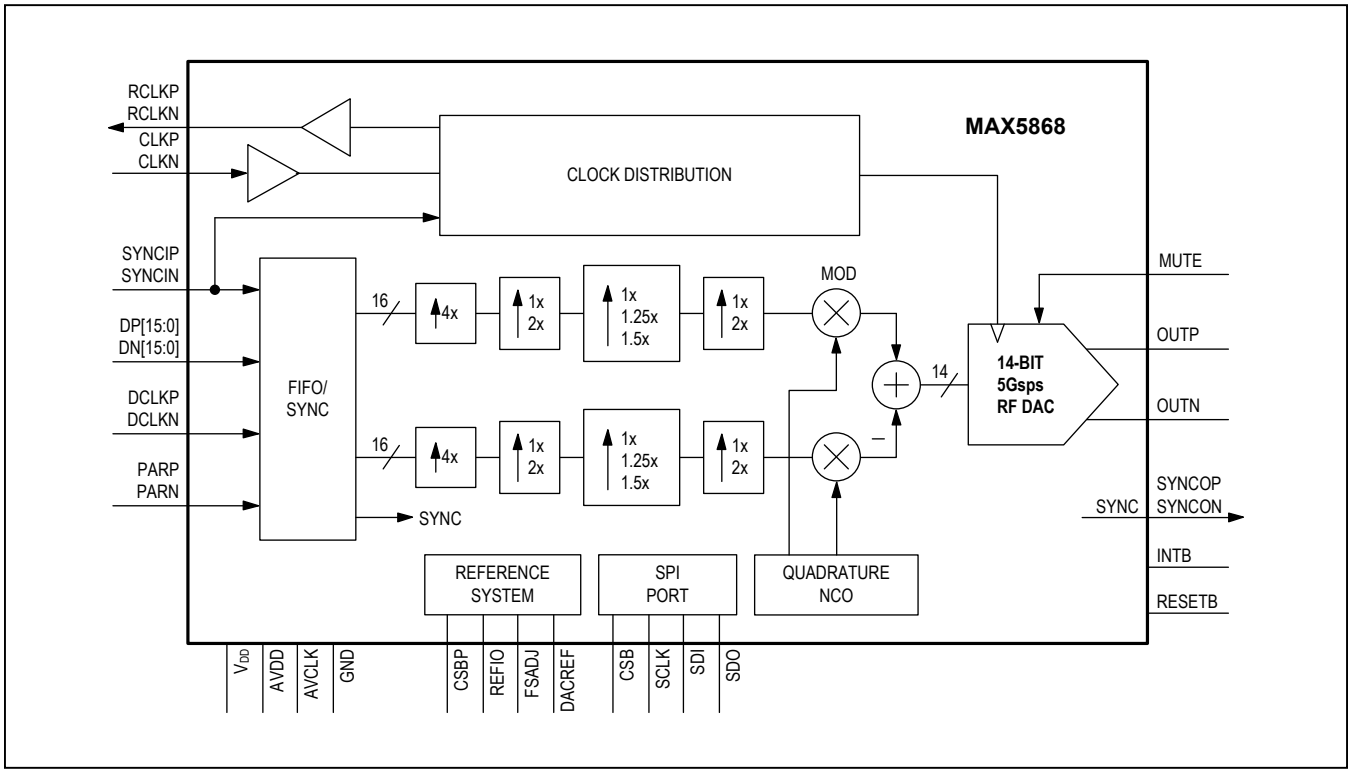
Ball Description

BALL	NAME	FUNCTION
A1	REFIO	Reference Voltage Input/Output. REFIO outputs an internal 1.2V bandgap reference voltage. REFIO has a 10kΩ series resistance and can be driven using an external 1.2V reference voltage. Connect a 1µF capacitor between REFIO and DACREF.
A2	CSBP	DAC Current Source Bypass. Connect a 1µF capacitor between CSBP and DACREF.
A3, A10	AVCLK	1.0V Supply Input for Clock
A4, A5, A8, A9, B4, B5, B8, B9, C2, C3	AVDD2	Analog 1.8V Supply Input
A6, B6	OUTP	Positive Terminal of Differential DAC Output
A7, B7	OUTN	Negative Terminal of Differential DAC Output
A11, A12	AVCLK2	1.8V Supply Input for Clock
B1	DACREF	DAC Reference Ground. Do not connect to ground (GND).
B2	FSADJ	Analog Input for DAC Full-Scale Output Current Adjustment. A resistor from FSADJ to DACREF sets the full-scale output current of the DAC. To obtain a 29.5385mA full-scale output current using the internal reference voltage, connect a 1.3kΩ resistor between FSADJ and DACREF.
B3, B10, B11, B12, C4–C10, D4–D10, E3–E12, F3, F5–F8, F10, F11, F12, G4–G10, H4, H10	GND	Ground
C1, D1, D2, D3, G11, G12, H11, H12	GND	Must be grounded for normal operation.
C11, C12	CLKP	DAC Clock Positive Input. An internal 100Ω termination resistor connects CLKP to CLKN.
D11, D12	CLKN	DAC Clock Negative Input
E1	SCLK	Digital CMOS Input for Serial Port Interface Clock
E2	CSB	Digital CMOS Input for Serial Port Interface Chip Selection Bar. MAX5868 is selected when CSB = low.
F1	SDI	Digital CMOS Input for Serial Port Interface Data Input. Serial port data is latched on the rising edge of SCLK.
F2	RESETB	Digital CMOS Input with Internal Pulldown to Ground. Device is reset when RESETB = low. Set RESETB low during device startup. RESETB must be set high for normal operation after startup.
F4, F9	AVDD	Analog 1.0V Supply Input
G1	SDO	Digital CMOS Output for Serial Port Interface Data Output. Serial port data is clocked out from MAX5868 on the falling edge of SCLK.
G2	INTB	Digital CMOS Output for Interrupt. Types of interrupts are defined by the EINT SPI register. The cause of the interrupt is determined by reading the STATUS SPI register.
BALL	**NAME**	**FUNCTION**

Ball Description (continued)

G3	MUTE	Digital CMOS Input MUTE = high puts the device into mute mode. MUTE = low puts the device into normal operation mode.
H1	PARP	LVDS Positive Input for Parity Bit. A differential 100Ω termination resistor is on-chip between PARP and PARN.
H2	SYNCIP	LVDS Positive Input for Synchronization. A differential 100Ω termination resistor is on-chip between SYNCIP and SYNCIN.
H3	SYNCOP	LVDS Positive Output for Synchronization
H5–H9, J6, J7, J8	V_{DD}	1.0V Supply Input for Digital Core
J1	PARN	LVDS Negative Input for Parity Bit
J2	SYNCIN	LVDS Negative Input for Synchronization
J3	SYNCON	LVDS Negative Output for Synchronization
J4, J5, J9, J10	V_{DD2}	1.8V Supply Input for Digital I/O
J11	TDC	Temperature Sensor Diode Cathode. Connect TDC and TDA to ground if not used.
J12	TDA	Temperature Sensor Diode Anode. Connect TDC and TDA to ground if not used.
K1, K3, K9, K11, L1–L12,	DP15–DP0	LVDS Positive Data Input for DAC Data. DP15 is MSB. Offset binary format is default. A differential 100Ω termination resistor is on chip between each data pair DPx and DNx.
K2, K4, K10, K12, M1–M12	DN15–DN0	LVDS Negative Inputs for DAC Data. DN15 is MSB. Offset binary format is default.
K5	DCLKP	LVDS Positive Input for DAC Data Clock. A differential 100Ω termination resistor is on-chip between DCLKP and DCLKN.
K6	DCLKN	LVDS Negative Input for DAC Data Clock
K7	RCLKP	LVDS Positive Output for Reference Data Clock Equal to 1/2 the Expected Input Data Rate (f_{DATA}) Operating in Double Data Rate (DDR)
K8	RCLKN	LVDS Negative Output for Reference Data Clock Equal to 1/2 the Expected Input Data Rate (f_{DATA}) Operating in Double Data Rate (DDR)

Functional Diagram



Detailed Description

The MAX5868 is a high-performance interpolating and modulating 16-bit 5Gsps RF DAC designed for EPoC, digital video broadcast, and downstream DOCSIS CMTS modulators. The device can synthesize up to 500MHz of instantaneous bandwidth at frequencies up to the Nyquist bandwidth ($f_{CLK}/2$) of the DAC. The major functional blocks of the device include a 16-bit parallel LVDS interface, a cascade of interpolation filters, a digital quadrature modulator and NCO, and a 14-bit, 5Gsps RF DAC. The supporting functional blocks include the clock distribution system, reference system, and SPI interface. See detailed *Functional Diagram*.

Input baseband data is supplied to the device in quadrature via a 16-bit parallel LVDS interface (DP[15:0]/DN[15:0]). The data streams for I and Q channels are time interleaved, therefore the data rate through the input port is twice the input data rate to the I and Q channels. Data can be fed to the device in nibble (4 bit), byte (8 bit) or word (16 bit) modes, allowing for flexibility to optimize the number and speed of the LVDS data pairs driving the DAC.

Before entering the DSP portion of the signal path, the data timing is realigned in the input FIFO buffer to ensure accurate data capture. The FIFO buffer allows the input data port to be synchronized with an external data clock (DCKLP/DCKLN). The input data clock needs to be frequency locked with the DAC clock (CLKP/CLKN) but there are no restrictions on its phase. The device expects even parity and can be configured to produce an interrupt when parity errors are detected. 16-bit input data enhances the accuracy of the interpolation and modulation functions and ensures true 14-bit data is presented to the RF DAC core.

The DSP path consists of a chain of configurable interpolation filters. Interpolation rates of 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x or 24x can be selected by bypassing one or more of the interpolation filters. Interpolation reduces the required input data rate to the device relaxing the requirements on the FPGA or ASIC. In addition, interpolation increases the separation between the desired signal and its aliased image easing filter design requirements.

After passing through the interpolation stages, the signal is modulated using the LO signal generated by the NCO

and the digital quadrature modulator. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis with 32 bits of frequency setting resolution. Placing the modulator at the output of the interpolator chain allows for fully agile placement of the output carrier frequency within the Nyquist bandwidth of the DAC. The quadrature modulator produces a real signal at its output, which is in turn fed into the 14-bit DAC core where it is converted to an analog RF signal. The analog output produces a full-scale current between 10mA and 30mA driving loads up to 50Ω differential.

The clock distribution system provides a low noise differential input buffer for the external master DAC clock (CLKP/CLKN) and delivers all necessary clocks to all the DAC blocks. The DAC clock input accepts a differential sine-wave or square-wave signal. The device outputs a divided reference clock (RCLKP/RCLKN) that is equal to 1/2 the expected input data rate (f_{DATA}) operating in Double Data Rate (DDR) to facilitate synchronization with the FPGA or ASIC driving its data port. Two additional signals, SYNCI and SYNCO, are provided to facilitate synchronizing multiple MAX5868 devices.

The reference system delivers the reference current to the DAC current source array and all bias currents necessary for the circuit operation. The reference system also includes a band-gap reference, which can be used as a reference for the DAC full scale current.

The SPI port is a bidirectional interface and is used for configuring the device and reading/writing status and control registers.

The device operates from 1.8V and 1.0V power supply voltages and consumes 1.5W at 5Gsps.

Reference Interface

The device operates with either the on-chip 1.2V band-gap reference or an external reference voltage source as shown in Figure 1 and Figure 2. REFIO serves as the input for an external, low-impedance reference source, or as the reference output when the internal reference is used. REFIO must be decoupled to DACREF with a 1µF capacitor when using the internal reference. REFIO must be buffered with an external amplifier if heavier loading is required, due to the 10kΩ series resistance.

The reference circuit employs a control amplifier designed to regulate the full-scale, differential output current, I_{OUTFS}. The output current is calculated as follows:

$$I_{OUTFS} = 32 \times I_{REF}$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$) and I_{OUTFS} is the full-scale output current of the DAC. Using the 1.2V (typical) internal reference and R_{SET} of 1.28kΩ results in a full-scale output current of 30mA. In general, the dynamic performance of the DAC improves with increasing full-scale current.

Analog Output

The device is a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to AVDD2 providing a 50Ω differential output resistance. In addition to the signal current, a constant current sink (I_{FIX}) equal to one half I_{OUTFS} is connected to each differential DAC output. N = 14 and is the number

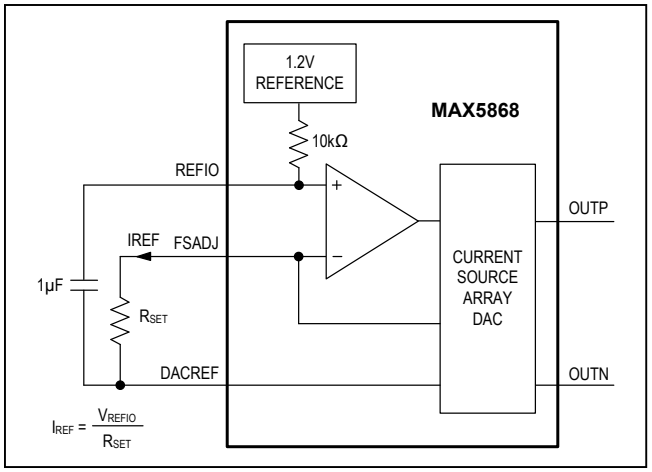


Figure 1. Reference Architecture, Internal Reference Configuration

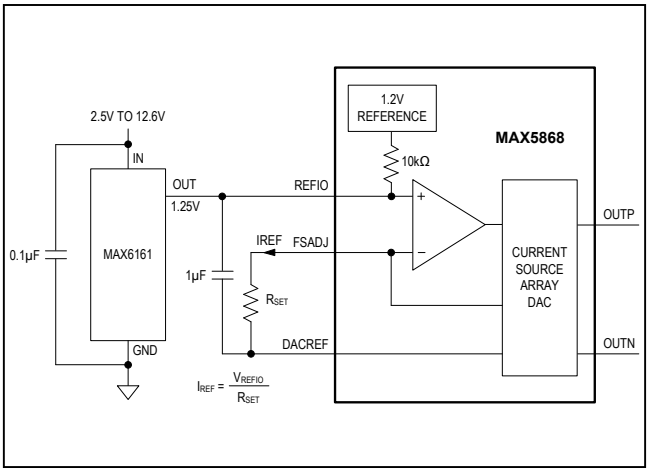


Figure 2. Reference Architecture, External Reference Configuration

of bits of resolution of the DAC core. Figure 3 shows an equivalent circuit for the internal output structure of the device. The circuit has some resistive, capacitive and inductive elements. These elements have been minimized by design in order to achieve the highest possible output bandwidth (2250MHz typical).

In addition, the device requires a differential external termination (i.e. double termination). This external termination can be accomplished with a differential 50Ω load or a single-ended 50Ω load interfaced through a transformer. RF chokes to the AVDD2 supply should be used with the transformer coupled output. A typical transformer coupled configuration for high-frequency operation is shown in Figure 3.

For applications where the DC information is important, the output configuration in Figure 4 can be used. 25Ω resistors to AVDD2 are required for DC coupling. The DC configuration will lower the output common-mode which may reduce performance slightly. The device is not compatible with an unterminated output when using the upper portion of the full-scale current range. Lowering the full-scale current to 20mA or less may allow use of the outputs without external terminations, though performance will be impacted in this configuration.

Clock Interface

The MAX5868 DAC is updated on the rising edge of the clock supplied to the differential high frequency clock input (CLKP/CLKN) and supports a maximum frequency of 4.96GHz. The high-frequency clock should be a balanced fully differential signal with a 50%, or near 50%, duty cycle. The clock input has internal (on-chip) 100Ω differential termination. The clock inputs requires a minimum of 0dBm input power. The clock inputs must be AC-coupled to the clock source as they are self biased internally.

Data Interface

The LVDS data interface includes a 16-bit wide interleaved I/Q data input (DP[15:0]/DN[15:0]), a parity bit input (PARP/PARN), a data clock input (DCLKP/DCLKN), a synchronization input (SYNCIP/SYNCIN) and a synchronization output (SYNCOP/SYNCON). Each LVDS input is terminated internally with a differential 100Ω resistor. DC coupling is required and the logic levels must meet the requirements specified in the *Electrical Characteristics* table.

The complex, interleaved data (I and Q) is latched into the device in one of three interface configuration modes using either offset binary or two's complement data format. The three interface configuration modes are Word (16 bit), Byte (8 bit) and Nibble (4 bit) modes. Both the interface configuration modes and data format are set by programming the CfgChipOM register accessible through the SPI interface. The default is Word mode for interface configuration and offset binary for data format. Data inversion can also be user programmed for the Q-data (default is no inversion).

The data interface operates in Double Date Rate (DDR) for all interface configurations. The input data clock DCLK must be frequency locked with the DAC clock. The device outputs a LVDS divided reference clock (RCLKP/RCLKN) which is equal to 1/2 the expected input data rate (f_{DATA}) operating in DDR. DCLK must be frequency locked to

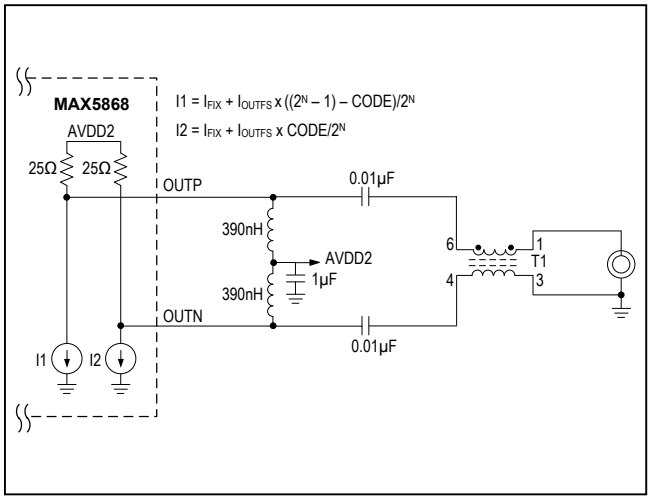


Figure 3. Typical DAC Output Configuration

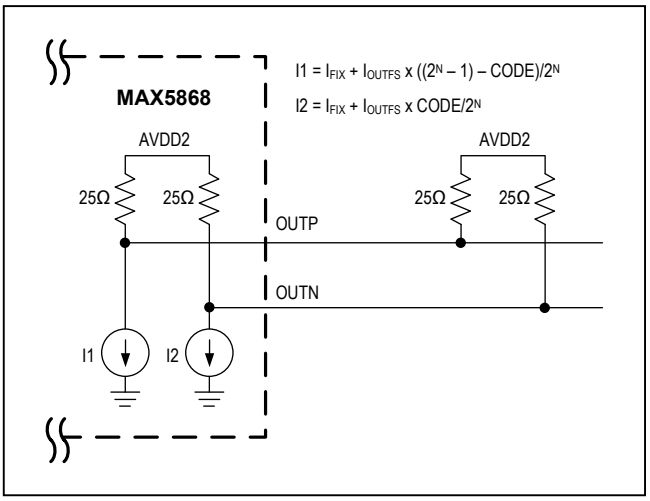


Figure 4. Output Configuration for Low-Frequency Operation

RCLK; however, there are no restrictions to the relative phase of these two clock signals.

In 16-bit Word mode, each rising DCLK edge marks an I and Q interleaved data pair, which are demultiplexed into an I and Q data stream inside the chip, where a FIFO buffer allows the input data to be synchronized with the data clock DCLK.

The 8-bit Byte and 4-bit Nibble modes are provided to reduce active I/O pin count and are typically used when higher interpolation rates are used. In Byte and Nibble modes, only 8 bits or 4 bits of the input data LVDS pairs (instead of 16 LVDS pairs) are used along with the SYNCI signal, which is used to carry framing alignment information.

In all data interface configuration modes, the DCLK, DP[15:0]/DN[15:0], SYNCI, and PAR signals need to be time aligned. In Word mode, I-data is associated with the rising edge of DCLK, and Q-data is associated with the falling edge of DCLK. See Data Setup Time and Data Hold Time requirements in *Electrical Characteristics* table. The interface supports DCLK frequencies up to 620MHz. With the DDR mode, a maximum input rate 1240Mwps can be achieved for the data (I + Q). Once the data is clocked into MAX5868, the FIFO is used to match the external clock domain (DCLK) with the internal clock domain (RCLK). As stated above, DCLK must be frequency locked to RCLK. A FIFO overflow and underflow will activate interrupt register bits: one for overflow and one for underflow.

The device expects even parity and can be programmed to generate an interrupt on the INTB pin when parity errors are detected. In all modes, the parity is calculated and compared over the 16-bit data width plus the additional parity bit supplied to the PARP/PARN input. For example, an even parity means the XOR of the 16-bit data and the parity bit (17 bits total) results in a '0'. In Word mode, the SYNCI signal is not required for data frame alignment. If parity is not used, the PARP/PARN input should be a valid LVDS logic '1' or '0' at all times. The device can also be configured to mute the DAC output when parity errors are detected.

Relative timing diagrams for the LVDS interface in Word, Byte, and Nibble modes are shown in Figure 5.

Word Mode Operation

Word mode is the default input interface. All 16 bits are used in this mode where D[15] is the MSB and D[0] is the LSB.

SYNCI is not required for framing alignment in this mode. See the *SYNC Functionality* section for further details on synchronizing multiple devices.

Parity is applied coincident with the word input, I parity with I data and Q parity with Q data.

The rising edge of DCLK captures the I-data and the falling edge of DCLK captures the Q-data. In terms of timing, the parity bit should be treated as a data bit, as it is routed the same as the data bits inside the chip.

Byte Mode Operation

Operating in the Byte mode, data is input 8 bits at a time. The data input sequence for Byte mode is: I[15-8], I[7-0], Q[15-8], Q[7-0], I[15-8], etc. The active data pins for Byte mode are: D[13] (MSB byte), D[12], D[9], D[8], D[6], D[5], D[3] and D[2] (LSB byte).

An internal counter is used to demux the input data into two separate 16-bit data busses. The internal counter is reset when a rising edge is detected on the SYNCI input. A rising edge, '0' to '1' transition should be applied to SYNCI with the first byte of the first I data word. SYNCI may be pulsed high with each new I data word, but is not required once the system is synchronized. See the *SYNC Functionality* section for further details on synchronizing multiple devices.

Parity, PARP/PARN, is captured along with the least significant byte (LSB byte). However, it may be applied with the entire word.

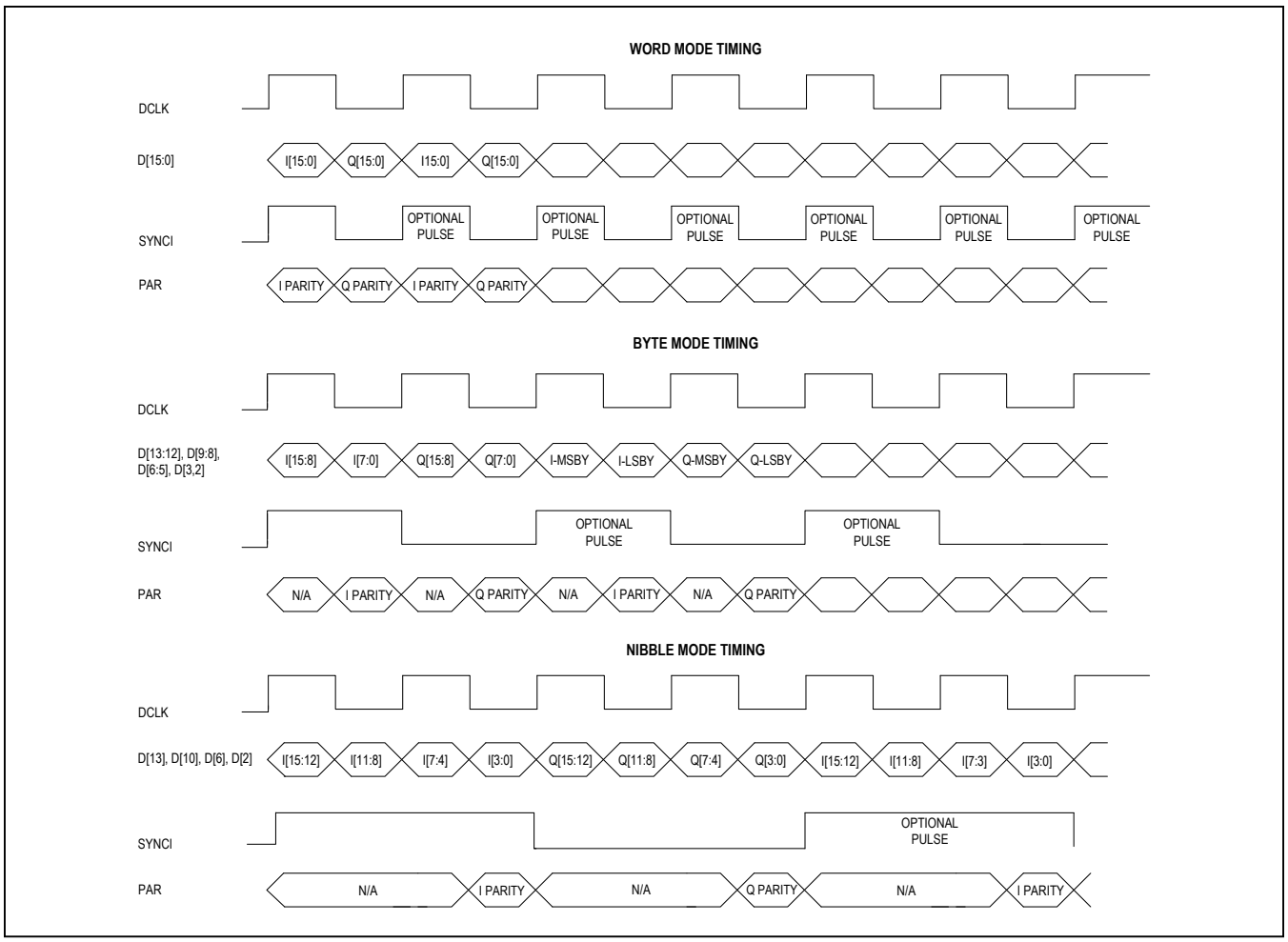


Figure 5. LVDS Timing

Nibble Mode Operation

Operating in the Nibble mode, data is input 4 bits at a time. The data sequence at the input pins is: I[15:12], I[11:8], I[7:4], I[3:0], Q[15:12], Q[11:8], Q[7:4], Q[3:0], I[15:12], I[11:8], etc. The active data pins for the Nibble mode are: D[13] (MSB nibble), D[10], D[6] and D[2] (LSB nibble). One nibble is captured on each edge of the DCLK signal.

An internal counter is used to demux the input data into two separate 16 bit data busses. The rising edge of the SYNCI signal is used to set the initial phase of a frame tracking counter. This counter output is used to control the data frame assembler. The counter rollover value is determined by the state of the byte and nibble mode controls. A rising edge, '0' to '1' transition should be applied to SYNCI with the first nibble of the first I data word. SYNCI may be pulsed high with each new I data word, but is not required once the system is synchronized. See the *SYNC Functionality* section for further details on synchronizing multiple devices.

Parity, PARP/PARN, is captured along with the least significant nibble (LSB nibble). However, it may be applied with the entire word.

Interpolation Filters

Interpolation rates of 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, and 24x are supported and are user selectable. The default rate is 10x interpolation. The interpolation filters support a maximum I+Q signal bandwidth of 504.68MHz in 16-bit Word mode when using a 4x interpolation rate (f_{DAC} = 2480Msps) or 8x interpolation rate (f_{DAC} = 4960Msps). The typical passband ripple is less than 0.1dB for all interpolation modes. The block diagram for the interpolation filter signal path is shown in Figure 6.

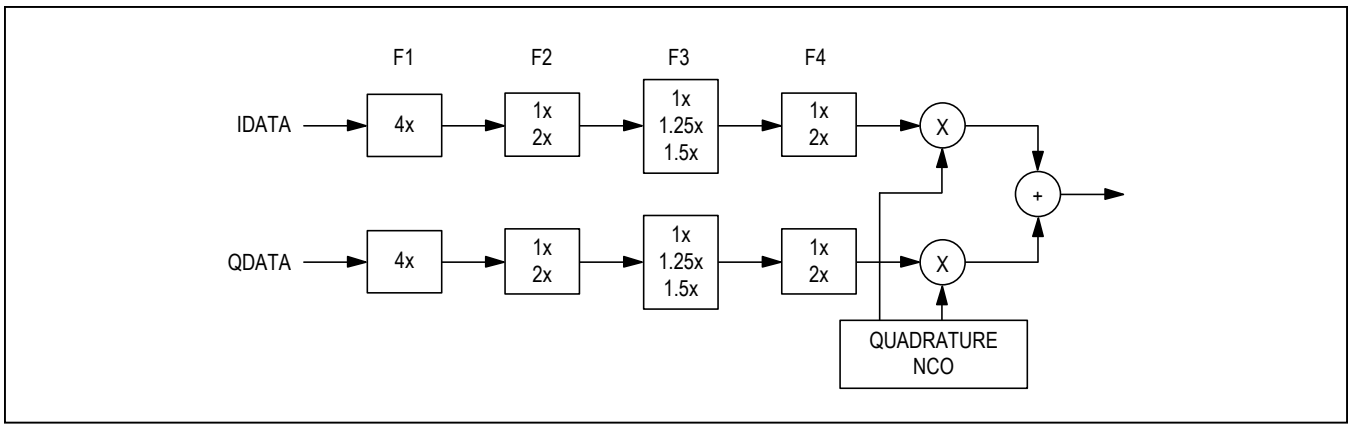


Figure 6. Interpolator/Modulator Block Diagram

The interpolation filters for the desired interpolation rate are programmed in the CfgDSP register accessible through the serial control interface. The DAC update rate equals the input sample rate (f_{S_IN}) multiplied by the interpolation rate. The input data rate (f_{DATA}) is determined by the input sample rate and data format (nibble, byte, or word). The MAX5868 outputs a reference clock for use in the data generation system. The RCLKP/RCLKN outputs are LVDS signals at a frequency equal to 1/2 the expected input data rate (f_{DATA}) operating in DDR. The RCLKP/RCLKN frequency is calculated as follows:

$$f_{RCLK} = \left(f_{DAC} / R\right) \times DMode$$

where:

f_{RCLK} = Reference clock frequency

f_{DAC} = DAC update rate = DAC clock frequency (f_{CLK})

R = Programmed interpolation rate

DMode = Input data format mode

= 1 for word mode

= 2 for byte mode

= 4 for nibble mode

The data clock in the FPGA or ASIC, $f_{DATACLK}$, can be derived from the reference clock output of the DAC, f_{RCLK}. The relationship between the various clocks and data rates are as follows:

- $f_{DAC} = R \times f_{S\_IN}$ where f_{S_IN} = input sample rate for the interleaved complex I/Q data set
- $f_{DATA} = 2 \times f_{S\_IN} \times DMode$
- $f_{DATACLK} = f_{DATA}/2$ (DDR data) = f_{RCLK}

There are some constraints with respect to interpolation rate, data input rates and the DAC clock frequency. These are:

- The input data rate, f_{DATA}, must not exceed the maximum data rate frequency (1240Mwps) specified in the *Electrical Characteristics* table
- The DAC clock frequency, f_{CLK}, must not exceed the maximum clock frequency (4960MHz) specified in the *Electrical Characteristics* table, and
- The reference clock output, f_{RCLK}, or the data clock, $f_{DATACLK}$, must not exceed the maximum frequency (620MHz) specified in the *Electrical Characteristics* table. Higher interpolation rates may be required when using byte or nibble input modes to ensure $f_{DATACLK}$ does not exceed 620MHz.

Frequency Planning

Using a DAC to generate communication transmit signals requires consideration of aliased harmonics and internally generated divided clocks. To ensure the dominant second and third order harmonics do not fold back into the signal band, the DAC update rate needs to be greater than four times the highest frequency in the band of interest.

Figure 7 and 8 show the location of the 2nd and 3rd harmonic distortion products for the case of the DAC being updated at 2.5 times and 4 times the maximum desired frequency in the band of interest (e.g. 1000MHz for DOCSIS 3.0 DRFI).

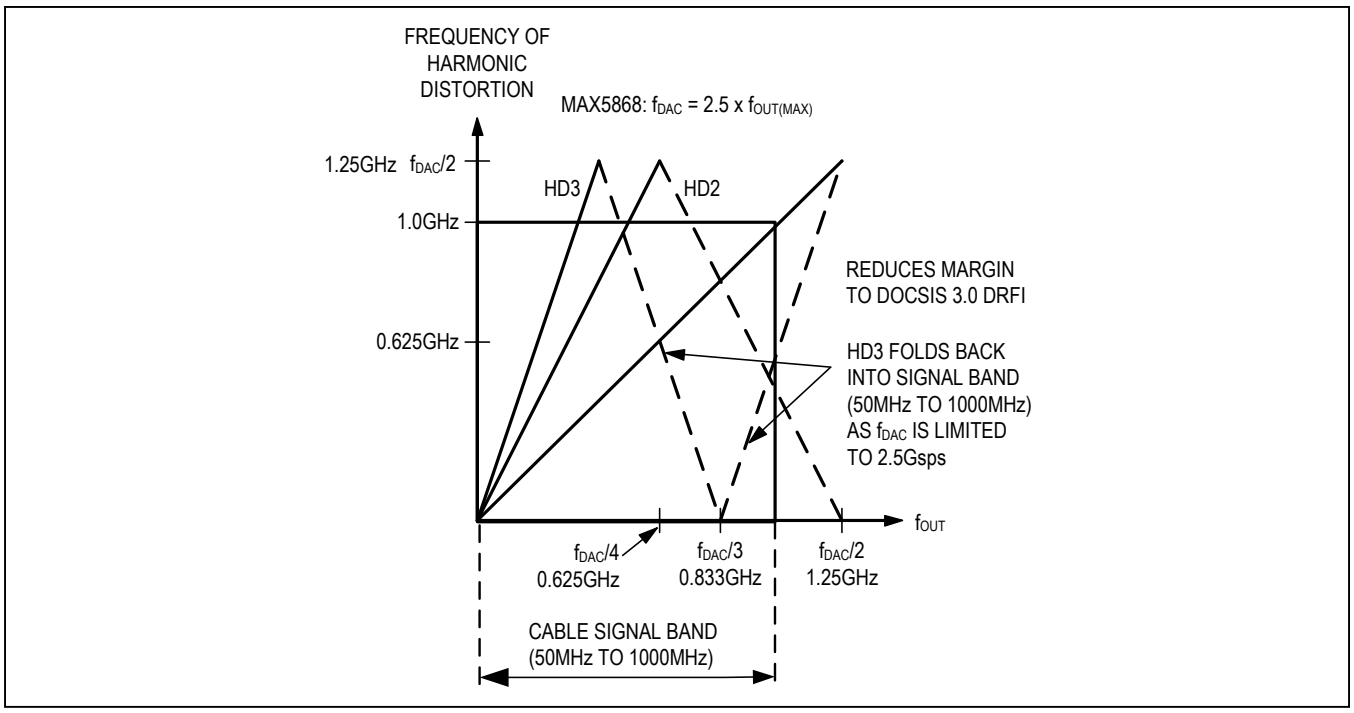


Figure 7. Example of Incorrect Frequency Planning

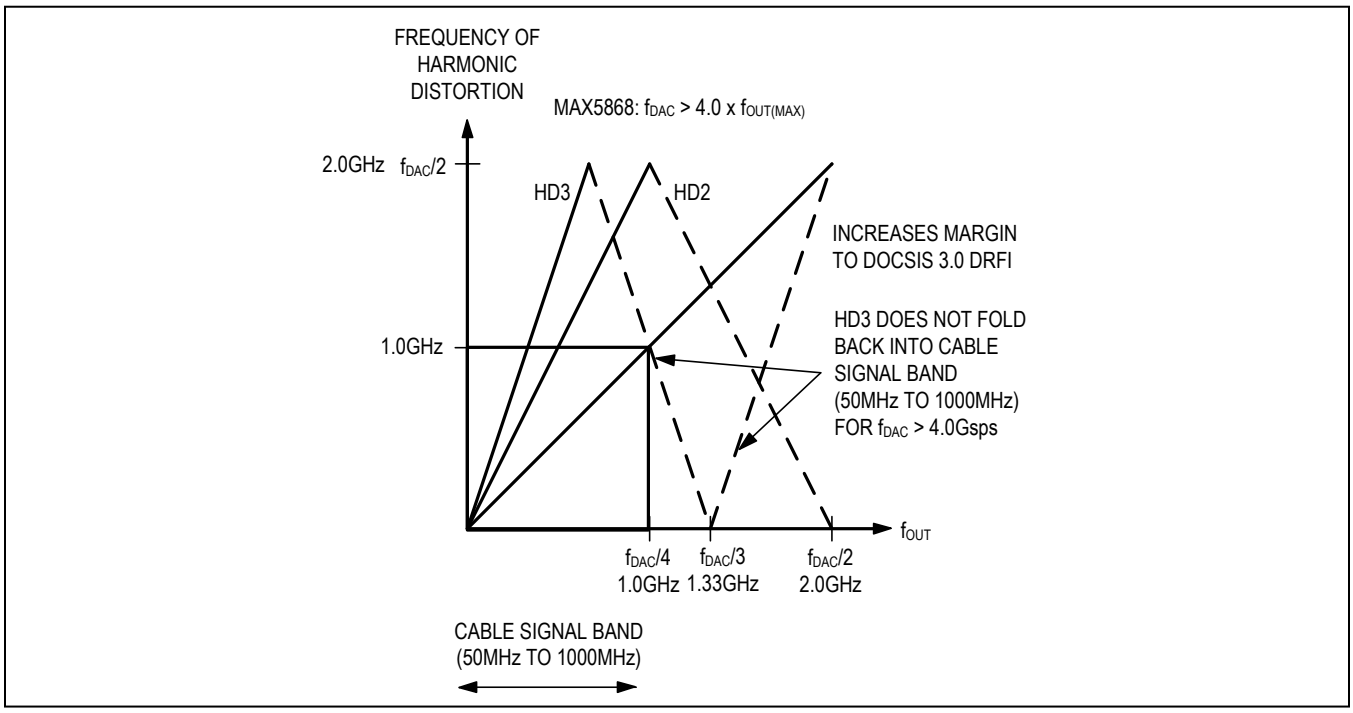


Figure 8. Example of Correct Frequency Planning

Signal Bandwidth

The MAX5868 can generate a maximum I/Q complex signal bandwidth of 504.68MHz when operating in 16-bit Word mode at f_{DAC} = 4960Msps and 8x interpolation (or f_{DAC} = 2480Msps and 4x interpolation) for output frequencies ranging from DC to Nyquist.

The actual signal bandwidth is dependent on the input sample rate (f_{S_IN}), or the DAC update rate (f_{DAC}) divided by the interpolation setting (R), and the interpolation filter passband width (PBW = 0.407, expressed as a percentage of the input sample rate). The I/Q complex DAC signal bandwidth is calculated as:

$$\text{DAC Signal Bandwidth} = 2 \times (f_{DAC}/R) \times (PBW)$$

The complex I/Q signals are converted to a real signal using a digital quadrature modulator and quadrature NCO. The real bandwidth is centered around the NCO frequency.

Complex Modulator and NCO

The device includes a complex modulator comprised of a complex NCO driving two multipliers followed by an adder Figure 9). The complex modulator produces the result:

$$I(n) \times COS(\omega n) - Q(n) \times SIN(\omega n)$$

where I and Q are filtered and interpolated versions of the input I-data and Q-data.

The complex NCO can synthesize a frequency in the range from 0Hz to $f_{DAC}/2$ using a 33-bit phase accumulator. The synthesized frequency is calculated as follows:

$$f_{NCO} = \frac{FCW\_full}{2^{33}} \times f_{DAC}$$

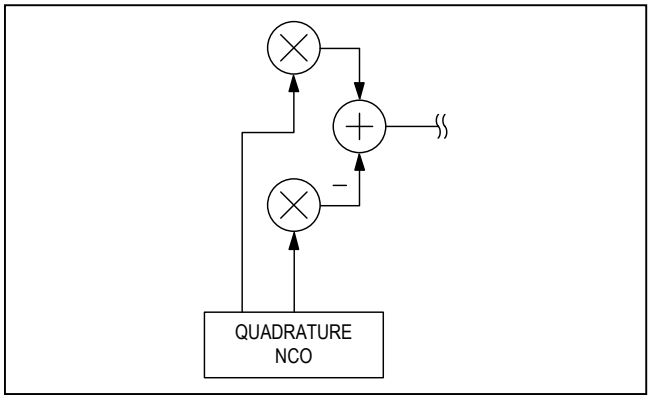


Figure 9. Complex NCO and Modulator

FCW_full is the rational value of the frequency control word. A unique feature of the MAX5868 NCO is that the frequency can be programmed with either an integer or with rational values that provide increased NCO resolution. The value of FCW_full is stored in three variables as shown here.

$$FCW\_full = FCW + \frac{NFW}{DFW}$$

where:

FCW_full is the full resolution frequency control word

FCW is the integer portion of FCW_full

NFW is the numerator of the rational portion of FCW_full

DFW is the denominator of the rational portion of FCW_full

FCW_full is calculated as:

$$FCW\_full = f_{NCO} \times \frac{2^{33}}{f_{DAC}}$$

The default values for NFW (0) and DFW (1) allow the NCO to work like a standard integer NCO with frequency control word FCW. The NCO block diagram is shown in Figure 10.

For general usage, FCW, NFW, and DFW are calculated as follows:

1) Compute FCW_full as shown above
2) Set FCW = the integer portion of FCW_full
3) Set FCW_Remain = FCW_full - FCW
4) Calculate NFW = round(FCW_Remainder x 2^{18} -1)
5) Calculate DFW = round(NFW/FCW_Remainder)
6) If desired, NFW and DFW can be reduced at this point

Example:

Assume f_{DAC} = 4960MHz, f_{NCO} = 1023MHz, then

1) $$FCW\_full = 1023MHz \times \frac{2^{33}}{4960MHz} = 1771674009.6$$
2) FCW = floor(FCW_full) = 1771674009
3) FCW_Remainder = FCW_full - FCW = 0.6
4) NFW = 0.6 x (2^{18} - 1) = round (157285.8) = 157286
5) DFW = NFW/FCW_Remainder = 157286/0.6 = round(262143.3333) = 262143

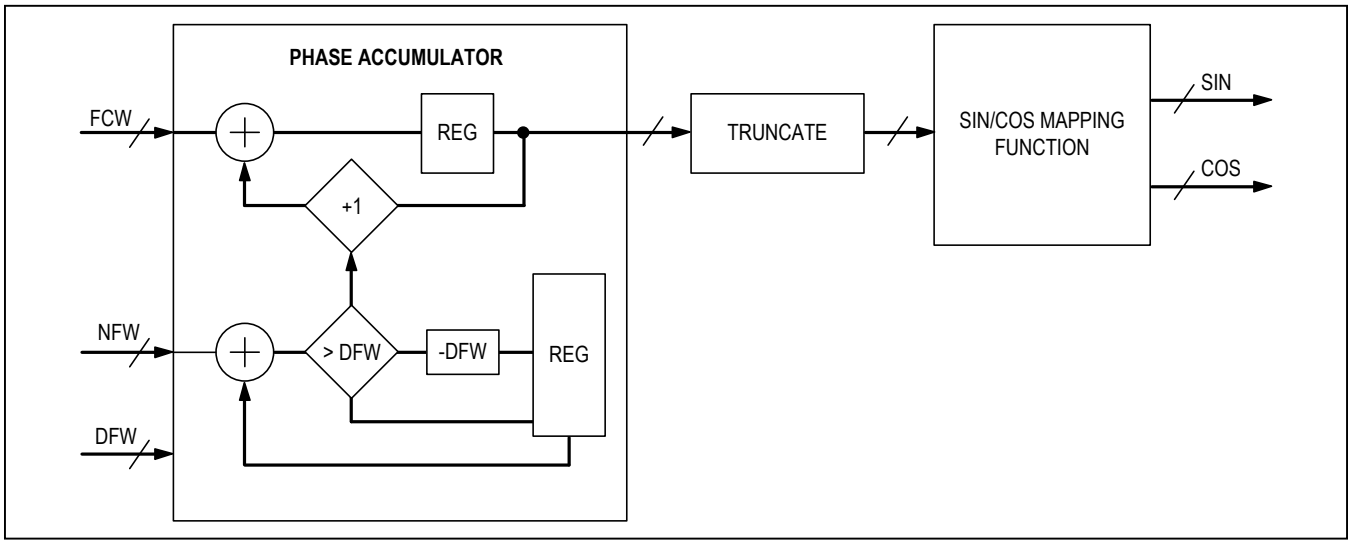


Figure 10. NCO Block Diagram

Verify:

1) FCW_full = FCW + NFW/DFW = 1771674009 + 157286/262143 = 1771674009.6000008
2) f_{NCO}=FCW_full/2^{33}xf_{DAC}=1771674009.6000008/2^{33} x 4960MHz = 1023.000MHz

In many communication applications the DAC is updated at a frequency which is a multiple of 10.24MHz allowing the NCO frequency to be set on an exact 1Hz, 10Hz, 100Hz, 1kHz, or 10kHz grid. To determine the required FCW, NFW, and DFW values to accomplish this, use the following procedure:

1) Find N: Choose the frequency grid f_{GRID} (1Hz, 10Hz, 100Hz, 1kHz or 10kHz) and set N = log (f_{GRID})
2) Find M: Determine reference frequency multiplier M

$$M = f_{DAC}/10.24MHz$$

3) Find k and L: Express M as a multiple of highest possible power of two and an integer

$$M = 2^k \times L$$

4) Compute DFW:

$$DFW = L \times 10^N$$

5) Compute FCW:

$$FCW = round(2^{23-k} \times f_{NCO}(Hz)/(DFW \times 10^{4-N}))$$

6) Compute NFW:

$$NFW = frac(2^{23-k} \times f_{NCO}(Hz)/(DFW \times 10^{4-N})) \times DFW$$

Example:

Assume f_{DAC} = 4.9152GHz, f_{NCO} = 1.84201GHz placed on 1kHz grid

1) N = log(1kHz) = 3
2) M = 4.9152GHz/10.24MHz = 480
3) M = 480 = 2^5 x 15 (k = 5, L = 15)
4) DFW = 15 x 10^3 = 15000
5) FCW = round(2^{18} x 1.84201e+9/(15000 x 10^1)) = 3219145796
6) NFW = frac(2^{18} x 1.84201e+9/(15000 x 10^1)) x 15000 = 4000

Verify:

1) FCW_full = 3219145796 + 4000/15000 = 3219145796.2666(6)
2) f_{NCO} = 3219145796.2666(6)/2^{33} x 4.9152GHz = 1.84201GHz

Programming the NCO is accomplished using the following procedure.

1) Write the FCW into the CfgNCO register
2) Enable access to the CfgNCO-E register by writing the access key (0x18) to CfgADKey
3) Write the NFW and DFW along with the NCO Extended Mode Enable bit to CfgNCO-E register
4) Ensure a DCLK signal is applied to the device
5) Write the NCOLoad bit to the CfgDSP register
6) Observe the new center frequency at the DAC output

Initialization Sequence

The MAX5868 must be powered up using the following procedure to ensure the correct and expected functionality:

1) Hold RESETB low while performing the following:
   - Apply power to the device. There are no sequencing requirements but all supplies need to present.
   - Connect the external reference, if used.
   - Apply the DAC clock signal (CLKP/CLKN) and allow the frequency to stabilize.
2) Set RESETB high
   - Wait a minimum of 350,000 DAC clock cycles.
   - Write CfgDSP (register address 0x01) with 0xiC, where "i" is the 4 bit hex value corresponding to the desired interpolation rate. Bits 2 and 3 for the hex value C represent the RstDSP and RstFIFO bits, respectively. Table 1 lists specific values for each of the various interpolation rates.

   Note that RstDSP and RstFIFO are not self-clearing bits.
   - Write CfgDSP (register address 0x01) to clear RstDSP bit. Leave the RstFIFO bit and interpolation rate as previously defined. For example, if the previous value was 0xFC (24x interpolation case), the new value to clear the RstDSP would be 0xF4.
3) Apply the DCLKP/DCLKN. The frequency must match the RCLKP/RCLKN reference clock output to prevent FIFO overflow/underflow errors.
4) Write register CfgDSP (address 0x01) to clear the RstFIFO bit. Leave the previously set interpolation rate. For example, if the previous value was 0xF4 (24x Interpolation case), the new value to clear RstFIFO would be 0xF0.
5) Program the NCO to the desired frequency. See the *Complex Modulator and NCO* section. For example, to program the NCO frequency to 1842.5MHz with 10kHz resolution using the extended frequency setting registers with a DAC clock frequency of 4960MHz, use the following sequence:
   - Write address 0x02 with 0xBE – CfgNCO LSByte
   - Write address 0x03 with 0x82
   - Write address 0x04 with 0x8C
   - Write address 0x05 with 0x63 – CfgNCO MSByte
   - Write address 0x60 (CfgADKey) with 0x18 – Enable access to Extended Frequency Control Word Register (CfgNCO-E)
   - Write address 0x6B with 0x03

Table 1. Interpolation Selection

INTERPOLATION RATE	REGISTER DATA INCLUDING RSTDSP AND RSTFIFO
24x	0xFC
20x	0xEC
16x	0xDC
12x	0xCC
10x	0x0C
8x	0xBC
6x	0xAC
5x	0x9C
4x	0x8C

   - Write address 0x6C with 0x00
   - Write address 0x6D with 0x7C
   - Write address 0x6E with 0x00
   - Write address 0x6F with 0x80
   - Write address 0x60 with 0x00 (Disable access to CfgNCO-E)
6) Set the NCOLD bit in CfgDSP (address 0x01). From the previous example, the previous value was 0xF0 (24x interpolation), the new write value is 0xF1. Note that NCOLD is a self-clearing bit.
7) Apply the data stream to the DAC inputs (D[15:0]P/N, PARP/PARN).
8) Enable the DAC output by clearing the MUTE bit in the CfgChipOM register (address 0x00). The data format must be set at this time.
   - If using offset binary, write address 0x00 with 0x01
   - If using two's complement, write address 0x00 with 0x00

SYNC Functionality

In addition to providing the framing alignment information for Byte and Nibble mode operation, the SYNCI input signal can be used to reset the internal clock dividers and to synchronize multiple devices. The SYNCI reset function is enabled by programming the CfgSync SPI register.

In single DAC or unsynchronized multi-DAC applications, either the RESETB input or SYNCI input pulse are used to reset and start the internal clock dividers. Using SYNCI resets the internal clock divider and internal interpola-

tion/modulation data path without disrupting the state of internal (SPI) control registers. The internal NCO and in the DSP data path is also reset by enabling SYNCI (CfgSync.NCO_Sync bit) thus the NCOs in multiple MAX5868s are also synchronized.

The SYNCI reset function requires a SYNCI pulse for one complete I+Q period. The signal must be high for a minimum one DCLK cycle when operating in Word mode. The pulse must be high for 2 DCLK cycles when using Byte mode and high for 4 DCLK cycles when using Nibble mode.

When not enabled to perform reset/restart function, the SYNCI input will propagate through the DSP data path and DAC input serializer to the SYNCO (LVDS) output pins and thus carry synchronization and latency information in the signal edge timing. In addition, the interpolation mode can also be verified by observing the width of the synchronization output pulse.

If desired the SYNCO pins can be monitored by additional circuitry to verify or fine tune the synchronization to within one DAC clock period. Fine tuning of synchronization to within one DAC clock period is provided by programming the CfgSync register to advance or retard data samples to the DAC by up to ±8 samples.

The synchronization accuracy between outputs of the DACs is limited only by the time skews between the clocks delivered to the DAC clock inputs and by matching of the internal clock propagation time in multiple MAX5868 devices. Internal clock propagation matching is estimated to be less than 50ps.

Synchronization is achieved by using the SYNCI LVDS input, SYNCO LVDS output and by controlling bits *ClkDiv_Sync, iFIFO_Sync*, *OIF_dinc* and *OIF_ddec* in the *CfgSync* control register accessible through the SPI interface. The CfgSync control register and the function of the control bits used in synchronization are described in Table 13.

During the synchronization process the DAC can produce voltage glitches at the output. The output signal slew rate may exceed the programmed limit during DAC synchronization. Therefore, the user should mute the DAC output signal before initiating synchronization. The DAC output can be muted by ramping down the input signal amplitude in the digital domain, or using the MUTE function.

The synchronization input SYNCI serves dual functions depending on the state of bits *ClkDiv_Sync and iFIFO_Sync*. If *ClkDiv_Sync and iFIFO_Sync* are set to one, forcing one on SYNCI input will synchronously reset the MAX5868. If *ClkDiv_Sync and iFIFO_Sync* are set to zero, the signal forced at SYNCI is sent to the SYNCO output through a path having latency identical to the latency of the DAC input DSP path. The timing of the SYNCO outputs of multiple DACs can be then compared and fine adjusted using the *OIF_dinc* and *OIF_ddec* control bits.

Synchronization Procedure

1) Set ClkDiv_Sync and iFIFO_Sync to one.
2) Pulse SYNCI high for at least one I+Q period synchronously to DCLK. The FPGA/ASIC generating DAC input data D[15:0] should be used to generate the SYNCI signal. The SYNCI transitions should be aligned with the input data transitions and they should be simultaneous in all devices being synchronized.
3) After pulsing SYNCI as described in step 2), the DACs are aligned to within one DAC clock cycle. If more precise synchronization is needed proceed to step 4).
4) Set ClkDiv_Sync and iFIFO_Sync to zero.
5) Pulse SYNCI synchronously to DCLK and simultaneously in all DACs for at least one DCLK cycle and measure the timing skew between the SYNCO outputs from two MAX5868 devices that need to be precisely aligned.
6) Use OIF_dinc and OIF_ddec control bits in one of the DACs to precisely align SYNCO outputs of the two MAX5868 devices.
7) Repeat the alignment of SYNCO outputs for all remaining MAX5868 devices using one of the devices as a common reference.

Figure 11 shows how the multiple DAC synchronization can be verified. Two tones with the same frequency and amplitude but 180° out of phase are supplied to the digital inputs of two MAX5868 DACs. The RF outputs of both DACs are combined. The accuracy of the two DAC synchronization is inversely proportional to the combined signal power.

Initialization and the MUTE Function

The MAX5868 requires a minimum of 350,000 clock cycles at power up to complete its internal initialization. Any adjustments to the internal timing by the user, such as resetting the clock dividers, can create significant signal glitches at the DAC output. The device has a DAC MUTE function to eliminate these potentially damaging transients. The DAC output is muted at power up. The user must turn muting off via the SPI interface when ready to transmit.

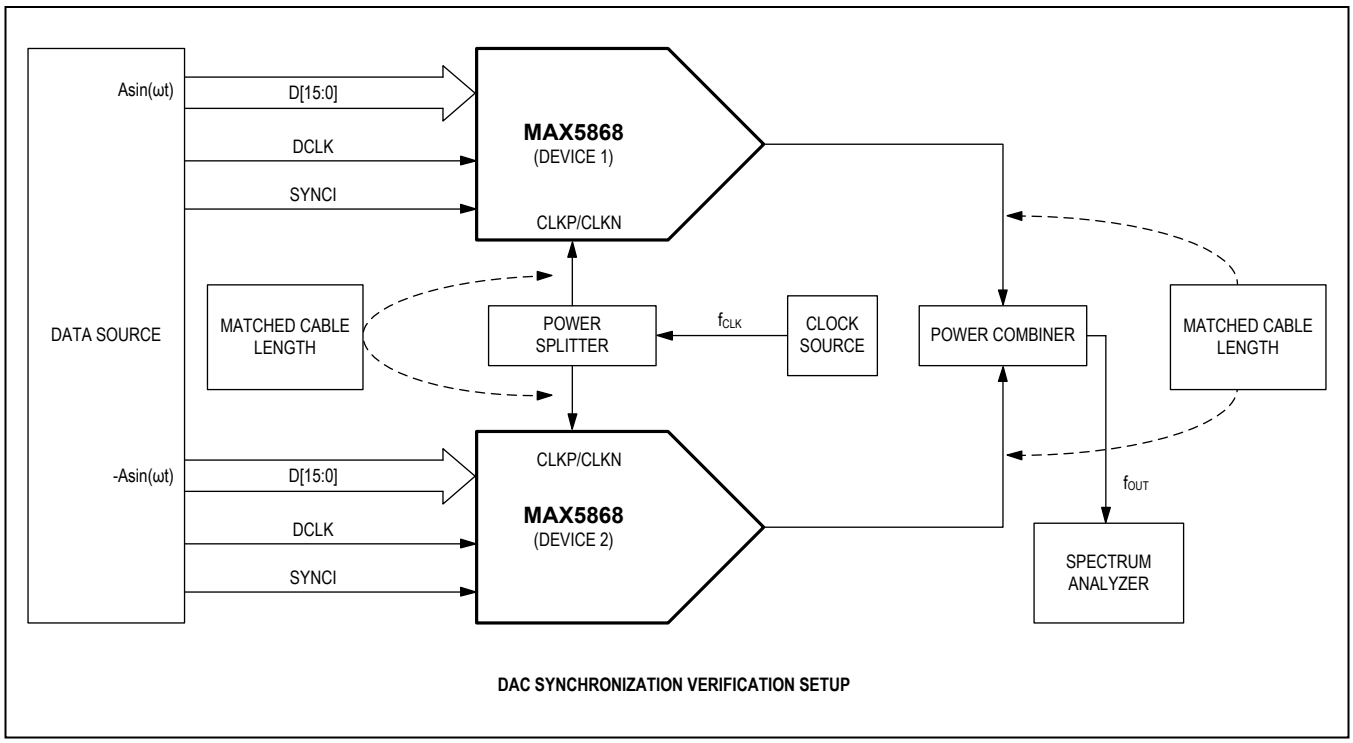


Figure 11. DAC Synchronization Verification Setup

Power Supplies

All of the signals that interface with the MAX5868 pins (e.g. clock, LVDS digital I/O, OUTN/P) are referenced to a 1.8V supply. There are three supply domains: clock, digital I/O, and analog. Each of these domains has a 1.8V level as well as a 1.0V core level. For the clock and digital I/O domains, both supply levels are required for a total of four supplies: AVCLK2 (1.8V) and AVCLK (1.0V) for clock, V_{DD2} (1.8V) and V_{DD} (1.0V) for digital I/O. The analog supply domain is treated differently. There is a 1.8V level (AVDD2) for the OUTP/N signal and the reference circuitry. The reference circuits are the only core devices biased at 1.8V. The analog domain 1.0V level (AVDD) is established by an LDO and powers the DAC core. Dedicated pins for the AVDD (1.0V) supply are provided so external bypass capacitance can be added if needed.

Peak-Detector Circuitry

The device includes a digital peak detector for use in monitoring the amplitude of the interpolated and modulated data. The peak detector is configured through the SPI interface to count an event either above or below a user-programmed threshold during a user-defined window. The threshold is programmed via the 8-bit CfgPDT register in two's complement format and has a range from -100% to 99.2% of the full-scale output current with approximately 0.8% resolution. Positive or negative peak detection is configured using the CfgPD.Mode bit. The 48-bit CfgPDMC register (six 8-bit registers) is used to define the maximum number of DAC clock cycles for the peak detector function. When this count is reached, the STATUS.PDDONE bit will be set and generate an interrupt if enabled by the EINT register. After the interrupt, the threshold crossing count recorded in the StatPd register is ready to be read. The CfgPD.Reset bit is used to reset the event count and the CfgPD.Start bit is used to start the peak detector counter.

Interrupt System

The INTB pin is a CMOS output port that signals an interrupt condition when in the low state. The interrupt system is composed of an interrupt register and an interrupt mask. The interrupt signal is a logic NOR of the bitwise AND operation of the interrupt register and the interrupt mask. In the MAX5868, seven interrupt bits are defined: 2 bits for I or Q parity errors, 3 bits for a FIFO collision

Table 2. Interrupt Generation

BIT	NAME	FUNCTION†
7	PARI	Latched status set when a parity error on the Input Interface I-sample is detected
6	PARQ	Latched status set when a parity error on the Input Interface Q-sample is detected
5	FCOL	Latched status set when the Input FIFO write and read pointers collide causing FIFO underflow or overflow
4	F1A	Latched status set when the Input FIFO write and read pointers are away from each other by one sample
3	F2A	Latched status set when the Input FIFO write and read pointers are away from each other by two samples
2	TRDY	Latched status set when trim loading is complete
1	—	Not used
0	PDDONE	Latched status set when the peak detector status update is complete. The peak detector configuration registers are DSP.CfgPD, DSP.CfgPDT, DSP.CfgPDMC and the peak monitor status register is DSP.StatPD

†Nomenclature Format: RegisterBankName.RegisterName

(1-away and 2-away), 1 bit for Trim ready, and 1 bit for the DAC Peak Detector Status update complete. Figure 12 shows the interrupt generation process. The interrupt mask and register can be modified through the serial interface. Table 2 shows all the status register bits that can be enabled to generate an interrupt.

Digital Control Pins

The MAX5868 contains two 1.8V CMOS logic digital control pins, RESETB and MUTE. The device is placed in a reset state when RESETB is low. This control line is level sensitive. On power-up RESETB should remain low until all supply voltages have stabilized.

The MUTE pin defines when the part enters the mute mode. A high logic level places the device in mute mode while a low state establishes normal operation. In mute mode the DAC digital input is set to midscale. The main purpose of mute is to eliminate any transmit power during the receive time of a TDMA system. In addition, there is a mute configuration programmed through the serial interface that enables the mute mode internally regardless of the state of the MUTE pin. A duplication of the interrupt mask registers as Mute Enable registers generate the internal mute signal. Figure 13 shows all the status register bits that can be enabled to generate internal mute. The internal control state of the DAC is preserved while the MAX5868 is in the mute state.

Serial Control Interface

The serial interface is composed of four 1.8V CMOS logic signal pins: CSB, SCLK, SDI, and SDO. The device always operates as a slave with the master controlling the CSB, SCLK, and SDI inputs. SDO is high impedance except when the device is transmitting. CSB is the chip select pin. While in the low state, the device is open to communication through the SCLK, SDI, and SDO pins.

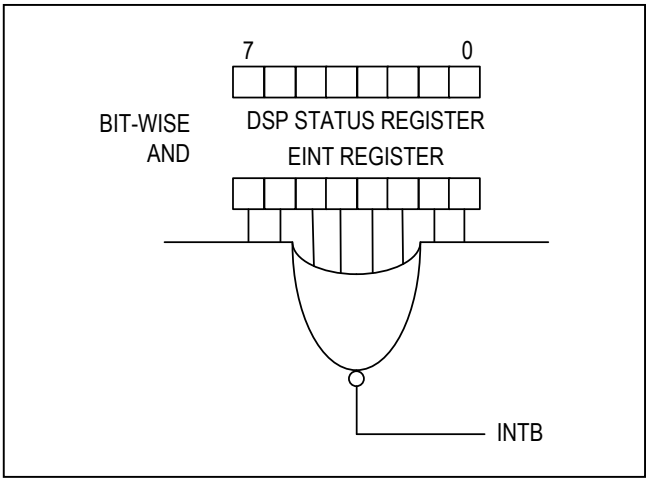


Figure 12. Interrupt Generation

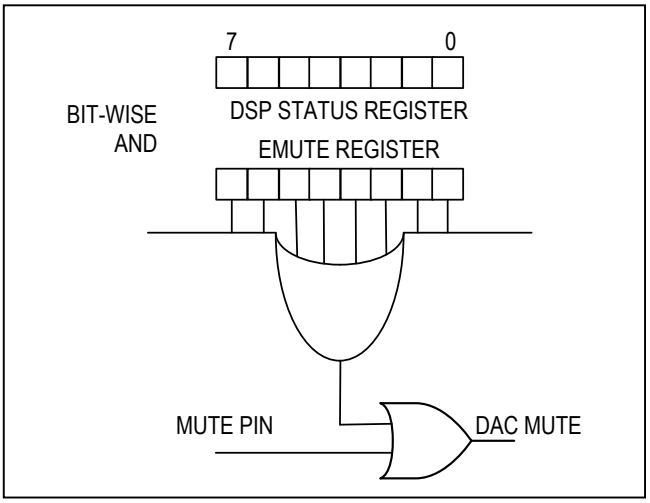


Figure 13. DAC Mute Generation

Each communication cycle is composed of a read/write prefix bit, an address word, and an input word or an output word. The serial interface clock, SCLK, latches data into the device on the rising edge and clocks data out on the falling edge. A one for the R/W bit signifies a read operation and a zero indicates a write operation. See Figure 14.

The R/$\overline{W}$ bit followed by the address word are sent to the device through the SDI pin. The address word is 11 bits wide and it is transmitted MSB to LSB.

During a write operation, a data byte (8 bits) is immediately written to the device after the last address bit. The data byte is transmitted from the controller to the device in order of MSB to LSB.

During a read operation, the data byte is transmitted from the device to the master on the SDO signal line. The transmission starts on the falling edge of SCLK immediately after the address word LSB is latched. The data byte from the device is also transmitted in order of MSB to LSB. The SDO driver enters a high-impedance state on the next falling SCLK edge immediately after the data byte LSB is transmitted.

CSB must toggle from low to high before another communication cycle can execute. The SDO and SDI signals can be tied together to achieve an SDIO communication pin.

Figure 14 shows a single write sequence and a single read sequence. Figure 15 shows the details of the timing requirements for the serial interface.

The user has access to 15 internal registers, which serve various functions including control of the device operation reporting the status of specific operational parameters.

Table 3 lists the register definitions. Table 4 to Table 18 define the functionality of each register.

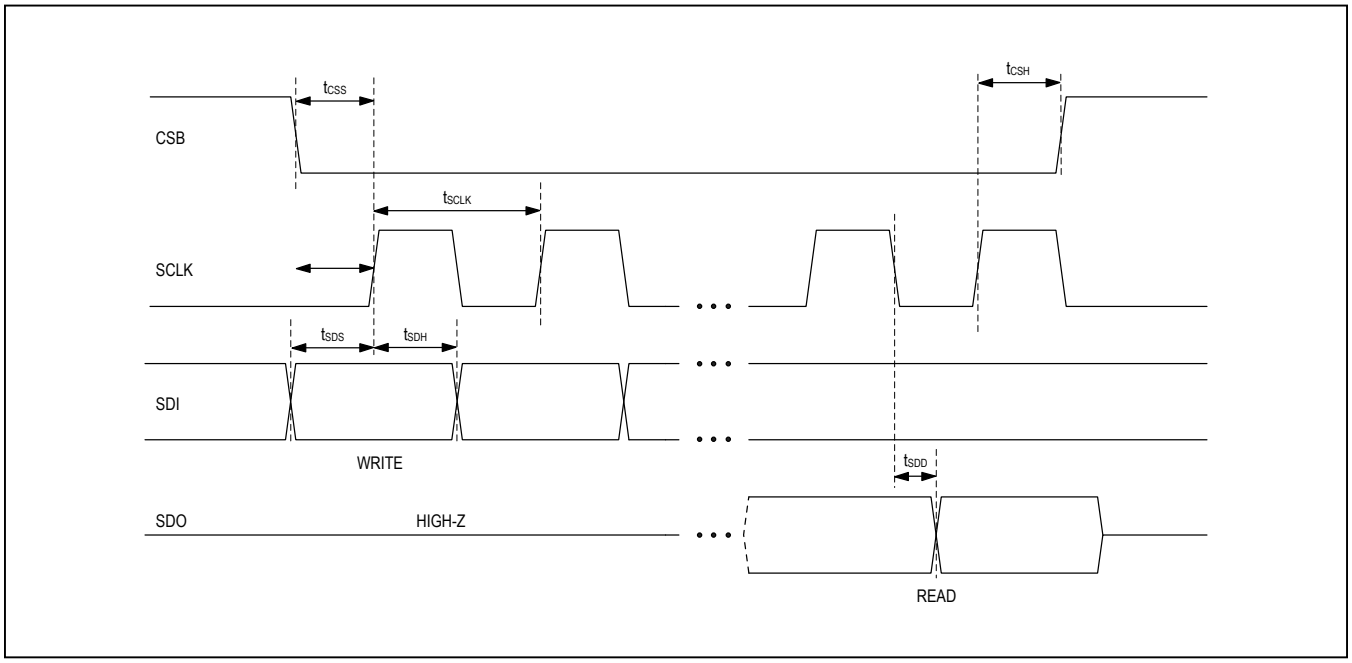


Figure 14. SPI Timing

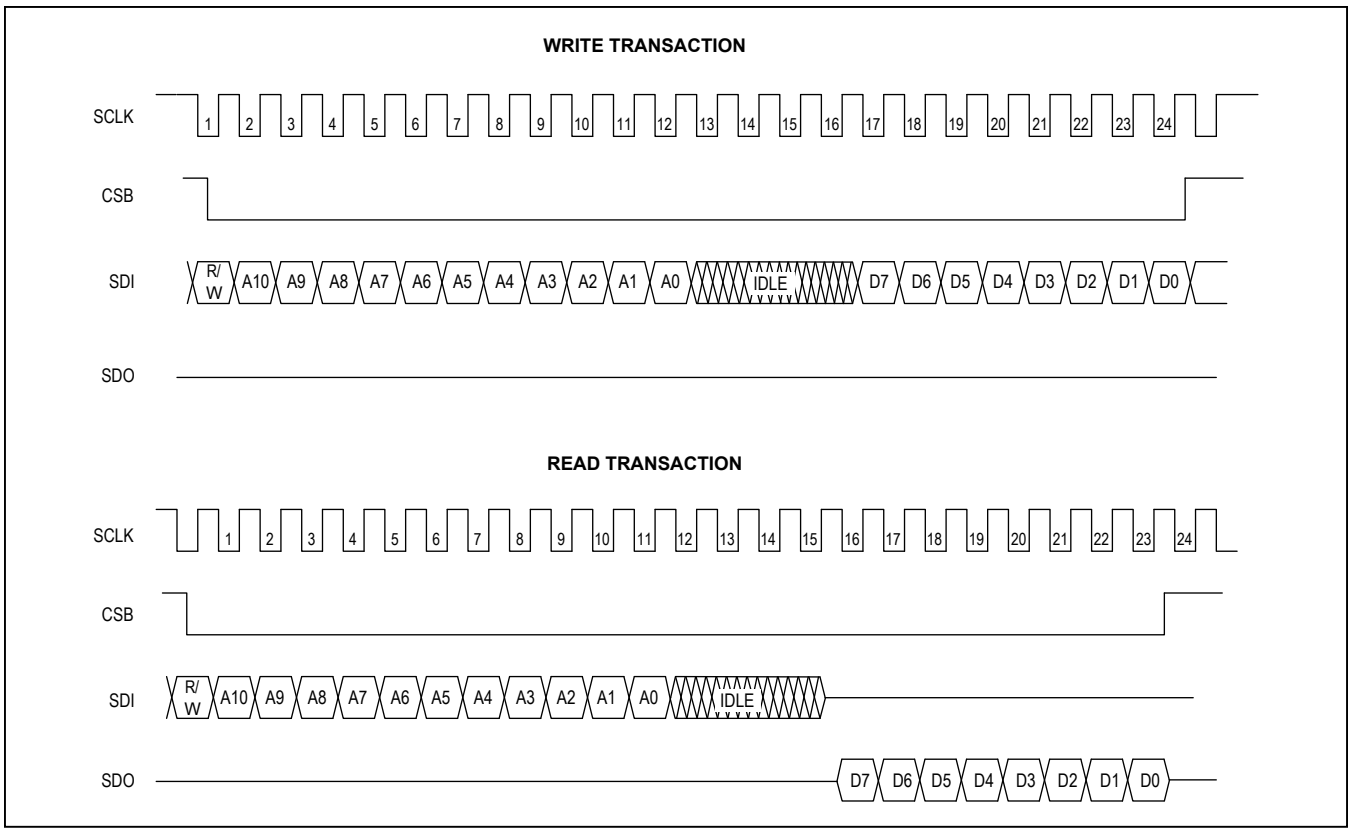


Figure 15. SPI Write and Read Transactions

Table 3. SPI Register Descriptions

REGISTER NAME	BYTE	READ/WRITE	ADDRESS (DECIMAL)	DESCRIPTION
CHIP OPERATION MODE				
CfgChipOM	1	R/W	0	Configure Chip Operation Mode: data interface modes, data format, reset, and mute/normal mode.
DSP ENGINE OPERATION				
CfgDSP	1	R/W	1	Configure DSP Engine. Interpolation rate, reset DSP and FIFO, enable saturation detection, NCO load.
CfgNCO	4	R/W	2–5	Configure NCO Frequency Control Word
CfgPD	1	R/W	6	Configure Peak Detector
CfgPDT	1	R/W	7	Configure Peak Detector Threshold
CfgPDMC	6	R/W	8–13	Configure Peak Detector Maximum Count, 8 x 6 = 48 bits
StatPD	2	R	14–15	Peak Detector Status
CfgSync	1	R/W	80	Configure SYNCI and SYNCO Functionality
CfgFIFO	1	R/W	81	Configure Input FIFO
CfgADKey	1	R/W	96	Configure Advanced Digital Key Access
CfgNCO-E	1	R/W	107–111	Configure NCO Extended Resolution
CHIP INTERRUPT				
EMUTE	1	R/W	84	Mute Enable Mask
EINT	1	R/W	85	Interrupt Enable Mask
STATUS	1	R/W	86	Status
DEVICE SERIAL NUMBER				
DevSN	3	R	87	Device Serial Number. Total 8 x 3 = 24 bits

Note: *Do not write to registers with addresses not listed in Table 3. Register addresses not listed are reserved for factory use.*

Configuration Register Definitions

Table 4. Configure Chip Operation Mode Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x00	1	**CfgChipOM**	Configure Chip Operation Mode							
		Bit	7	6	5	4	3	2	1	0
		Name	NA	DIM1	DIM0	INVQ	Reset	Mute	NA	DFMT
		Default	0	0	0	0	0	1	0	1

Bits 6:5: DIM[1:0] (Data Interface Mode)

00 = Data interface in 16-bit word mode (default).

01 = Data interface in 8-bit byte mode.

10 = Data interface in 4-bit nibble mode.

11 = Reserved.

Bit 4: INVQ (Invert Q Data)

1 = Enable I-Q data Q being inverted to make I+Q.

0 = Disable I-Q data Q being inverted to make I-Q (default).

Bit 3: Reset

1 = Global reset for the entire chip.

0 = No reset.

Bit 2: Mute

1 = Put chip (DAC) into mute mode.

0 = Chip in normal mode.

Bit 0: DFMT (Data Format)

1 = Input data in offset binary format (default).

0 = Input data in two’s complement format.

Table 5. Configure DSP Engine Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x01	1	**CfgDSP**	Configure DSP Engine							
		Bit	7	6	5	4	3	2	1	0
		Name	R3	R2	R1	R0	RstDSP	RstFIFO	NA	NCOLD
		Default	0	0	0	0	0	0	0	0

Bits 7:4: R[3:0]. Define interpolation ratio.

4'b1111	→	24x	4'b1100	→	12x	4'b1010	→	6x
4'b1110	→	20x	4'b0xxx	→	10x	4'b1001	→	5x
4'b1101	→	16x	4'b1011	→	8x	4'b1000	→	4x

Bit 3: RstDSP (Reset DSP)

1 = Reset DSP (Input FIFO, interpolation filters, complex modulator, NCO).

0 = No reset.

Bit 2: RstFIFO (Reset FIFO)

1 = Reset input data FIFO and DAC FIFO to default status.

0 = No reset.

Bit 0: NCOLD (NCO Load)

Write a 1 to load NCO configuration. This bit is self-clearing.

Table 6. Configure NCO Frequency Control Word Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
	4	**CfgNCO**	Configure NCO Frequency Control Word							
0x02		Bit	7	6	5	4	3	2	1	0
		Name	FCW7	FCW6	FCW5	FCW4	FCW3	FCW2	FCW1	FCW0
0x03		Bit	15	14	13	12	11	10	9	8
		Name	FCW15	FCW14	FCW13	FCW12	FCW11	FCW10	FCW9	FCW8
0x04		Bit	23	22	21	20	19	18	17	16
		Name	FCW23	FCW22	FCW21	FCW120	FCW19	FCW18	FCW17	FCW16
0x05		Bit	31	30	29	28	27	26	25	24
		Name	FCW31	FCW30	FCW29	FCW28	FCW27	FCW26	FCW25	FCW24
		Default	32'h00000000							

Bits 31:0: FCW[31:0]. FCW31 is the frequency control word MSB. FCW0 is the frequency control word LSB.

Table 7. Configure NCO Extended Frequency Control Word Access Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x60	1	**CfgADKey**	Configure Advanced Digital Access Key							
		Bit	7	6	5	4	3	2	1	0
		Name	ADKEY7	ADKEY6	ADKEY5	ADKEY4	ADKEY3	ADKEY2	ADKEY1	ADKEY0

BITS [7:0]: ADKEY[7:0] Write 0x18 to this address to access extended NCO Frequency Control register.
Write 0x00 to this address after updating the extended NCO Frequency Control register to disable further access.

Table 8. Configure NCO Extended Frequency Control Word Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
		CfgNCO-E	Configure NCO Extended Resolution							
0x6B	5	Bit	7	6	5	4	3	2	1	0
		Name	NFW7	NFW6	NFW5	NFW4	NFW3	NFW2	NFW1	NFW0
0x6C		Bit	15	14	13	12	11	10	9	8
		Name	NFW15	NFW14	NFW13	NFW12	NFW11	NFW10	NFW9	NFW8
0x6D		Bit	23	22	21	20	19	18	17	16
		Name	DFW5	DFW4	DFW3	DFW2	DFW1	DFW0	NFW17	NFW16
0x6E		Bit	31	30	29	28	27	26	25	24
		Name	DFW13	DFW12	DFW11	DFW10	DFW9	DFW8	DFW7	DFW6
0x6F		Bit	39	38	37	36	35	34	33	32
		Name	NCOEE	NA	NA	DWF18	DWF17	DFW16	DWF15	DFW14
		Default	40'h0000040000							

Bits[17:0]: NFW[17:0] Numerator for extended NCO range, rational portion of FCW_full
Bits[36:18]: DFW[18:0] Denominator for the extended NCO range, rational portion of FCW_full
Bits[38:37] Unused
Bit[39]: NCOEE (**NCO Extended Mode Enable**)

Table 9. Configure Peak Detector Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x06	1	**CfgPD**	Configure Peak Detector							
		Bit	7	6	5	4	3	2	1	0
		Name	NA	NA	NA	NA	NA	Start	Mode	Reset
		Default	—	—	—	—	—	0	0	0

Bit 2: Start. Peak detector start.

Bit 1: Mode

1 = Count samples above the threshold.

0 = Count samples below the threshold.

Bit 0: Reset. Writing a 1 resets the peak detector count stored in the StatPD register. This bit is self-clearing.

Table 10. Configure Peak Detector Threshold Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
	1	**CfgPDT**	Configure Peak Detector Threshold							
0x07		Bit	7	6	5	4	3	2	1	0
		Name	PDT7	PDT6	PDT5	PDT4	PDT3	PDT2	PDT1	PDT0
		Default	8'h00							

Bits 7:0: PDT[7:0] (Peak Detector Threshold) Two's complement 8-bit value with a range from -100% (8'h80) to +99.2% (8'h7F) of Full Scale.

Table 11. Configure Peak Detector Maximum Count Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
	6	**CfgPDMC**	Configure Peak Detector Maximum Count, 8 x 6 = 48 bits							
0x08		Bit	7	6	5	4	3	2	1	0
		Name	PDMC7	PDMC6	PDMC5	PDMC4	PDMC3	PDMC2	PDMC1	PDMC0
0x09		Bit	15	14	13	12	11	10	9	8
		Name	PDMC15	PDMC14	PDMC13	PDMC12	PDMC11	PDMC10	PDMC9	PDMC8
0x0A		Bit	23	22	21	20	19	18	17	16
		Name	PDMC23	PDMC22	PDMC21	PDMC20	PDMC19	PDMC18	PDMC17	PDMC16
0x0B		Bit	31	30	29	28	27	26	25	24
		Name	PDMC31	PDMC30	PDMC29	PDMC28	PDMC27	PDMC26	PDMC25	PDMC24
0x0C		Bit	39	38	37	36	35	34	33	32
		Name	PDMC39	PDMC38	PDMC37	PDMC36	PDMC35	PDMC34	PDMC33	PDMC32
0x0D		Bit	47	46	45	44	43	42	41	40
		Name	PDMC47	PDMC46	PDMC45	PDMC44	PDMC43	PDMC42	PDMC41	PDMC40
		Default	40'h0000 0000 0000							

Bits 47:0: PDMC[47:0] (Peak Detector Maximum Count) Offset binary format, defines maximum number of DAC clock cycles for the peak detector function. When this count is reached, the STATUS.PDDONE bit will be set.

Table 12. Peak Detector Status Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
	2	**StatPD**	Peak Detector Status							
0x0E		Bit	7	6	5	4	3	2	1	0
		Name	PDST7	PDST6	PDST5	PDST4	PDST3	PDST2	PDST1	PDST0
0x0F		Bit	15	14	13	12	11	10	9	8
		Name	X	X	X	X	PDST11	PDST10	PDST9	PDST8
		Default	12'h000							

Bits 11:0: PDST[11:0] (Peak Detector Status) Indicates threshold crossing count.

Table 13. Configure SYNCI and SYNCO Functionality Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x50	1	**CfgSync**	Configure SYNCI and SYNCO Functionality							
		Bit	7	6	5	4	3	2	1	0
		Name	NA	ClkDiv_ Sync	iFIFO_ Sync	NCO_ Sync	NA	SYNCO _Sel	OIF_ dinc	OIF_ ddec
		Default	0	0	0	0	0	0	0	0

Bit 6: ClkDiv_Sync

1 = Enable SYNCI reset to the clock divider block.

0 = Disable SYNCI reset to the clock divider block.

Bit 5: iFIFO_Sync

1 = Enable SYNCI reset to the input FIFO.

0 = Disable SYNCI reset to the input FIFO.

Bit 4: NCO_Sync

1 = Enable SYNCI reset to the NCO.

0 = Disable SYNCI reset to the NCO.

Bit 2: SYNCO_Sel (SYNCO Select)

1 = NCO 0-phase detection output on SYNCO signal.

0 = SYNCI is passed through to SYNCO.

Bit 1: OIF_dinc (Output FIFO Delay Increase) Toggle 0 to 1. Increase delay of the output interface by one DAC clock cycle. This bit is self-clearing. Maximum delay offset is ±8 DAC clock cycles.

Bit 0: OIF_ddec (Output FIFO Delay Decrease) Toggle 0 to 1. Decrease delay of the output interface by one DAC clock cycle. This bit is self-clearing. Maximum delay offset is ±8 DAC clock cycles.

Table 14. Configure Input FIFO Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x51	1	**CfgFIFO**	Configure Input FIFO							
		Bit	7	6	5	4	3	2	1	0
		Name	RdPtrAdj3	RdPtrAdj2	RdPtrAdj1	RdPtrAdj0	Off	DupI	SwapIQ	RevBitOrd
		Default	0	0	0	0	0	0	0	0

Bits 7:4: RdPtrAdj[3:0] (Read Pointer Adjust). Adjust read pointer by adding this value to the free-running read pointer.

Bit 3: Off

1 = Input FIFO is bypassed.

0 = Input FIFO is not bypassed.

Bit 2: DupI (Duplicate I Enable)

1 = Duplicate I.

0 = Do not duplicate I.

Bit 1: SwapIQ (Swap I/Q Order Enable)

1 = Reverse I/Q order.

0 = Normal I/Q order.

Bit 0: RevBitOrd (Reverse LSB/MSB Bit Order Enable)

1 = Reverse LSB/MSB order.

0 = Normal LSB/MSB order.

Table 15. Enable Mute Mask Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x54	1	**EMUTE**	Enable Mute Mask							
		Bit	7	6	5	4	3	2	1	0
		Name	EM7	EM6	EM5	EM4	EM3	EM2	EM1	EM0
		Default	0	0	0	0	0	0	0	0

Bits 7:0: EM[7:0] (Enable Mute Mask)

1 = Enable mute bit x in the STATUS register.

0 = Disable mute bit x in the STATUS register.

Table 16. Enable Interrupt Mask Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x55	1	**EINT**	Enable Interrupt Mask							
		Bit	7	6	5	4	3	2	1	0
		Name	EINT7	EINT6	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
		Default	0	0	0	0	0	1	0	0

Bits 7:0: EINT[7:0] (Enable Interrupt Mask)

1 = Enable interrupt bit x in the STATUS register.

0 = Disable interrupt bit x in the STATUS register.

Table 17. Status Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
0x56	1	**STATUS**	Status							
		Bit	7	6	5	4	3	2	1	0
		Name	PARI	PARQ	FCOL	F1A	F2A	TRDY	—	PDDONE
		Default	0	0	0	0	0	0	0	0

Bits 7:6: PAR[I:Q] (Parity Error: I and Q Data)

1 = Parity error in x-data, where x = I or Q.

0 = No Parity error in x-data.

Bit 5: FCOL (FIFO R/W Pointer Collision)

1 = Input FIFO read/write pointers are in collision, indicating FIFO underflow/overflow.

0 = Input FIFO read/write pointers are not in collision.

Bit 4: F1A (FIFO R/W Pointers 1-Away)

1 = Input FIFO read/write pointers are 1-away.

0 = Input FIFO read/write pointers are not 1-away.

Bit 3: F2A (FIFO R/W Pointers 2-Away)

1 = Input FIFO read/write pointers are 2-away.

0 = Input FIFO read/write pointers are not 2-away.

Bit 2: TRDY

1 = Trim loading complete.

0 = Trim loading not complete.

Bit 0: PDDONE (Peak Detector Status Update)

1 = Peak detector status update done.

0 = Peak detector status update in progress. Writing 0 clears a bit and writing 1 does nothing.

Table 18. Device Serial Number Register Bitmap

ADDRESS	BYTE	REGISTER NAME	DESCRIPTION							
	3	**DevSN**	Device Serial Number. Total 8 x 3 = 24 bits							
0x57		Bit	7	6	5	4	3	2	1	0
		Name	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
0x58		Bit	15	14	13	12	11	10	9	8
		Name	SN15	SN14	SN13	SN12	SN11	SN10	SN9	SN8
0x59		Bit	23	22	21	20	19	18	17	16
		Name	SN23	SN22	SN21	SN20	SN19	SN18	SN17	SN16

Bits 23:0: SN[23:0]. 16.77 million unique serial numbers programmed during factory test.

Static Performance Parameter Definitions

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB.

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes, with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the specified accuracy.

Adjacent Channel Power (ACP)

Adjacent channel power is commonly used in combination with DOCSIS-compliant QAM signals. ACP is the ratio in dB between the power in a channel at a specified frequency offset from the edge of the transmitted channel block, and power in the lowest frequency channel of the transmitted block. ACP provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5868EXE+	-40°C to +85°C	144 CBGSA

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
144 CSBGA	X14400+4	21-0169	90-0289

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—
1	6/14	Updated *Package Thermal Characteristics* and settling time typical specifications	2, 4

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