19-3631; Rev 2; 10/08

EVALUATION KIT AVAILABLE

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs



## General Description

The MAX5894 programmable interpolating, modulating, 500Msps, dual digital-to-analog converter (DAC) offers superior dynamic performance and is optimized for high-performance wideband, single-carrier transmit applications. The device integrates a selectable 2x/4x/8x interpolating filter, a digital quadrature modulator, and dual 14-bit, high-speed DACs on a single integrated circuit. At 30MHz output frequency and 500Msps update rate, the in-band SFDR is 86dBc while consuming 1.1W. The device also delivers 73dB ACLR for two-carrier WCDMA at a 61.44MHz output frequency.

The selectable interpolating filters allow lower input data rates while taking advantage of the high DAC update rates. These linear-phase interpolation filters ease reconstruction filter requirements and enhance the passband dynamic performance. Individual offset and gain programmability allow the user to calibrate out local oscillator (LO) feedthrough and sideband suppression errors generated by analog quadrature modulators.

The MAX5894 features a $f_{IM}/4$ digital image-reject modulator. This modulator generates a quadrature-modulated IF signal that can be presented to an analog I/Q modulator to complete the upconversion process. A second digital modulation mode allows the signal to be frequency-translated with image pairs at $f_{IM}/2$ or $f_{IM}/4$.

The MAX5894 features a standard 1.8V CMOS, 3.3V tolerant data input bus for easy interface. A 3.3V SPI™ port is provided for mode configuration. The programmable modes include the selection of 2x/4x/8x interpolating filters, $f_{IM}/2$, $f_{IM}/4$ or no digital quadrature modulation with image rejection, channel gain and offset adjustment, and offset binary or two's complement data interface.

Pin-compatible 12- and 16-bit devices are also available. Refer to the MAX5893 data sheet for the 12-bit version and the MAX5895 data sheet for the 16-bit version.

## Applications

Base Stations: 3G UMTS, CDMA, and GSM

Broadband Wireless Transmitters

Broadband Cable Infrastructure

Instrumentation and Automatic Test Equipment (ATE)

Analog Quadrature Modulation Architectures

***Pin Configuration appears at end of data sheet.***

*SPI is a trademark of Motorola, Inc.*

*cdma2000 is a registered trademark of Telecommunications Industry Association.*

## Features

- **74dB ACLR at $f_{OUT}$ = 61.44MHz (Single-Carrier WCDMA)**
- **Meets 3G UMTS, cdma2000®, GSM Spectral Masks ($f_{OUT}$ = 122MHz)**
- **Noise Spectral Density = -154dBFS/Hz at $f_{OUT}$ = 16MHz**
- **91dBc SFDR at Low-IF Frequency (10MHz)**
- **88dBc SFDR at High-IF Frequency (50MHz)**
- **Low Power: 886mW ($f_{CLK}$ = 250MHz)**
- **User Programmable**
  - **Selectable 2x, 4x, or 8x Interpolating Filters**
    - **< 0.01dB Passband Ripple**
    - **> 99dB Stopband Rejection**
  - **Selectable Real or Complex Modulator Operation**
  - **Selectable Modulator LO Frequency: OFF, $f_{IM}/2$ or $f_{IM}/4$**
  - **Selectable Output Filter: Lowpass or Highpass**
  - **Channel Gain and Offset Adjustment**
- **EV Kit Available (Order the MAX5894 EV Kit)**

## Ordering Information

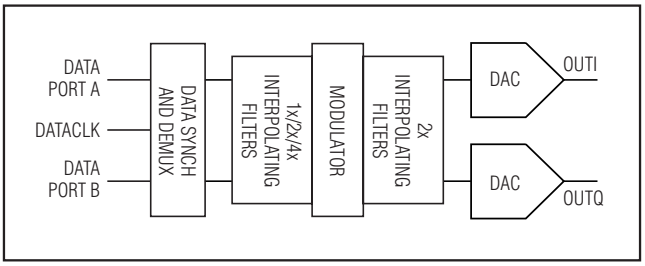
| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX5894EGK-D | -40°C to +85°C | 68 QFN-EP* |
| MAX5894EGK+D | -40°C to +85°C | 68 QFN-EP* |

*D = Dry pack.*
**EP = Exposed pad.*
*+Denotes a lead-free/RoHS-compliant package.*

## Selector Guide

| PART | RESOLUTION (BITS) | DAC UPDATE RATE (Msps) | INPUT LOGIC |
|---|---|---|---|
| MAX5893 | 12 | 500 | CMOS |
| MAX5894 | 14 | 500 | CMOS |
| MAX5895 | 16 | 500 | CMOS |
| MAX5898 | 16 | 500 | LVDS |

## Simplified Diagram



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## ABSOLUTE MAXIMUM RATINGS

$DV_{DD1.8}$, $AV_{DD1.8}$ to GND, DACREF .....-0.3V to +2.16V
$AV_{DD3.3}$, $AV_{CLK}$, $DV_{DD3.3}$ to GND, DACREF.....-0.3V to +3.9V
DATACLK, A0–A13, B0–B11,
SELIQ/B13, DATACLK/B12, $\overline{CS}$, $\overline{RESET}$, SCLK,
DIN and DOUT to GND, DACREF...-0.3V to ($DV_{DD3.3}$ + 0.3V)
CLKP, CLKN to GND, DACREF.....-0.3V to ($AV_{CLK}$ + 0.3V)
REFIO, FSADJ to GND, DACREF .....-0.3V to ($AV_{DD3.3}$ + 0.3V)
OUTIP, OUTIN, OUTQP,
OUTQN to GND, DACREF.....-1V to ($AV_{DD3.3}$ + 0.3V)
DOUT, DATACLK, DATACLK/B12 Continuous Current.....8mA
Continuous Power Dissipation ($T_A$ = +70°C)
68-Pin QFN (derate 41.7mW/°C above +70°C)
(Note 1) .....3333.3mW
Junction Temperature.....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Thermal Resistance $\theta_{JC}$ (Note 1).....0.8°C/W

**Note 1:** Thermal resistance based on a multilayer board with 4 x 4 via array in exposed pad area.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, DATACLK output mode, dual-port mode, 50Ω double-terminated outputs, external reference at 1.25V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE** | | | | | | | |
| Resolution | | | | | 14 | | Bits |
| Differential Nonlinearity | DNL | | | | ±0.5 | | LSB |
| Integral Nonlinearity | INL | | | | ±1.0 | | LSB |
| Offset Error | OS | | | -0.025 | 0.003 | +0.025 | %FS |
| Offset Drift | | | | | ±0.03 | | ppm/°C |
| Full-Scale Gain Error | $GE_{FS}$ | | | -4 | -0.6 | +4 | %FS |
| Gain-Error Drift | | | | | ±110 | | ppm/°C |
| Full-Scale Output Current | $I_{OUTFS}$ | | | 2 | | 20 | mA |
| Output Compliance | | | | -0.5 | | +1.1 | V |
| Output Resistance | $R_{OUT}$ | | | | 1 | | MΩ |
| Output Capacitance | $C_{OUT}$ | | | | 5 | | pF |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Maximum Clock Frequency | $f_{CLK}$ | | | 500 | | | MHz |
| Minimum Clock Frequency | $f_{CLK}$ | | | | | 1 | MHz |
| Maximum DAC Update Rate | $f_{DAC}$ | $f_{DAC} = f_{CLK}$ or $f_{DAC} = f_{CLK}/2$ | | 500 | | | Msps |
| Minimum DAC Update Rate | $f_{DAC}$ | $f_{DAC} = f_{CLK}$ or $f_{DAC} = f_{CLK}/2$ | | | | 1 | Msps |
| Maximum Input Data Rate | $f_{DATA}$ | | | 125 | | | MWps |
| Noise Spectral Density | | $f_{DATACLK}$ = 125MHz, $f_{OUT}$ = 16MHz, $f_{OFFSET}$ = 10MHz, -12dBFS | No interpolation | | -154 | | dBFS/Hz |
| | | | 2x interpolation | | -154 | | |
| | | | 4x interpolation | | -154 | | |
| | | $f_{DATACLK}$ = 125MHz, $f_{OUT}$ = 16MHz, $f_{OFFSET}$ = 10MHz, 0dBFS | 4x interpolation | | -151 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, DATACLK output mode, dual-port mode, 50Ω double-terminated outputs, external reference at 1.25V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| In-Band SFDR (DC to $f_{DATA}/2$) | SFDR | $f_{DATACLK}$ = 125MHz, interpolation off, 0dBFS | $f_{OUT}$ = 10MHz | | 91 | | dBc |
| | | | $f_{OUT}$ = 30MHz | | 85 | | |
| | | | $f_{OUT}$ = 50MHz | | 73 | | |
| | | $f_{DATACLK}$ = 125MHz, 2x interpolation, 0dBFS | $f_{OUT}$ = 10MHz | 77 | 89 | | |
| | | | $f_{OUT}$ = 30MHz | | 86 | | |
| | | | $f_{OUT}$ = 50MHz | | 85 | | |
| | | $f_{DATACLK}$ = 125MHz, 4x interpolation, 0dBFS | $f_{OUT}$ = 10MHz | | 91 | | |
| | | | $f_{OUT}$ = 30MHz | | 86 | | |
| | | | $f_{OUT}$ = 50MHz | | 88 | | |
| Two-Tone IMD | TTIMD | $f_{DATACLK}$ = 125MHz, $f_{OUT1}$ = 9MHz, $f_{OUT2}$ = 10MHz, -6.1dBFS | No interpolation | | -102 | | dBc |
| | | | 2x interpolation | | -102 | | |
| | | | 4x interpolation | | -102 | | |
| | | $f_{DATA}$ = 125MHz, $f_{OUT1}$ = 79MHz, $f_{OUT2}$ = 80MHz, -6.1dBFS | 2x interpolation, $f_{IM}/4$ complex modulation | | -73 | | |
| | | | 4x interpolation, $f_{IM}/4$ complex modulation | | -75 | | |
| | | $f_{DATACLK}$ = 62.5MHz, $f_{OUT1}$ = 9MHz, $f_{OUT2}$ = 10MHz, -6.1dBFS | 8x interpolation | | -99 | | |
| | | $f_{DATACLK}$ = 62.5MHz, $f_{OUT1}$ = 69MHz, $f_{OUT2}$ = 70MHz, -6.1dBFS | 8x interpolation, $f_{IM}/4$ complex modulation | | -70 | | |
| | | $f_{DATACLK}$ = 62.5MHz, $f_{OUT1}$ = 179MHz, $f_{OUT2}$ = 180MHz, -6.1dBFS | 8x, highpass interpolation, $f_{IM}/4$ complex modulation | | -63 | | |
| Four-Tone IMD | FTIMD | $f_{DATACLK}$ = 125MHz, $f_{OUT}$ spaced 1MHz apart from 32MHz, -12dBFS, 2x interpolation | | | -95 | | dBc |
| ACLR for WCDMA (Note 3) | ACLR | $f_{DATACLK}$ = 61.44MHz, $f_{OUT}$ = baseband | 4x interpolation | | 78 | | dB |
| | | | 8x interpolation | | 78 | | |
| | | $f_{DATACLK}$ = 122.88MHz, $f_{OUT}$ = 61.44MHz | 2x interpolation, $f_{IM}/4$ complex modulation | | 74 | | |
| | | $f_{DATACLK}$ = 122.88MHz, $f_{OUT}$ = 122.88MHz | 4x interpolation, $f_{IM}/4$ complex modulation | | 69 | | |

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

## ELECTRICAL CHARACTERISTICS (continued)

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, DATACLK output mode, dual-port mode, 50Ω double-terminated outputs, external reference at 1.25V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Propagation Delay | $t_{PD}$ | 1x interpolation (Note 4) | | 2.9 | | ns |
| Output Rise Time | $t_{RISE}$ | 10% to 90% (Note 5) | | 0.75 | | ns |
| Output Fall Time | $t_{FALL}$ | 10% to 90% (Note 5) | | 1 | | ns |
| Output Settling Time | | To 0.5% (Note 5) | | 11 | | ns |
| Output Bandwidth | | -1dB bandwidth (Note 6) | | 240 | | MHz |
| Passband Width | | Ripple < -0.01dB | | 0.4 x $f_{DATA}$ | | |
| Stopband Rejection | | 0.604 x $f_{DATA}$, 2x interpolation | | 100 | | dB |
| | | 0.604 x $f_{DATA}$, 4x interpolation | | 100 | | |
| | | 0.604 x $f_{DATA}$, 8x interpolation | | 100 | | |
| Data Latency | | 1x interpolation | | 22 | | Clock Cycles |
| | | 2x interpolation | | 70 | | |
| | | 4x interpolation | | 146 | | |
| | | 8x interpolation | | 311 | | |
| **DAC INTERCHANNEL MATCHING** | | | | | | |
| Gain Match | ΔGain | $f_{OUT}$ = DC - 80MHz, $I_{OUTFS}$ = 20mA | | ±0.1 | | dB |
| Gain-Match Tempco | ΔGain/°C | $I_{OUTFS}$ = 20mA | | ±0.02 | | ppm/°C |
| Phase Match | ΔPhase | $f_{OUT}$ = 60MHz, $I_{OUTFS}$ = 20mA | | ±0.13 | | Deg |
| Phase-Match Tempco | ΔPhase/°C | $f_{OUT}$ = 60MHz, $I_{OUTFS}$ = 20mA | | ±0.006 | | Deg/°C |
| DC Gain Match | | $I_{OUTFS}$ = 20mA | -0.25 | 0.04 | +0.25 | dB |
| Channel-to-Channel Crosstalk | | $f_{OUT}$ = 50MHz, $f_{DAC}$ = 250MHz, 0dBFS | | -90 | | dB |
| **REFERENCE** | | | | | | |
| Reference Input Range | | | 0.125 | | 1.250 | V |
| Reference Output Voltage | $V_{REFIO}$ | Internal reference | 1.14 | 1.20 | 1.27 | V |
| Reference Input Resistance | $R_{REFIO}$ | | | 10 | | kΩ |
| Reference Voltage Drift | | | | ±50 | | ppm/°C |
| **CMOS LOGIC INPUT/OUTPUT (A13–A0, SELIQ/B13, DATACLK/B12, B11–B0, DATACLK)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.7 x $DV_{DD1.8}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.3 x $DV_{DD1.8}$ | V |
| Input Current | $I_{IN}$ | | -20 | ±1 | +20 | µA |
| Input Capacitance | $C_{IN}$ | | | 3 | | pF |

## ELECTRICAL CHARACTERISTICS (continued)

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, DATACLK output mode, dual-port mode, 50Ω double-terminated outputs, external reference at 1.25V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | 200µA load | 0.8 x $DV_{DD3.3}$ | | | V |
| Output Low Voltage | $V_{OL}$ | 200µA load | | | 0.2 x $DV_{DD3.3}$ | V |
| Output Leakage Current | | Three-state | | 1 | | µA |
| Rise/Fall Time | | $C_{LOAD}$ = 10pF, 20% to 80% | | 1.6 | | ns |
| **CLOCK INPUT (CLKP, CLKN)** | | | | | | |
| Differential Input Voltage Swing | $V_{DIFF}$ | Sine-wave input | | > 1.5 | | $V_{P-P}$ |
| | | Square-wave input | | > 0.5 | | |
| Differential Input Slew Rate | | | | > 100 | | V/µs |
| Common-Mode Voltage | $V_{COM}$ | AC-coupled | | $AV_{CLK}$/2 | | V |
| Input Resistance | $R_{CLK}$ | | | 5 | | kΩ |
| Input Capacitance | $C_{CLK}$ | | | 3 | | pF |
| Minimum Clock Duty Cycle | | | | 45 | | % |
| Maximum Clock Duty Cycle | | | | 55 | | % |
| **CLKP/CLKN, DATACLK TIMING (Figure 4) (Notes 7, 8)** | | | | | | |
| CLK to DATACLK Delay | $t_D$ | DATACLK output mode, $C_{LOAD}$ = 10pF | | 6.2 | | ns |
| Data Hold Time, DATACLK Input/Output (Pin 14) | $t_{DH}$ | Capturing rising edge | 1.0 | | | ns |
| | | Capturing falling edge | 2.1 | | | |
| Data Setup Time, DATACLK Input/Output (Pin 14) | $t_{DS}$ | Capturing rising edge | 0.4 | | | ns |
| | | Capturing falling edge | -0.7 | | | |
| Data Hold Time, DATACLK/B10 Input/Output (Pin 27) | $t_{DH}$ | Capturing rising edge | 1.0 | | | ns |
| | | Capturing falling edge | 2.3 | | | |
| Data Setup Time, DATACLK/B10 Input/Output (Pin 27) | $t_{DS}$ | Capturing rising edge | 0.2 | | | ns |
| | | Capturing falling edge | -0.4 | | | |
| **SERIAL-PORT INTERFACE TIMING (Figure 3) (Note 7)** | | | | | | |
| SCLK Frequency | $f_{SCLK}$ | | | | 10 | MHz |
| $\overline{CS}$ Setup Time | $t_{SS}$ | | 2.5 | | | ns |
| Input Hold Time | $t_{SDH}$ | | 0 | | | ns |
| Input Setup Time | $t_{SDS}$ | | 4.5 | | | ns |
| Data Valid Duration | $t_{SDV}$ | | 6.5 | | 16.5 | ns |

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## ELECTRICAL CHARACTERISTICS (continued)

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, DATACLK output mode, dual-port mode, 50Ω double-terminated outputs, external reference at 1.25V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 2)

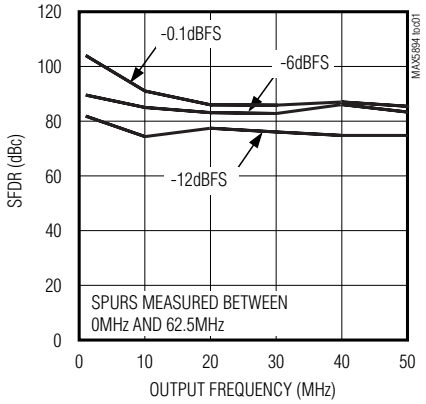
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | | |
| Digital Supply Voltage | $DV_{DD1.8}$ | | | 1.71 | 1.8 | 1.89 | V |
| Digital I/O Supply Voltage | $DV_{DD3.3}$ | | | 3.0 | 3.3 | 3.6 | V |
| Clock Supply Voltage | $AV_{CLK}$ | | | 3.135 | 3.3 | 3.465 | V |
| Analog Supply Voltage | $AV_{DD3.3}$ | | | 3.135 | 3.3 | 3.465 | V |
| | $AV_{DD1.8}$ | | | 1.71 | 1.8 | 1.89 | |
| Analog Supply Current | $I_{AVDD3.3}$ | $f_{CLK}$ = 250MHz, 2x interpolation, 0dBFS, $f_{OUT}$ = 10MHz | | | 110 | 130 | mA |
| | $I_{AVDD1.8}$ | $f_{CLK}$ = 250MHz, 2x interpolation, 0dBFS, $f_{OUT}$ = 10MHz | | | 27 | 32 | |
| Digital Supply Current | $I_{DVDD1.8}$ | $f_{CLK}$ = 250MHz, 2x interpolation, 0dBFS, $f_{OUT}$ = 10MHz | | | 225 | 250 | mA |
| Digital I/O Supply Current | $I_{DVDD3.3}$ | $f_{CLK}$ = 250MHz, 2x interpolation, 0dBFS, $f_{OUT}$ = 10MHz | | | 21 | 32 | mA |
| Clock Supply Current | $I_{AVCLK}$ | $f_{CLK}$ = 250MHz, 2x interpolation, 0dBFS, $f_{OUT}$ = 10MHz | | | 3 | 5 | mA |
| Total Power Dissipation | $P_{TOTAL}$ | $f_{CLK}$ = 250MHz, 2x interpolation, 0dBFS, $f_{OUT}$ = 10MHz | | | 886 | | mW |
| Power-Down Current | | All I/O are static high or low, bit 2 to bit 4 of address 00h are set high | $AV_{DD3.3}$ | | 450 | | µA |
| | | | $AV_{DD1.8}$ | | 1 | | |
| | | | $DV_{DD1.8}$ | | 10 | | |
| | | | $DV_{DD3.3}$ | | 100 | | |
| | | | $AV_{CLK}$ | | 1 | | |
| $AV_{DD3.3}$ Power-Supply Rejection Ratio | $PSRR_A$ | (Note 9) | | | 0.05 | | %FS/V |

**Note 2:** All limit specifications are 100% tested at $T_A \geq +25°C$. Specifications at $T_A < +25°C$ are guaranteed by design and characterization.
**Note 3:** 3.84MHz bandwidth, single carrier.
**Note 4:** Excludes data latency.
**Note 5:** Measured single-ended into a 50Ω load.
**Note 6:** Excludes sin(x)/x rolloff.
**Note 7:** Guaranteed by design and characterization.
**Note 8:** Setup and hold time specifications characterized with 3.3V CMOS logic levels.
**Note 9:** Parameter defined as the change in midscale output caused by a ±5% variation in the nominal supply voltage.

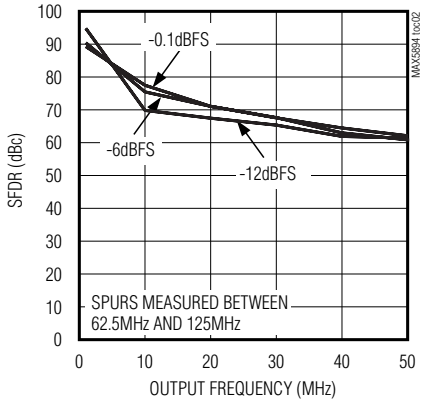
## Typical Operating Characteristics

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, output is transformer-coupled to 50Ω load, $T_A$ = +25°C, unless otherwise noted.)

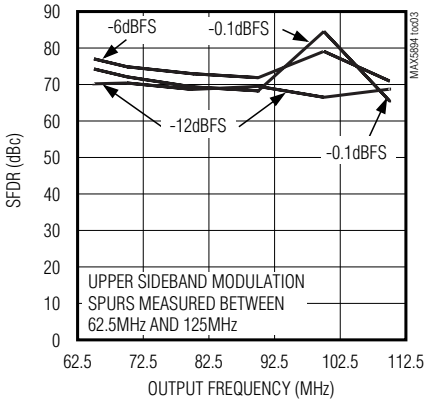
**IN-BAND SFDR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 2x INTERPOLATION**



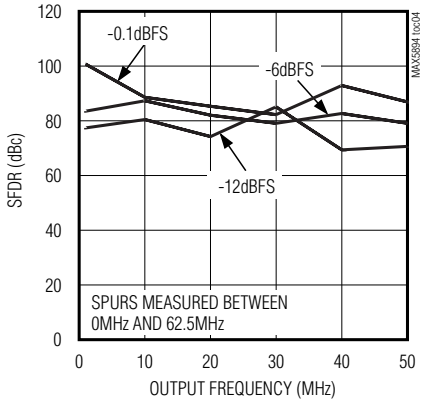

**OUT-OF-BAND SFDR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 2x INTERPOLATION**



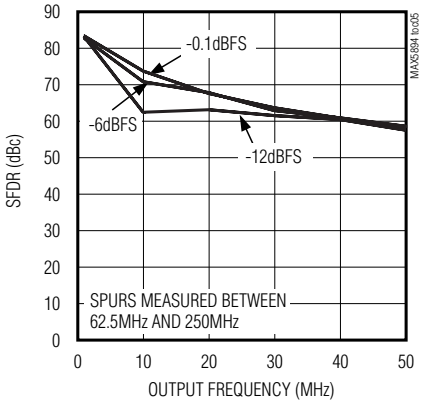

**IN-BAND SFDR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 2x INTERPOLATION**



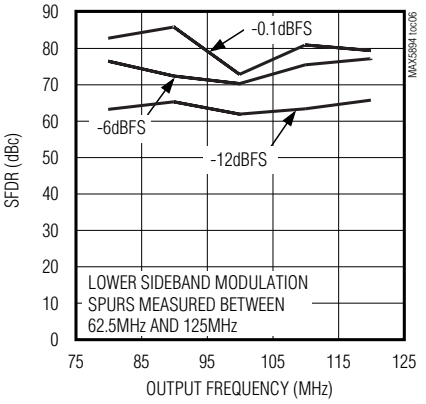

**IN-BAND SFDR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 4x INTERPOLATION**



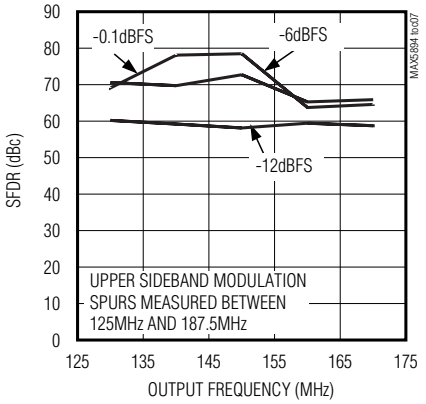

**OUT-OF-BAND SFDR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 4x INTERPOLATION**



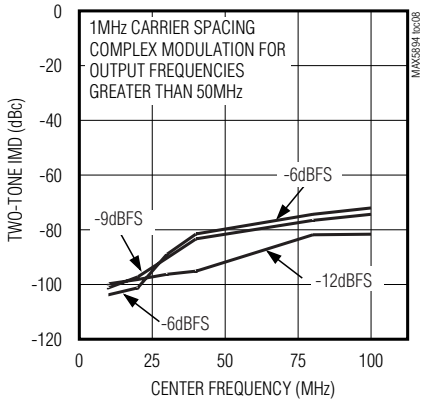

**IN-BAND SFDR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 4x INTERPOLATION**



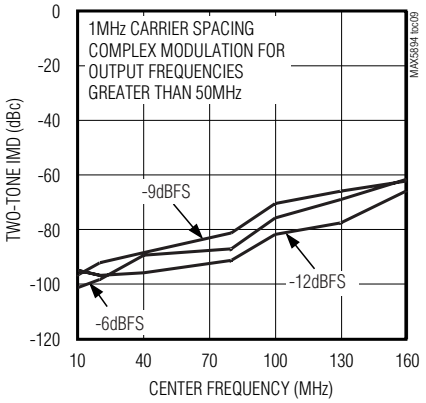

**IN-BAND SFDR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 4x INTERPOLATION**




**TWO-TONE IMD vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 2x INTERPOLATION**




**TWO-TONE IMD vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 125Mwps, 4x INTERPOLATION**

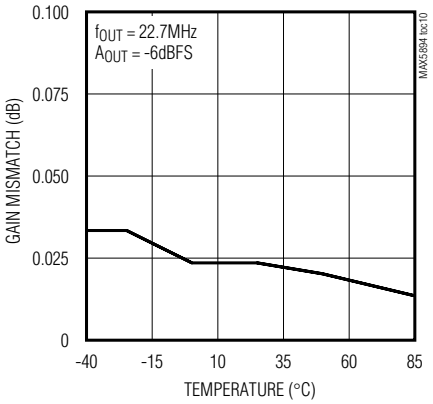


# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

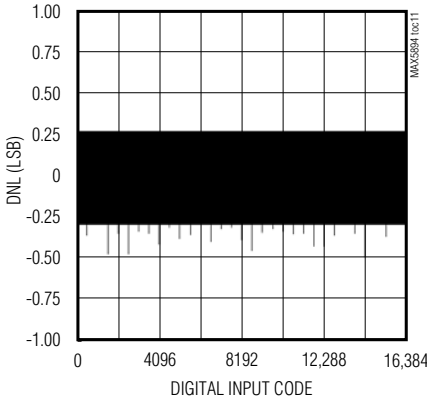
## Typical Operating Characteristics (continued)

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, output is transformer-coupled to 50Ω load, $T_A$ = +25°C, unless otherwise noted.)

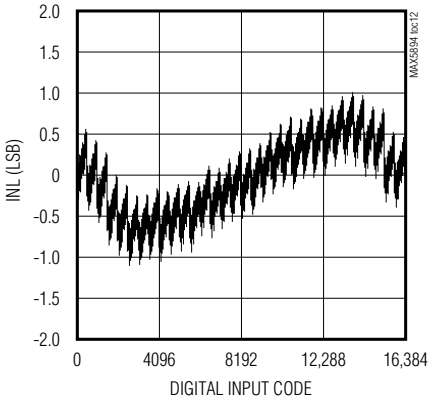
**GAIN MISMATCH vs. TEMPERATURE**
**$f_{DATA}$ = 125Mwps, 2x INTERPOLATION**



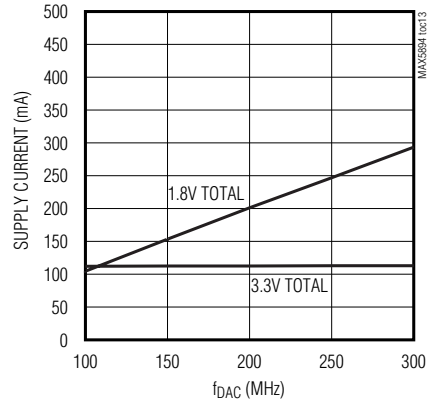

**DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE**



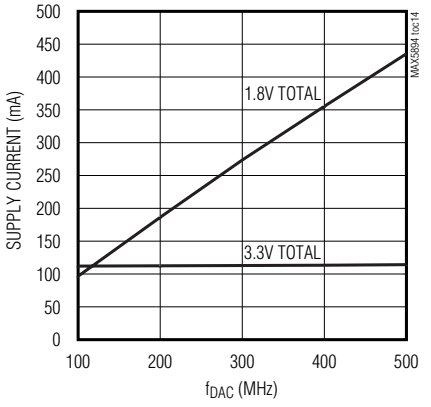

**INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE**



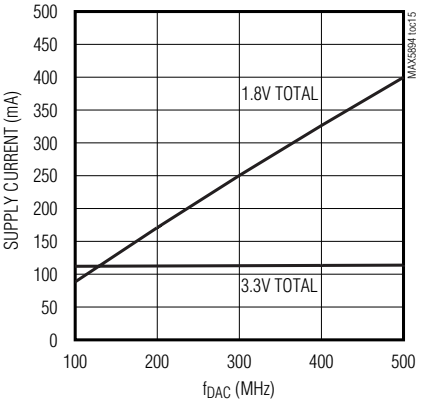

**SUPPLY CURRENT vs. DAC UPDATE RATE**
**2x INTERPOLATION, $f_{OUT}$ = 5MHz**




**SUPPLY CURRENT vs. DAC UPDATE RATE**
**4x INTERPOLATION, $f_{OUT}$ = 5MHz**




**SUPPLY CURRENT vs. DAC UPDATE RATE**
**8x INTERPOLATION, $f_{OUT}$ = 5MHz**

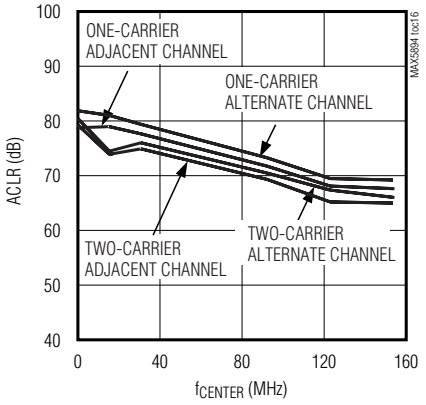


# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

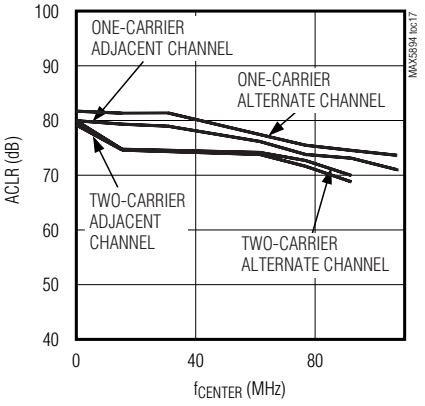
## Typical Operating Characteristics (continued)

($DV_{DD1.8}$ = $AV_{DD1.8}$ = 1.8V, $AV_{CLK}$ = $AV_{DD3.3}$ = $DV_{DD3.3}$ = 3.3V, modulator off, 2x interpolation, output is transformer-coupled to 50Ω load, $T_A$ = +25°C, unless otherwise noted.)

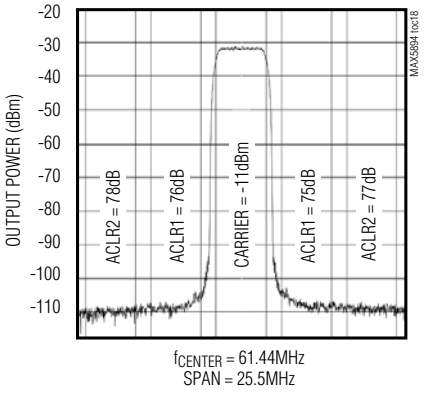
**WCDMA ACLR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 122.88Mwps, 4x INTERPOLATION**



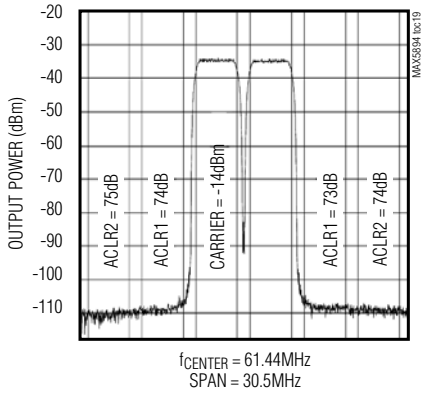

**WCDMA ACLR vs. OUTPUT FREQUENCY**
**$f_{DATA}$ = 76.8Mwps, 4x INTERPOLATION**



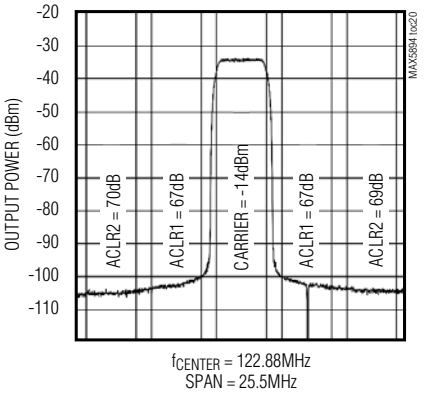

**WCDMA ACLR SPECTRAL PLOT**
**$f_{DATA}$ = 61.44Mwps, 8x INTERPOLATION**



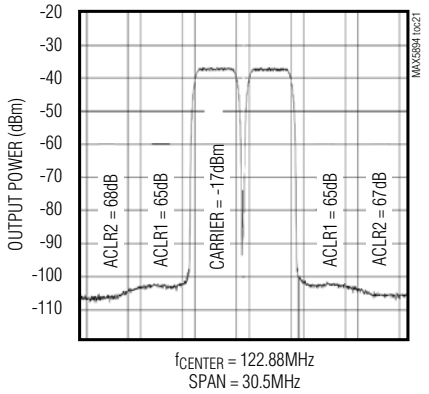

**TWO-CARRIER WCDMA ACLR SPECTRAL PLOT**
**$f_{DATA}$ = 61.44Mwps, 8x INTERPOLATION**




**WCDMA ACLR SPECTRAL PLOT**
**$f_{DATA}$ = 122.88Mwps, 4x INTERPOLATION**




**TWO-CARRIER WCDMA ACLR SPECTRAL PLOT**
**$f_{DATA}$ = 122.88Mwps, 4x INTERPOLATION**



# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

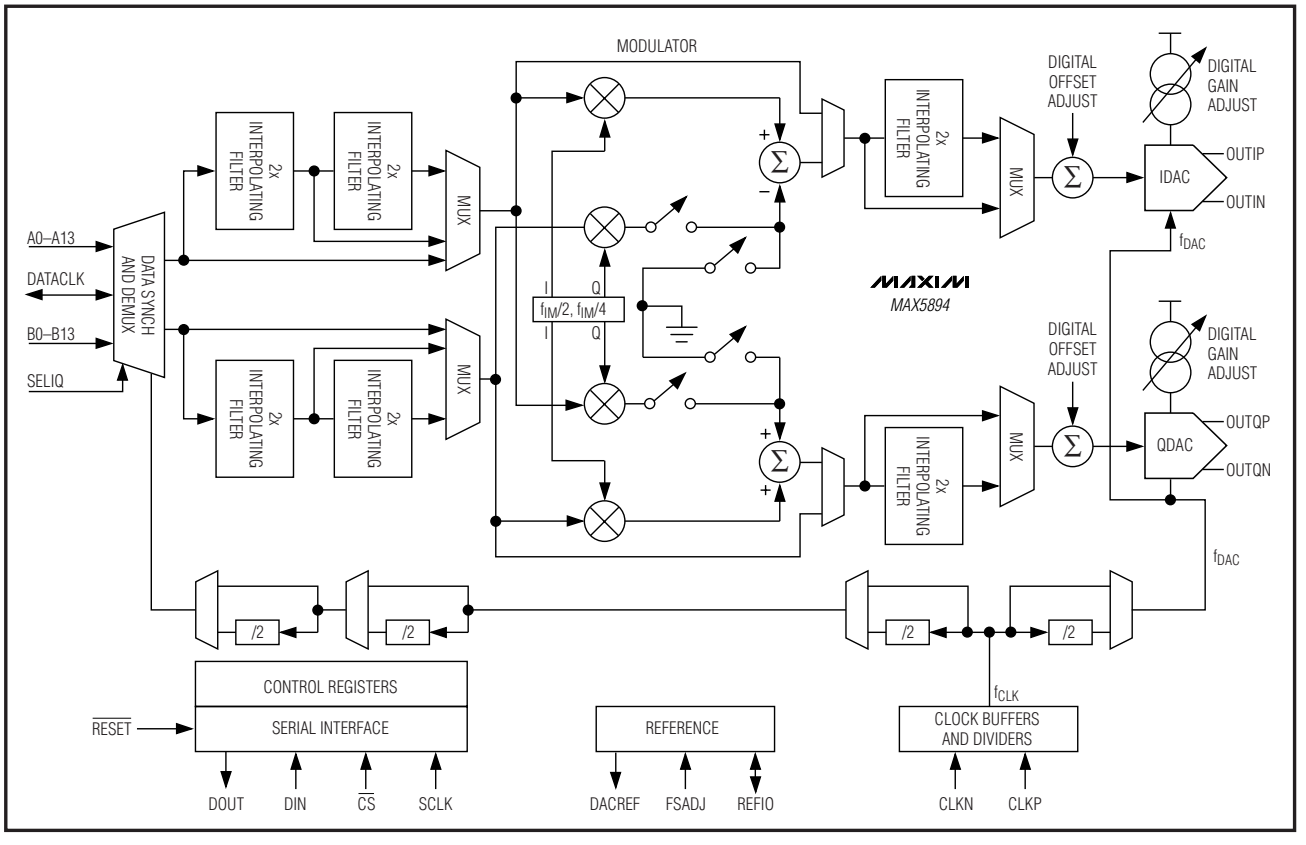
## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | CLKP | Noninverting Differential Clock Input. Internally biased to $AV_{CLK}/2$. |
| 2 | CLKN | Inverting Differential Clock Input. Internally biased to $AV_{CLK}/2$. |
| 3, 4, 5, 24, 25, 42, 43 | N.C. | Internally Connected. Do not connect. |
| 6, 21, 30, 37 | $DV_{DD1.8}$ | Digital Power Supply. Accepts a 1.71V to 1.89V supply range. Bypass each pin to ground with a 0.1µF capacitor as close to the pin as possible. |
| 7–12, 15–20, 22, 23 | A13–A0 | A-Port Data Inputs.<br>Dual-port mode:<br>I-channel data input. Data is latched on the rising/falling edge (programmable) of the DATACLK.<br>Single-port mode:<br>I-channel and Q-channel data input, with SELIQ. |
| 13, 44 | $DV_{DD3.3}$ | CMOS I/O Power Supply. Accepts a 3.0V to 3.6V supply range. Bypass each pin to ground with a 0.1µF capacitor as close to the pin as possible. |
| 14 | DATACLK | Programmable Data Clock Input/Output. See the *DATACLK Modes* section for details. |
| 26 | SELIQ/B13 | Select I-/Q-Channel Input or B-Port MSB Input.<br>Single-port mode:<br>If SELIQ = LOW, data is latched into Q-channel on the rising/falling edge (programmable) of the DATACLK.<br>If SELIQ = HIGH, data is latched into I-channel on the rising/falling edge (programmable) of the DATACLK.<br>Dual-port mode:<br>Q-channel MSB input. |
| 27 | DATACLK/B12 | Alternate DATACLK Input/Output or B-Port Bit 12 Input.<br>Single-port mode:<br>See the *DATACLK Modes* section for details.<br>Dual-port mode:<br>Q-channel bit 12 input.<br>If unused connect to GND. |
| 28, 29, 31–36, 38–41 | B11–B0 | B-Port Data Bits 11–0.<br>Dual-port mode:<br>Q-channel inputs. Data is latched on the rising/falling (programmable) edge of the DATACLK.<br>Single-port mode:<br>Connect to GND. |
| 45 | DOUT | Serial-Port Data Output |
| 46 | DIN | Serial-Port Data Input |
| 47 | SCLK | Serial-Port Clock Input. Data on DIN is latched on the rising edge of SCLK. |
| 48 | $\overline{CS}$ | Serial-Port Interface Select. Drive $\overline{CS}$ low to enable serial-port interface. |
| 49 | $\overline{RESET}$ | Reset Input. Set $\overline{RESET}$ low during power-up. |
| 50 | REFIO | Reference Input/Output. Bypass to ground with a 1µF capacitor as close to the pin as possible. |
| 51 | DACREF | Current-Set Resistor Return Path. For a 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. Internally connected to GND. **DO NOT USE AS AN EXTERNAL GROUND CONNECTION.** |
| 52 | FSADJ | Full-Scale Adjust Input. This input sets the full-scale output current of the DAC. For a 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 53, 67 | $AV_{DD1.8}$ | Low Analog Power Supply. Accepts a 1.71V to 1.89V supply range. Bypass each pin to GND with a 0.1µF capacitor as close to the pin as possible. |
| 54, 56, 59, 61, 64, 66 | GND | Ground |
| 55, 60, 65 | $AV_{DD3.3}$ | Analog Power Supply. Accepts a 3.135V to 3.465V supply range. Bypass each pin to GND with a 0.1µF capacitor as close to the pin as possible. |
| 57 | OUTQN | Inverting Differential DAC Current Output for Q-Channel |
| 58 | OUTQP | Noninverting Differential DAC Current Output for Q-Channel |
| 62 | OUTIN | Inverting Differential DAC Current Output for I-Channel |
| 63 | OUTIP | Noninverting Differential DAC Current Output for I-Channel |
| 68 | $AV_{CLK}$ | Clock Power Supply. Accepts a 3.135V to 3.465V supply range. Bypass to ground with a 0.1µF capacitor as close to the pin as possible. |
| — | EP | Exposed Pad. Must be connected to GND through a low-impedance path. |

## Functional Diagram



# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

## Detailed Description

The MAX5894 dual, 500Msps, high-speed, 14-bit, current-output DAC provides superior performance in communication systems requiring low-distortion analog-signal reconstruction. The MAX5894 combines two DAC cores with 8x/4x/2x/1x programmable digital interpolation filters, a digital quadrature modulator, an SPI-compatible serial interface for programming the device, and an on-chip 1.20V reference. The full-scale output current range is programmable from 2mA to 20mA to optimize power dissipation and gain control.

Each channel contains three selectable interpolating filters making the MAX5894 capable of 1x, 2x, 4x, or 8x interpolation, which allows for low input data rates and high DAC update rates. When operating in 8x interpolation mode, the interpolator increases the DAC conversion rate by a factor of eight, providing an eight-fold increase in separation between the reconstructed waveform spectrum and its first image. The MAX5894 accepts either two's complement or offset binary input data format and can operate from either a single- or dual-port input bus.

The MAX5894 includes modulation modes at $f_{IM}/2$ and $f_{IM}/4$, where $f_{IM}$ is the data rate at the input of the modulator. If 2x interpolation is used, this data rate is 2x the input data rate. If 4x or 8x interpolation is used, this data rate is 4x the input data rate. Table 1 summarizes the modulator operating data rates for dual-port mode.

The power-down modes can be used to turn off each DAC's output current or the entire digital section. Programming both DACs into power-down simultaneously automatically powers down the digital interpolator filters. Note the SPI section is always active.

The analog and digital sections of the MAX5894 have separate power-supply inputs ($AV_{DD3.3}$, $AV_{DD1.8}$, $AV_{CLK}$, $DV_{DD3.3}$, and $DV_{DD1.8}$), which minimize noise coupling from one supply to the other. $AV_{DD1.8}$ and $DV_{DD1.8}$ operate from a typical 1.8V supply, and all other supply inputs operate from a typical 3.3V supply.

### Serial Interface

The SPI-compatible serial interface programs the MAX5894 registers. The serial interface consists of the $\overline{CS}$, DIN, SCLK, and DOUT. Data is shifted into DIN on the rising edge of the SCLK when $\overline{CS}$ is low. When $\overline{CS}$ is high, data presented at DIN is ignored and DOUT is in high-impedance mode. **Note: $\overline{CS}$ must transition high after each read/write operation.** DOUT is the serial data output for reading registers to facilitate easy debugging during development. DIN and DOUT can be connected together to form a 3-wire serial interface bus or remain separate and form a 4-wire SPI bus.

The serial interface supports two-byte transfer in a communication cycle. The first byte is a control byte written to the MAX5894 only. The second byte is a data byte and can be written to or read from the MAX5894.

**Table 1. Quadrature Modulator Operating Data Rates ($f_{IM}$ is the Data Rate at the Input of the Modulator) for Dual-Port Mode**

| INTERPOLATION RATE | MODULATION MODE ($f_{LO}$) | MODULATION FREQUENCY RELATIVE TO $f_{DAC}$ | MODULATION FREQUENCY RELATIVE TO $f_{DATA}$ |
|---|---|---|---|
| 1x | $f_{IM}/2$ | $f_{DAC}/2$ | $f_{DATA}/2$ |
| | $f_{IM}/4$ | $f_{DAC}/4$ | $f_{DATA}/4$ |
| 2x | $f_{IM}/2$ | $f_{DAC}/2$ | $f_{DATA}$ |
| | $f_{IM}/4$ | $f_{DAC}/4$ | $f_{DATA}/2$ |
| 4x | $f_{IM}/2$ | $f_{DAC}/2$ | $2 \times f_{DATA}$ |
| | $f_{IM}/4$ | $f_{DAC}/4$ | $f_{DATA}$ |
| 8x | $f_{IM}/2$ | $f_{DAC}/4$ | $2 \times f_{DATA}$ |
| | $f_{IM}/4$ | $f_{DAC}/8$ | $f_{DATA}$ |

When writing to the MAX5894, data is shifted into DIN; data is shifted out of DOUT in a read operation. Bits 0 to 3 of the control byte are the address bits. These bits set the address of the register to be written to or read from. Bits 4 to 6 of the control byte must always be set to 0. Bit 7 is a read/write bit: 0 for write operation and 1 for read operation. The most significant bit (MSB) is shifted in first in default mode. If the serial port is set to LSB-first mode, both the control byte and data byte are shifted LSB in first. Figures 1 and 2 show the SPI serial-interface operation in the default write and read mode, respectively. Figure 3 is a timing diagram for the SPI serial interface.

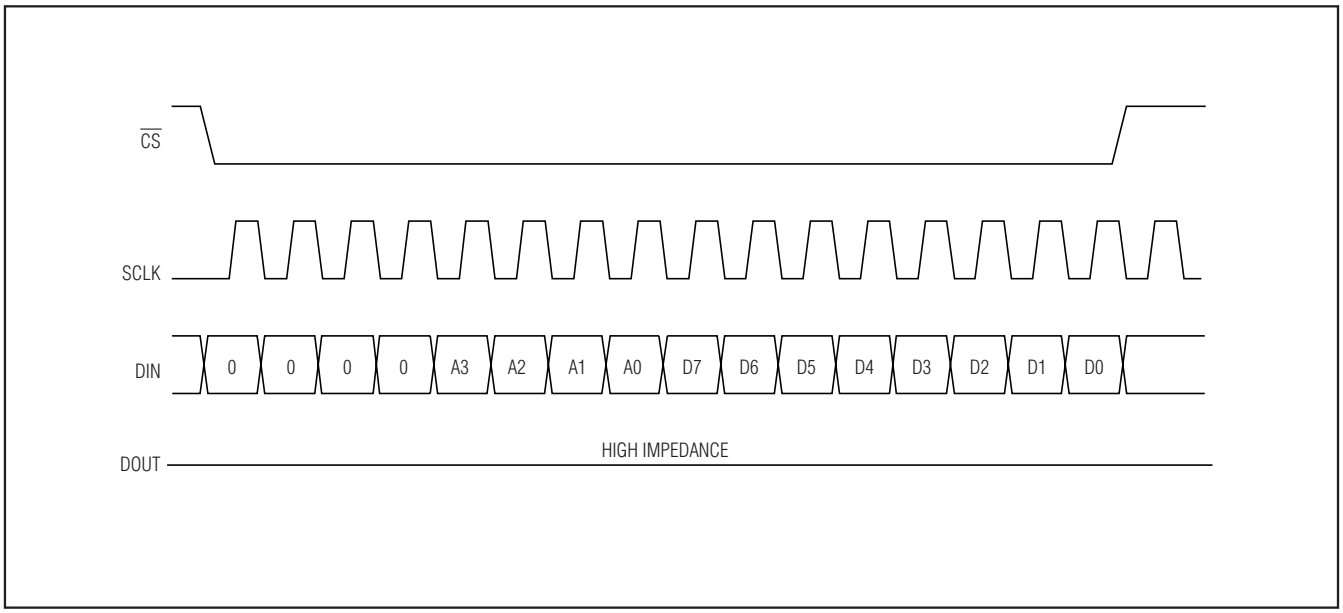



*Figure 1. SPI Serial-Interface Write Cycle, MSB-First Mode*

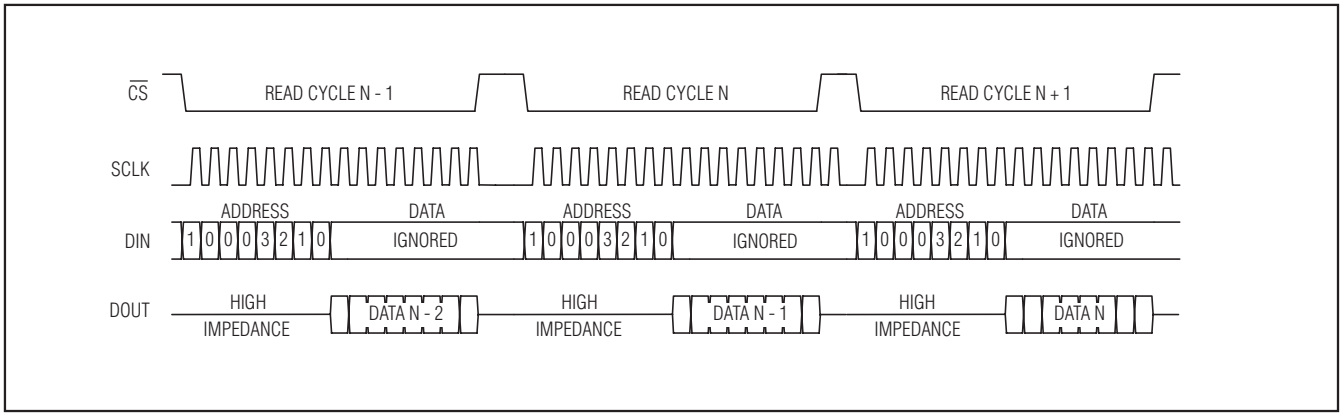



*Figure 2. SPI Serial-Interface Read Cycle, MSB-First Mode*

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

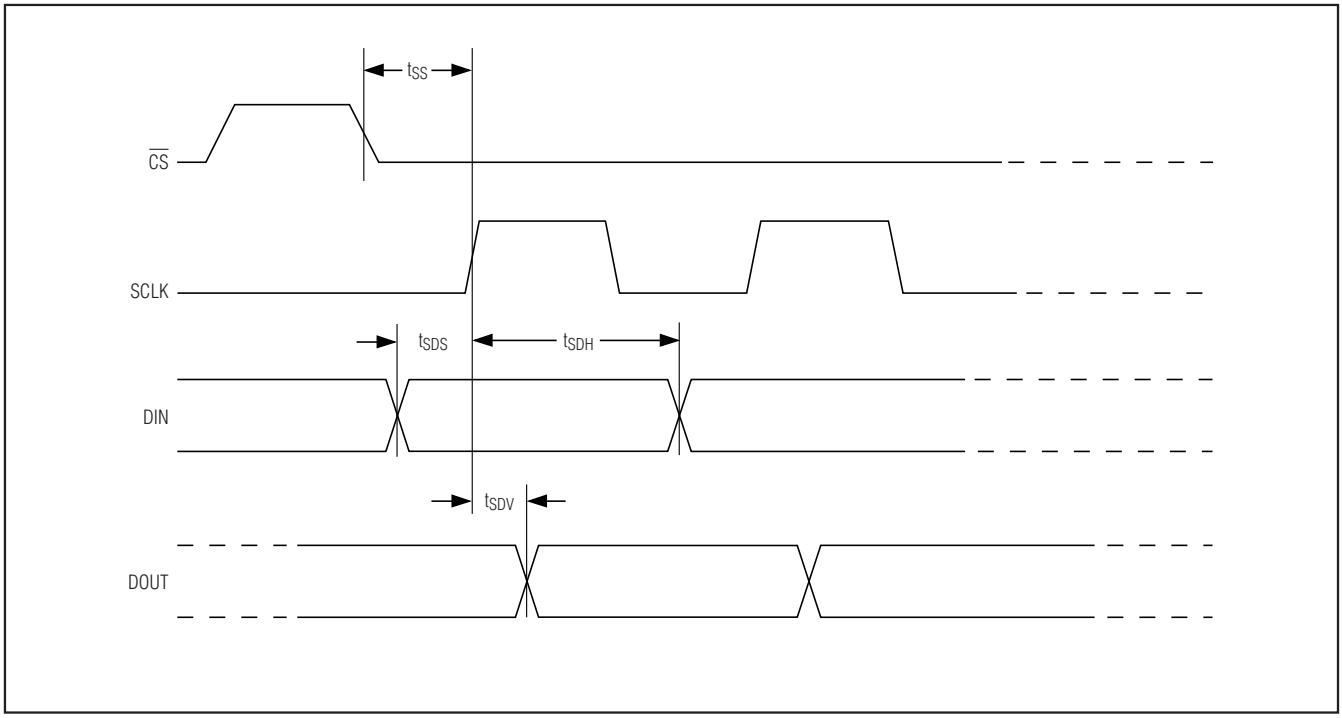



*Figure 3. SPI Serial-Interface Timing Diagram*

### Programming Registers

Programming its registers with the SPI serial interface sets the MAX5894 operation modes. Table 2 shows all of the registers. The following are descriptions of each register.

## Table 2. MAX5894 Programmable Registers

| ADD | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 00h | Unused | **0 = MSB first**<br>1 = LSB first | Software Reset<br>**0 = Normal**<br>1 = Reset all registers | Interpolator Power-Down<br>**0 = Normal**<br>1 = Power-down | IDAC Power-Down<br>**0 = Normal**<br>1 = Power-down | QDAC Power-Down<br>**0 = Normal**<br>1 = Power-down | Unused | |
| 01h | Interpolation Rate (Bit 7, Bit 6)<br>00 = No interpolation<br>01 = 2x interpolation<br>10 = 4x interpolation<br>**11 = 8x interpolation** | | Third Interpolation Filter Configuration<br>**0 = Lowpass**<br>1 = Highpass | Modulation Mode (Bit 4, Bit 3)<br>00 = Modulation off<br>01 = $f_{IM}/2$<br>**10 = $f_{IM}/4$**<br>11 = $f_{IM}/4$ | | Mixer Modulation Mode<br>0 = Complex<br>**1 = Real** | Modulation Sign<br>**0 = $e^{-j\omega}$**<br>1 = $e^{-j\omega}$ | Unused |
| 02h | **0 = Two's complement input data**<br>1 = Offset binary input data | **0 = Single port (A), interleaved I/Q**<br>1 = Dual port I/Q input | **0 = Clock output on DATACLK**<br>1 = Clock output on DATACLK/B12 | **0 = Input data latched on rising clock edge**<br>1 = Input data latched on falling clock edge | **0 = Data clock input enabled**<br>1 = Data clock output enabled | Data Synchronizer<br>**0 = Enabled**<br>1 = Disabled | Unused | |
| 03h | Unused | | | | | | | |
| 04h | 8-Bit IDAC Fine-Gain Adjustment (see the *Gain Adjustment* section). Bit 7 is MSB and bit 0 is LSB. **Default: 00h** | | | | | | | |
| 05h | Unused | | | | 4-Bit IDAC Coarse-Gain Adjustment (see the *Gain Adjustment* section). Bit 3 is MSB and bit 0 is LSB. **Default: Fh** | | | |
| 06h | 10-Bit IDAC Offset Adjustment (see the *Offset Adjustment* section). Bits 7 to 0 of the 06h register are the MSB bits. Bit 1 and bit 0 are the LSB bits in 07h register. **Default: 000h** | | | | | | | |
| 07h | IDAC IOFFSET Direction<br>**0 = Current on OUTIN**<br>1 = Current on OUTIP | Unused | | | | | IDAC Offset Adjustment Bit 1 (see 06h register) | IDAC Offset Adjustment Bit 0 (see 06h register) |
| 08h | 8-Bit QDAC Fine-Gain Adjustment (see the *Gain Adjustment* section). Bit 7 is MSB and bit 0 is LSB. **Default: 00h** | | | | | | | |
| 09h | Unused | | | | 4-Bit QDAC Coarse-Gain Adjustment (see the *Gain Adjustment* section). Bit 3 is MSB and bit 0 is LSB. **Default: Fh** | | | |
| 0Ah | 10-Bit QDAC Offset Adjustment (see the *Offset Adjustment* section). Bits 7 to 0 of the 0Ah register are the MSB bits. Bit 1 and bit 0 are the LSB bits in 0Bh register. **Default: 000h** | | | | | | | |
| 0Bh | QDAC IOFFSET Direction<br>**0 = Current on OUTQN**<br>1 = Current on OUTQP | Unused | | | | | QDAC Offset Adjustment Bit 1 (see 0Ah register) | QDAC Offset Adjustment Bit 0 (see 0Ah register) |
| 0Ch | Reserved, do not write to these bits. | | | | | | | |
| 0Dh | Reserved, do not write to these bits. | | | | | | | |
| 0Eh | Reserved, do not write to these bits. | | | | | | | |

*Conditions in **bold** are default states after reset.*

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

**Address 00h**

Bit 6 Logic 0 (default) causes the serial port to use MSB first address/data format. When set to a logic 1, the serial port uses LSB first address/data format.

Bit 5 When set to a logic 1, all registers reset to their default state (this bit included).

Bit 4 Logic 1 stops the clock to the digital interpolators. DAC outputs hold last value prior to interpolator power-down.

Bit 3 IDAC power-down mode. A logic 1 to this bit powers down the IDAC.

Bit 2 QDAC power-down mode. A logic 1 to this bit powers down the QDAC.

**Note:** If both bit 2 and bit 3 are 1, the MAX5894 is in full-power-down mode, leaving only the serial interface active.

**Address 01h**

Bits 7, 6 Configure the interpolation filters according to the following table:

| | |
|---|---|
| 00 | 1x (no interpolation) |
| 01 | 2x |
| 10 | 4x |
| 11 | 8x (default) |

Bit 5 Logic 0 configures FIR3 as a lowpass digital filter (default). A logic 1 configures FIR3 as a highpass digital filter.

Bits 4, 3 Configure the modulation frequency according to the following table:

| | |
|---|---|
| 00 | No modulation |
| 01 | $f_{IM}/2$ modulation |
| 10 | $f_{IM}/4$ modulation (default) |
| 11 | $f_{IM}/4$ modulation |

where $f_{IM}$ is the data rate at the input of the modulator.

Bit 2 Configures the modulation mode for either real or complex (image reject) modulation. Logic 1 sets the modulator to the real mode (default). Complex modulation is only available for $f_{IM}/4$ modulation.

Bit 1 Quadrature modulator sign inversion. With I-channel data leading Q-channel data by 90°, logic 0 sets the complex modulation to be $e^{-jw}$ (default), cancelling the upper image when used with an external quadrature modulator. A logic 1 sets the complex modulation to be $e^{+jw}$, cancelling the lower image when used with an external quadrature modulator.

**Address 02h**

Bit 7 Logic 0 (default) configures the data port for two's complement. A logic 1 configures the data ports for offset binary.

Bit 6 Logic 0 (default) configures the data bus for single-port, interleaved I/Q data. I and Q data enter through one 14-bit bus. Logic 1 configures the data bus for dual-port I/Q data. I and Q data enter on separate buses.

Bit 5 Logic 0 (default) configures the data clock for pin 14. A logic 1 configures the data clock for pin 27 (DATACLK/B12).

Bit 4 Logic 0 (default) sets the internal latches to latch the data on the rising edge of DATACLK. A logic 1 sets the internal latches to latch the data on the falling edge of DATACLK.

Bit 3 Logic 0 (default) configures the DATACLK pin (pin 14 or pin 27) to be an input. A logic 1 configures the DATACLK pin to be an output.

Bit 2 Logic 0 (default) enables the data synchronizer circuitry. A logic 1 disables the data synchronizer circuitry.

**Address 03h**

Bits 7–0 Unused.

**Address 04h**

Bits 7–0 These 8 bits define the binary number for fine-gain adjustment of the IDAC full-scale current (see the *Gain Adjustment* section). Bit 7 is the MSB. Default is all zeros.

**Address 05h**

Bits 3–0 These four bits define the binary number for the coarse-gain adjustment of the IDAC full-scale current (see the *Gain Adjustment* section). Bit 3 is the MSB. Default is all ones.

**Address 06h, Bits 7–0; Address 07h, Bit 1 and Bit 0**

These 10 bits represent a binary number that defines the magnitude of the offset added to the IDAC output (see the *Offset Adjustment* section). Default is all zeros.

**Address 07h**

Bit 7 Logic 0 (default) adds the 10 bits offset current to OUTIN. A logic 1 adds the 10 bits offset current to OUTIP.

**Address 08h**

Bits 7–0 These eight bits define the binary number for fine-gain adjustment of the QDAC full-scale current (see the *Gain Adjustment* section). Bit 7 is the MSB. Default is all zeros.

**Address 09h**

Bits 3–0 These four bits define the binary number for the coarse-gain adjustment of the QDAC full-scale current (see the *Gain Adjustment* section). Bit 3 is the MSB. Default is all ones.

**Address 0Ah, Bits 7–0; Address 0Bh, Bit 1 and Bit 0**

These 10 bits represent a binary number that defines the magnitude of the offset added to the QDAC output (see the *Offset Adjustment* section). Default is all zeros.

**Address 0Bh**

Bit 7 Logic 0 (default) adds the 10 bits offset to OUTQN. A logic 1 adds the 10 bits offset to OUTQP.

### *Offset Adjustment*

Offset adjustment is achieved by adding a digital code to the DAC inputs. The code OFFSET (see equation below), as stored in the relevant control registers, has a range from 0 to 1023 and a sign bit. The applied DAC offset is stored in the register, providing an offset adjustment range of ±1023 LSB codes. The resolution is 1 LSB.

$$I_{OFFSET} = \frac{OFFSET}{2^{14}} \times I_{OUTFS}$$

### *Gain Adjustment*

Gain adustment is peformed by varying the full-scale current according to the following formula:

$$I_{OUTFS} = \left[\left(\frac{3 \times I_{REF}}{4}\right)\left(\frac{COARSE\ +1}{16}\right) + \left(\frac{3 \times I_{REF}}{32}\right)\left(\frac{FINE}{256}\right)\right]\left(\frac{1024}{24}\right)$$

where $I_{REF}$ is the reference current (see the *Reference Input/Output* section). COARSE is the register content of registers 05h and 09h for the I- and Q-channel, respectively. FINE is the register content of register 04h and 08h for the I- and Q-channel, respectively. The range of coarse is from 0 to 15, with 15 being the default. The range for FINE is from 0 to 255 with 0 being the default. The gain can be adjusted in steps of approximately 0.01dB.

### *Single-Port/Dual-Port Data-Input Modes*

The MAX5894 is capable of capturing data in single-port and dual-port modes (selected through bit 6, address 02h). In single-port mode, the data for both DAC channels is latched on the A port (A13–A0). The channel for the input data is determined by the state of the SELIQ/B13 (pin 26) bit. When SELIQ is set to logic-high, the input data is presented to the I-channel, when set to logic-low, the input data is presented to the Q-channel. The unused B-port inputs (DATACLK/B12, B11–B0) should be grounded when running in single-port mode.

Dual-port mode, as the name implies, requires that each channel receives its data from a separate data bus. SELIQ/B13 and DATACLK/B12 revert to data bit inputs for the Q-channel in dual-port mode.

The MAX5894 control registers can be programmed to allow either signed or unsigned binary format (bit 7, address 02h) data in either single-port or dual-port mode. Table 3 shows the corresponding DAC output levels when using signed or unsigned data modes.

## Table 3. DAC Output Code Table

| DIGITAL INPUT CODE | | OUT_P | OUT_N |
|---|---|---|---|
| OFFSET BINARY (UNSIGNED) | TWO'S COMPLEMENT (SIGNED) | | |
| 00 0000 0000 0000 | 10 0000 0000 0000 | 0 | $I_{OUTFS}$ |
| 01 1111 1111 1111 | 00 0000 0000 0000 | $I_{OUTFS}/2$ | $I_{OUTFS}/2$ |
| 11 1111 1111 1111 | 01 1111 1111 1111 | $I_{OUTFS}$ | 0 |

### *Data Synchronization Modes*

Data synchronization circuitry is provided to allow operation with an input data clock. The data clock must be frequency locked to the DAC clock ($f_{DAC}$), but can have arbitrary phase with respect to the DAC clock. The synchronization circuitry allows for phase jitter on the input data clock of up to ±1 data clock cycles. Synchronization is initially established when the reset pin is asynchronously deasserted and the input data clock has been running for at least four clock cycles. Subsequently, the MAX5894 monitors the phase rela-

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tionship and detects if the phase drifts more than ±1 data clock cycle. If this occurs, the synchronizer automatically re-establishes synchronization. However, during the resynchronization phase, up to 8 data words may be lost or repeated.

Bit 2 of register 02h disables or enables (default) the automatic data clock phase detection. Disabling the data synchronization circuitry requires the data clock and the DAC clock phase to be locked.

### DATACLK Modes

The MAX5894 has a main DATACLK available at pin 14. An alternate DATACLK is available at pin 27 (DATACLK/B12) when configured in single-port data input mode (bit 5, address 02h). The DATACLK can be configured to accept an input clock signal for latching the input data, or to source a clock signal that can drive up to 10pF load while latching the input data (bit 3, address 02h). If DATACLK is configured as an output, it is frequency divided from the CLKP/CLKN input, depending on the operating mode, see Table 4.

**Table 4. Clock Frequency Ratios in Various Modes**

| INPUT MODE | INTERPOLATION RATE | $f_{DATA}:f_{CLK}$ | $f_{DAC}:f_{CLK}$ |
|---|---|---|---|
| Single Port | 1x | 1:1 | 1:2 |
| | 2x | 1:1 | 1:1 |
| | 4x | 1:2 | 1:1 |
| | 8x | 1:4 | 1:1 |
| Dual Port | 1x | 1:1 | 1:1 |
| | 2x | 1:2 | 1:1 |
| | 4x | 1:4 | 1:1 |
| | 8x | 1:8 | 1:1 |

The MAX5894 can be configured to latch the input data on either the rising edge or falling edge of the DATACLK signal (bit 4, address 02h). Figure 4 shows the timing requirements between the DATACLK signal and the input-data bus with latching on the rising edge.

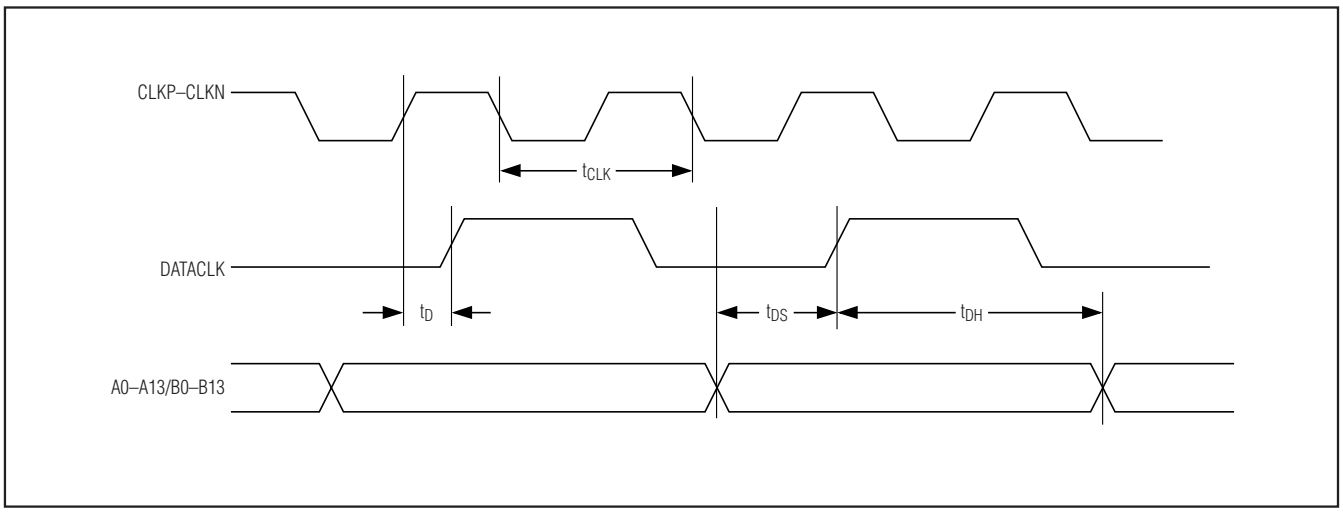


*Figure 4. Data-Input Timing Diagram*

### Interpolating Filter

The MAX5894 features three cascaded FIR half-band filters. The interpolating filters are enabled or disabled in combinations to support 1x (no interpolation), 2x, 4x, or 8x interpolation. Bits 7 and 6 of register 01h set the interpolation rate (see Table 2). The last interpolation filter is located after the modulator. In the 8x interpolation mode, the last filter (FIR3) can be configured as lowpass or highpass (bit 5, address 01h) to select the lower or upper sideband from the modulation output. The frequency responses of these three filters are plotted in Figures 5–8.

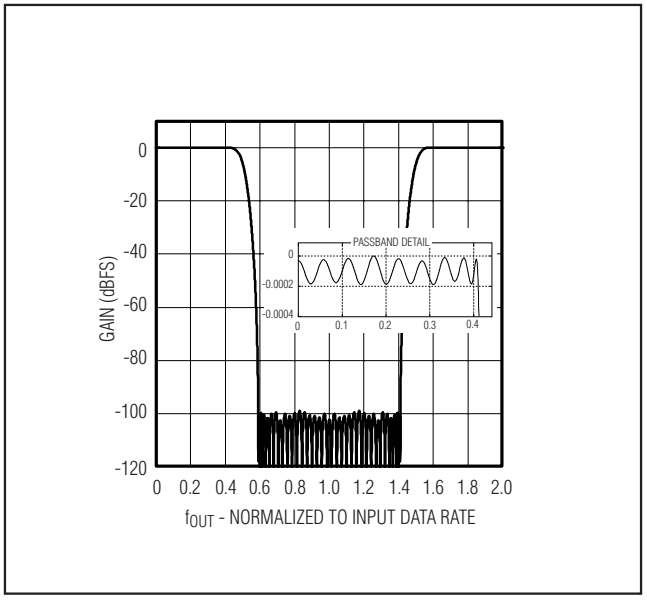


*Figure 5. Interpolation Filter Frequency Response, 2x Interpolation Mode*

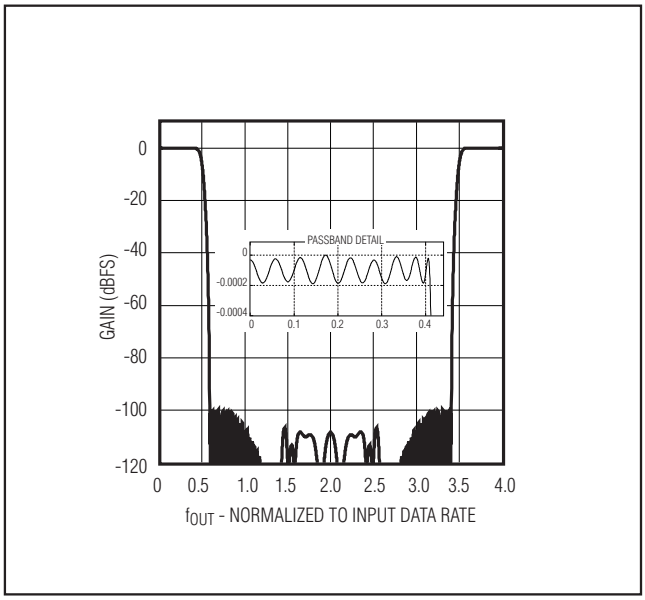


*Figure 6. Interpolation Filter Frequency Response, 4x Interpolation Mode*

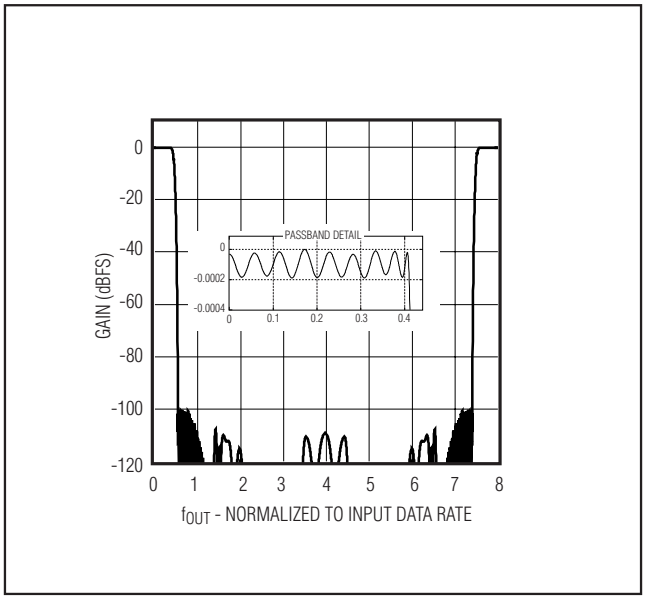


*Figure 7. Interpolation Filter Frequency Response, 8x Interpolation Mode (FIR3 Lowpass Mode)*

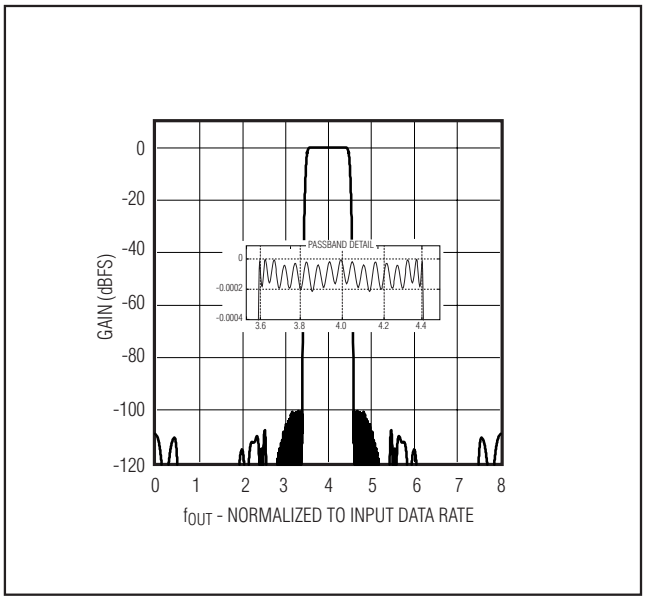


*Figure 8. Interpolation Filter Frequency Response, 8x Interpolation Mode (FIR3 Highpass Mode)*

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

The programmable interpolation filters multiply the MAX5894 input data rate by a factor of 2x, 4x, or 8x to separate the reconstructed waveform spectrum and the DAC image. The original spectral images, appearing at around multiples of the input data rate, are attenuated by the internal digital filters. This feature provides three benefits:

1) Image separation reduces complexity of analog reconstruction filters.
2) Lower input data rates eliminate board-level high-speed data transmission.
3) Sin(x)/x rolloff is reduced over the effective bandwidth.

Figure 9 illustrates a practical example of the benefits when using the MAX5894 in 2x, 4x, and 8x interpolation modes with the third filter configured as a lowpass filter. With no interpolation filter, the first image signal appears in the second Nyquist zone between $f_S/2$ and $f_S$. The first interpolating filter removes this image. In fact, all of the

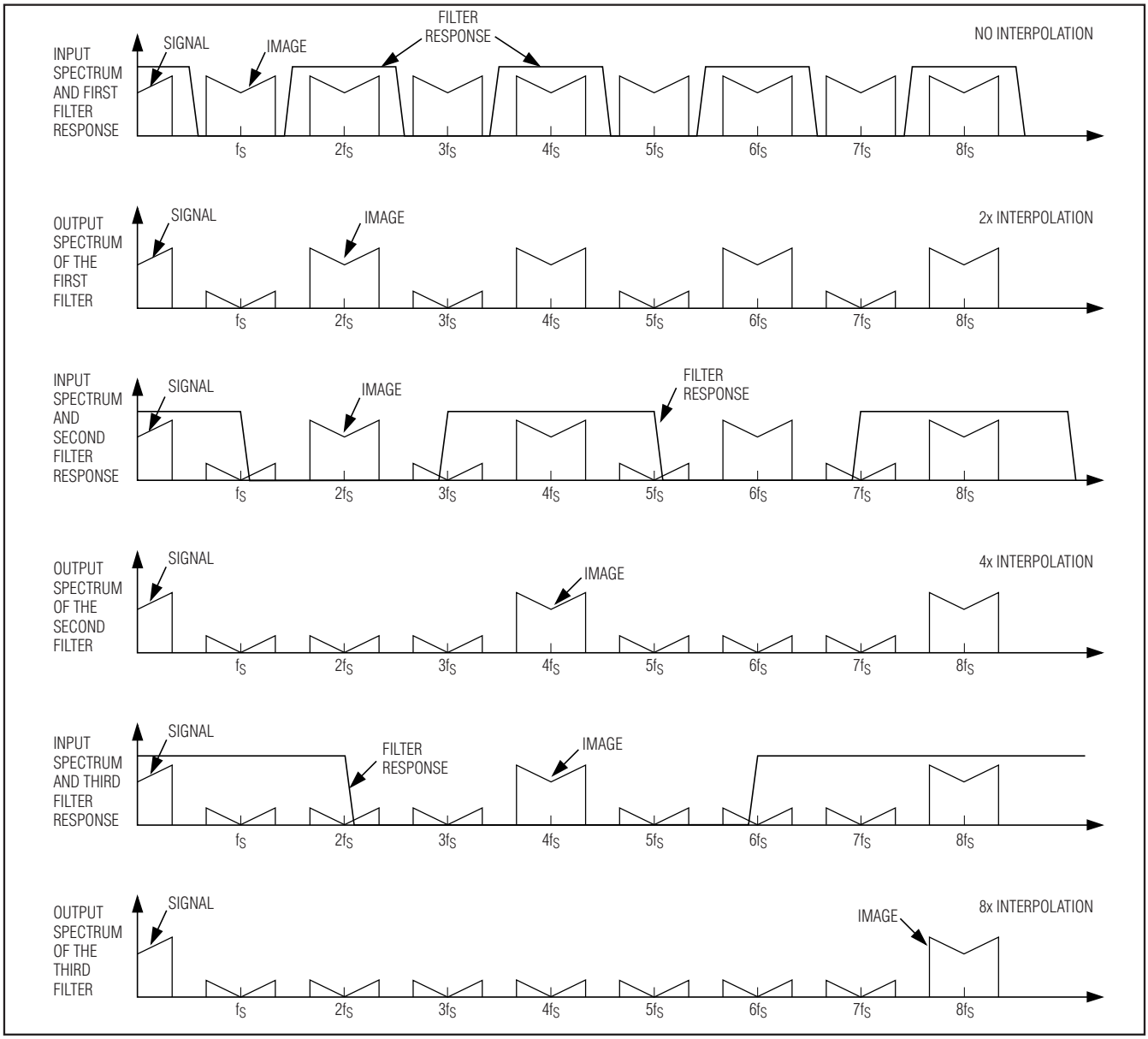


*Figure 9. Spectral Representation of Interpolating Filter Responses (Output Frequencies are Relative to the Data Input Frequency, $f_S$)*

images at odd numbers of $f_S$ are filtered. At the output of the first filter, the images are at $2f_S$, $4f_S$, etc. This signal is then passed to the second interpolating filter, which is similar to the first filter and removes the images at $2f_S$, $6f_S$, $10f_S$, etc. Finally, the third filter removes images at $4f_S$, $12f_S$, $20f_S$, etc. Figures 10, 11, and 12 similarly illustrate the spectral responses when using the interpolating filters combined with the digital modulator.

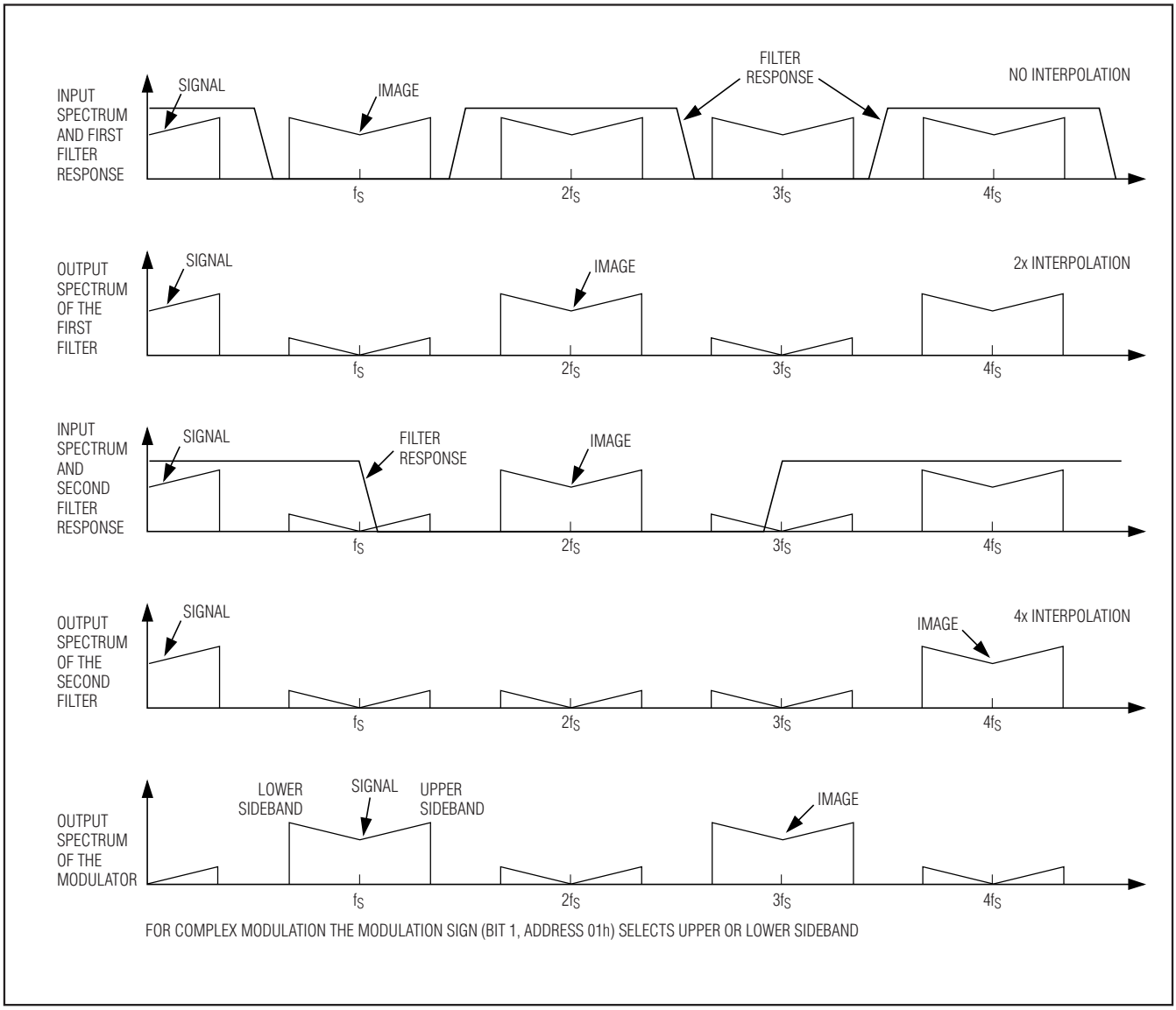


*Figure 10. Spectral Representation of 4x Interpolation Filter with $f_{IN}/4$ Modulation (Output Frequencies are Relative to the Data Input Frequency, $f_S$)*

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

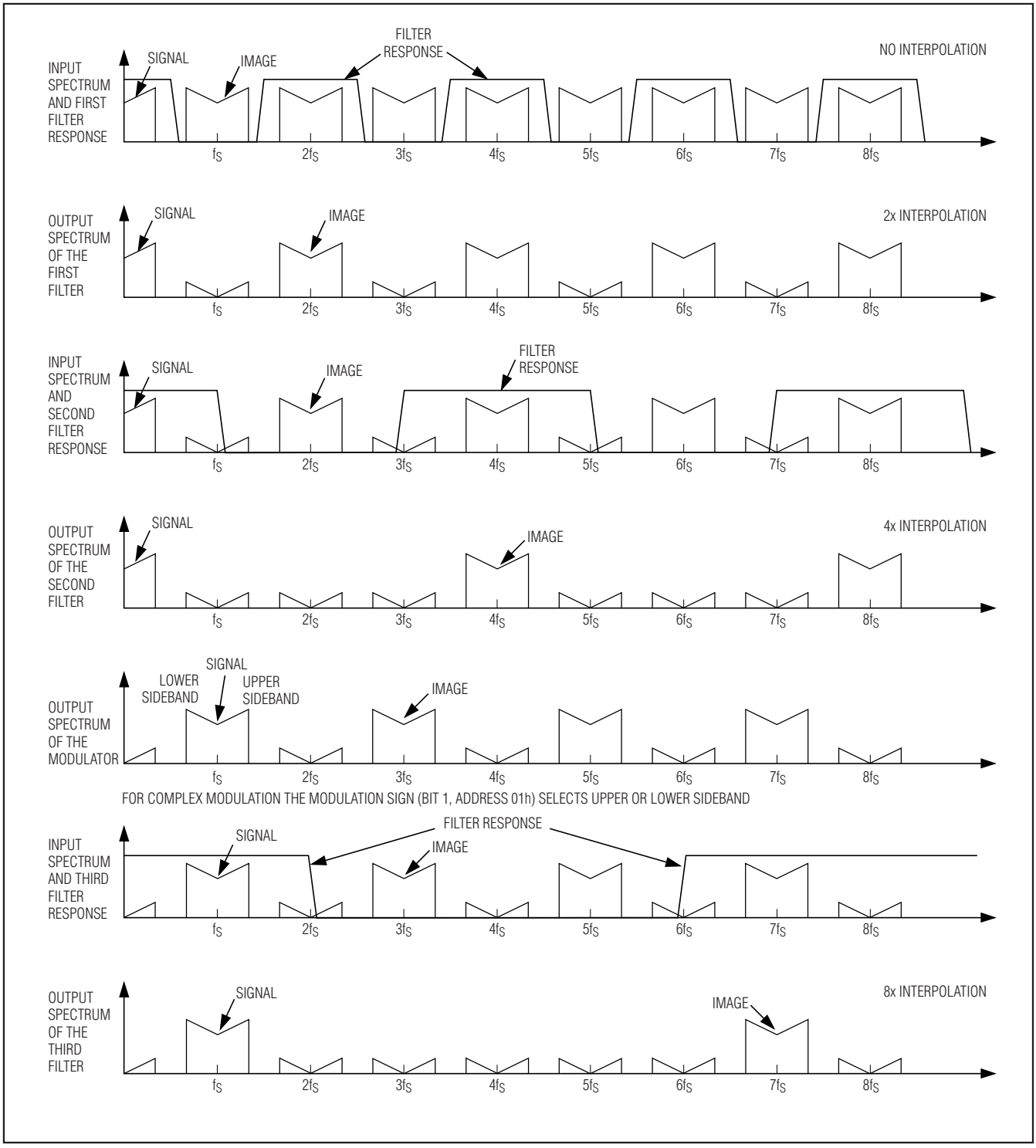


*Figure 11. Spectral Representation of 8x Interpolation Filter with $f_{IM}/4$ Modulation and Lowpass Mode Enabled (Output Frequencies are Relative to the Data Input Frequency, $f_S$)*

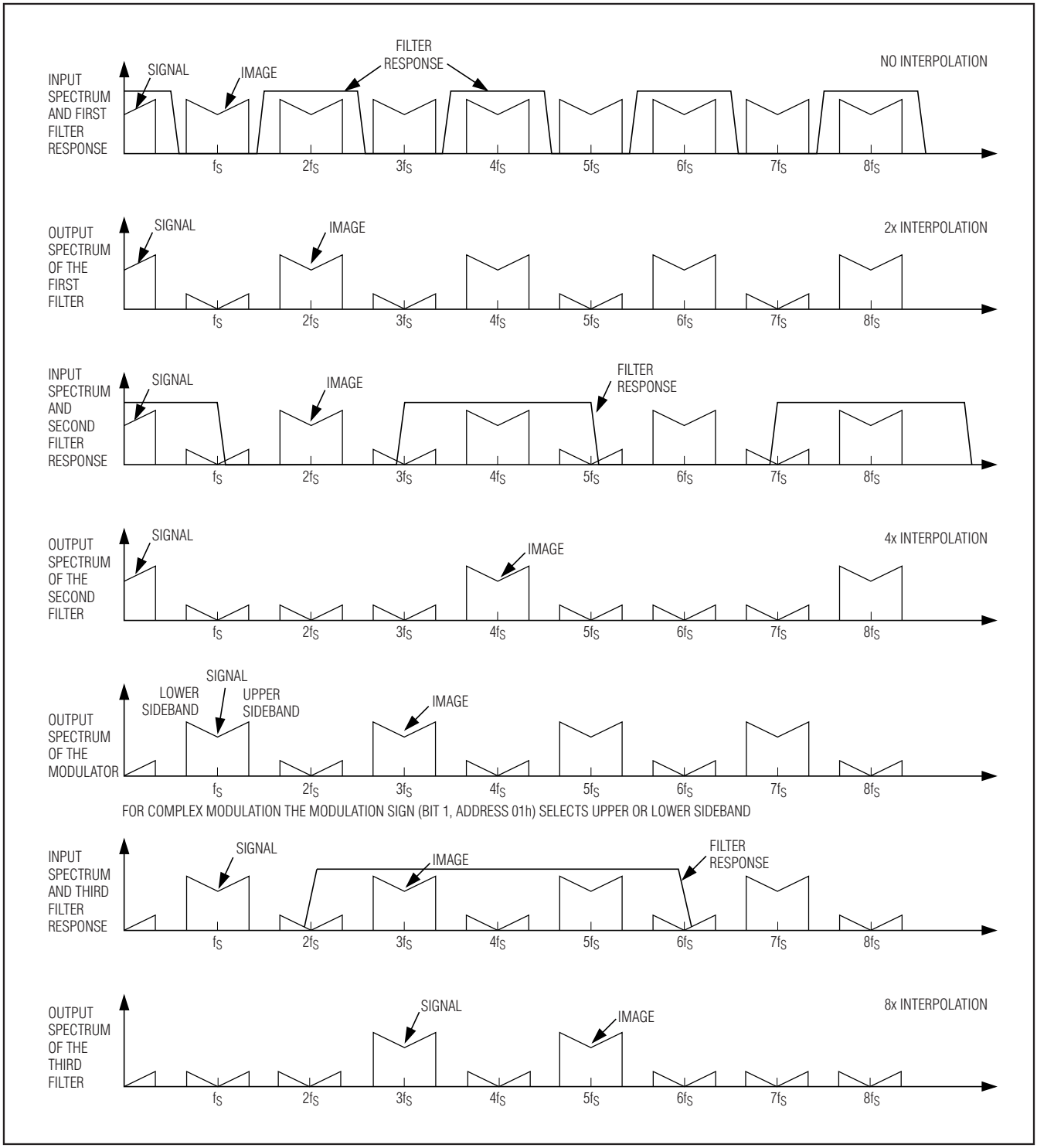


*Figure 12. Spectral Representation of 8x Interpolation Filter with $f_{IM}/4$ Modulation and Highpass Mode Enabled (Output Frequencies are Relative to the Data Input Frequency, $f_S$)*

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

### Digital Modulator

The MAX5894 features digital modulation at frequencies of $f_{IM}/2$ and $f_{IM}/4$, where $f_{IM}$ is the data rate at the input to the modulator. $f_{IM}$ equals $f_{DAC}$ in 1x, 2x, and 4x interpolation modes. In 8x interpolation mode, $f_{IM}$ equals $f_{DAC}/2$. The output rate of the modulator is always the same as the input data rate to the modulator.

In complex modulation mode, data from the second interpolation filter is frequency mixed with the on-chip in-phase and quadrature (I/Q) local oscillator (LO). Complex modulation provides the benefit of image sideband rejection when combined with an external quadrature modulator commonly found in wireless communication systems.

In the $f_{LO} = f_{IM}/4$ mode, real or complex modulation can be used. The modulator multiplies successive input data samples by the sequence [1, 0, -1, 0] for a cos(ωt). The modulator modulates the input signal up to $f_{IM}/4$, creating upper and lower images around $f_{IM}/4$. The quadrature LO sin(ωt) is realized by delaying the cos(ωt) sequence by one clock cycle. Using complex modulation, complex IF is generated. The complex IF combined with an external quadrature modulator provides image rejection. The sign of the LO can be changed to allow the user to select whether the upper or the lower image should be rejected (bit 1 of register 01h).

When $f_{IM}/2$ is chosen as the LO frequency, the input signal is multiplied by [-1, 1] on both channels. This produces images around $f_{IM}/2$. The complex image-reject modulation mode is not available for this LO frequency.

The outputs of the modulator can be expressed as:

$$I(t) = A(t) \times \cos(\omega t) - B(t) \times \sin(\omega t)$$
$$Q(t) = A(t) \times \sin(\omega t) + B(t) \times \cos(\omega t)$$

in complex modulation, $e^{+jwt}$

$$I(t) = A(t) \times \cos(\omega t) + B(t) \times \sin(\omega t)$$
$$Q(t) = A(t) \times \sin(\omega t) + B(t) \times \cos(\omega t)$$

in complex modulation, $e^{-jwt}$

where $\omega = 2 \times \pi \times f_{LO}$.

For real modulation, the outputs of the modulator can be expressed as:

$$I(t) = A(t) \times \cos(\omega t)$$
$$Q(t) = A(t) \times \cos(\omega t)$$

If more than one MAX5894 is used, their LO phases can be synchronized by simultaneously releasing $\overline{RESET}$. This sets the MAX5894 to its predefined initial phase.

### Device Reset

The MAX5894 can be reset by holding the $\overline{RESET}$ pin low for 10ns. This will program the control registers to their default values in Table 2. During power-on, $\overline{RESET}$ must be held low until all power supplies have stabilized. Alternatively, programming bit 5 of address 00h to a logic-high also resets the MAX5894 after power-up.

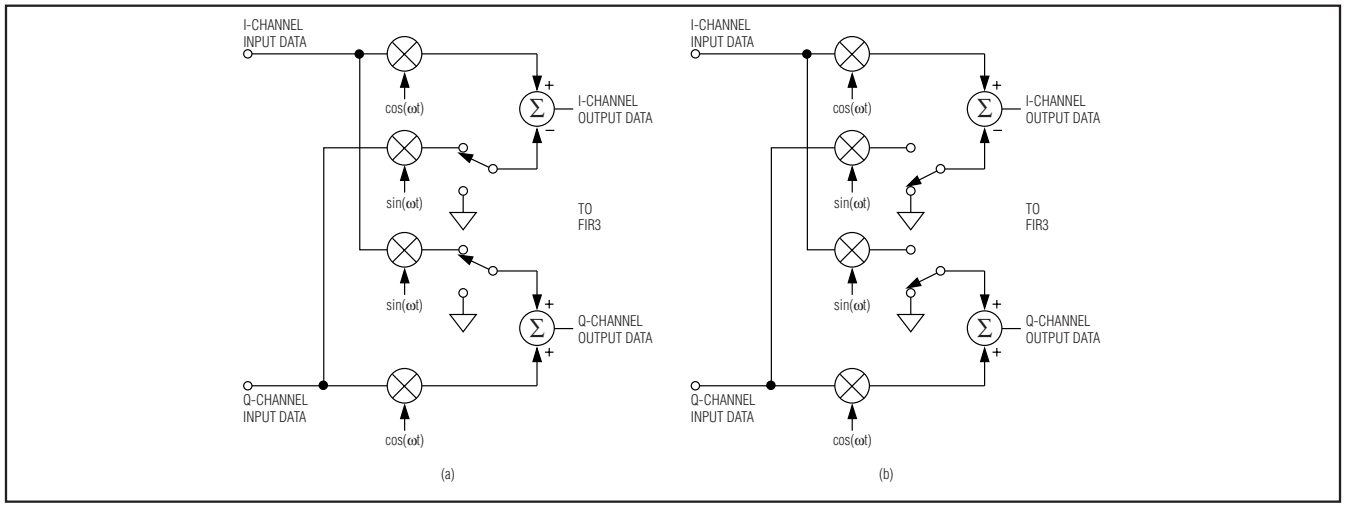


*Figure 13. (a) Modulator in Complex Modulation Mode; (b) Modulator in Real Modulation Mode*

### Power-Down Mode

The MAX5894 features three power-saving modes. Each DAC can be individually powered down through bits 2 and 3 of address 00h. The interpolation filters can also be powered down through bit 4 of address 00h, preserving the output level of each DAC (the DACs remain powered). Powering down both DACs automatically puts the MAX5894 into full power-down, including the interpolation filters.

## Applications Information

### Frequency Planning

System designers need to take the DAC into account during frequency planning for high-performance applications. Proper frequency planning can ensure that optimal system performance is achieved. The MAX5894 is designed to deliver excellent dynamic performance across wide bandwidths, as required for communication systems. As with all DACs, some combinations of output frequency and update rate produce better performance than others.

Harmonics are often folded down into the band of interest. Specifically, if the DAC outputs a frequency close to $f_S/N$, the Mth harmonic of the output signal will be aliased down to:

$$f = f_S - M \times f_{OUT} = f_S \left[ \frac{N-M}{N} \right]$$

Thus, if $N \approx (M + 1)$, the Mth harmonic will be close to the output frequency. SFDR performance of a current-steering DAC is often dominated by 3rd-order harmonic distortion. If this is a concern, placing the output signal at a different frequency other than $f_S/4$ should be considered.

Common to interpolating DACs are images near the divided clocks. In a DAC configured for 4x interpolation, this applies to images around $f_S/4$ and $f_S/2$. In a DAC configured for 8x interpolation, this applies to images around $f_S/8$, $f_S/4$, and $f_S/2$. Most of these images are not part of the in-band (0 to $f_{DATA}/2$) SFDR specification, though they are a consideration for out-of-band ($f_{DATA}/2$ - $f_{DAC}/2$) SFDR and may depend on the relationship of the DATACLK to DAC update clock (see the *Data Clock* section). When specifying the output reconstruction filter for other than baseband signals, these images should not be ignored.

### Data Clock

The MAX5894 features synchronizers that allow for arbitrary phase alignment between DATACLK and CLKP/CLKN. The DATACLK causes internal switching in the MAX5894 and the phase between DATACLK (input mode) to CLKP/CLKN influences the images at DATACLK. Optimum image rejection is achieved when DATACLK transitions are aligned with the falling edge of CLKP. Figure 14 shows the image level near DATACLK as a function of the DATACLK (input mode) to CLKP/CLKN phase at 500Msps, 4x interpolation for a 10MHz, -6dBFS output signal.

### Clock Interface

The MAX5894 features a flexible differential clock input (CLKP, CLKN) with a separate supply ($AV_{CLK}$) to achieve optimum jitter performance. It uses an ultra-low jitter clock to achieve the required noise density. Clock jitter must be less than $0.5ps_{RMS}$ to meet the specified noise density. For that reason, the CLKP/CLKN input source must be designed carefully. The differential clock (CLKN and CLKP) input can be driven from a single-ended or a differential clock source. Differential clock drive is required to achieve the best dynamic performance from the DAC. For single-ended operation, drive CLKP with a low noise source and bypass CLKN to GND with a 0.1µF capacitor.

The CLKP and CLKN pins are internally biased to $AV_{CLK}/2$. This allows the user to AC-couple clock

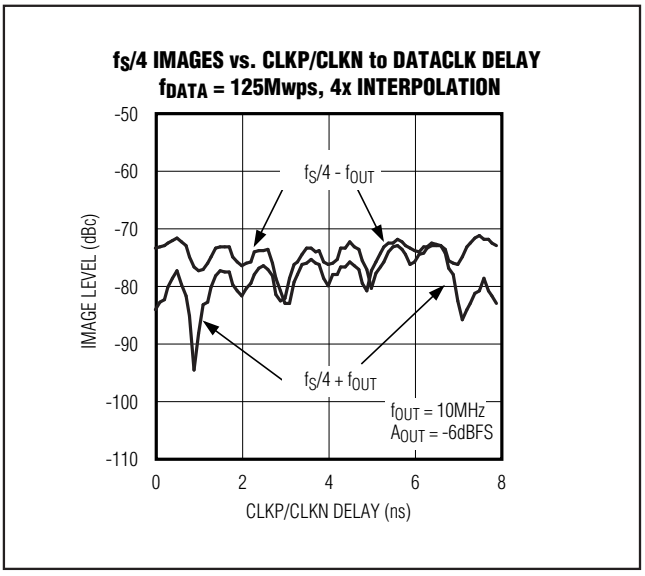


*Figure 14. Effect of CLKP/CLKN to DATACLK Phase on $f_S/4$ Images*

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sources directly to the device without external resistors to define the DC level. The input resistance of CLKP and CLKN is 5kΩ.

A convenient way to apply a differential signal is with a balun transformer as shown in Figure 15. Alternatively, these inputs may be driven from a CMOS-compatible clock source, however it is recommended to use sine-wave or AC-coupled differential ECL/PECL drive for best dynamic performance.

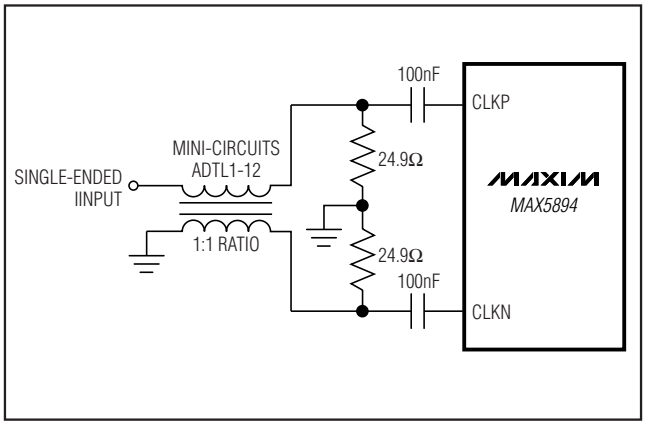


*Figure 15. Single-Ended-to-Differential Clock Conversion Using a Balun Transformer*

### Output Interface (OUTI, OUTQ)

The MAX5894 outputs complementary currents (OUTIP, OUTIN, OUTQP, and OUTQN) that can be utilized in a differential configuration. Load resistors convert these two output currents into a differential output voltage.

The differential output between OUTIP (OUTQP) and OUTIN (OUTQN) can be converted to a single-ended output using a transformer or a differential amplifier. Figure 16 shows a typical transformer-based application circuit for generation of IF output signals. In this configuration, the MAX5894 operates in differential mode, which reduces even-order harmonics, and increases the available output power. Pay close attention to the transformer core saturation characteristics when selecting a transformer. Transformer core saturation can introduce strong second harmonic distortion, especially at low output frequencies and high signal amplitudes. It is recommended to connect the transformer center tap to ground.

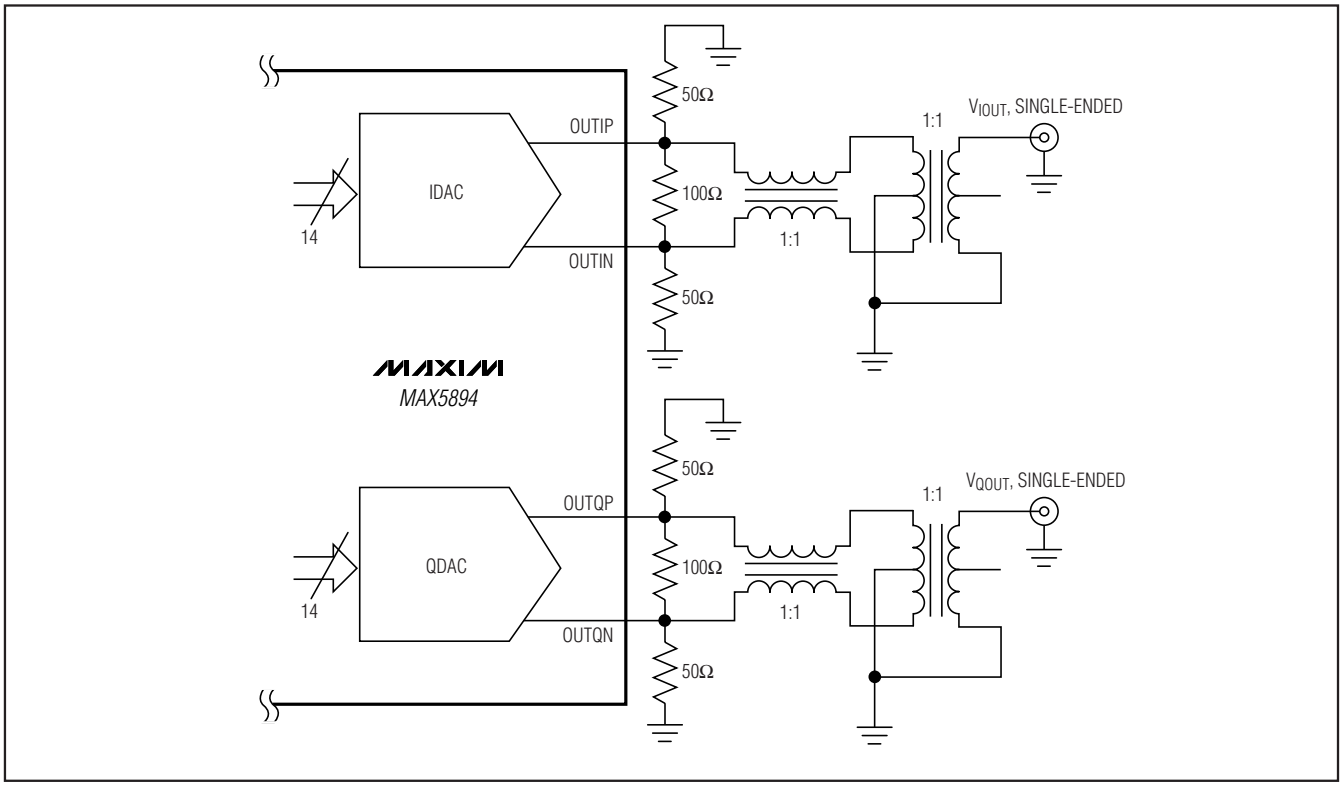


*Figure 16. Differential-to-Single-Ended Conversion Using Wideband RF Transformers*

If a transformer is not used, the outputs must have a resistive termination to ground. Figure 17 shows the MAX5894 output configured for differential DC-coupled mode. The DC-coupled configuration can be used to eliminate waveform distortion due to highpass filter effects. Applications include communication systems employing analog quadrature upconverters and requiring a high-speed DAC for baseband I/Q synthesis.

If a single-ended DC-coupled unipolar output is desirable, OUTIP (OUTQP) should be selected as the output, and connect OUTIN (OUTQN) to ground. Using the MAX5894 output single-ended is not recommended because it introduces additional noise and distortion.

The distortion performance of the DAC also depends on the load impedance. The MAX5894 is optimized for a 50Ω double termination. It can be used with a transformer output as shown in Figure 16 or just one 25Ω resistor from each output to ground and one 50Ω resistor between the outputs (Figure 17). Higher output termination resistors can be used, as long as each output voltage does not exceed +1V with respect to GND, but at the cost of degraded distortion performance and increased output noise voltage.

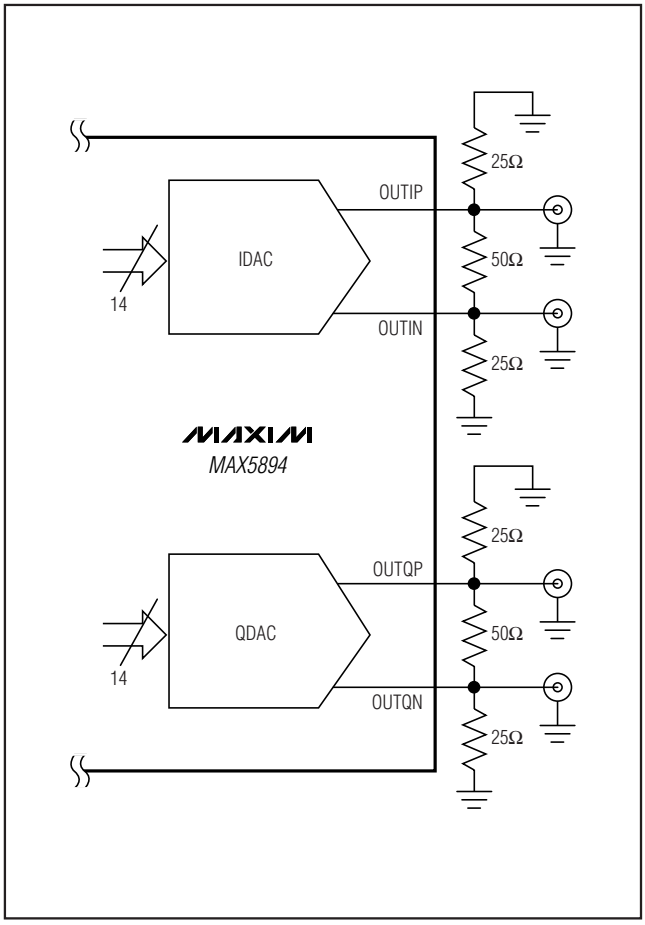


*Figure 17. The DC-Coupled Differential Output Configuration*

### Reference Input/Output

The MAX5894 supports operation with the on-chip 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source, and as the output if the DAC is operating with the internal reference.

For stable operation with the internal reference, REFIO should be decoupled to GND with a 1µF capacitor.

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REFIO must be buffered with an external amplifier, if heavy loading is required, due to its 10kΩ output resistance.

Alternatively, apply a temperature-stable external reference to REFIO (Figure 18). The internal reference is overdriven by the external reference. For improved accuracy and drift performance, choose a fixed output voltage reference such as the MAX6520 bandgap reference.

The MAX5894's reference circuit (Figure 19) employs a control amplifier, designed to regulate the full-scale current $I_{OUT}$ for the differential current outputs of the DAC. The output current can be calculated as:

$$I_{OUTFS} = 32 \times I_{REF} \times 16383/16384$$

where $I_{REF}$ is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$). Located between FSADJ and DACREF, $R_{SET}$ is the reference resistor, which determines the amplifier's output current for the DAC. Use Table 5 for a matrix of different $I_{OUTFS}$ and $R_{SET}$ selections.

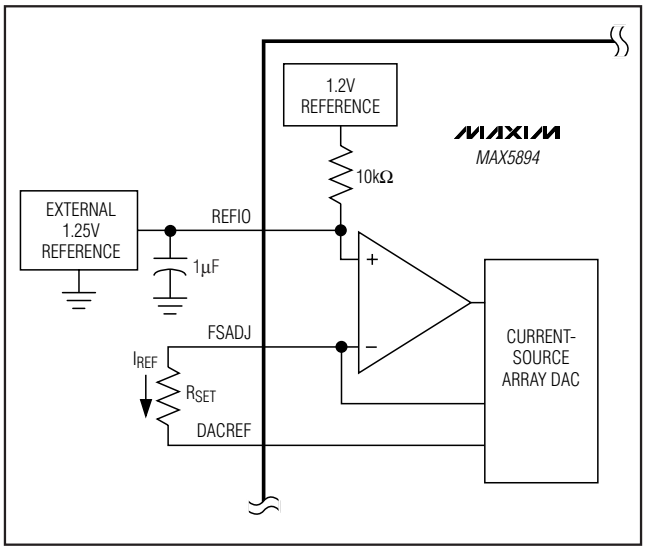


*Figure 18. Typical External Reference Circuit*

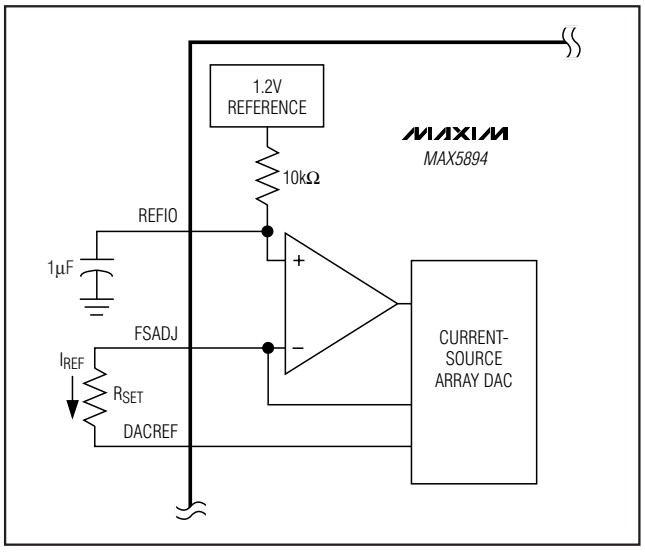


*Figure 19. MAX5894 Internal Reference Architecture*

## Table 5. $I_{OUTFS}$ and $R_{SET}$ Selection Matrix Based on a Typical 1.20V Reference Voltage

| FULL-SCALE CURRENT | REFERENCE CURRENT | $R_{SET}$ (kΩ) | | OUTPUT VOLTAGE |
|---|---|---|---|---|
| $I_{OUTFS}$ (mA) | $I_{REF}$ (µA) | CALCULATED | 1% EIA STD | $V_{IOUTP/N}$* ($mV_{P-P}$) |
| 2 | 62.50 | 19.2 | 19.1 | 100 |
| 5 | 156.26 | 7.68 | 7.5 | 250 |
| 10 | 312.50 | 3.84 | 3.83 | 500 |
| 15 | 468.75 | 2.56 | 2.55 | 750 |
| 20 | 625.00 | 1.92 | 1.91 | 1000 |

**Terminated into a 50Ω load.*

### Power Supplies, Bypassing, Decoupling, and Layout

Grounding and power-supply decoupling strongly influence the MAX5894 performance. Unwanted digital crosstalk can couple through the input, reference, power-supply, and ground connections, which can affect dynamic specifications like signal-to-noise ratio or spurious-free dynamic range. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX5894. Observe the grounding and power-supply decoupling guidelines for high-speed, high-frequency applications. Follow the power-supply and filter configuration guidelines to achieve optimum dynamic performance.

Using a multilayer PCB with separate ground and power-supply planes, run high-speed signals on lines directly above the ground plane. Since the MAX5894 has separate analog and digital sections, the PCB should include separate analog and digital ground sections with only one point connecting the three planes at the exposed pad under the MAX5894. Run digital signals above the digital ground plane and analog/clock signals above the analog/clock ground plane. Keep digital signals as far away from sensitive analog inputs, reference lines, and clock inputs as practical. Use a symmetric design of clock input and the analog output lines to minimize 2nd-order harmonic distortion components, thus optimizing the dynamic performance of the DAC. Keep digital signal paths short and run lengths matched to avoid propagation delay and data skew mismatches.

The MAX5894 requires five separate power-supply inputs for the analog ($AV_{DD1.8}$ and $AV_{DD3.3}$), digital ($DV_{DD1.8}$ and $DV_{DD3.3}$), and clock ($AV_{CLK}$) circuitry. Decouple each voltage supply pin with a separate 0.1µF capacitor as close to the device as possible and with the shortest possible connection to the appropriate ground plane. Minimize the analog and digital load capacitances for optimized operation. Decouple all power-supply voltages at the point they enter the PCB with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

**The exposed pad MUST be soldered to the ground.** Use multiple vias, an array of at least 4 x 4 vias, directly under the EP to provide a low thermal and electrical impedance path for the IC.

## Static Performance Parameter Definitions

### Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from either a best straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

### Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes with respect to the full-scale of the DAC. This error affects all codes by the same amount.

### Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

## Dynamic Performance Parameter Definitions

### Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the specified accuracy.

### Noise Spectral Density

The DAC output noise is the sum of the quantization noise and thermal noise. Noise spectral density is the noise power in 1Hz bandwidth, specified in dBFS/Hz.

### Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog output (RMS value) to the RMS quantization error (residual error). The ideal, theoretical maximum SNR can be derived from the DAC's resolution (N bits):

$$SNR_{dB} = 6.02_{dB} \times N + 1.76_{dB}$$

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However, noise sources such as thermal noise, reference noise, clock jitter, etc., affect the ideal reading. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

### Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of their next largest distortion component. SFDR is usually measured in dBc and with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

### Two-/Four-Tone Intermodulation Distortion (IMD)

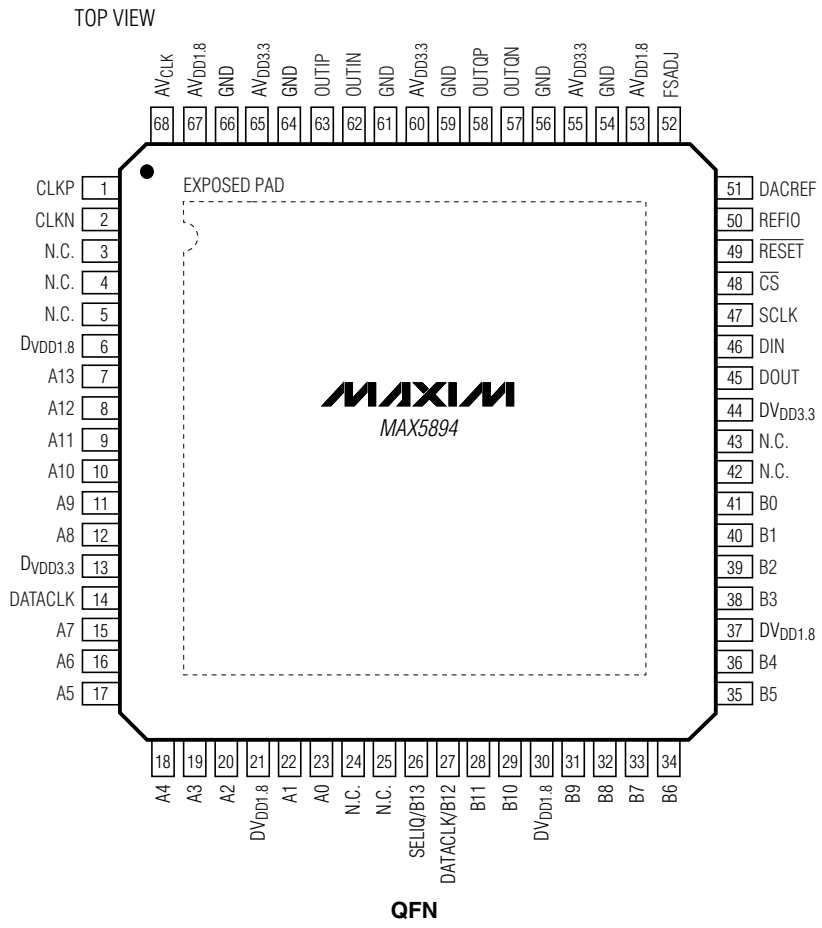
The two-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD products to either output tone.

### Adjacent Channel Leakage Power Ratio (ACLR)

Commonly used in combination with WCDMA (wideband code-division multiple-access), ACLR reflects the leakage power ratio in dB between the measured powers within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

## Pin Configuration




**QFN**

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 68 QFN-EP | G6800-4 | **21-0122** |

# 14-Bit, 500Msps, Interpolating and Modulating Dual DAC with CMOS Inputs

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | — | Initial release | — |
| 1 | 4/07 | — | — |
| 2 | 10/08 | Add note to setup and hold specifications. | 5, 6 |

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