19-3263; Rev 1; 7/04

Positive High-Voltage, Hot-Swap Controllers

General Description

The MAX5933A–MAX5933F/MAX5947A/B/C fully integrated hot-swap controllers for +9V to +80V positive supply rails (MAX5947A/B/C), allow for the safe insertion and removal of circuit cards into live backplanes without causing glitches on the backplane power-supply rail. The MAX5947B is pin- and function-compatible with the LT1641-2. The other devices offer added features such as a choice of active-high or active-low power-good outputs (PWRGD/$\overline{\text{PWRGD}}$), latched/autoretry fault management, and autoretry duty-cycle options of 3.75% or 0.94% (see the *Selector Guide*).

The MAX5933A–MAX5933F are available with a default undervoltage lockout threshold of +31V and operate over a supply voltage range of +33V to +80V. The MAX5947A/B/C are available with a default undervoltage of +8.3V. All devices feature a programmable analog foldback current limit. If the device remains in current limit for more than a programmable time, the external n-channel MOSFET is either latched off (MAX5933A/MAX5933C/MAX5947A) or is set to automatically restart after a timeout delay (MAX5933B/MAX5933D/MAX5933E/MAX5933F/MAX5947B/MAX5947C).

The MAX5933_ and MAX5947_ operate in the extended temperature range of -40°C to +85°C. These devices are available in an 8-pin SO package.

Applications

Hot Board Insertion

Electronic Circuit Breakers

Industrial High-Side Switch/Circuit Breakers

Network Routers and Switches

24V/48V Industrial/Alarm Systems

Features

- ♦ **Pin- and Function-Compatible with the LT1641-2 (MAX5947B)**
- ♦ **Provides Safe Hot Swap for +9V to +80V Power-Supply Range (MAX5947A/B/C)**
- ♦ **Safe Board Insertion and Removal from Live Backplanes**
- ♦ **Latched/Autoretry Management**
- ♦ **Active-Low or Active-High Power-Good Output**
- ♦ **Programmable Foldback Current Limiting**
- ♦ **High-Side Drive for an External N-Channel MOSFET**
- ♦ **Built-In Thermal Shutdown**
- ♦ **Undervoltage Lockout (UVLO)**
- ♦ **Overvoltage Protection**
- ♦ **User-Programmable Supply Voltage Power-Up Rate**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5933_ESA*	-40°C to +85°C	8 SO
MAX5947_ESA*	-40°C to +85°C	8 SO

**Insert the desired suffix from the Selector Guide into the blank to complete the part number.*

Typical Application Circuit and Pin Configuration appear at end of data sheet.

Selector Guide

PART	LATCHED FAULT PROTECTION	AUTORETRY FAULT PROTECTION	PWRGD OUTPUT LOGIC	DUTY CYCLE (%)	DEFAULT UVLO (V)	SUPPLY VOLTAGE RANGE (V)
MAX5933A	Yes	—	High	—	31	33 to 80
MAX5933B	—	Yes	High	3.75	31	33 to 80
MAX5933C	Yes	—	Low	—	31	33 to 80
MAX5933D	—	Yes	Low	3.75	31	33 to 80
MAX5933E	—	Yes	High	0.94	31	33 to 80
MAX5933F	—	Yes	Low	0.94	31	33 to 80
MAX5947A	Yes	—	Low	—	8.3	9 to 80
MAX5947B	—	Yes	High	3.75	8.3	9 to 80
MAX5947C	—	Yes	Low	3.75	8.3	9 to 80

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V_{CC} ....-0.3V to +85V
SENSE, FB, ON ....-0.3V to (V_{CC} + 0.3V)
TIMER, PWRGD, $\overline{PWRGD}$......................................-0.3V to +85V
GATE ....-0.3V to +95V
Maximum GATE Current ....-50mA, +150mA
Maximum Current into Any Other Pin...............................±50mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).................470mW
Operating Temperature Range ....-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
ESD Rating (Human Body Model).....................................2000V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +24V (MAX5947A/B/C), V_{CC} = +48V (MAX5933A–MAX5933F), GND = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	MAX5947A/B/C		9		80	V
		MAX5933A–MAX5933F		33		80	
Supply Current	I_{CC}	V_{ON} = 3V, V_{CC} = 80V			1.4	3.5	mA
V_{CC} Undervoltage Lockout	V_{LKO}	V_{CC} low-to-high transition	MAX5947A/B/C	7.5	8.3	8.8	V
			MAX5933A–MAX5933F	29.5	31	32.5	
V_{CC} Undervoltage Lockout Hysteresis	$V_{LKOHYST}$	MAX5947A/B/C			0.4		V
		MAX5933A–MAX5933F			2		
FB High-Voltage Threshold	V_{FBH}	FB low-to-high transition		1.280	1.313	1.345	V
FB Low-Voltage Threshold	V_{FBL}	FB high-to-low transition		1.221	1.233	1.245	V
FB Hysteresis	V_{FBHYST}				80		mV
FB Input Bias Current	I_{INFB}	V_{FB} = 0V		-1		+1	µA
FB Threshold Line Regulation	ΔV_{FB}	$V_{CC(MIN)} \le V_{CC} \le$ 80V, ON = 0V, T_A = 0°C to +70°C				0.05	mV/V
SENSE Trip Voltage (V_{CC} - V_{SENSE})	$V_{SENSETRIP}$	V_{FB} = 0V, T_A = 0°C to +70°C		8	12	17	mV
		V_{FB} = 1V, T_A = 0°C to +70°C		39	47	55	
GATE Pullup Current	I_{GATEUP}	Charge pump on, V_{GATE} = 7V		-5	-10	-20	µA
GATE Pulldown Current	I_{GATEDN}	Any fault condition, V_{GATE} = 2V		35	70	100	mA
External N-Channel Gate Drive	ΔV_{GATE}	V_{GATE} - V_{CC}	MAX5933A–MAX5933F	10	13.6	18	V
			V_{CC} = 10.8V to 20V, MAX5947A/B/C	4.5	6.2	18.0	
			V_{CC} = 20V to 80V, MAX5947A/B/C	10	13.2	18	
TIMER Pullup Current	$I_{TIMERUP}$	V_{TIMER} = 0V		-24	-80	-120	µA
TIMER Pulldown Current	$I_{TIMERON}$	V_{TIMER} = 1V	MAX5933A–MAX5933D, MAX5947A/B/C	1.5	3	4.5	µA
			MAX5933E/MAX5933F	0.37	0.75	1.12	
ON Logic-High Threshold	V_{ONH}	ON low-to-high transition		1.280	1.313	1.345	V
ON Logic-Low Threshold	V_{ONL}	ON high-to-low transition		1.221	1.233	1.245	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +24V (MAX5947A/B/C), V_{CC} = +48V (MAX5933A–MAX5933F), GND = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ON Hysteresis	V_{ONHYST}			80		mV
ON Input Bias Current	I_{INON}	V_{ON} = 0V	-1		+1	µA
PWRGD Leakage Current	I_{OH}	V_{PWRGD} = 80V			10	µA
$\overline{PWRGD}$ Leakage Current	I_{OL}	$V_{\overline{PWRGD}}$ = 80V			10	µA
PWRGD/$\overline{PWRGD}$ Output Low Voltage		I_O = 2mA			0.4	V
		I_O = 4mA			2.5	
SENSE Input Bias Current	I_{SENSE}	V_{SENSE} = 0V to V_{CC}	-1		+3	µA
Thermal Shutdown		Temperature rising		+150		°C
Thermal Shutdown Hysteresis				20		°C
ON Low-to-GATE Low Propagation Delay	t_{PHLON}	C_{GATE} = 0, Figures 1, 2		6		µs
ON High-to-GATE High Propagation Delay	t_{PLHON}	C_{GATE} = 0, Figures 1, 2		1.7		µs
FB Low-to-PWRGD Low Propagation Delay	t_{PHLFB}	Figures 1, 3		3.2		µs
FB High-to-PWRGD High Propagation Delay	t_{PLHFB}	Figures 1, 3		1.5		µs
(V_{CC} - V_{SENSE}) High-to-GATE Low Propagation Delay	$t_{PHLSENSE}$	T_A = +25°C, C_{GATE} = 0, Figures 1, 4	0.5		2	µs

Note 1: All currents into the device are positive and all currents out of the device are negative. All voltages are referenced to ground, unless otherwise noted.

Test Circuit and Timing Diagrams

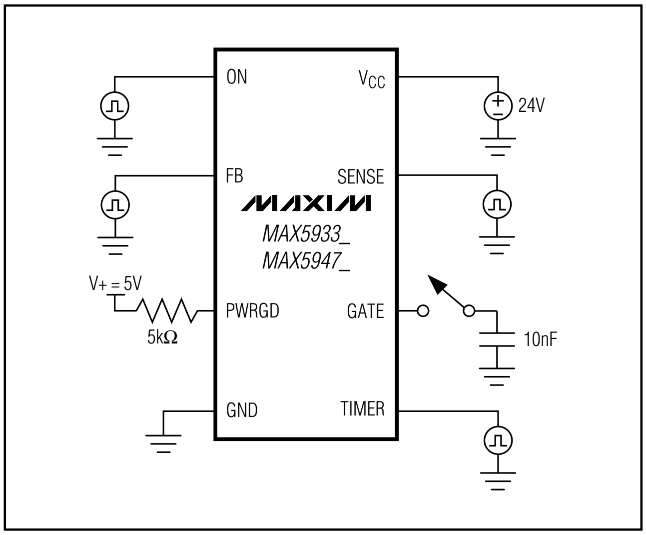


Figure 1. Test Circuit

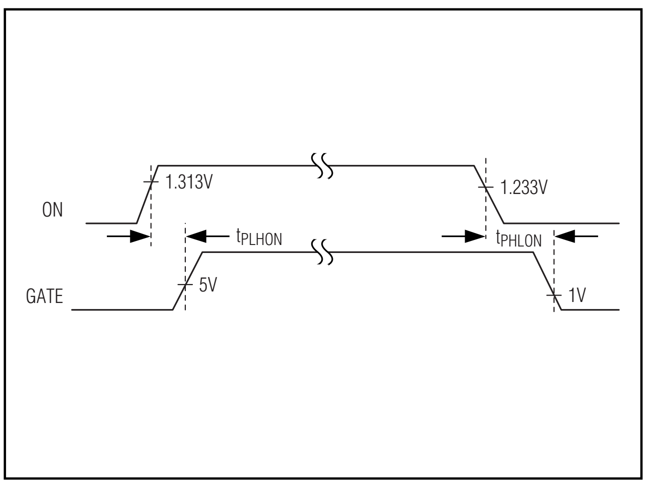


Figure 2. ON to GATE Timing

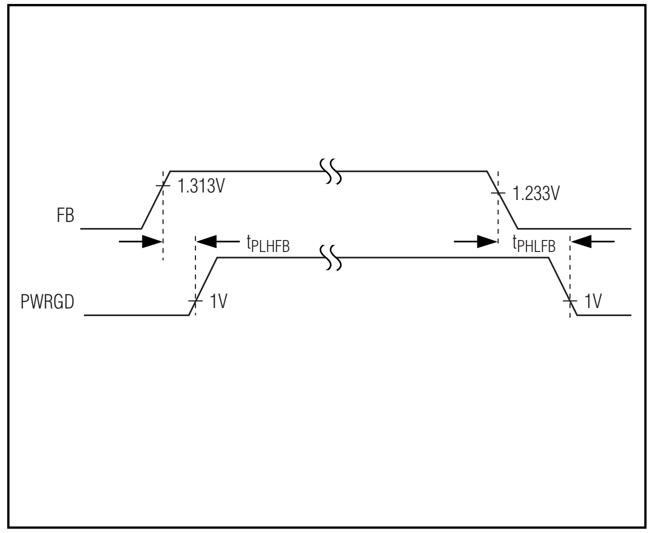


Figure 3. FB to PWRGD Timing

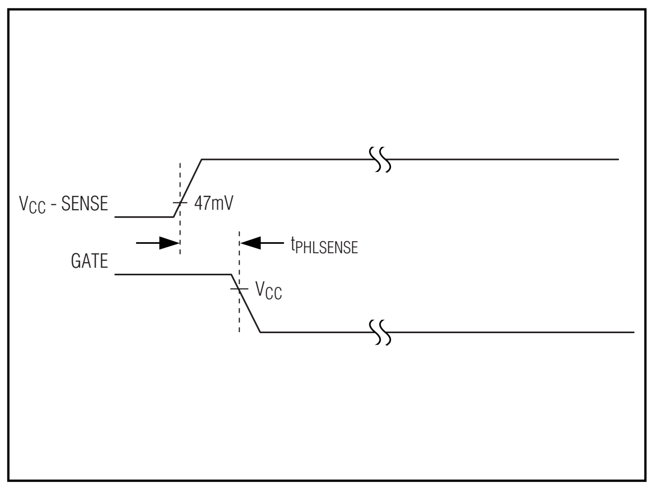
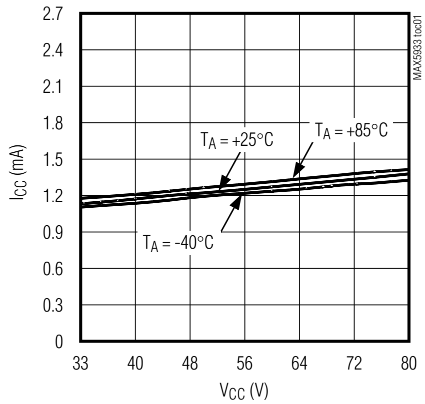


Figure 4. SENSE to GATE Timing

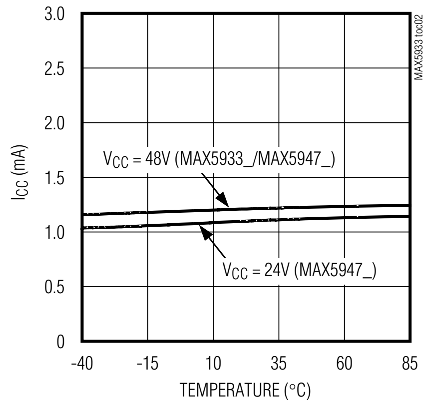
Typical Operating Characteristics

(V_{CC} = +48V, T_A = +25°C, unless otherwise noted.)

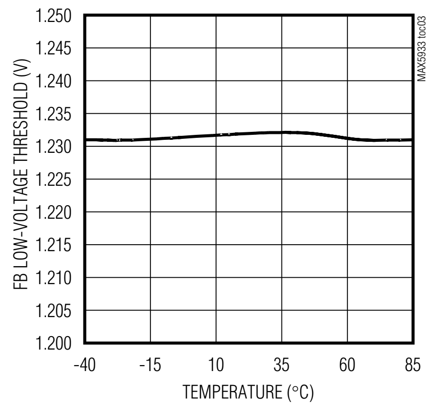
I_{CC} vs. V_{CC}



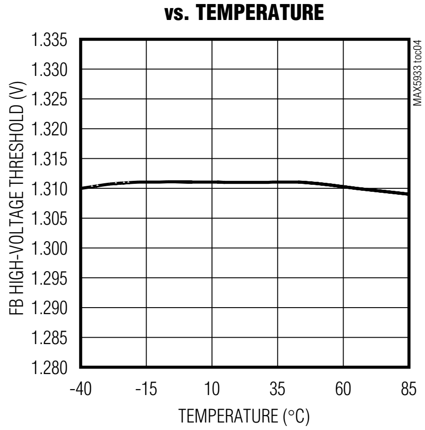
I_{CC} vs. TEMPERATURE



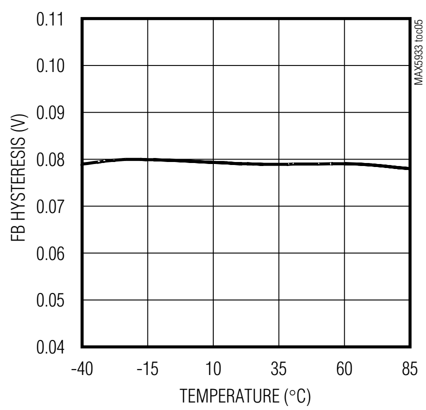
FB LOW-VOLTAGE THRESHOLD vs. TEMPERATURE



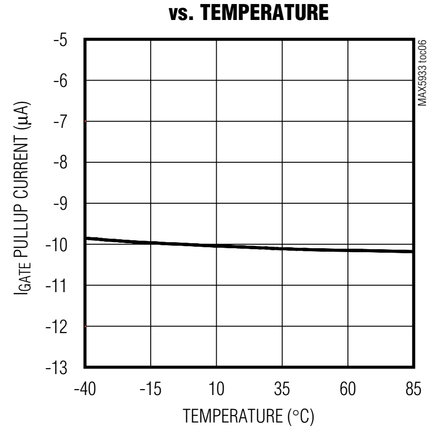
FB HIGH-VOLTAGE THRESHOLD vs. TEMPERATURE



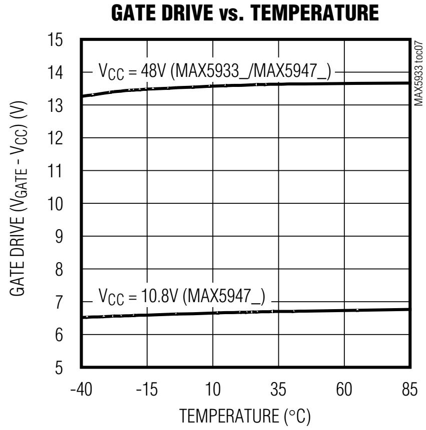
FB HYSTERESIS vs. TEMPERATURE



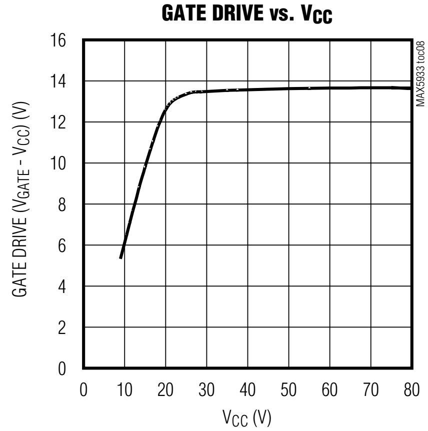
I_{GATE} PULLUP CURRENT vs. TEMPERATURE



GATE DRIVE vs. TEMPERATURE



MAX5947_ GATE DRIVE vs. V_{CC}

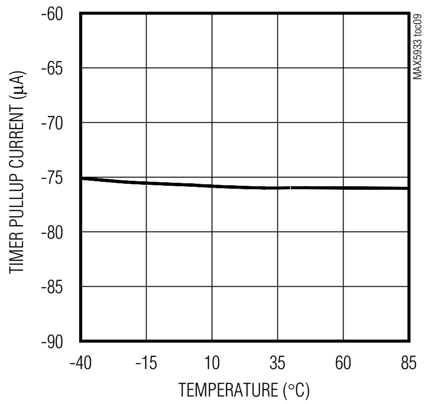


Positive High-Voltage, Hot-Swap Controllers

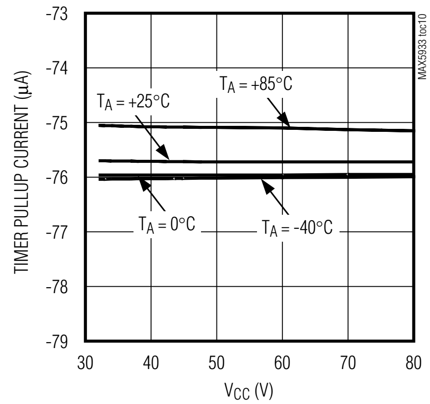
Typical Operating Characteristics (continued)

(V_{CC} = +48V, T_A = +25°C, unless otherwise noted.)

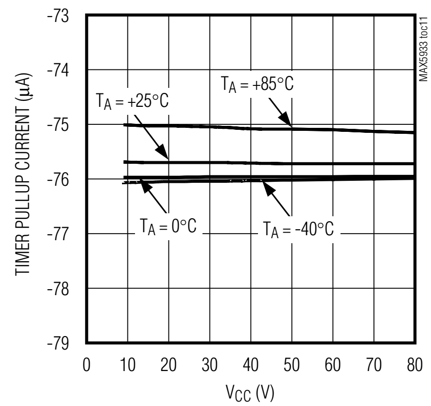
TIMER PULLUP CURRENT vs. TEMPERATURE



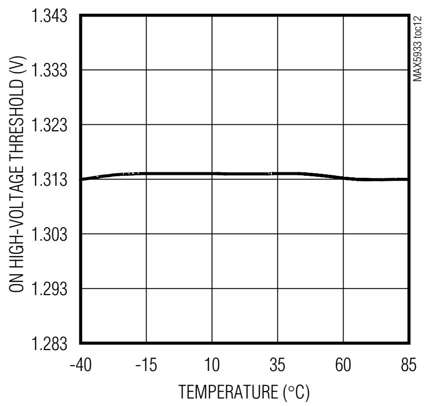
MAX5933_ TIMER PULLUP CURRENT vs. V_{CC}



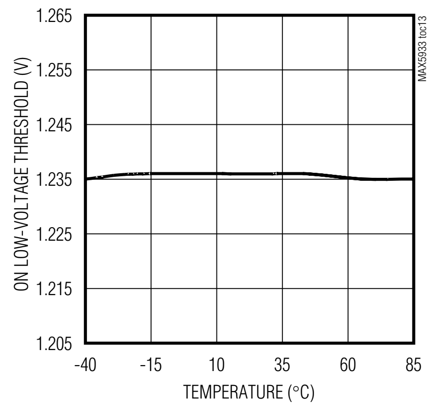
MAX5947_ TIMER PULLUP CURRENT vs. V_{CC}



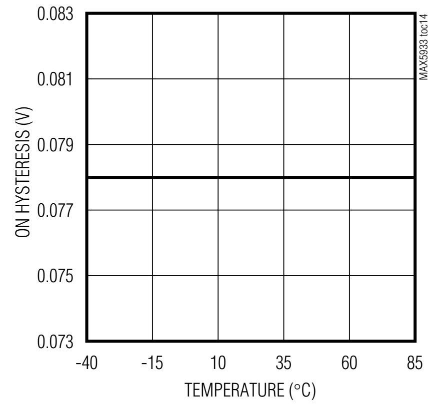
ON HIGH-VOLTAGE THRESHOLD vs. TEMPERATURE



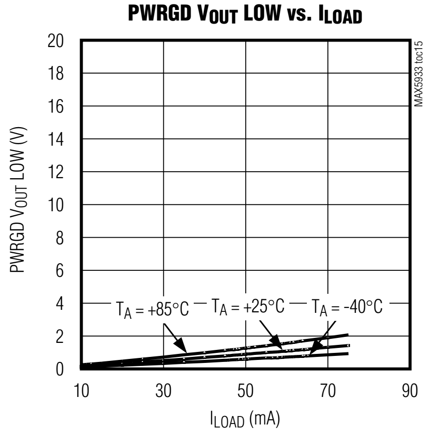
ON LOW-VOLTAGE THRESHOLD vs. TEMPERATURE



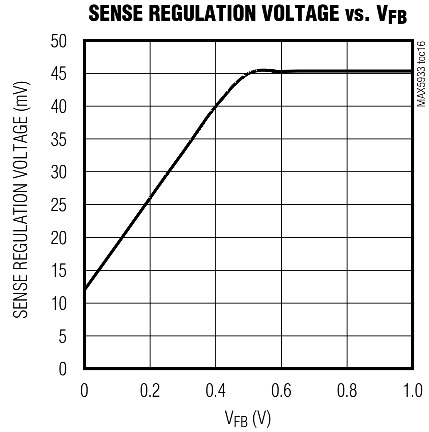
ON HYSTERESIS vs. TEMPERATURE



PWRGD V_{OUT} LOW vs. I_{LOAD}



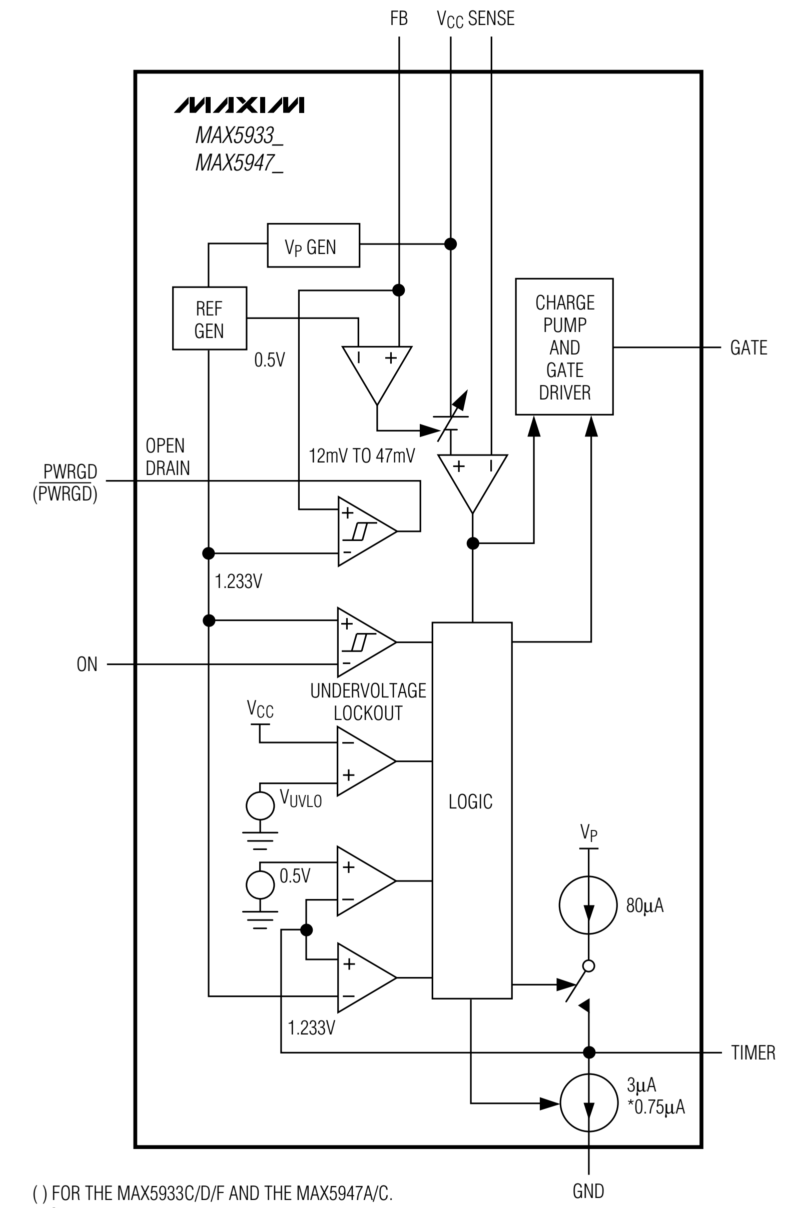
SENSE REGULATION VOLTAGE vs. V_{FB}



Pin Description

PIN	NAME	FUNCTION
1	ON	ON/OFF Control Input. ON is used to implement the undervoltage lockout threshold and resets the part after a fault condition for the latched-off version (MAX5933A/MAX5933C/MAX5947A, see the *Detailed Description* section).
2	FB	Power-Good Comparator Input. Connect a resistive divider from output to FB to GND to monitor the output voltage (see the *Power-Good Detection* section). FB is also used as a feedback for the current-limit foldback function.
3	PWRGD/ $\overline{PWRGD}$	Open-Drain Power-Good Output. PWRGD is high ($\overline{PWRGD}$ is low) when V_{FB} is higher than V_{FBH}. PWRGD is low ($\overline{PWRGD}$ is high) when V_{FB} is lower than V_{FBL}.
4	GND	Ground
5	TIMER	Timing Input. Connect a capacitor from TIMER to GND to program the maximum time the part is allowed to remain in current limit (see the *TIMER* section).
6	GATE	Gate-Drive Output. The high-side gate drive for the external N-channel MOSFET (see the *GATE Voltage* section).
7	SENSE	Current-Sense Input. Connect a sense resistor from V_{CC} to SENSE and the drain of the external n-channel MOSFET.
8	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 0.1µF capacitor. Input voltage range is from +9V to +80V for the MAX5947A/B/C. Input voltage range is from +33V to +80V for the MAX5933A–MAX5933F.

Functional Diagram



( ) FOR THE MAX5933C/D/F AND THE MAX5947A/C.
*FOR THE MAX5933E/MAX5933F.

Detailed Description

The MAX5933_ and MAX5947_ are fully integrated hot-swap controllers for positive supply rails. The devices allow for the safe insertion and removal of circuit cards into live backplanes without causing glitches on the backplane power-supply rail. During startup, the MAX5933_ and MAX5947_ act as current regulators using an external sense resistor and a MOSFET to limit the amount of current drawn by the load.

The MAX5933_ operate from a +33V to +80V supply voltage range and have a default undervoltage lockout (UVLO) set to +31V. The MAX5947_ operate from a +9V to +80V supply voltage range and have a default UVLO set to +8.3V. The UVLO threshold is adjustable using a resistive divider connected from V_{CC} to ON to GND (see Figure 5).

The MAX5933_ and MAX5947_ monitor the input voltage, the output voltage, the output current, and the die temperature. These devices feature power-good outputs (PWRGD/$\overline{PWRGD}$) to indicate the status of the output voltage by monitoring the voltage at FB (see the *Power-Good Detection* section).

As shown in Figure 5, a sense resistor is connected between V_{CC} and SENSE to regulate the voltage across the sense resistor (V_{IN} - V_{SENSE}) to 47mV when the voltage at FB ≥ 0.5V. The current-limit threshold ($V_{SENSETRIP}$) decreases linearly from 47mV to 12mV as FB decreases from 0.5V to 0V.

An undervoltage fault is detected when ON goes below the threshold (V_{ONL} = 1.233V) and the voltage at GATE goes low as a result to turn off the MOSFET. ON must pass the V_{ONH} = 1.313V threshold to turn on the MOSFET again.

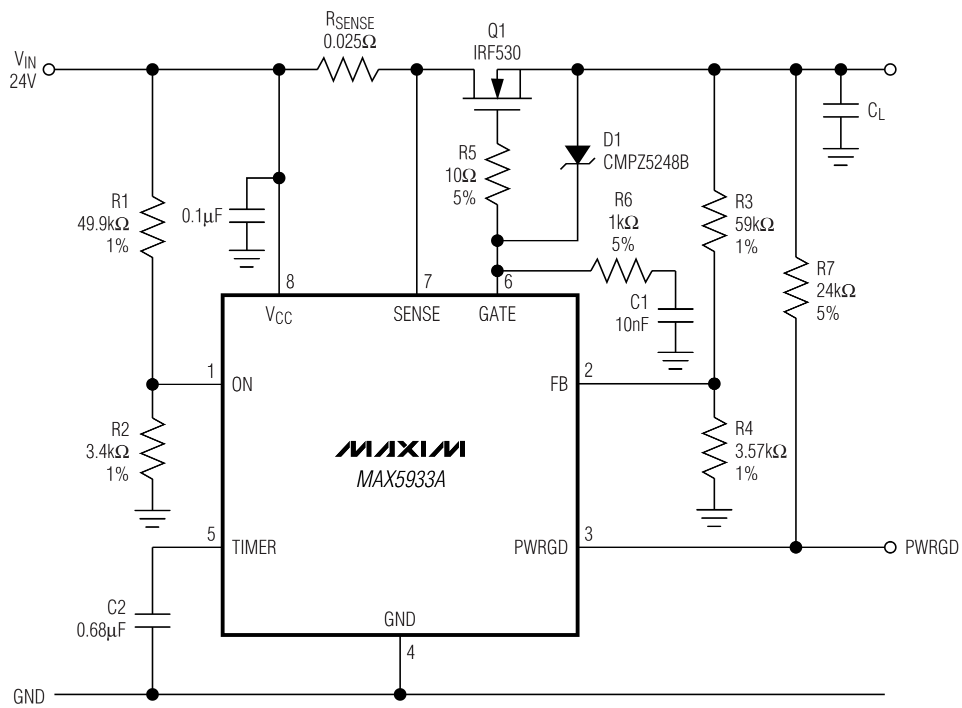


Figure 5. Application Circuit

Applications Information

Hot-Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors on the boards draw high peak currents from the backplane power bus as they charge up. The transient currents can permanently damage the connector pins and glitch the system supply, causing other boards in the system to reset.

Power-Up Sequence

The power supply on a board is controlled by placing an external n-channel MOSFET (Q1) in the power path (Figure 5). Resistor R_{SENSE} provides current detection and capacitor C1 provides control of the GATE slew rate. Resistor R6 provides current control-loop compensation, while R5 prevents high-frequency oscillations in Q1. Resistors R1 and R2 provide undervoltage sensing.

After the power pins first make contact, transistor Q1 is turned off. When the voltage at ON exceeds the turn-on threshold voltage, the voltage on V_{CC} exceeds the undervoltage lockout threshold, and when the voltage on TIMER is less than 1.233V, transistor Q1 turns on (Figure 6).

The voltage at GATE rises with a slope equal to 10µA/C1 and the supply inrush current is set at:

$$I_{INRUSH} = C_L \times 10\mu A/C1$$

When the voltage across the current-sense resistor R_{SENSE} reaches $V_{SENSETRIP}$, the inrush current is limited by the internal current-limit circuitry that adjusts the voltage on GATE to maintain a constant voltage across the sense resistor.

Once the voltage at the output has reached its final value, as sensed by resistors R3 and R4, PWRGD goes high or $\overline{PWRGD}$ goes low.

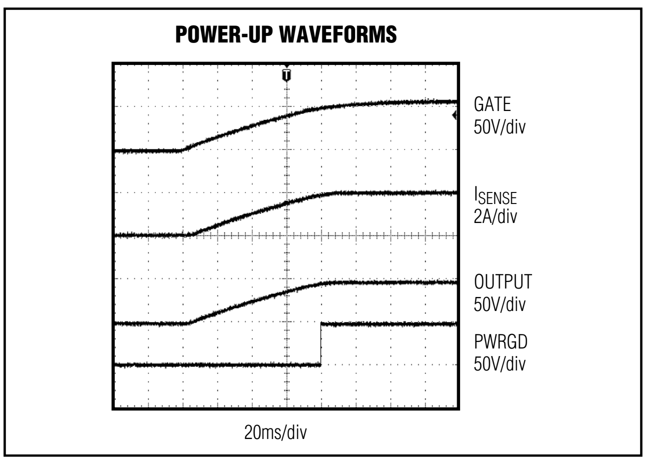


Figure 6. Power-Up Waveforms

Short-Circuit Protection

The MAX5933_/MAX5947_ feature a programmable foldback current limit with an electronic circuit breaker that protects against short circuits or excessive supply currents. The current limit is set by placing a sense resistor between V_{CC} (pin 8) and SENSE (pin 7).

To prevent excessive power dissipation in the pass transistor and to prevent voltage spikes on the input supply during short-circuit conditions at the output, the current folds back as a function of the output voltage that is sensed at FB (Figure 7).

When the voltage at FB is 0V, the current-limit circuit drives GATE to force a constant 12mV drop across the sense resistor. As the output voltage at FB increases, the voltage across the sense resistor increases until FB reaches 0.5V. At this point, the voltage across the sense resistor is held constant at 47mV.

The maximum current limit is calculated as:

$$I_{LIMIT} = 47mV / R_{SENSE}$$

For a 0.025Ω sense resistor, the current limit is set at 1.88A and folds back to 480mA when the output is shorted to ground.

The MAX5933_/MAX5947_ also feature a variable overcurrent response time. The time required to regulate Q1's drain current depends on:

1) Q1's input capacitance
2) GATE capacitor C1 and compensation resistor R6
3) The internal delay from SENSE to GATE

Figure 8 shows the delay from a voltage step at SENSE until GATE voltage starts falling, as a function of overdrive.

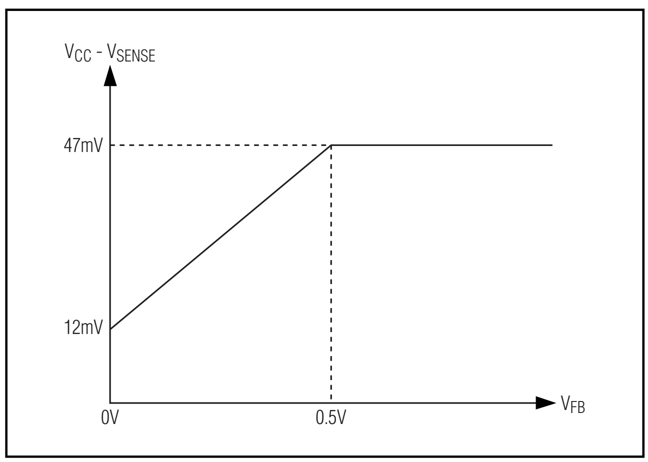


Figure 7. Current-Limit Sense Voltage vs. Feedback Voltage

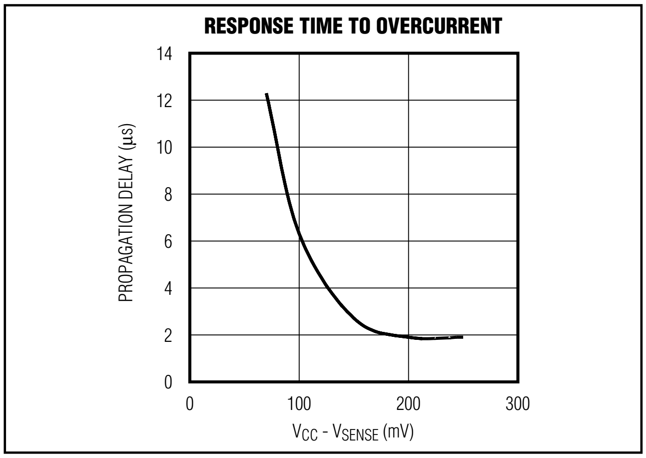


Figure 8. Response Time to Overcurrent

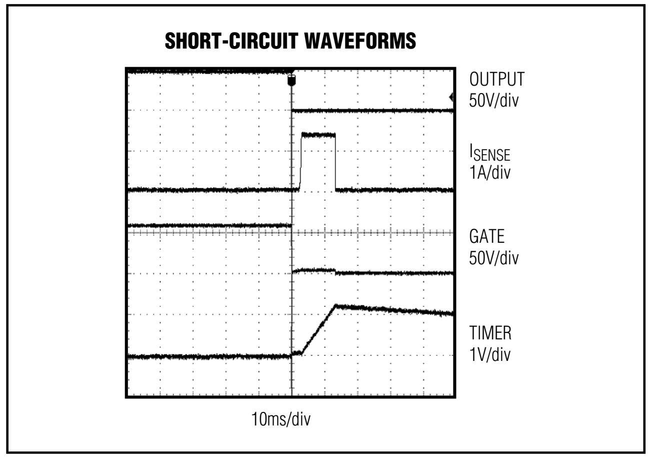


Figure 9. Short-Circuit Waveforms

TIMER

TIMER provides a method for programming the maximum time the device is allowed to operate in current limit. When the current-limit circuitry is not active, TIMER is pulled to GND by a 3µA current source. After the current-limit circuit becomes active, an 80µA pullup current source is connected to TIMER, and the voltage rises with a slope equal to 77µA/C_{TIMER}, as long as the current-limit circuit remains active. Once the desired maximum current-limit time is chosen, the capacitor value is:

$$C(nF) = 65 \times t(ms)$$

or

$$T_{LIMIT} = (C_{TIMER}/80\mu A) \times 1.233V$$

When the current-limit circuit turns off, TIMER is discharged to GND by the 3µA current source.

Whenever TIMER reaches 1.233V, the internal fault latch is set. GATE is immediately pulled to GND and TIMER is pulled back to GND by the 3µA current source. When TIMER falls below 0.5V, ON is pulsed low to reset the internal fault latch.

The waveform in Figure 9 shows how the output latches off following a short circuit. The drop across the sense resistor is held at 12mV as the timer ramps up. Since the output did not rise, FB remains below 0.5V and the circuit latches off. For Figure 9, C_T = 100nF.

Undervoltage and Overvoltage Detection

ON can be used to detect an undervoltage condition at the power-supply input. ON is internally connected to an analog comparator with 80mV of hysteresis. If ON falls below its threshold voltage (1.233V), GATE is pulled low and is held low until ON is high again.

Figure 10 shows an overvoltage detection circuit. When the input voltage exceeds the Zener diode's breakdown voltage, D1 turns on and starts to pull TIMER high. After TIMER is pulled higher than 1.233V, the fault latch is set and GATE is pulled to GND immediately, turning off transistor Q1 (see Figure 11). Operation is restored either by interrupting power or by pulsing ON low.

Power-Good Detection

The MAX5933_/MAX5947_ include a comparator for monitoring the output voltage. The noninverting input (FB) is compared against an internal 1.233V precision reference and exhibits 80mV hysteresis. The comparator's output (PWRGD) is open drain and capable of operating from a pullup as high as 80V. The $\overline{PWRGD}$ is similar to PWRGD with an opposite polarity (active low) output.

The PWRGD ($\overline{PWRGD}$) can be used to directly enable/disable a power module with an active-high enable input. Figure 12 shows how to use PWRGD to control an active-low enable-input power module. Signal inversion is accomplished by transistor Q2 and R7.

Supply Transient Protection

The MAX5933_/MAX5947_ are 100% tested and guaranteed to be safe from damage with supply voltages up to 80V. However, spikes above 85V may damage the device. During a short-circuit condition, the large change in currents flowing through the power-supply traces can cause inductive voltage spikes which could exceed 85V. To minimize the spikes, the power-trace parasitic inductance should be minimized by using wider traces or heavier trace plating and a 0.1µF bypass capacitor placed between V_{CC} and GND. A transient voltage suppressor (TVS) at the input can also prevent damage from voltage surges.

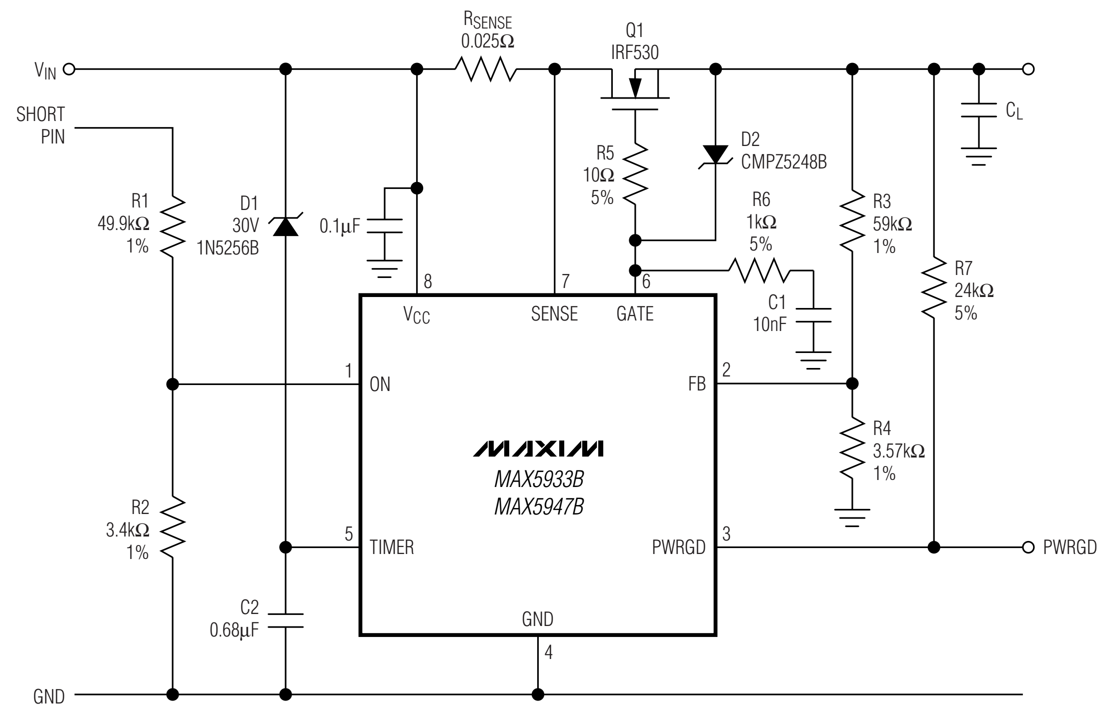


Figure 10. Overvoltage Detection

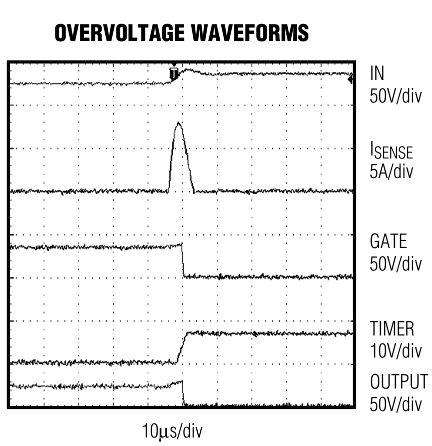


Figure 11. Overvoltage Waveforms

GATE Voltage

A curve of Gate Drive vs. V_{CC} is shown in Figure 13. GATE is clamped to a maximum voltage of 18V above the input voltage. At a minimum input-supply voltage of 33V, the minimum gate drive voltage is 10V. When the input supply voltage is higher than 20V, the gate-drive voltage is at least 10V and a standard n-channel MOSFET can be used. Using the MAX5947 in applications over a 9V to 20V range, a logic-level N-FET must be used with a proper protection Zener diode between its gate and source (see D1 in Figure 5).

Thermal Shutdown

If the MAX5933_/MAX5947_ die temperature reaches +150°C, an overtemperature fault is generated. As a result, GATE goes low and turns the external MOSFET off. The MAX5933_/MAX5947_ die temperature must cool down below +130°C before the overtemperature fault condition is removed.

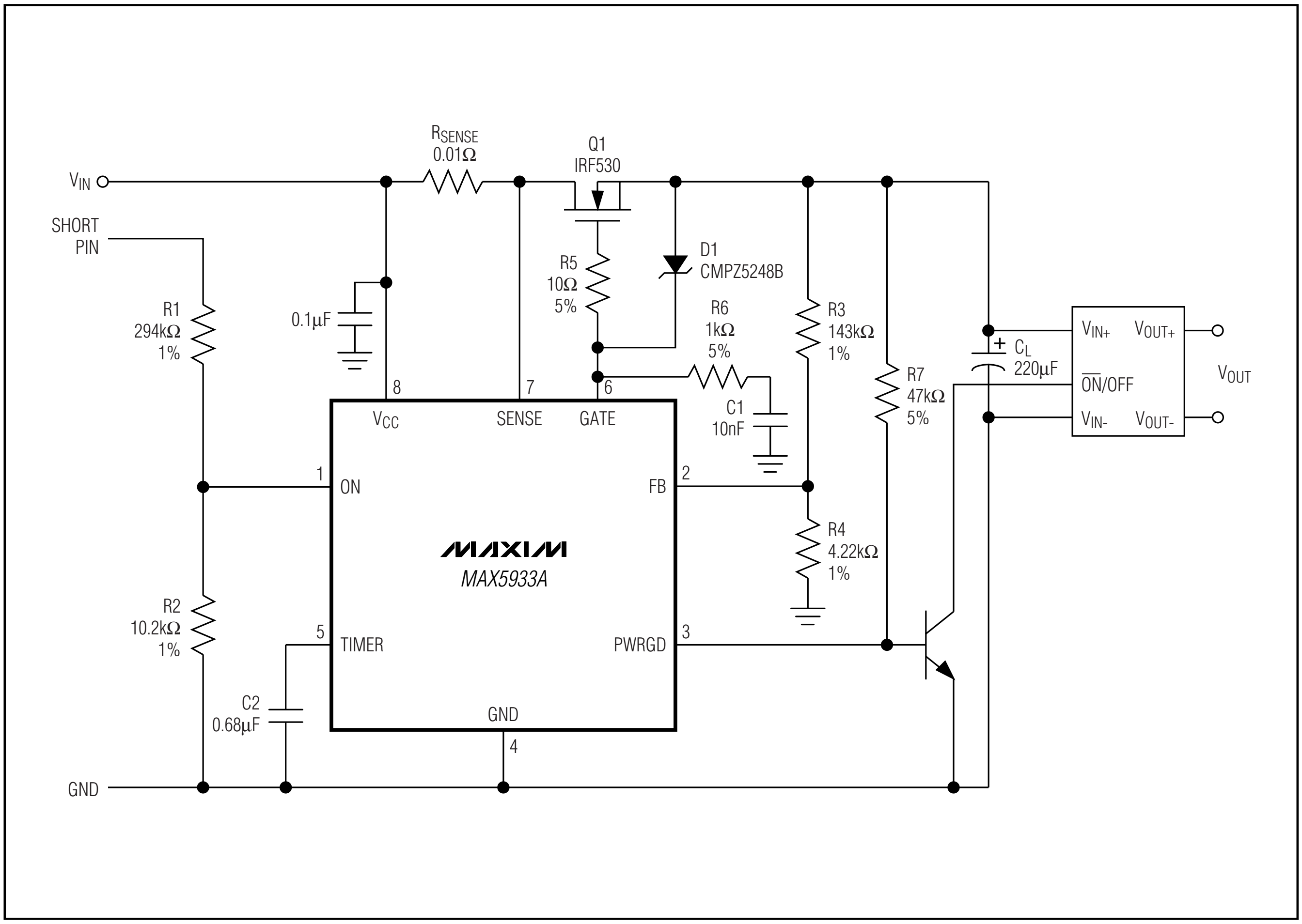


Figure 12. Active-Low Enable Module

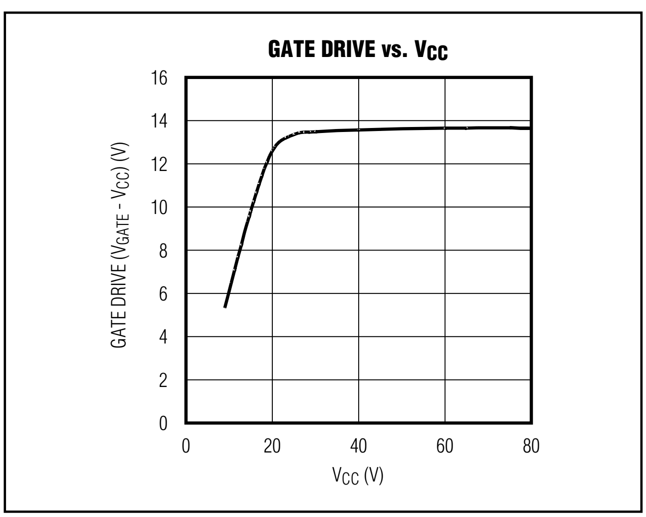


Figure 13. Gate Drive vs. Supply Voltage

Layout Considerations

To achieve accurate current sensing, a Kelvin connection is recommended. The minimum trace width for 1oz copper foil is 0.02in per amplifier to ensure the trace stays at a reasonable temperature. However, 0.03in. per amplifier or wider is recommended. Note that 1oz copper exhibits a sheet resistance of approximately 530µΩ/square. Small resistances add up quickly in high-current applications. To improve noise immunity, connect the resistor-divider to ON close to the device, and keep traces to V_{CC} and GND short. A 0.1µF capacitor from ON to GND also helps reject induced noise. Figure 14 shows a layout that addresses these issues. It is recommended that 2oz copper is used, particularly as the external MOSFET must be thermally coupled to the MAX5933_/MAX5947_ to ensure proper thermal-shutdown operation.

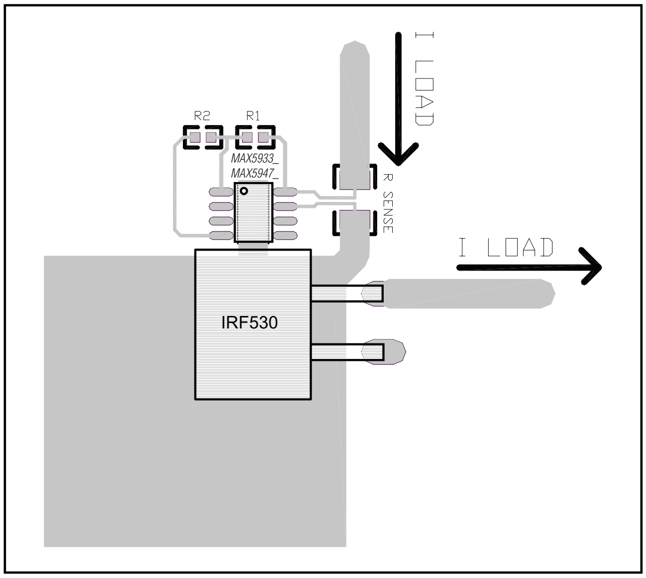


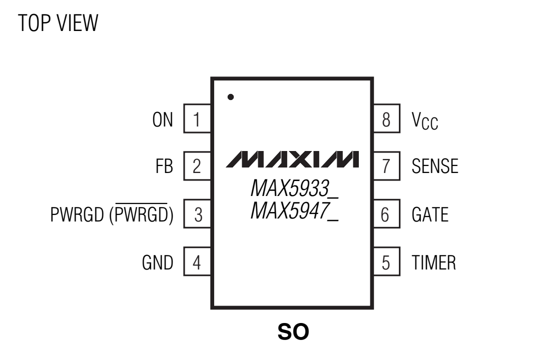
Figure 14. Recommended Layout for R1, R2, and R_{SENSE}

Chip Information

TRANSISTOR COUNT: 1573

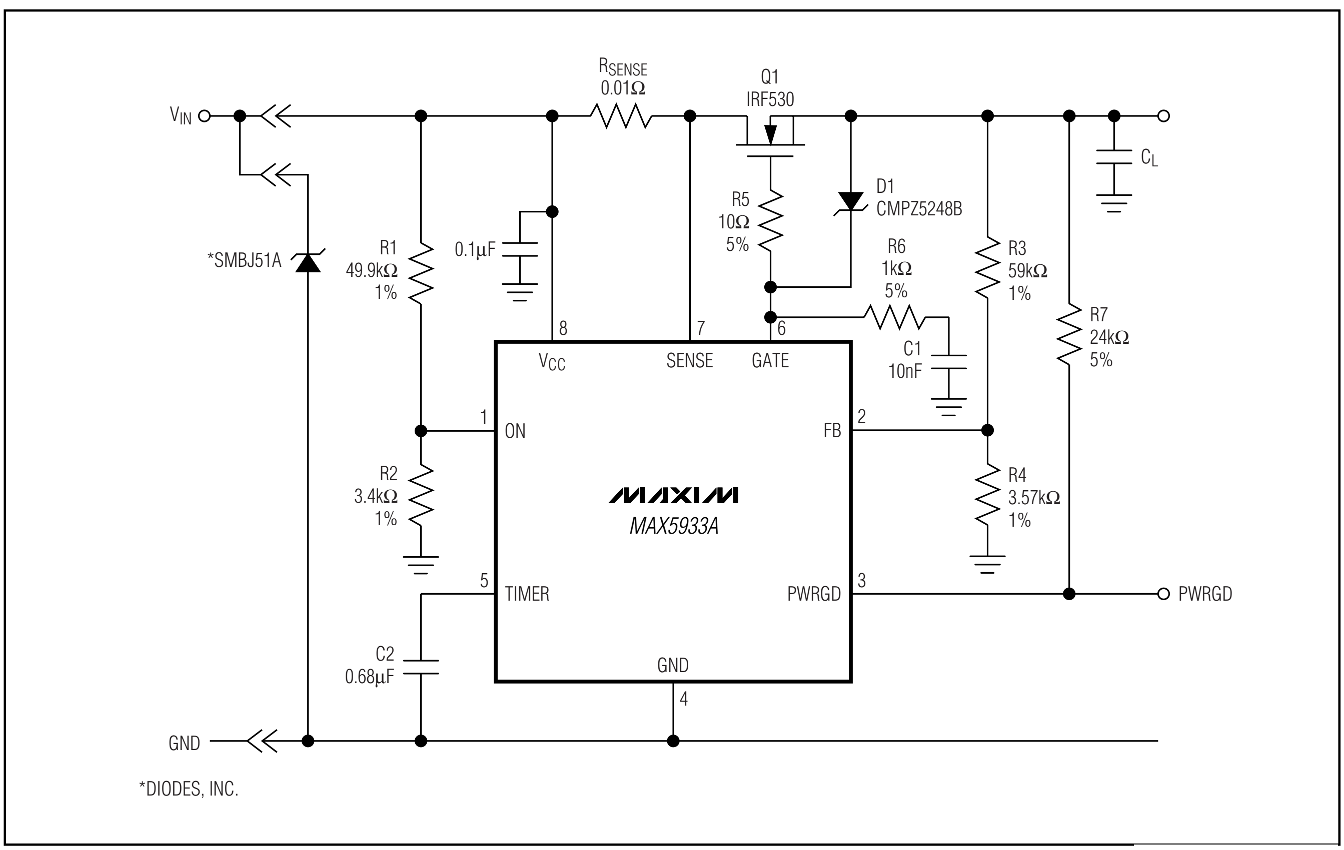
PROCESS: BiCMOS

Pin Configuration



( ) ONLY FOR THE MAX5933C/D/F/MAX5947A/MAX5947C.

Typical Application Circuit

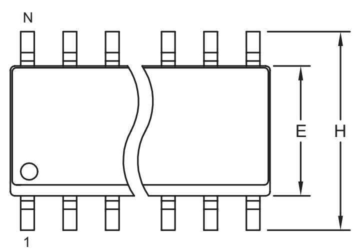


Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN.EPS

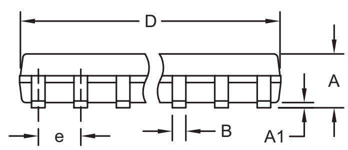
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



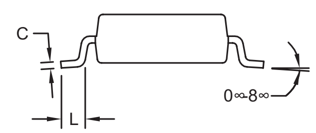
TOP VIEW

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1