19-3293; Rev. 2; 9/96

MAXIM

CMOS Monolithic Voltage Converter

General Description

The MAX660 monolithic, charge-pump voltage inverter converts a +1.5V to +5.5V input to a corresponding -1.5V to -5.5V output. Using only two low-cost capacitors, the charge pump's 100mA output replaces switching regulators, eliminating inductors and their associated cost, size, and EMI. Greater than 90% efficiency over most of its load-current range combined with a typical operating current of only 120µA provides ideal performance for both battery-powered and board-level voltage conversion applications. The MAX660 can also double the output voltage of an input power supply or battery, providing +9.35V at 100mA from a +5V input.

A frequency control (FC) pin selects either 10kHz typ or 80kHz typ (40kHz min) operation to optimize capacitor size and quiescent current. The oscillator frequency can also be adjusted with an external capacitor or driven with an external clock. The MAX660 is a pin-compatible, high-current upgrade of the ICL7660.

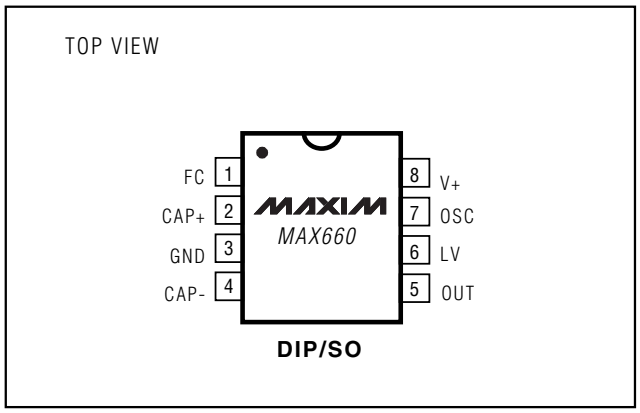
The MAX660 is available in both 8-pin DIP and small-outline packages in commercial, extended, and military temperature ranges.

For 50mA applications, consider the MAX860/MAX861 pin-compatible devices (also available in ultra-small µMAX packages).

Applications

Laptop Computers
Medical Instruments
Interface Power Supplies
Hand-Held Instruments
Operational-Amplifier Power Supplies

Pin Configuration



Features

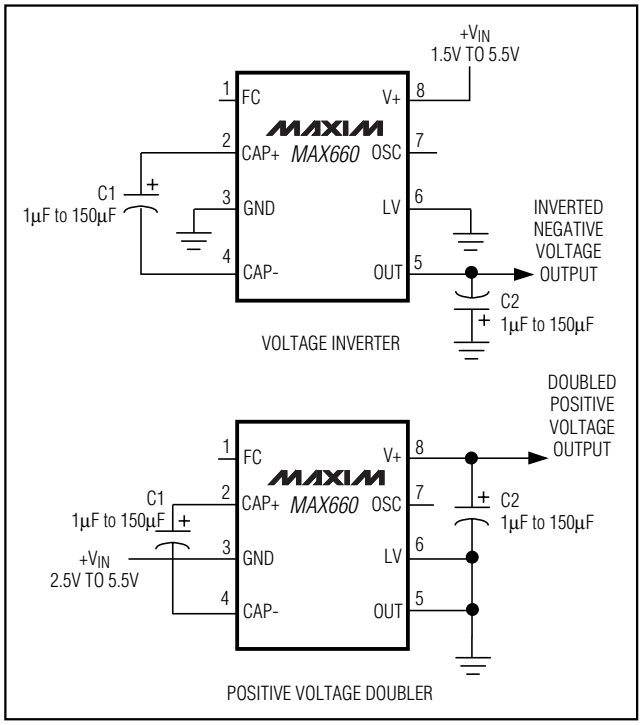
- **Small Capacitors**
- **0.65V Typ Loss at 100mA Load**
- **Low 120µA Operating Current**
- **6.5Ω Typ Output Impedance**
- **Guaranteed R_{OUT} < 15Ω for C1 = C2 = 10µF**
- **Pin-Compatible High-Current ICL7660 Upgrade**
- **Inverts or Doubles Input Supply Voltage**
- **Selectable Oscillator Frequency: 10kHz/80kHz**
- **88% Typ Conversion Efficiency at 100mA (I_L to GND)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX660CPA	0°C to +70°C	8 Plastic DIP
MAX660CSA	0°C to +70°C	8 SO
MAX660C/D	0°C to +70°C	Dice*
MAX660EPA	-40°C to +85°C	8 Plastic DIP
MAX660ESA	-40°C to +85°C	8 SO
MAX660MJA	-55°C to +125°C	8 CERDIP

**Contact factory for dice specifications.*

Typical Operating Circuits



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

CMOS Monolithic Voltage Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND, or GND to OUT) .....+6V
LV Input Voltage .....(OUT - 0.3V) to (V+ + 0.3V)
FC and OSC Input Voltages.....The least negative of (OUT - 0.3V) or (V+ - 6V) to (V+ + 0.3V)
OUT and V+ Continuous Output Current.....120mA
Output Short-Circuit Duration to GND (Note 1) 1sec
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above + 70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX660C_ _ .....0°C to +70°C
MAX660E_ _ .....-40°C to +85°C
MAX660MJA .....-55°C to +125°C
Storage Temperature Range..... -65°to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: OUT may be shorted to GND for 1sec without damage, but shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above +85°C, OUT must not be shorted to GND or V+, even instantaneously, or device damage may result.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, C1 = C2 = 150µF, test circuit of Figure 1, FC = open, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER			MIN	TYP	MAX	UNITS
Operating Supply Voltage	R_L = 1kΩ	Inverter, LV = open	3.0		5.5	V
		Inverter, LV = GND	1.5		5.5	
		Doubler, LV = OUT	2.5		5.5	
Supply Current	No load	FC = open, LV = open		0.12	0.5	mA
		FC = V+, LV = open		1	3	
Output Current	$T_A \le +85°C$, OUT more negative than -4V		100			mA
	$T_A > +85°C$, OUT more negative than -3.8V		100			
Output Resistance (Note 3)	I_L = 100mA	$T_A \le +85°C$, C1 = C2 = 10µF, FC = V+ (Note 4)			15	Ω
		$T_A \le +85°C$, C1 = C2 = 150µF		6.5	10.0	
		$T_A \le +85°C$			12	
Oscillator Frequency	FC = open		5	10		kHz
	FC = V+		40	80		
OSC Input Current	FC = open			±1		µA
	FC = V+			±8		
Power Efficiency	R_L = 1kΩ connected between V+ and OUT		96	98		%
	R_L = 500Ω connected between OUT and GND		92	96		
	I_L = 100mA to GND			88		
Voltage-Conversion Efficiency	No load		99.00	99.96		%

Note 2: In the test circuit, capacitors C1 and C2 are 150µF, 0.2Ω maximum ESR, aluminum electrolytics. Capacitors with higher ESR may reduce output voltage and efficiency. See *Capacitor Selection* section.
Note 3: Specified output resistance is a combination of internal switch resistance and capacitor ESR. See *Capacitor Selection* section.
Note 4: The ESR of C1 = C2 ≤ 0.5Ω. Guaranteed by correlation, not production tested.

Typical Operating Characteristics

All curves are generated using the test circuit of Figure 1 with V+ =5V, LV = GND, FC = open, and T_A = +25°C, unless otherwise noted. The charge-pump frequency is one-half the oscillator frequency. Test results are also valid for doubler mode with GND = +5V, LV = OUT, and OUT = 0V, unless otherwise noted; however, the input voltage is restricted to +2.5V to +5.5V.

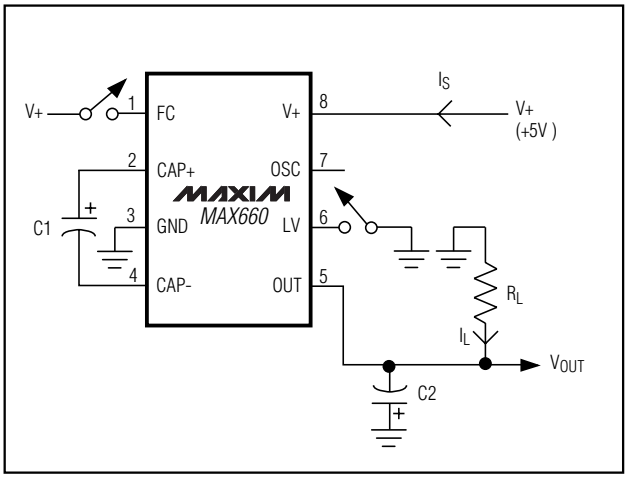
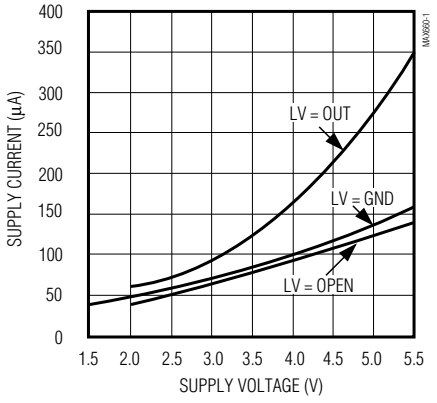
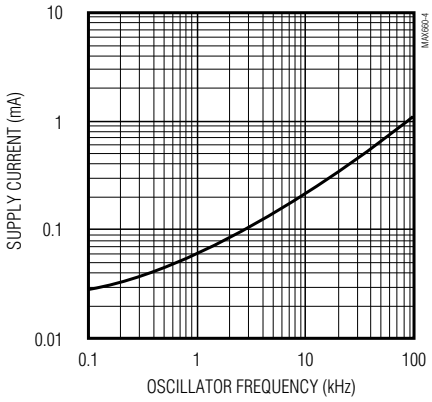


Figure 1. MAX660 Test Circuit

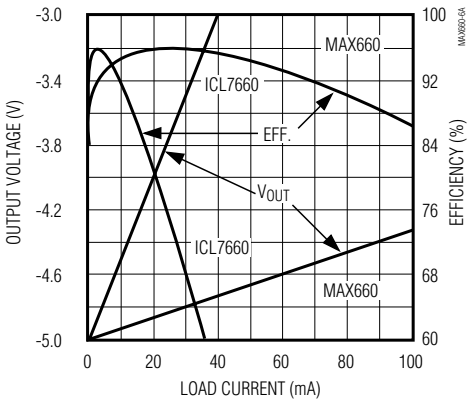
SUPPLY CURRENT vs. SUPPLY VOLTAGE



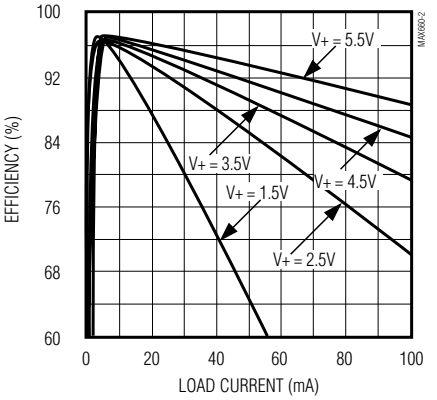
SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



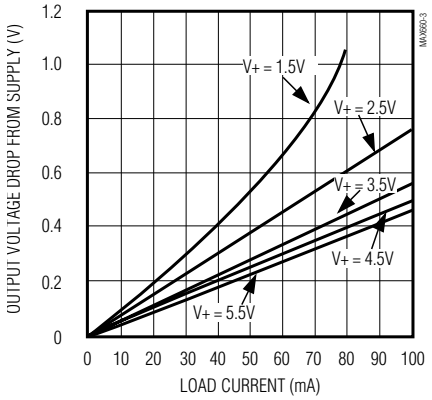
OUTPUT VOLTAGE AND EFFICIENCY vs. LOAD CURRENT, V+ = 5V



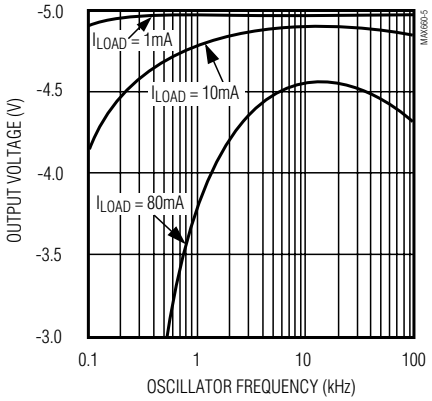
EFFICIENCY vs. LOAD CURRENT



OUTPUT VOLTAGE DROP vs. LOAD CURRENT



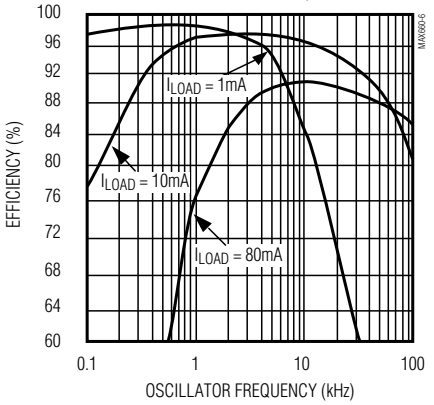
OUTPUT VOLTAGE vs. OSCILLATOR FREQUENCY



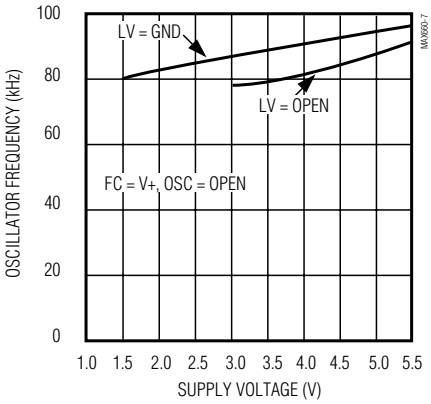
CMOS Monolithic Voltage Converter

Typical Operating Characteristics (continued)

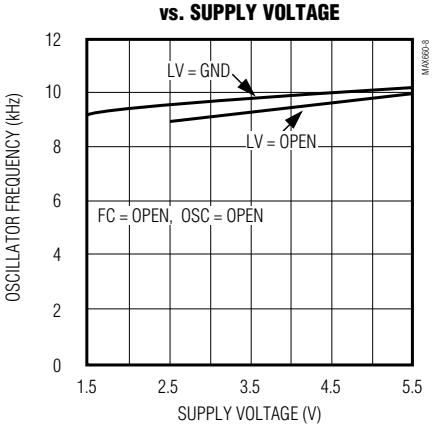
EFFICIENCY vs. OSCILLATOR FREQUENCY



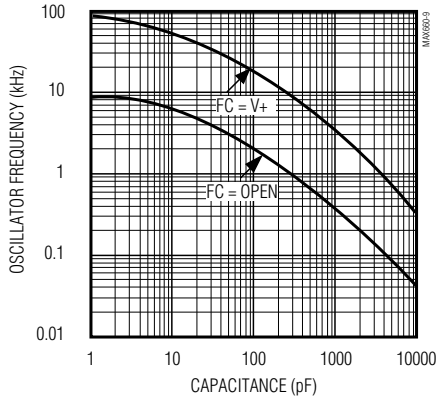
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



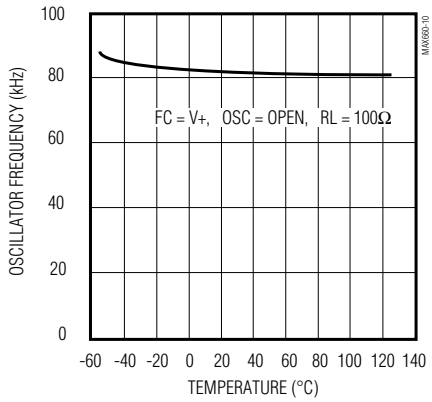
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



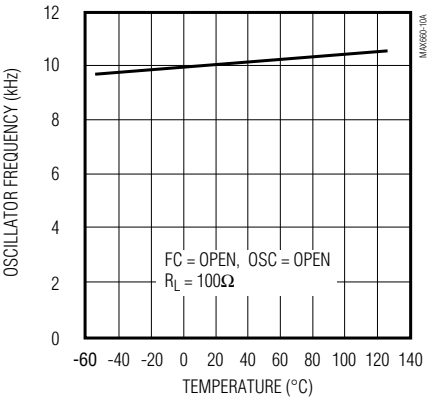
OSCILLATOR FREQUENCY vs. EXTERNAL CAPACITANCE



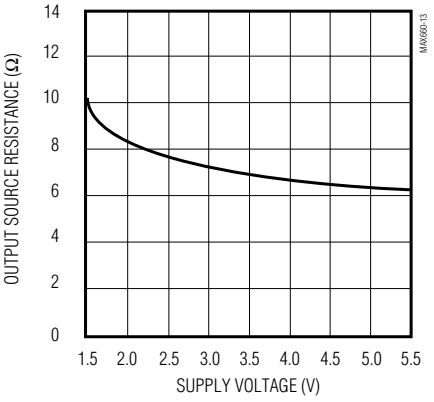
OSCILLATOR FREQUENCY vs. TEMPERATURE



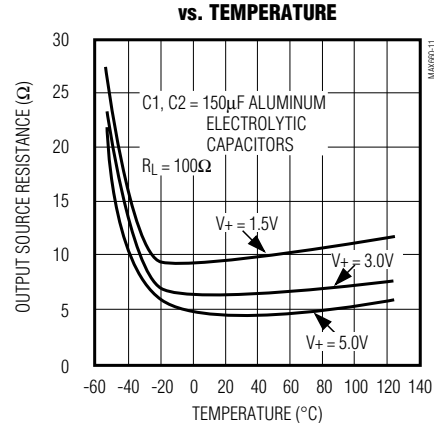
OSCILLATOR FREQUENCY vs. TEMPERATURE



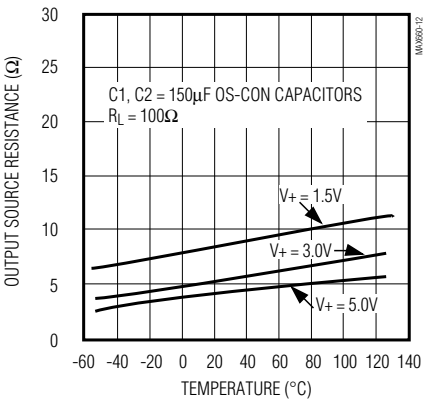
OUTPUT SOURCE RESISTANCE vs. SUPPLY VOLTAGE



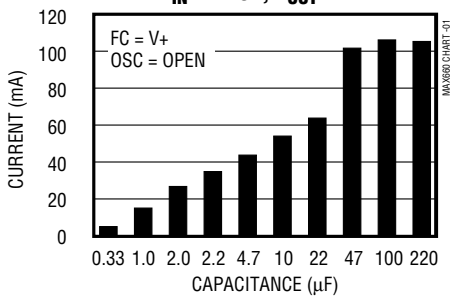
OUTPUT SOURCE RESISTANCE vs. TEMPERATURE



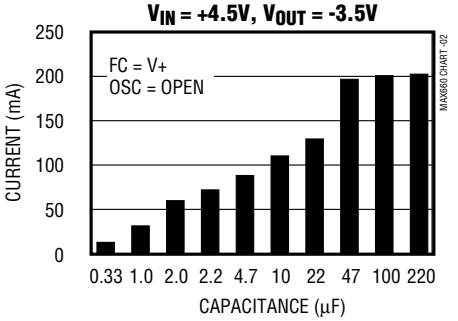
OUTPUT SOURCE RESISTANCE vs. TEMPERATURE



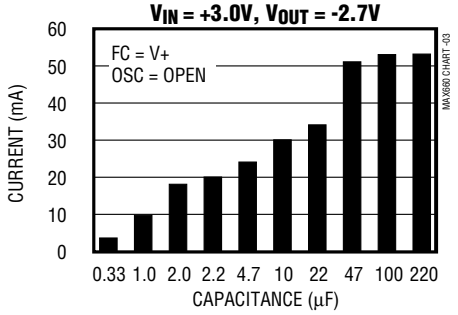
OUTPUT CURRENT vs. CAPACITANCE: V_{IN} = +4.5V, V_{OUT} = -4V



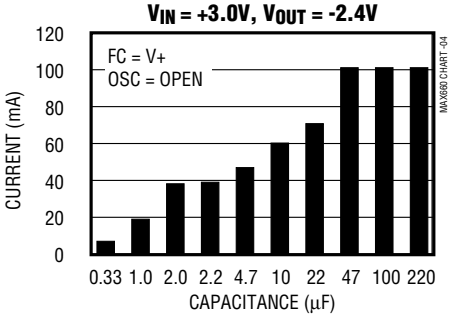
OUTPUT CURRENT vs. CAPACITANCE: V_{IN} = +4.5V, V_{OUT} = -3.5V



OUTPUT CURRENT vs. CAPACITANCE: V_{IN} = +3.0V, V_{OUT} = -2.7V



OUTPUT CURRENT vs. CAPACITANCE: V_{IN} = +3.0V, V_{OUT} = -2.4V



Pin Description

PIN	NAME	FUNCTION	
		INVERTER	DOUBLER
1	FC	Frequency Control for internal oscillator, FC = open, f_{OSC} = 10kHz typ; FC = V+, f_{OSC} = 80kHz typ (40kHz min), FC has no effect when OSC pin is driven externally.	Same as Inverter
2	CAP+	Charge-Pump Capacitor, Positive Terminal	Same as Inverter
3	GND	Power-Supply Ground Input	Power-Supply Positive Voltage Input
4	CAP-	Charge-Pump Capacitor, Negative Terminal	Same as Inverter
5	OUT	Output, Negative Voltage	Power-Supply Ground Input
6	LV	Low-Voltage Operation Input. Tie LV to GND when input voltage is less than 3V. Above 3V, LV may be connected to GND or left open; when overdriving OSC, LV must be connected to GND.	LV must be tied to OUT for all input voltages.
7	OSC	Oscillator Control Input. OSC is connected to an internal 15pF capacitor. An external capacitor can be added to slow the oscillator. Take care to minimize stray capacitance. An external oscillator may also be connected to overdrive OSC.	Same as Inverter; however, do not over-drive OSC in voltage-doubling mode.
8	V+	Power-Supply Positive Voltage Input	Positive Voltage Output

CMOS Monolithic Voltage Converter

Detailed Description

The MAX660 capacitive charge-pump circuit either inverts or doubles the input voltage (see *Typical Operating Circuits*). For highest performance, low effective series resistance (ESR) capacitors should be used. See *Capacitor Selection* section for more details.

When using the inverting mode with a supply voltage less than 3V, LV must be connected to GND. This bypasses the internal regulator circuitry and provides best performance in low-voltage applications. When using the inverter mode with a supply voltage above 3V, LV may be connected to GND or left open. The part is typically operated with LV grounded, but since LV may be left open, the substitution of the MAX660 for the ICL7660 is simplified. LV must be grounded when overdriving OSC (*see Changing Oscillator Frequency* section). Connect LV to OUT (for any supply voltage) when using the doubling mode.

Applications Information

Negative Voltage Converter

The most common application of the MAX660 is as a charge-pump voltage inverter. The operating circuit uses only two external capacitors, C1 and C2 (see *Typical Operating Circuits*).

Even though its output is not actively regulated, the MAX660 is very insensitive to load current changes. A typical output source resistance of 6.5Ω means that with an input of +5V the output voltage is -5V under light load, and decreases only to -4.35V with a load of 100mA. Output source resistance vs. temperature and supply voltage are shown in the *Typical Operating Characteristics* graphs.

Output ripple voltage is calculated by noting the output current supplied is solely from capacitor C2 during one-half of the charge-pump cycle. This introduces a peak-to-peak ripple of:

$$V_{RIPPLE} = \frac{I_{OUT}}{2(f_{PUMP})\,(C2)} + I_{OUT}\,(ESR_{C2})$$

For a nominal f_{PUMP} of 5kHz (one-half the nominal 10kHz oscillator frequency) and C2 = 150µF with an ESR of 0.2Ω, ripple is approximately 90mV with a 100mA load current. If C2 is raised to 390µF, the ripple drops to 45mV.

Positive Voltage Doubler

The MAX660 operates in the voltage-doubling mode as shown in the *Typical Operating Circuit.* The no-load output is 2 x V_{IN}.

Other Switched-Capacitor Converters

Please refer to Table 1, which shows Maxim's charge-pump offerings.

Changing Oscillator Frequency

Four modes control the MAX660's clock frequency, as listed below:

FC	OSC	Oscillator Frequency
Open	Open	10kHz
FC = V+	Open	80kHz
Open or FC = V+	External Capacitor	See *Typical Operating Characteristics*
Open	External Clock	External Clock Frequency

When FC and OSC are unconnected (open), the oscillator runs at 10kHz typically. When FC is connected to V+, the charge and discharge current at OSC changes from 1.0µA to 8.0µA, thus increasing the oscillator

Table 1. Single-Output Charge Pumps

	MAX828	MAX829	MAX860	MAX861	MAX660	MAX1044	ICL7662	ICL7660
Package	SOT 23-5	SOT 23-5	SO-8, µMAX	SO-8, µMAX	SO-8	SO-8, µMAX	SO-8	SO-8, µMAX
Op. Current (typ, mA)	0.06	0.15	0.2 at 6kHz, 0.6 at 50kHz, 1.4 at 130kHz	0.3 at 13kHz, 1.1 at 100kHz, 2.5 at 250kHz	0.12 at 5kHz, 1 at 40kHz	0.03	0.25	0.08
Output Ω (typ)	20	20	12	12	6.5	6.5	125	55
Pump Rate (kHz)	12	35	6, 50, 130	13, 100, 150	5, 40	5	10	10
Input (V)	1.25 to 5.5	1.25 to 5.5	1.5 to 5.5	1.5 to 5.5	1.5 to 5.5	1.5 to 10	1.5 to 10	1.5 to 10

frequency eight times. In the third mode, the oscillator frequency is lowered by connecting a capacitor between OSC and GND. FC can still multiply the frequency by eight times in this mode, but for a lower range of frequencies (see *Typical Operating Characteristics*).

In the inverter mode, OSC may also be overdriven by an external clock source that swings within 100mV of V+ and GND. Any standard CMOS logic output is suitable for driving OSC. When OSC is overdriven, FC has no effect. Also, LV must be grounded when overdriving OSC. Do not overdrive OSC in voltage-doubling mode.

Note: In all modes, the frequency of the signal appearing at CAP+ and CAP- is one-half that of the oscillator. Also, an undesirable effect of lowering the oscillator frequency is that the effective output resistance of the charge pump increases. This can be compensated by increasing the value of the charge-pump capacitors (see *Capacitor Selection* section and *Typical Operating Characteristics*).

In some applications, the 5kHz output ripple frequency may be low enough to interfere with other circuitry. If desired, the oscillator frequency can then be increased through use of the FC pin or an external oscillator as described above. The output ripple frequency is one-half the selected oscillator frequency. Increasing the clock frequency increases the MAX660's quiescent current, but also allows smaller capacitance values to be used for C1 and C2.

Capacitor Selection

Three factors (in addition to load current) affect the MAX660 output voltage drop from its ideal value:

1) MAX660 output resistance
2) Pump (C1) and reservoir (C2) capacitor ESRs
3) C1 and C2 capacitance

The voltage drop caused by MAX660 output resistance is the load current times the output resistance. Similarly, the loss in C2 is the load current times C2's ESR. The loss in C1, however, is larger because it handles currents that are greater than the load current during charge-pump operation. The voltage drop due to C1 is therefore about four times C1's ESR multiplied by the load current. Consequently, a low (or high) ESR capacitor has a much greater impact on performance for C1 than for C2.

Generally, as the pump frequency of the MAX660 increases, the capacitance values required to maintain comparable ripple and output resistance diminish proportionately. The curves of Figure 2 show the total circuit

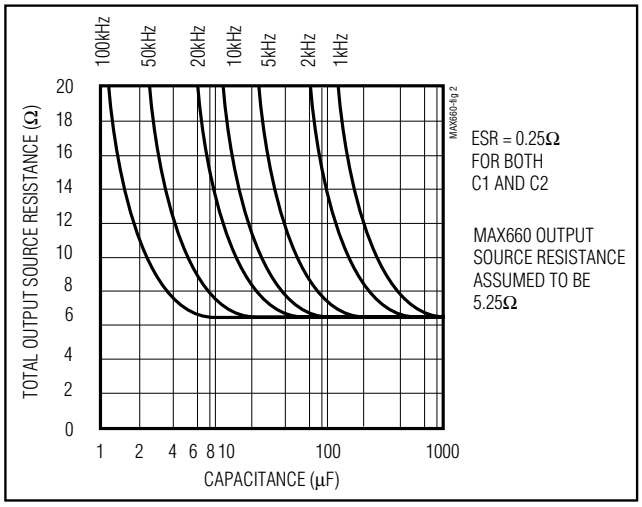


Figure 2. Total Output Source Resistance vs. C1 and C2 Capacitance (C1 = C2)

output resistance for various capacitor values (the pump and reservoir capacitors' values are equal) and oscillator frequencies. These curves assume 0.25Ω capacitor ESR and a 5.25Ω MAX660 output resistance, which is why the flat portion of the curve shows a 6.5Ω (R_O MAX660 + 4 (ESR_{C1}) + ESR_{C2}) effective output resistance. Note: R_O = 5.25Ω is used, rather than the typical 6.5Ω, because the typical specification includes the effect of the ESRs of the capacitors in the test circuit.

In addition to the curves in Figure 2, four bar graphs in the *Typical Operating Characteristics* show output current for capacitances ranging from 0.33µF to 220µF. Output current is plotted for inputs of 4.5V (5V-10%) and 3.0V (3.3V-10%), and allow for 10% and 20% output droop with each input voltage. As can be seen from the graphs, the MAX660 6.5Ω series resistance limits increases in output current vs. capacitance for values much above 47µF. Larger values may still be useful, however, to reduce ripple.

To reduce the output ripple caused by the charge pump, increase the reservoir capacitor C2 and/or reduce its ESR. Also, the reservoir capacitor must have low ESR if filtering high-frequency noise at the output is important.

Not all manufacturers guarantee capacitor ESR in the range required by the MAX660. In general, capacitor ESR is inversely proportional to physical size, so larger capacitance values and higher voltage ratings tend to reduce ESR.

CMOS Monolithic Voltage Converter

The following is a list of manufacturers who provide low-ESR electrolytic capacitors:

Manufacturer/ Series	Phone	Fax	Comments
AVX TPS Series	(803) 946-0690	(803) 626-3123	Low-ESR tantalum SMT
AVX TAG Series	(803) 946-0690	(803) 626-3123	Low-cost tantalum SMT
Matsuo 267 Series	(714) 969-2491	(714) 960-6492	Low-cost tantalum SMT
Sprague 595 Series	(603) 224-1961	(603) 224-1430	Aluminum electrolytic thru-hole
Sanyo MV-GX Series	(619) 661-6835	(619) 661-1055	Aluminum electrolytic SMT
Sanyo CV-GX Series	(619) 661-6835	(619) 661-1055	Aluminum electrolytic thru-hole
Nichicon PL Series	(847) 843-7500	(847) 843-2798	Low-ESR tantalum SMT
United Chemi-Con (Marcon)	(847) 696-2000	(847) 696-9278	Ceramic SMT
TDK	(847) 390-4373	(847) 390-4428	Ceramic SMT

Cascading Devices

To produce larger negative multiplication of the initial supply voltage, the MAX660 may be cascaded as shown in Figure 3. The resulting output resistance is approximately equal to the sum of the individual MAX660 R_{OUT} values. The output voltage, where n is an integer representing the number of devices cascaded, is defined by $V_{OUT} = -n\ (V_{IN})$.

Paralleling Devices

Paralleling multiple MAX660s reduces the output resistance. As illustrated in Figure 4, each device requires its own pump capacitor C1, but the reservoir capacitor C2 serves all devices. The value of C2 should be increased by a factor of n, where n is the number of devices. Figure 4 shows the equation for calculating output resistance.

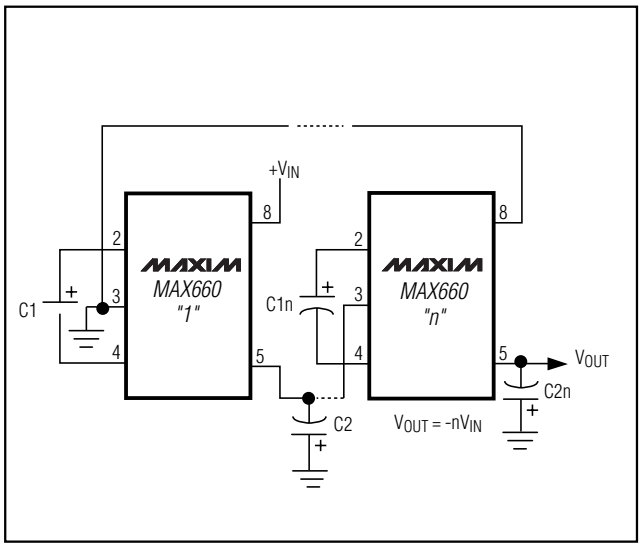


Figure 3. Cascading MAX660s to Increase Output Voltage

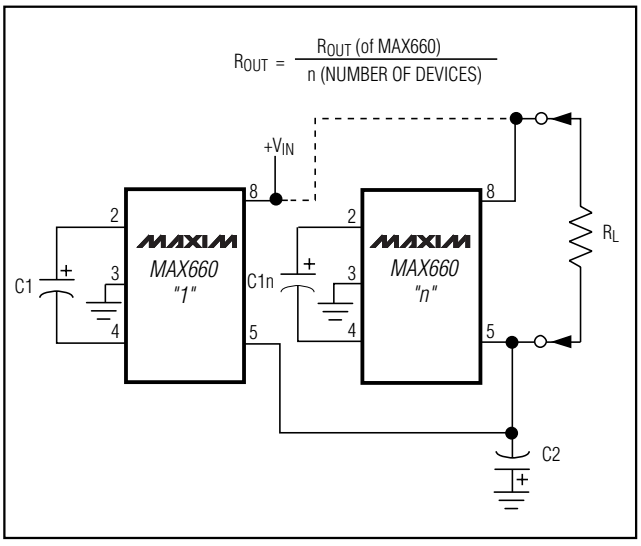


Figure 4. Paralleling MAX660s to Reduce Output Resistance

Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 5. In this circuit, capacitors C1 and C3 perform the pump and reservoir functions respectively for generation of the negative voltage. Capacitors C2 and C4 are respectively pump and reservoir for the multiplied positive voltage. This circuit configuration, however, leads to higher source impedances of the generated supplies. This is due to the finite impedance of the common charge-pump driver.

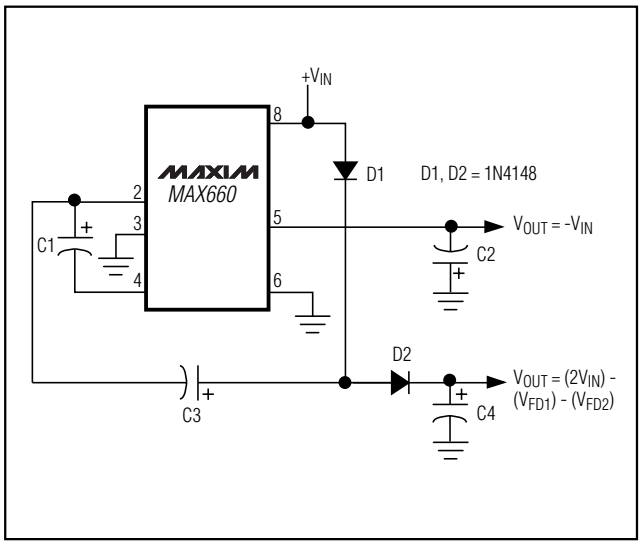


Figure 5. Combined Positive Multiplier and Negative Converter

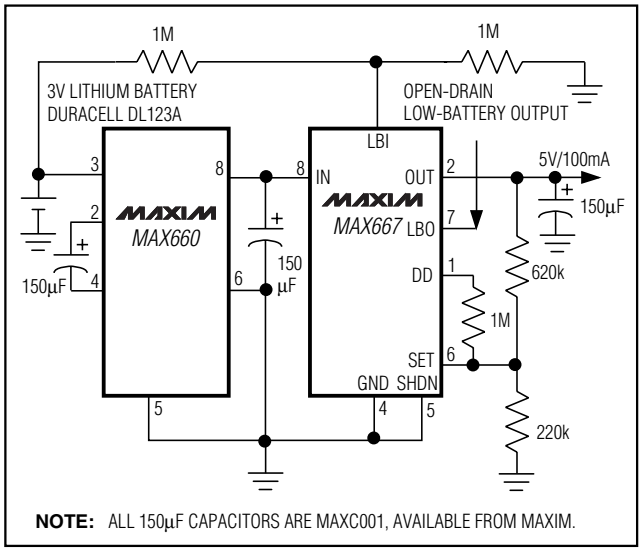
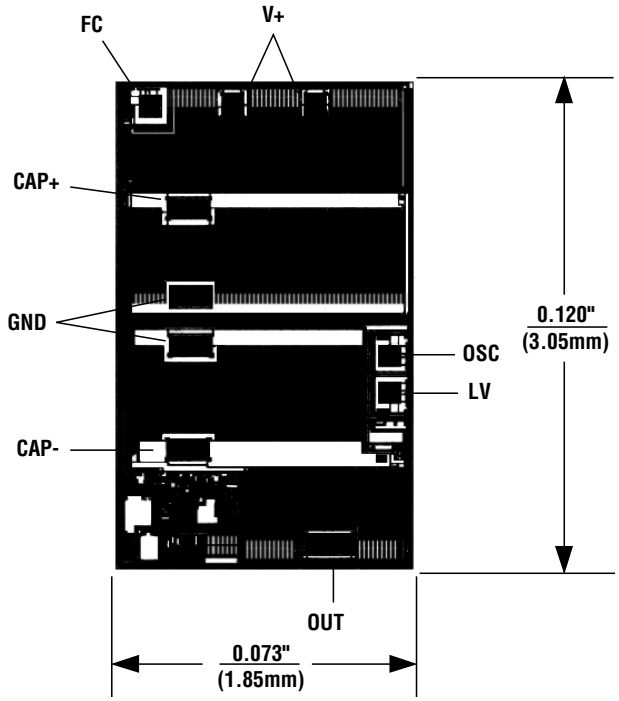


Figure 6. MAX660 generates a +5V regulated output from a 3V lithium battery and operates for 16 hours with a 40mA load.

CMOS Monolithic Voltage Converter

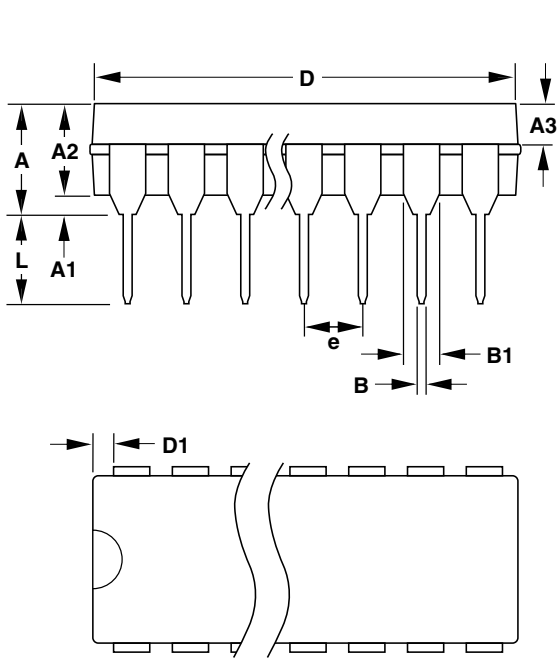
Chip Topography



TRANSISTOR COUNT = 89

SUBSTRATE CONNECTED TO V+.

Package Information

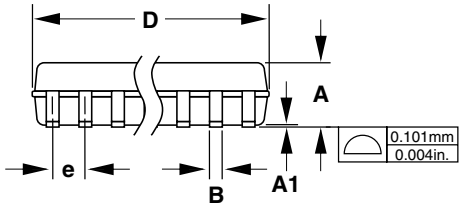


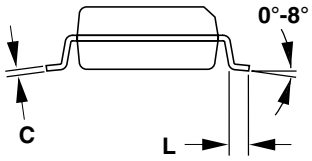
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

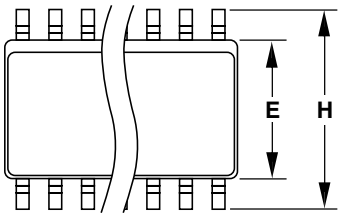
PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



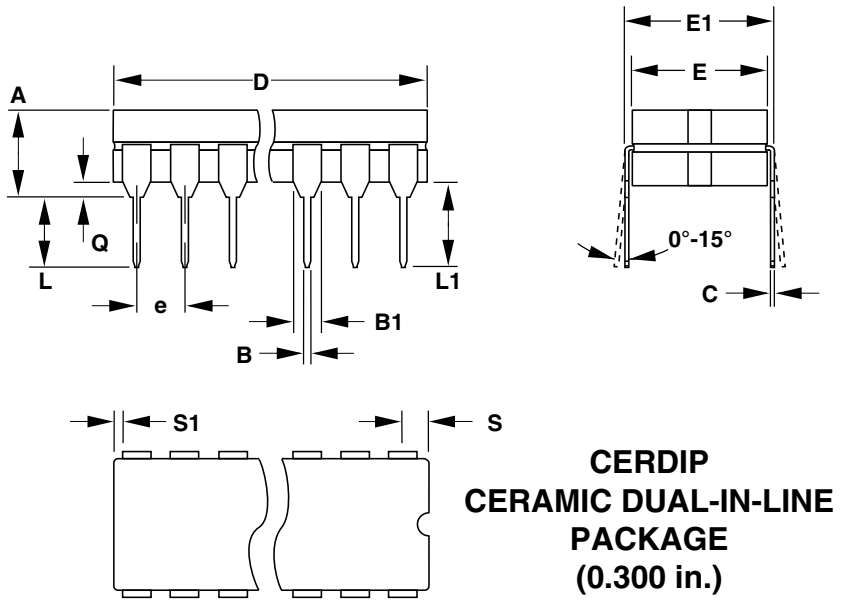
Narrow SO
SMALL-OUTLINE
PACKAGE
(0.150 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

CMOS Monolithic Voltage Converter

Package Information (continued)



CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0045A

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