

### **General Description**

The MAX6715-MAX6729 are ultra-low-voltage microprocessor (µP) supervisory circuits designed to monitor two or three system power-supply voltages. These devices assert a system reset if any monitored supply falls below its factorytrimmed or adjustable threshold and maintain reset for a minimum timeout period after all supplies rise above their thresholds. The integrated dual/triple supervisory circuits significantly improve system reliability and reduce size compared to separate ICs or discrete components.

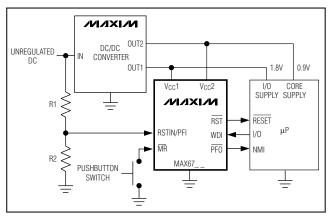
These devices monitor primary supply voltages (VCC1) from 1.8V to 5.0V and secondary supply voltages (VCC2) from 0.9V to 3.3V with factory-trimmed reset threshold voltage options (see Reset Voltage Threshold Suffix Guide). An externally adjustable RSTIN input option allows customers to monitor a third supply voltage down to 0.62V. These devices are guaranteed to be in the correct reset output logic state when either VCC1 or VCC2 remains greater than 0.8V.

A variety of push-pull or open-drain reset outputs along with watchdog input, manual reset input, and power-fail input/output features are available (see Selector Guide). Select reset timeout periods from 1.1ms to 1120ms (min) (see Reset Timeout Period Suffix Guide). The MAX6715-MAX6729 are available in small 5, 6, and 8-pin SOT23 packages and operate over the -40°C to +85°C temperature range.

### **Applications**

Multivoltage Systems Telecom/Networking Equipment Computers/Servers Portable/Battery-Operated Equipment Industrial Equipment Printer/Fax Set-Top Boxes

### **Typical Operating Circuit**



#### **Features**

- ♦ V<sub>CC</sub>1 (primary supply) Reset Threshold Voltages from 1.58V to 4.63V
- ♦ V<sub>CC</sub>2 (secondary supply) Reset Threshold Voltages from 0.79V to 3.08V
- ♦ Externally Adjustable RSTIN Threshold for Auxiliary/Triple-Voltage Monitoring (0.62V internal reference)
- Watchdog Timer Option 35s (min) Long Startup Period 1.12s (min) Normal Timeout Period
- **♦ Manual Reset Input Option**
- ♦ Power-Fail Input/Power-Fail Output Option (Push-Pull and Open-Drain Active-Low)
- ♦ Guaranteed Reset Valid Down to Vcc1 or  $V_{CC2} = 0.8V$
- **♦ Reset Output Logic Options**
- **♦ Immune to Short Vcc Transients**
- ♦ Low Supply Current 14µA (typ) at 3.6V
- ♦ Small 5, 6, and 8-Pin SOT23 Packages

### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX6715UTDT	-40°C to +85°C	6 SOT23-6
MAX6716UTDT	-40°C to +85°C	6 SOT23-6
MAX6717UKDT	-40°C to +85°C	5 SOT23-5
MAX6718UKDT	-40°C to +85°C	5 SOT23-5
MAX6719UTDT	-40°C to +85°C	6 SOT23-6
MAX6720UTDT	-40°C to +85°C	6 SOT23-6

**Note:** The first "\_\_" are placeholders for the threshold voltage levels of the devices. Desired threshold levels are set by the part number suffix found in the Reset Voltage Threshold Suffix Guide. The " " after the D is a placeholder for the reset timeout delay time. Desired delay time is set using the timeout period suffix found in the Reset Timeout Period Suffix Guide. For example the MAX6716UTLTD3-T is a dual-voltage supervisor  $V_{TH}1 = 4.625V$ , V<sub>TH</sub>2 = 3.075V, and 210ms (typ) timeout period.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Ordering Information continued at end of data sheet.

Pin Configurations and Selector Guide appear at end of data sheet.

NIXIN

Maxim Integrated Products 1

#### **ABSOLUTE MAXIMUM RATINGS**

Terminal Voltage (with respect to GND)	
V <sub>CC</sub> 1, V <sub>CC</sub> 2	
Open-Drain RST, RST1, RST2, PFO, RST	0.3V to +6V
Push-Pull RST, RST1, PFO, RST	$-0.3V$ to $(V_{CC}1 + 0.3V)$
Push-Pull RST2	$-0.3V$ to $(V_{CC}2 + 0.3V)$
RSTIN, PFI, MR, WDI	0.3V to +6V
Input Current/Output Current (all pins)	20mA

Continuous Power Dissipation ( $T_A = +70$ °C)	
5-Pin SOT23-5 (derate 7.1mW/°C above +70°C) .	571mW
6-Pin SOT23-6 (derate 8.7mW/°C above +70°C) .	696mW
8-Pin SOT23-8 (derate 8.9mW/°C above +70°C).	714mW
Operating Temperature Range40°	°C to +85°C
Storage Temperature Range65°C	C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC}1 = V_{CC}2 = 0.8V \text{ to } 5.5V, \text{GND} = 0, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 1)

PARAMETER	SYMBOL	OL CONDITIONS		TYP	MAX	UNITS			
Supply Voltage	Vcc		0.8		5.5	V			
	1004	V <sub>CC</sub> 1 < 5.5V, all I/O pins open		15	39	_			
Supply Current	ICC1	V <sub>CC</sub> 1 < 3.6V, all I/O pins open		10	28				
Supply Current	loos	V <sub>CC</sub> 2 < 3.6V, all I/O pins open		4	11	- μΑ			
	I <sub>CC2</sub>	$V_{\rm CC}$ 2 < 2.75V, all I/O pins open		3	9				
		L (falling)	4.500	4.625	4.750				
		M (falling)	4.250	4.375	4.500				
		T (falling)	3.000	3.075	3.150				
		S (falling)	2.850	2.925	3.000				
V <sub>CC</sub> 1 Reset Threshold	V <sub>TH1</sub>	R (falling)	2.550	2.625	2.700	V			
		Z (falling)	2.250	2.313	2.375				
		Y (falling)	2.125	2.188	2.250				
		W (falling)	1.620	1.665	1.710				
		V (falling)	1.530	1.575	1.620				
		T (falling)	3.000	3.075	3.150				
		S (falling)	2.850	2.925	3.000				
		R (falling)	2.550	2.625	2.700	- - -			
		Z (falling)	2.250	2.313	2.375				
		Y (falling)	2.125	2.188	2.250				
		W (falling)	1.620	1.665	1.710				
V <sub>CC</sub> 2 Reset Threshold	V <sub>TH2</sub>	V (falling)	1.530	1.575	1.620	V			
		I (falling)	1.350	1.388	1.425				
		H (falling)	1.275	1.313	1.350				
		G (falling)	1.080	1.110	1.140				
		F (falling)	1.020	1.050	1.080	1			
		E (falling)	0.810	0.833	0.855				
		D (falling)	0.765	0.788	0.810	1			
Reset Threshold Tempco				20		ppm/°C			
Reset Threshold Hysteresis	V <sub>H</sub> YST	Referenced to V <sub>TH</sub> typical		0.5		%			

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC}1 = V_{CC}2 = 0.8V \text{ to } 5.5V, \text{ GND} = 0, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$  Typical values are at  $T_A = +25^{\circ}\text{C}.)$  (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>CC</sub> to Reset Output Delay	t <sub>RD</sub>	V <sub>CC</sub> 1 = (V <sub>TH</sub> 1 + 100mV) to (V <sub>TH</sub> 1 - 100mV) or V <sub>CC</sub> 2 = (V <sub>TH</sub> 2 + 75mV) to (V <sub>TH</sub> 2 - 75mV)		20		μs
		D1	1.1	1.65	2.2	
		D2	8.8	13.2	17.6	
Donat Timesout Dovied		D3	140	210	280	
Reset Timeout Period	t <sub>RP</sub>	D5	280	420	560	ms
		D6	560	840	1120	
		D4	1120	1680	2240	
ADJUSTABLE RESET COMPA	RATOR INPU	T (MAX6719/MAX6720/MAX6723-MAX6727)				
RSTIN Input Threshold	V <sub>RSTIN</sub>		611	626.5	642	mV
RSTIN Input Current	IRSTIN		-25		+25	nA
RSTIN Hysteresis				3		mV
RSTIN to Reset Output Delay	trstind	V <sub>RSTIN</sub> to (V <sub>RSTIN</sub> - 30mV)		22		μs
POWER-FAIL INPUT (MAX6728	B/MAX6729)		•			•
PFI Input Threshold	VPFI		611	626.5	642	mV
PFI Input Current	I <sub>PFI</sub>		-25		+25	nA
PFI Hysteresis	VpfH			3		mV
PFI to PFO Delay	tDPF	(V <sub>PFI</sub> + 30mV) to (V <sub>PFI</sub> - 30mV)		2		μs
MANUAL RESET INPUT (MAXE	6715-MAX672	2/MAX6725-MAX6729)				
MR Input Voltage	VIL			0.3	$3 \times V_{CC}1$	V
wh input voitage	VIH		$0.7 \times V_{\rm C}$	C1		V
MR Minimum Pulse Width			1			μs
MR Glitch Rejection				100		ns
MR to Reset Delay	t <sub>MR</sub>			200		ns
MR Pullup Resistance			25	50	80	kΩ
WATCHDOG INPUT (MAX6721	-MAX6729)					
Watchdog Timeout Period	t <sub>WD</sub>	First watchdog period after reset timeout period	35	54	72	S
		Normal mode	1.12	1.68	2.24	
WDI Pulse Width	twDI	(Note 2)	50			ns
WDI Input Voltoco	VIL			0.3	$3 \times V_{CC1}$	V
WDI Input Voltage	VIH		$0.7 \times V_{\rm C}$	C1		V
WDI Input Current	IwDI	WDI = 0 or V <sub>CC</sub> 1	-1		+1	μΑ

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC}1 = V_{CC}2 = 0.8V \text{ to } 5.5V, \text{ GND} = 0, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 1)

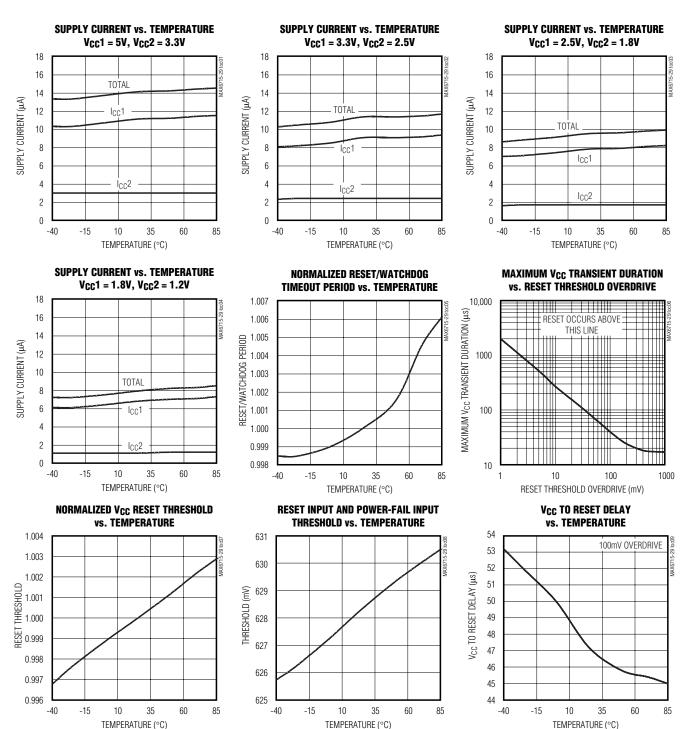
PARAMETER	SYMBOL	CONDITIONS	MIN T	YP MAX	UNITS
RESET/POWER-FAIL OUTPUTS	3		•		
		V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 0.8V, I <sub>SINK</sub> = 1μA, output asserted		0.3	
		V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 1.0V, I <sub>SINK</sub> = 50µA, output asserted		0.3	
RST/RST1/RST2/PFO Output LOW (Push-Pull or Open-Drain)	V <sub>OL</sub>	V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 1.2V, I <sub>SINK</sub> = 100μA, output asserted		0.3	V
(i dan-i dii di Operi-Diairi)		V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 2.7V, I <sub>SINK</sub> = 1.2mA, output asserted		0.3	
		V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 4.5V, I <sub>SINK</sub> = 3.2mA, output asserted		0.4	
		V <sub>CC</sub> 1 ≥ 1.8V, I <sub>SOURCE</sub> = 200μA, output not asserted	0.8 × V <sub>CC</sub> 1		
RST/RST1/PFO Output HIGH (Push-Pull Only)	VoH	V <sub>CC</sub> 1 ≥ 2.7V, I <sub>SOURCE</sub> = 500μA, output not asserted	0.8 × V <sub>CC</sub> 1	V	
(Pusri-Puli Only)		V <sub>CC</sub> 1 ≥ 4.5V, I <sub>SOURCE</sub> = 800µA, output not asserted	0.8 × V <sub>CC</sub> 1		
		V <sub>CC</sub> 2 ≥ 1.8V, I <sub>SOURCE</sub> = 200μA, output not asserted	0.8 × V <sub>CC</sub> 2		
RST2 Output HIGH (Push-Pull Only)	VoH	V <sub>CC</sub> 2 ≥ 2.7V, I <sub>SOURCE</sub> = 500μA, output not asserted	0.8 × V <sub>CC</sub> 2	V	
(Lagir all Grilly)		V <sub>CC</sub> 2 ≥ 4.5V, I <sub>SOURCE</sub> = 800µA, output not asserted	0.8 × V <sub>CC</sub> 2		
		V <sub>CC</sub> 1 ≥ 1.0V, I <sub>SOURCE</sub> = 1μA, reset asserted	0.8 × V <sub>CC</sub> 1		
RST		V <sub>CC</sub> 1 ≥ 1.8V, I <sub>SOURCE</sub> = 150μA, reset asserted	0.8 × V <sub>CC</sub> 1		
Output HIGH (Push-Pull Only)	Voh	V <sub>CC</sub> 1 ≥ 2.7V, I <sub>SOURCE</sub> = 500μA, reset asserted	0.8 × V <sub>CC</sub> 1		V
		V <sub>CC</sub> 1 ≥ 4.5V, I <sub>SOURCE</sub> = 800μA, reset asserted	0.8 × V <sub>CC</sub> 1		
		V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 1.8V, I <sub>SINK</sub> = 500μA, reset not asserted		0.3	
RST Output LOW (Push-Pull or Open Drain)	V <sub>OL</sub>	V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 2.7V, I <sub>SINK</sub> = 1.2mA, reset not asserted	0.3		V
(i dair i dii di Operi Diairi)		V <sub>CC</sub> 1 or V <sub>CC</sub> 2 ≥ 4.5V, I <sub>SINK</sub> = 3.2mA, reset not asserted		0.4	
RST/RST1/RST2/PFO Output Open-Drain Leakage Current		Output not asserted		0.5	μΑ
RST Output Open-Drain Leakage Current		Output asserted		0.5	μА

Note 1: Devices tested at +25°C. Overtemperature limits are guaranteed by design and not production tested.

Note 2: Parameter guaranteed by design.

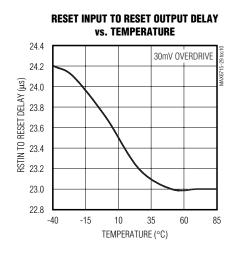
### Typical Operating Characteristics

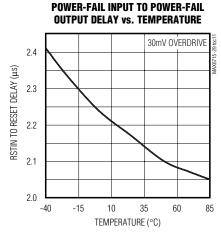
 $(V_{CC}1 = 5V, V_{CC}2 = 3.3V, T_A = +25^{\circ}C, unless otherwise noted.)$ 

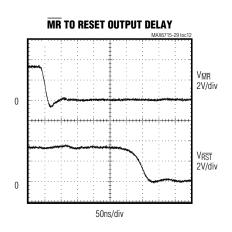


### Typical Operating Characteristics (continued)

 $(V_{CC}1 = 5V, V_{CC}2 = 3.3V, T_A = +25^{\circ}C, unless otherwise noted.)$ 







### **Pin Description**

	PIN								
MAX6715/ MAX6716	MAX6717/ MAX6718	MAX6719/ MAX6720	MAX6721/ MAX6722	MAX6723/ MAX6724	MAX6725/ MAX6726	MAX6727	MAX6728/ MAX6729	NAME	FUNCTION
1	1	1	1	1	1	1, 4	1	RST/ RST1	Active-Low Reset Output, Open-Drain or Push-Pull. RST/RST1 changes from high to low when V <sub>CC</sub> 1 or V <sub>CC</sub> 2 drops below the selected reset thresholds, RSTIN is below threshold, MR is pulled low, or the watchdog triggers a reset. RST/RST1 remains low for the reset timeout period after V <sub>CC</sub> 1/V <sub>CC</sub> 2/RSTIN exceed the device reset thresholds, MR goes low to high, or the watchdog triggers a reset. Open-drain outputs require an external pullup resistor. Push-pull outputs are referenced to V <sub>CC</sub> 1.

## Pin Description (continued)

MAX6715/ MAX6716	MAX6717/ MAX6718	MAX6719/ MAX6720	MAX6721/ MAX6722	MAX6723/ MAX6724	MAX6725/ MAX6726	MAX6727	MAX6728/ MAX6729	NAME	FUNCTION
5							_	RST2	Active-Low Reset Output, Open-Drain or Push-Pull. RST2 changes from high to low when V <sub>CC</sub> 1 or V <sub>CC</sub> 2 drops below the selected reset thresholds or MR is pulled low. RST2 remains low for the reset timeout period after V <sub>CC</sub> 1/V <sub>CC</sub> 2 exceed the device reset thresholds or MR goes low to high. Open-drain outputs require an external pullup resistor. Push-pull outputs are referenced to V <sub>CC</sub> 2.
2	2	2	2	2	2	2	2	GND	Ground
3	3	3	3	_	5	5	5	MR	Active-Low Manual Reset Input. Internal 50kΩ pullup to V <sub>CC</sub> 1. Pull low to force a reset. Reset remains active as long as MR is low and for the reset timeout period after MR goes high. Leave unconnected or connect to V <sub>CC</sub> 1 if unused.
4	4	4	4	4	6	6	6	V <sub>CC</sub> 2	Secondary Supply Voltage Input. Powers the device when it is above V <sub>CC</sub> 1 and input for secondary reset threshold monitor.
6	5	6	6	6	8	8	8	V <sub>CC</sub> 1	Primary Supply Voltage Input. Powers the device when it is above V <sub>CC</sub> 2 and input for primary reset threshold monitor.

## Pin Description (continued)

			P	IN					
MAX6715/ MAX6716	MAX6717/ MAX6718	MAX6719/ MAX6720	MAX6721/ MAX6722	MAX6723/ MAX6724	MAX6725/ MAX6726	MAX6727	MAX6728/ MAX6729	NAME	FUNCTION
			5	3	3	3	3	WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and the reset output asserts for the reset timeout period. The internal watchdog timer clears whenever a reset is asserted or WDI sees a rising or falling edge. The watchdog has a long timeout period (35s min) after each reset event and a short timeout period (1.12s min) after the first valid WDI transition.
_	_	5	_	5	7	7	_	RSTIN	Undervoltage Reset Comparator Input. High- impedance input for adjustable reset monitor. The reset output is asserted when RSTIN falls below the 0.626V internal reference voltage. Set the monitored voltage reset threshold with an external resistor-divider network. Connect RSTIN to V <sub>CC</sub> 1 or V <sub>CC</sub> 2 if not used.
_	_	_	_	_	_	_	7	PFI	Power-Fail Voltage Monitor Input. High- impedance input for internal power-fail monitor comparator. Connect PFI to an external resistor- divider network to set the power-fail threshold voltage (0.626V typical internal reference voltage). Connect to GND, V <sub>CC</sub> 1, or V <sub>CC</sub> 2 if not used.

### Pin Description (continued)

	PIN									
MAX6715/ MAX6716	MAX6717/ MAX6718	MAX6719/ MAX6720	MAX6721/ MAX6722	MAX6723/ MAX6724	MAX6725/ MAX6726	MAX6727	MAX6728/ MAX6729	NAME	FUNCTION	
_			_	_			4	PFO	Active-Low Power-Fail Monitor Output, Open- Drain or Push-Pull. PFO is asserted low when PFI is less than 0.626V. PFO deasserts without a reset timeout period. Open- drain outputs require an external pullup resistor. Push-pull outputs are referenced to VCC1.	
					4			RST	Active-High Reset Output, Open-Drain or Push-Pull. RST changes from low to high when VCC1 or VCC2 drops below selected reset thresholds, RSTIN is below threshold, MR is pulled low, or the watchdog triggers a reset. RST remains HIGH for the reset timeout period after VCC1/ VCC 2/RSTIN exceed the device reset thresholds, MR goes low to high, or the watchdog triggers a reset. Open-drain outputs require an external pullup resistor. Push-pull outputs are referenced to VCC1.	

### **Detailed Description**

#### **Supply Voltages**

The MAX6715–MAX6729 microprocessor ( $\mu P$ ) supervisory circuits maintain system integrity by alerting the  $\mu P$  to fault conditions. These ICs are optimized for systems that monitor two or three supply voltages. The outputreset state is guaranteed to remain valid while either VCC1 or VCC2 is above 0.8V.

#### **Threshold Levels**

Input voltage threshold level combinations are indicated by a two-letter code in the *Reset Voltage Threshold* 

Suffix Guide (Table 1). Contact factory for availability of other voltage threshold combinations.

#### **Reset Outputs**

The MAX6715–MAX6729 provides an active-low reset output (RST) and the MAX6725/MAX6726 provides both an active-high (RST) and an active-low reset output (RST). RST, RST, RST1, and RST2 are asserted when the voltage at either VCC1 or VCC2 falls below the voltage threshold level, RSTIN drops below threshold, or MR is pulled low. Once reset is asserted it stays low for the reset timeout period (see Table 2). If VCC1, VCC2, or RSTIN goes below the reset threshold before the reset timeout period is completed, the internal timer

restarts. The MAX6715/MAX6717/MAX6719/MAX6721/MAX6723/MAX6725/MAX6727/MAX6728 contain opendrain reset outputs, while the MAX6716/MAX6718/MAX6720/MAX6722/MAX6724/MAX6726/MAX6729 contain push-pull reset outputs. The MAX6727 provides two separate open-drain  $\overline{RST}$  outputs driven by the same internal logic.

#### Manual Reset Input

Many microprocessor-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on  $\overline{\text{MR}}$  asserts the reset output. Reset remains asserted while  $\overline{\text{MR}}$  is low and for the reset timeout period (tRP) after  $\overline{\text{MR}}$  returns high. This input has an internal 50k $\Omega$  pullup resistor to VCC1 and can be left unconnected if not used.  $\overline{\text{MR}}$  can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{\text{MR}}$  to GND to create a manual reset function; external debounce circuitry is not required. If  $\overline{\text{MR}}$  is driven from long cables or if the device is used in a noisy environment, connect a 0.1 $\mu$ F capacitor from  $\overline{\text{MR}}$  to GND to provide additional noise immunity.

#### Adjustable Input Voltage

The MAX6719/MAX6720 and MAX6723–MAX6727 provide an additional input to monitor a third system voltage. The threshold voltage at RSTIN is typically 626mV. Connect a resistor-divider network to the circuit as shown in Figure 1 to establish an externally controlled threshold voltage, VEXT\_TH.

$$V_{EXT\_TH} = 626 \text{mV}((R1 + R2)/R2)$$

Low leakage current at RSTIN allows the use of largevalued resistors resulting in reduced power consumption of the system.

#### **Watchdog Input**

The watchdog monitors  $\mu P$  activity through the watchdog input (WDI). To use the watchdog function, connect WDI to a bus line or  $\mu P$  I/O line. When WDI remains high or low for longer than the watchdog timeout period, the reset output asserts.

The MAX6721–MAX6729 include a dual-mode watch-dog timer to monitor  $\mu P$  activity. The flexible timeout architecture provides a long period initial watchdog mode, allowing complicated systems to complete lengthy boots, and a short period normal watchdog mode, allowing the supervisor to provide quick alerts

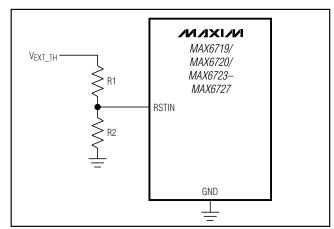


Figure 1. Monitoring a Third Voltage

when processor activity fails. After each reset event (V<sub>CC</sub> power-up/brownout, manual reset, or watchdog reset), there is a long initial watchdog period of 35s minimum. The long watchdog period mode provides an extended time for the system to power-up and fully initialize all  $\mu$ P and system components before assuming responsibility for routine watchdog updates.

The normal watchdog timeout period (1.12s min) begins after the first transition on WDI before the conclusion of the long initial watchdog period (Figure 2). During the normal operating mode, the supervisor will issue a reset pulse for the reset timeout period if the  $\mu P$  does not update the WDI with a valid transition (high-to-low or low-to-high) within the standard timeout period (1.12s min).

#### **Power-Fail Comparator**

PFI is the noninverting input to a comparator. If PFI is less than V<sub>PFI</sub> (626.5mV), PFO goes low. Common uses for the power-fail comparator include monitoring preregulated input of the power supply (such as a battery) or

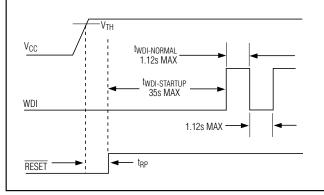


Figure 2. Normal Watchdog Startup Sequence

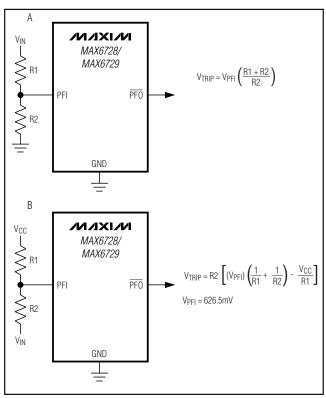


Figure 3. Using Power-Fail Input to Monitor an Additional Power-Supply a)  $V_{IN}$  is Positive b)  $V_{IN}$  is Negative

providing an early power-fail warning so software can conduct an orderly system shutdown. It can also be used to monitor supplies other than VCC1 or VCC2 by setting the power-fail threshold with a resistor-divider, as shown in Figure 3. PFI is the input to the power-fail comparator. The typical comparator delay is 2µs from PFI to PFO. Connect PFI to ground of VCC1 if unused.

# Ensuring a Valid Reset Output Down to VCC = 0

The MAX6715–MAX6729 are guaranteed to operate properly down to V<sub>CC</sub> = 0.8V. In applications that require valid reset levels down to V<sub>CC</sub> = 0 use a pull-down resistor at  $\overline{RST}$  to ground. The resistor value used is not critical, but it must be large enough not to load the reset output when V<sub>CC</sub> is above the reset threshold. For most applications,  $100 k\Omega$  is adequate. This configuration does not work for the open-drain outputs of the MAX6715/MAX6717/MAX6719/MAX6721/MAX6723/MAX6725/MAX6727/MAX6728. For push-pull, active-high RST output connect the external resistor as a pullup from RST to V<sub>CC</sub>1.

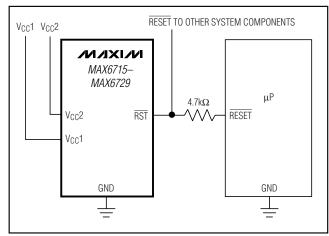


Figure 4. Interfacing to µPs with Bidirectional Reset I/O

### Applications Information

# Interfacing to µPs with Bidirectional Reset Pins

Most microprocessors with bidirectional reset pins can interface directly to open-drain  $\overline{RST}$  output options. Systems simultaneously requiring a push-pull  $\overline{RST}$  output and a bidirectional reset interface can be in logic contention. To prevent contention, connect a  $4.7k\Omega$  resistor between  $\overline{RST}$  and the  $\mu P$ 's reset I/O port as shown in Figure 4.

# Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 3mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage-divider (see the *Power-Fail Comparator* section). If additional noise margin is desired, connect a resistor between PFO and PFI as shown in Figure 5. Select the values of R1, R2, and R3 so PFI sees VPFI (626mV) when VEXT falls to its power-fail trip point (VFAIL) and when VIN rises to its power-good trip point (VGOOD). The hysteresis window extends between the specified VFAIL and VGOOD thresholds. R3 adds the additional hysteresis by sinking current from the R1/R2 divider network when PFO is logic low and sourcing current into the network when PFO is logic high. R3 is typically an order of magnitude greater than R1 or R2.

The current through R2 should be at least 2.5 $\mu$ A to ensure that the 25nA (max) PFI input current does not significantly shift the trip points. Therefore, R2 < V<sub>PFI</sub>/2.5 $\mu$ A < 248k $\Omega$  for most applications. R3 will provide additional hysteresis for PFO push-pull (V<sub>OH</sub> = V<sub>CC</sub>1) or open-drain (V<sub>OH</sub> = V<sub>PULLUP</sub>) applications.

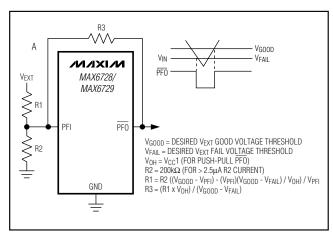


Figure 5. Adding Hysteresis to Power-Fail for Push-Pull PFO

#### **Monitoring an Additional Power Supply**

These  $\mu P$  supervisors can monitor either positive or negative supplies using a resistor voltage-divider to PFI. PFO can be used to generate an interrupt to the  $\mu P$  or cause reset to assert (Figure 3).

#### Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit shown in Figure 3. When the negative supply is valid, PFO is low. When the negative supply voltage drops, PFO goes high. The circuit's accuracy is affected by the PFI threshold tolerance, VCC, R1, and R2.

#### **Negative-Going Vcc Transients**

The MAX6715-MAX6729 supervisors are relatively immune to short-duration negative-going VCC transients (glitches). It is usually undesirable to reset the µP when VCC experiences only small glitches. The Typical Operating Characteristics show Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going V<sub>CC</sub> pulses, starting above V<sub>TH</sub> and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going VCC transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold). the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to the VCC pin provides additional transient immunity.

#### **Watchdog Software Considerations**

Setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low, helps the

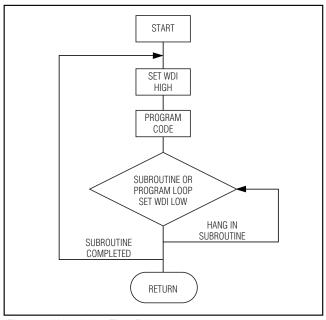


Figure 6. Watchdog Flow Diagram

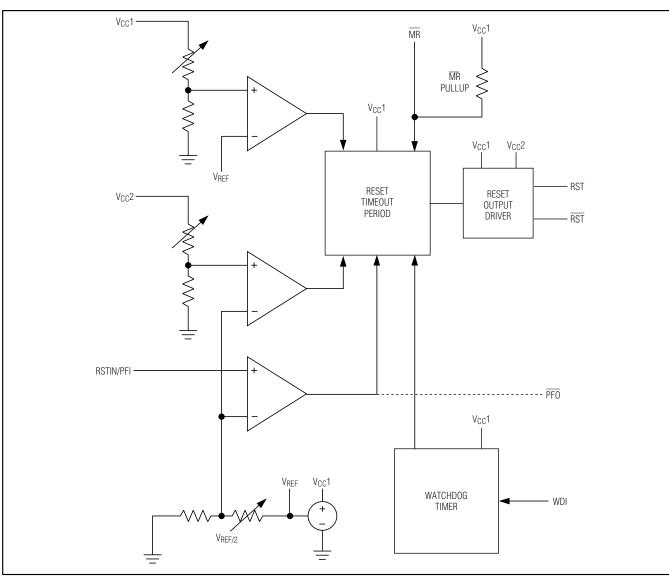
watchdog timer to closely monitor software execution. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out. Figure 6 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

**Chip Information** 

**TRANSISTOR COUNT: 1072** 

PROCESS: BICMOS

### **Functional Diagram**



#### **Selector Guide**

PART NUMBER	NUMBER OF VOLTAGE MONITORS	OPEN- DRAIN RESET	OPEN- DRAIN RESET	PUSH- PULL RESET	PUSH- PULL RESET	MANUAL RESET	WATCH- DOG INPUT	POWER- FAIL INPUT/ OUTPUT
MAX6715	2	2	_	_	_	√	_	_
MAX6716	2	_	_	2	_	√	_	_
MAX6717	2	1	_	_	_	√	_	_
MAX6718	2	_	_	1	_	$\sqrt{}$	_	_
MAX6719	3	1	_	_	_	$\sqrt{}$	_	_
MAX6720	3	_	_	1		$\sqrt{}$	_	_
MAX6721	2	1	_	_	_	$\sqrt{}$	√	_
MAX6722	2	_	_	1	_	$\sqrt{}$	√	_
MAX6723	3	1	_			_	√	_
MAX6724	3	_	_	1	_	_	$\sqrt{}$	
MAX6725	3	1	1	_	_	$\sqrt{}$	$\sqrt{}$	_
MAX6726	3	_	_	1	1	$\sqrt{}$	√	_
MAX6727	3	2	_	_	_	$\sqrt{}$	√	
MAX6728	3	1	_		_	√	√	√ (open drain)
MAX6729	3	_	_	1	_	$\sqrt{}$	√	√ (push-pull)

### Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX6721UTDT	-40°C to +85°C	6 SOT23-6
MAX6722UTDT	-40°C to +85°C	6 SOT23-6
MAX6723UTDT	-40°C to +85°C	6 SOT23-6
MAX6724UTDT	-40°C to +85°C	6 SOT23-6
<b>MAX6725</b> KADT	-40°C to +85°C	8 SOT23-8
MAX6726KADT	-40°C to +85°C	8 SOT23-8
MAX6727KADT	-40°C to +85°C	8 SOT23-8
MAX6728KADT	-40°C to +85°C	8 SOT23-8
MAX6729KADT	-40°C to +85°C	8 SOT23-8

**Note:** The first "\_\_" are placeholders for the threshold voltage levels of the devices. Desired threshold levels are set by the part number suffix found in the Reset Voltage Threshold Suffix Guide. The "\_" after the D is a placeholder for the reset timeout delay time. Desired delay time is set using the timeout period suffix found in the Reset Timeout Period Suffix Guide. For example the MAX6716UTLTD3-T is a dual-voltage supervisor  $V_{TH1} = 4.625V$ ,  $V_{TH2} = 3.075V$ , and 210ms (typ) timeout period.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Table 1. Reset Voltage Threshold Suffix Guide\*\*

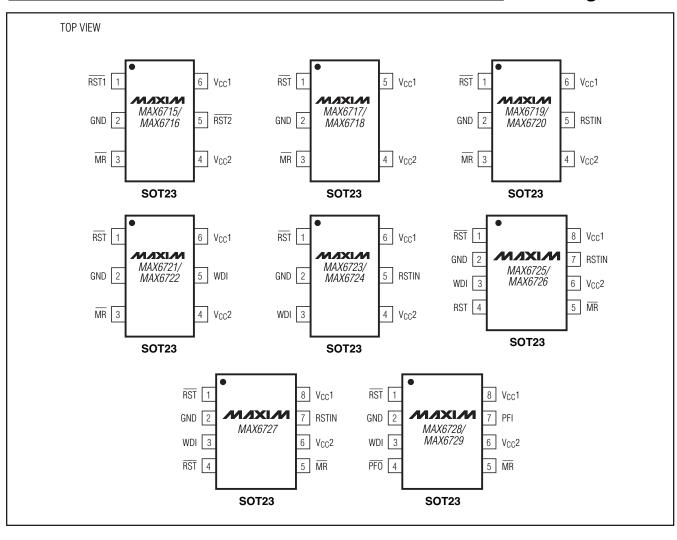
PART NUMBER SUFFIX ()	V <sub>CC</sub> 1 NOMINAL VOLTAGE THRESHOLD (V)	V <sub>CC</sub> 2 NOMINAL VOLTAGE THRESHOLD (V)
LT	4.625	3.075
MS	4.375	2.925
MR	4.375	2.625
TZ	3.075	2.313
SY	2.925	2.188
RY	2.625	2.188
TW	3.075	1.665
sv	2.925	1.575
RV	2.625	1.575
TI	3.075	1.388
SH	2.925	1.313
RH	2.625	1.313
TG	3.075	1.110
SF	2.925	1.050
RF	2.625	1.050
TE	3.075	0.833
SD	2.925	0.788
RD	2.625	0.788
ZW	2.313	1.665
YV	2.188	1.575
ZI	2.313	1.388
YH	2.188	1.313
ZG	2.313	1.110
YF	2.188	1.050
ZE	2.313	0.833
YD	2.188	0.788
WI	1.665	1.388
VH	1.575	1.313
WG	1.665	1.110
VF	1.575	1.050
WE	1.665	0.833
VD	1.575	0.788

<sup>\*\*</sup>Standard versions are shown in bold and are available in a D3 timeout option only. Standard versions require 2,500 piece order increments and are typically held in sample stock. There is a 10,000 order increment on nonstandard versions. Other threshold voltages may be available, contact factory for availability.

**Table 2. Reset Timeout Period Suffix Guide** 

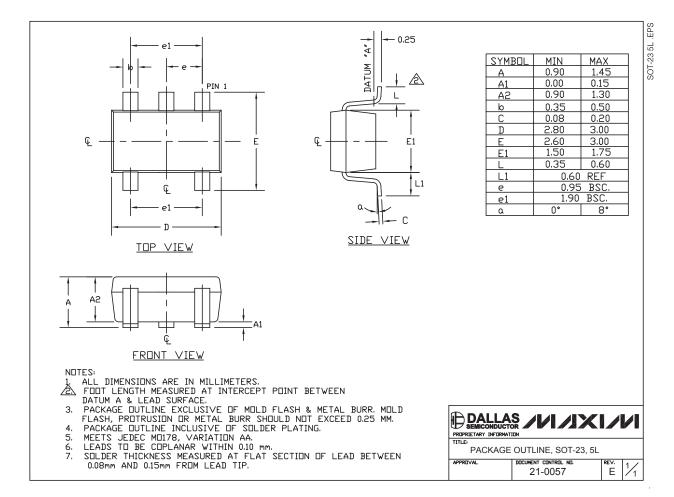
TIMEOUT	ACTIVE TIMEOUT PERIOD	
PERIOD SUFFIX	MIN [ms]	MAX [ms]
D1	1.1	2.2
D2	8.8	17.6
D3	140	280
D5	280	560
D6	560	1120
D4	1120	2240

### **Pin Configurations**



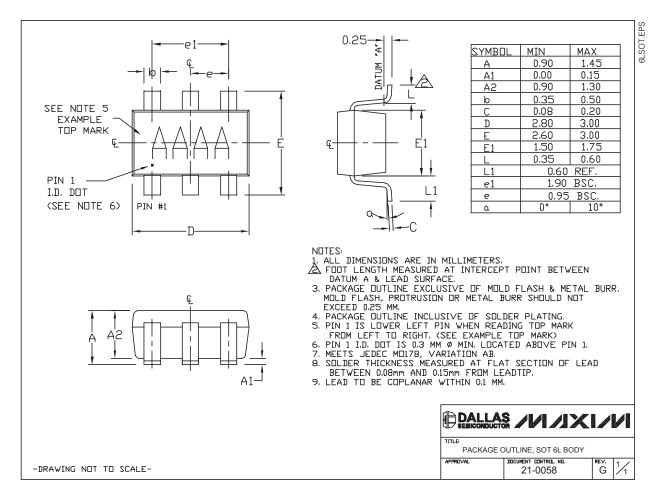
### **Package Information**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>.)



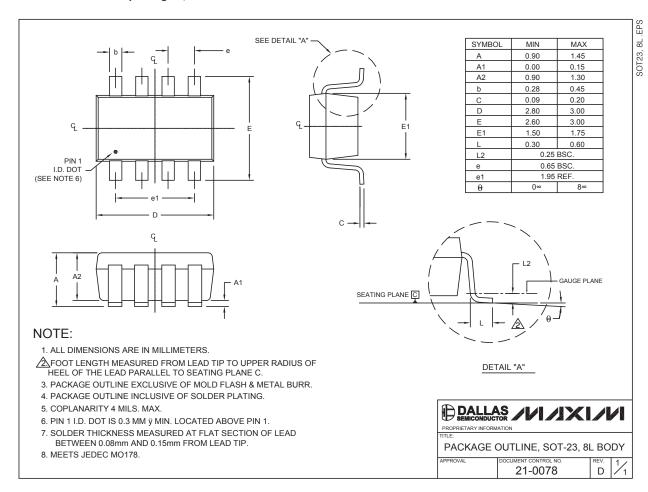
### Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>.)



### **Package Information (continued)**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <a href="https://www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>.)



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