MAX6956 2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port LED Display Driver and I/O Expander

General Description

The MAX6956 compact, serial-interfaced LED display driver/I/O expander provide microprocessors with up to 28 ports. Each port is individually user configurable to either a logic input, logic output, or common-anode (CA) LED constant-current segment driver. Each port configured as an LED segment driver behaves as a digitally controlled constant-current sink, with 16 equal current steps from 1.5mA to 24mA. The LED drivers are suitable for both discrete LEDs and CA numeric and alphanumeric LED digits.

Each port configured as a general-purpose I/O (GPIO) can be either a push-pull logic output capable of sinking 10mA and sourcing 4.5mA, or a Schmitt logic input with optional internal pullup. Seven ports feature configurable transition detection logic, which generates an interrupt upon change of port logic level. The MAX6956 is controlled through an I²C-compatible 2-wire serial interface, and uses four-level logic to allow 16 I²C addresses from only 2 select pins.

The MAX6956AAX and MAX6956ATL have 28 ports and are available in 36-pin SSOP and 40-pin thin QFN packages, respectively. The MAX6956AAI and MAX6956ANI have 20 ports and are available in 28-pin SSOP and 28-pin DIP packages, respectively.

For an SPI-interfaced version, refer to the MAX6957 data sheet. For a lower cost pin-compatible port expander without the constant-current LED drive capability, refer to the MAX7300 data sheet.

Applications

- Set-Top Boxes
- Panel Meters
- White Goods
- Automotive
- Bar Graph Displays
- Industrial Controllers
- System Monitoring

Typical Operating Circuit appears at end of data sheet.

Features

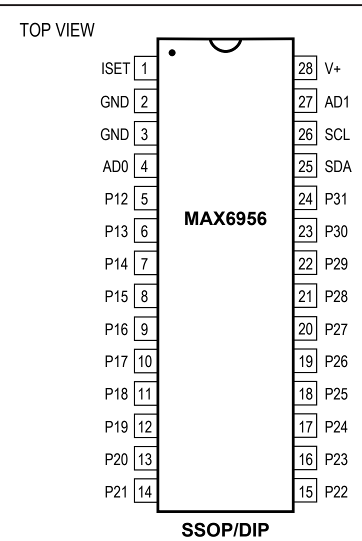
- 400kbps I²C-Compatible Serial Interface
- 2.5V to 5.5V Operation
- -40°C to +125°C Temperature Range
- 20 or 28 I/O Ports, Each Configurable as
  - Constant-Current LED Driver
  - Push-Pull Logic Output
  - Schmitt Logic Input
  - Schmitt Logic Input with Internal Pullup
- 11µA (max) Shutdown Current
- 16-Step Individually Programmable Current Control for Each LED
- Logic Transition Detection for Seven I/O Ports

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6956ANI+	-40°C to +125°C	28 DIP
MAX6956AAI+	-40°C to +125°C	28 SSOP
MAX6956AAX+	-40°C to +125°C	36 SSOP
MAX6956ATL+	-40°C to +125°C	40 Thin QFN-EP*
MAX6956AAX/V	-40°C to +125°C	36 SSOP
MAX6956AAX/V+T	-40°C to +125°C	36 SSOP

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Pin Configurations



Pin Configurations continued at end of data sheet.

Absolute Maximum Ratings

Voltage (with Respect to GND)
V+ ....-0.3V to +6V
SCL, SDA, AD0, AD1 ....0.3V to +6V
All Other Pins ....-0.3V to (V+ + 0.3V)
P4–P31 Current...±30mA
GND Current 800mA
Continuous Power Dissipation
28-Pin PDIP (derate 14.3mW/°C above T_A = +70°C) ... 1143mW
28-Pin SSOP (derate 9.1mW/°C above T_A = +70°C)......727mW
36-Pin SSOP (derate 11.8mW/°C above T_A = +70°C)....941mW
40-Pin TQFN (derate 26.3mW/°C above T_A = +70°C)..2105mW
Operating Temperature Range
(T_{MIN} to T_{MAX}) .... -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow)
Lead(Pb)-free packages ....+260°C
Packages containing lead(Pb)..................................+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Typical Operating Circuit, V+ = 2.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.5		5.5	V
Shutdown Supply Current	I_{SHDN}	All digital inputs at V+ or GND	T_A = +25°C		5.5	8	µA
			T_A = -40°C to +85°C			10	
			T_A = T_{MIN} to T_{MAX}			11	
Operating Supply Current	I_{GPOH}	All ports programmed as outputs high, no load, all other inputs at V+ or GND	T_A = +25°C		180	230	µA
			T_A = -40°C to +85°C			250	
			T_A = T_{MIN} to T_{MAX}			270	
Operating Supply Current	I_{GPOL}	All ports programmed as outputs low, no load, all other inputs at V+ or GND	T_A = +25°C		170	210	µA
			T_A = -40°C to +85°C			230	
			T_A = T_{MIN} to T_{MAX}			240	
Operating Supply Current	I_{LED}	All ports programmed as LED outputs, all LEDs off, no load, all other inputs at V+ or GND	T_A = +25°C		110	135	µA
			T_A = -40°C to +85°C			140	
			T_A = T_{MIN} to T_{MAX}			145	
INPUTS AND OUTPUTS							
Logic-High Input Voltage Port Inputs	V_{IH}			0.7 x V+			V
Logic-Low Input Voltage Port Inputs	V_{IL}					0.3 x V+	V
Input Leakage Current	I_{IH}, I_{IL}	GPIO inputs without pullup, V_{PORT} = V+ to GND		-100	±1	+100	nA
GPIO Input Internal Pullup to V+	I_{PU}	V+ = 2.5V		12	19	30	µA
		V+ = 5.5V		80	120	180	
Hysteresis Voltage GPIO Inputs	ΔV_I				0.3		V
Output High Voltage	V_{OH}	GPIO outputs, I_{SOURCE} = 2mA, T_A = -40°C to +85°C		V+ - 0.7			V
		GPIO outputs, I_{SOURCE} = 1mA, T_A = T_{MIN} to T_{MAX} (Note 2)		V+ - 0.7			
Port Sink Current	I_{OL}	V_{PORT} = 0.6V		2	10	18	mA
Output Short-Circuit Current	I_{OLSC}	Port configured output low, shorted to V+		2.75	11	20	mA

Electrical Characteristics (continued)

(Typical Operating Circuit, V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Drive LED Sink Current, Port Configured as LED Driver	I_{DIGIT}	V+ = 2.5V, V_{LED} = 2.3V at maximum LED current	9.5	13.5	18	mA
		V+ = 3.3V, V_{LED} = 2.4V at maximum LED current (Note 2)	18.5	24	27.5	
		V+ = 5.5V, V_{LED} = 2.4V at maximum LED current	19	25	30	
Port Drive Logic Sink Current, Port Configured as LED Driver	I_{DIGIT_SC}	V+ = 2.5V, V_{OUT} = 0.6V at maximum sink current	18.5	23	28	mA
		V+ = 5.5V, V_{OUT} = 0.6V at maximum sink current	19	24	28	
Input High-Voltage SDA, SCL, AD0, AD1	V_{IH}		0.7 x V+			V
Input Low-Voltage SDA, SCL, AD0, AD1	V_{IL}				0.3 x V+	V
Input Leakage Current SDA, SCL	I_{IH}, I_{IL}		-50		50	nA
Input Capacitance		(Note 2)			10	pF
Output Low-Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.4	V

Timing Characteristics (Figure 2)

(V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

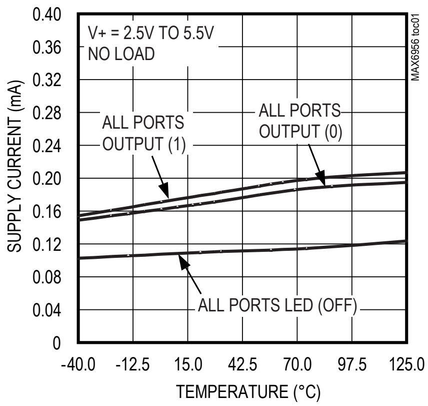
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 3)	15		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 2, 4)		20 + $0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 2, 4)		20 + $0.1C_b$	300	ns
Fall Time of SDA Transmitting	$t_{F,TX}$	(Notes 2, 5)		20 + $0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 2, 6)	0		50	ns
Capacitive Load for Each Bus Line	C_b	(Note 2)			400	pF

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 5: I_{SINK} ≤ 6mA. C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 6: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

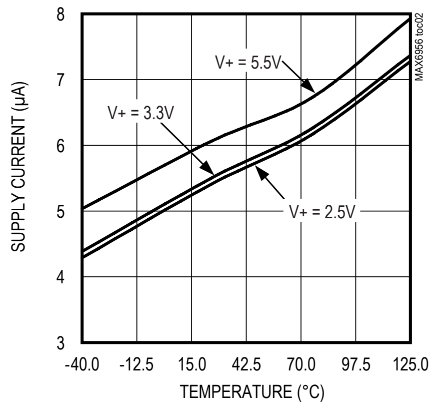
Typical Operating Characteristics

(R_{ISET} = 39kΩ, T_A = +25°C, unless otherwise noted.)

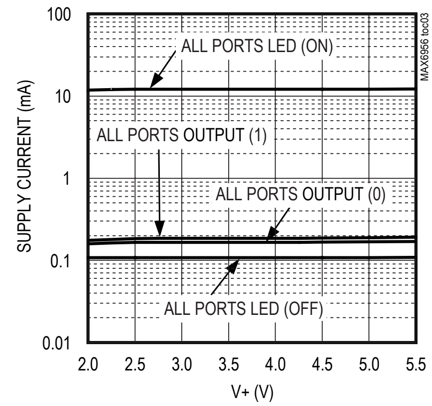
OPERATING SUPPLY CURRENT vs. TEMPERATURE



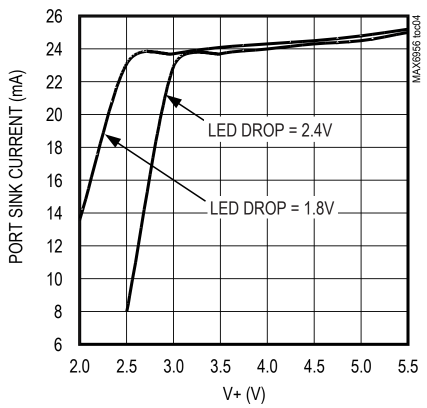
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



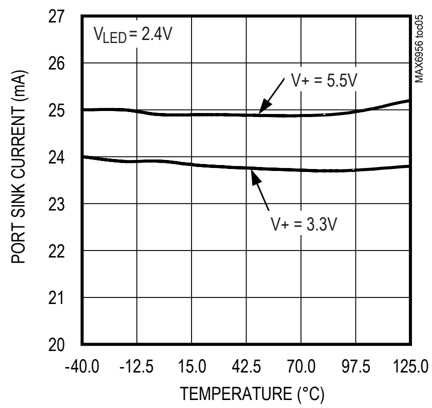
OPERATING SUPPLY CURRENT vs. V+ (NO LOADS)



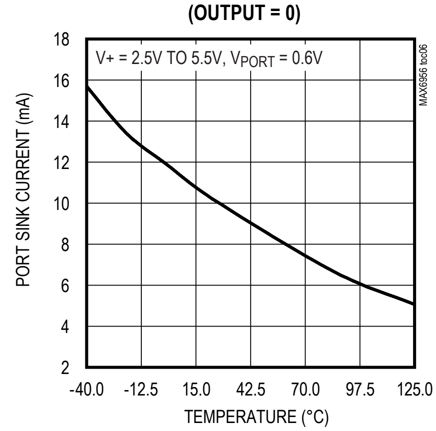
LED DRIVER SINK CURRENT vs. V+



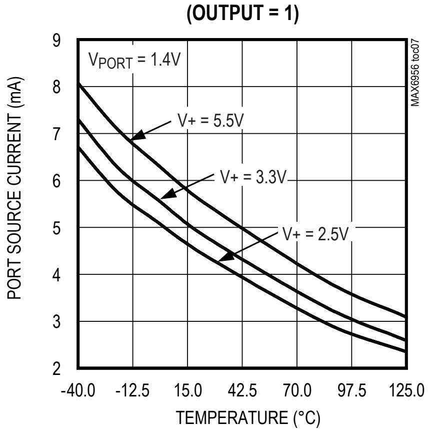
LED DRIVER SINK CURRENT vs. TEMPERATURE



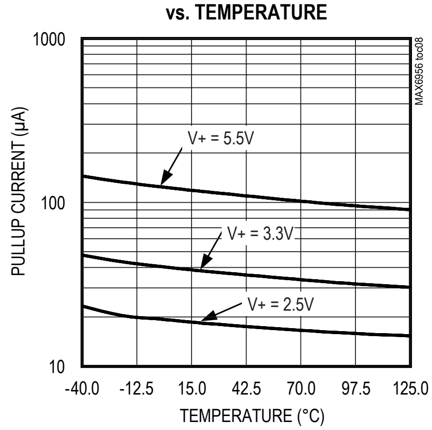
GPO SINK CURRENT vs. TEMPERATURE (OUTPUT = 0)



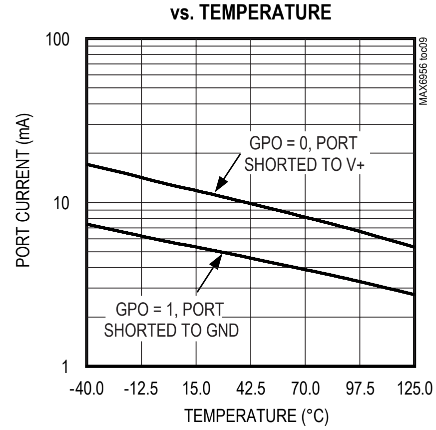
GPO SOURCE CURRENT vs. TEMPERATURE (OUTPUT = 1)



GPI PULLUP CURRENT vs. TEMPERATURE



GPO SHORT-CIRCUIT CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
SSOP/DIP	SSOP	TQFN		
1	1	36	ISET	Segment Current Setting. Connect ISET to GND through a resistor (R_{ISET}) to set the maximum segment current.
2, 3	2, 3	37, 38, 39	GND	Ground
4	4	40	AD0	Address Input 0. Sets device slave address. Connect to either GND, V+, SCL, SDA to give four logic combinations. See Table 3.
5–24	—	—	P12–P31	LED Segment Drivers and GPIO. P12 to P31 can be configured as CA LED drivers, GPIO outputs, CMOS logic inputs, or CMOS logic inputs with weak pullup resistor.
—	5–32	1–10, 12–19, 21–30	P4–P31	LED Segment Drivers and GPIO. P4 to P31 can be configured as CA LED drivers, GPIO outputs, CMOS logic inputs, or CMOS logic inputs with weak pullup resistor.
—	—	11, 20, 31	N.C.	No Connection
25	33	32	SDA	I^2C-Compatible Serial Data I/O
26	34	33	SCL	I^2C-Compatible Serial Clock Input
27	35	34	AD1	Address Input 1. Sets device slave address. Connect to either GND, V+, SCL, SDA to give four logic combinations. See Table 3.
28	36	35	V+	Positive Supply Voltage. Bypass V+ to GND with minimum 0.047µF capacitor.
—	—	—	EP	Exposed Pad (TQFN Only). Not internally connected. Connect EP to ground plane for maximum thermal performance.

Detailed Description

The MAX6956 LED driver/GPIO peripheral provides up to 28 I/O ports, P4 to P31, controlled through an I^2C-compatible serial interface. The ports can be configured to any combination of constant-current LED drivers, logic inputs and logic outputs, and default to logic inputs on power-up. When fully configured as an LED driver, the MAX6956 controls up to 28 LED segments with individual 16-step adjustment of the constant current through each LED segment. A single resistor sets the maximum segment current for all segments, with a maximum of 24mA per segment. The MAX6956 drives any combination of discrete LEDs and CA digits, including seven-segment and starburst alphanumeric types.

Figure 1 is the MAX6956 functional diagram. Any I/O port can be configured as a push-pull output (sinking 10mA, sourcing 4.5mA), or a Schmitt-trigger logic input. Each input has an individually selectable internal pullup resistor. Additionally, transition detection allows seven ports (P24 through P30) to be monitored in any maskable combination for changes in their logic status. A detected transition is flagged through a status register bit, as well as an interrupt pin (port P31), if desired.

The *Typical Operating Circuit* shows two MAX6956s working together controlling three monocolor 16-segment-plus-DP displays, with five ports left available for GPIO (P26–P31 of U2).

The port configuration registers set the 28 ports, P4 to P31, individually as either LED drivers or GPIO. A pair of bits in registers 0x09 through 0x0F sets each port's configuration (Tables 1 and 2).

The 36-pin MAX6956AAX has 28 ports, P4 to P31. The 28-pin MAX6956ANI and MAX6956AAI make only 20 ports available, P12 to P31. The eight unused ports should be configured as outputs on power-up by writing 0x55 to registers 0x09 and 0x0A. If this is not done, the eight unused ports remain as unconnected inputs and quiescent supply current rises, although there is no damage to the part.

Register Control of I/O Ports and LEDs Across Multiple Drivers

The MAX6956 offers 20 or 28 I/O ports, depending on package choice. These can be applied to a variety of combinations of different display types, for example: seven, 7-segment digits (Figure 7). This example requires two MAX6956s, with one digit being driven by both devices, half by one MAX6956, half by the other (digit 4 in this example). The two drivers are static, and therefore do not need to be synchronized. The MAX6956 sees CA digits as multiple discrete LEDs. To simplify access to displays

Table 1. Port Configuration Map

REGISTER	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Port Configuration for P7, P6, P5, P4	0x09	P7		P6		P5		P4	
Port Configuration for P11, P10, P9, P8	0x0A	P11		P10		P9		P8	
Port Configuration for P15, P14, P13, P12	0x0B	P15		P14		P13		P12	
Port Configuration for P19, P18, P17, P16	0x0C	P19		P18		P17		P16	
Port Configuration for P23, P22, P21, P20	0x0D	P23		P22		P21		P20	
Port Configuration for P27, P26, P25, P24	0x0E	P27		P26		P25		P24	
Port Configuration for P31, P30, P29, P28	0x0F	P31		P30		P29		P28	

Table 2. Port Configuration Matrix

MODE	FUNCTION	PORT REGISTER (0x20–0x5F)	PIN BEHAVIOR	ADDRESS CODE (HEX)	PORT CONFIGURATION BIT PAIR	
					UPPER	LOWER
Output	LED Segment Driver	Register bit = 0	High impedance	0x09 to 0x0F	0	0
		Register bit = 1	Open-drain current sink, with sink current (up to 24mA) determined by the appropriate current register			
Output	GPIO Output	Register bit = 0	Active-low logic output	0x09 to 0x0F	0	1
		Register bit = 1	Active-high logic output			
Input	GPIO Input Without Pullup	Register bit = input logic level	Schmitt logic input	0x09 to 0x0F	1	0
Input	GPIO Input with Pullup		Schmitt logic input with pullup	0x09 to 0x0F	1	1

Note: *The logic is inverted between the two output modes; a high makes the output go low in LED segment driver mode (0x00) to turn that segment on; in GPIO output mode (0x01), a high makes the output go high.*

that overlap two MAX6956s, the MAX6956 provides four virtual ports, P0 through P3. To update an overlapping digit, send the same code twice as an eight-port write, once to P28 through P35 of the first driver, and again to P0 through P7 of the second driver. The first driver ignores the last 4 bits and the second driver ignores the first 4 bits.

Two addressing methods are available. Any single port (bit) can be written (set/cleared) at once; or, any sequence of eight ports can be written (set/cleared) in any combination at once. There are no boundaries; it is equally acceptable to write P0 through P7, P1 through P8, or P31 through P38 (P32 through P38 are nonexistent, so the instructions to these bits are ignored).

Using 8-bit control, a seven-segment digit with a decimal point can be updated in a single byte-write, a 14-segment digit with DP can be updated in two byte-writes, and 16-segment digits with DP can be updated in two byte-writes plus a bit write. Also, discrete LEDs and GPIO port bits can be lit and controlled individually without affecting other ports.

Shutdown

When the MAX6956 is in shutdown mode, all ports are forced to inputs (which an be read), and the pullup current sources are turned off. Data in the port and control registers remain unaltered, so port configuration and output levels are restored when the MAX6956 is taken out of shutdown. The display driver can still be programmed while in shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at GND or V+ potential. Shutdown mode is exited by setting the S bit in the configuration register (Table 8).

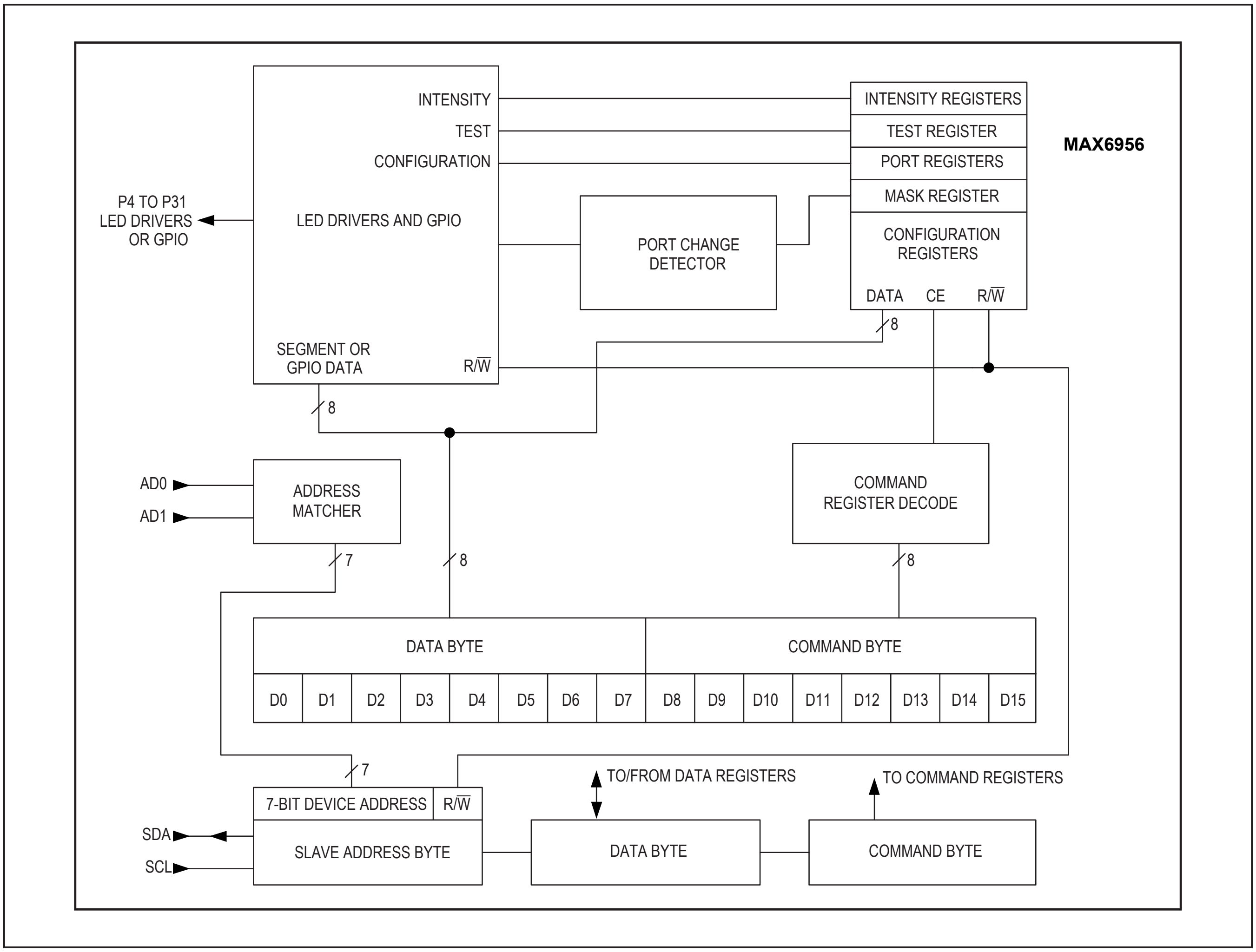


Figure 1. MAX6956 Functional Diagram

Shutdown mode is temporarily overridden by the display test function.

Serial Interface

Serial Addressing

The MAX6956 operates as a slave that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX6956, and generates the SCL clock that synchronizes the data transfer (Figure 2).

The MAX6956 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The MAX6956 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX6956 7-bit slave address plus R/W bit (Figure 6), a register address byte, one or more data bytes, and finally a STOP condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has

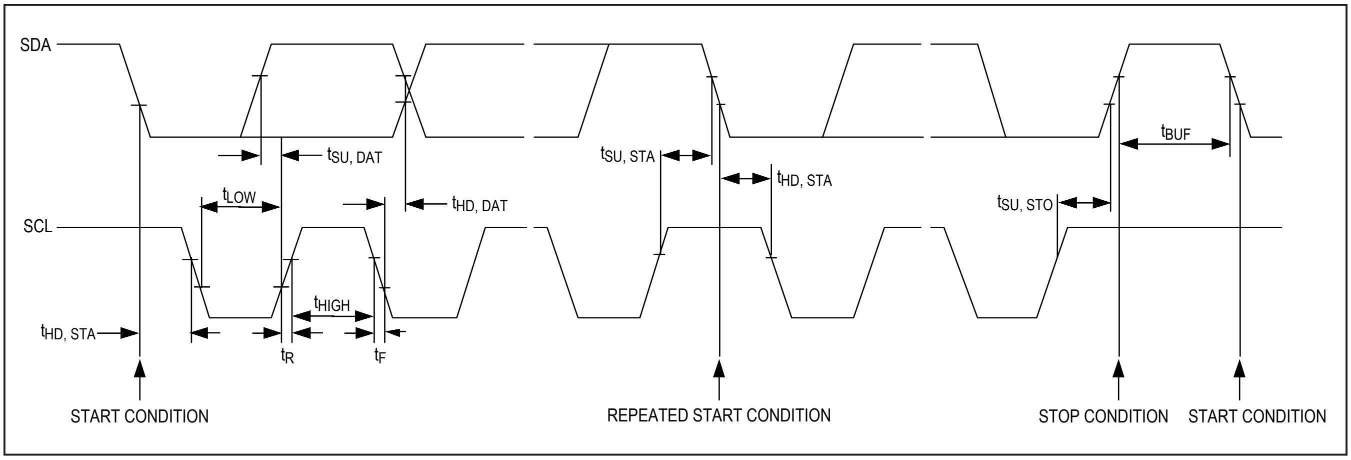


Figure 2. 2-Wire Serial Interface Timing Details

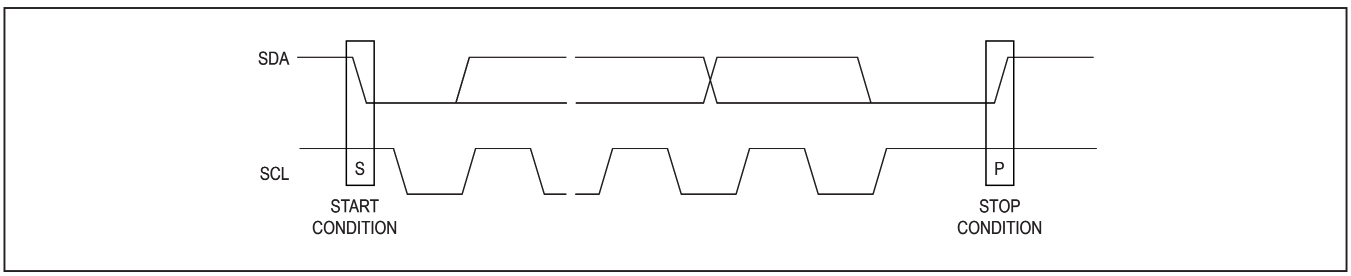


Figure 3. Standard Stop Conditions

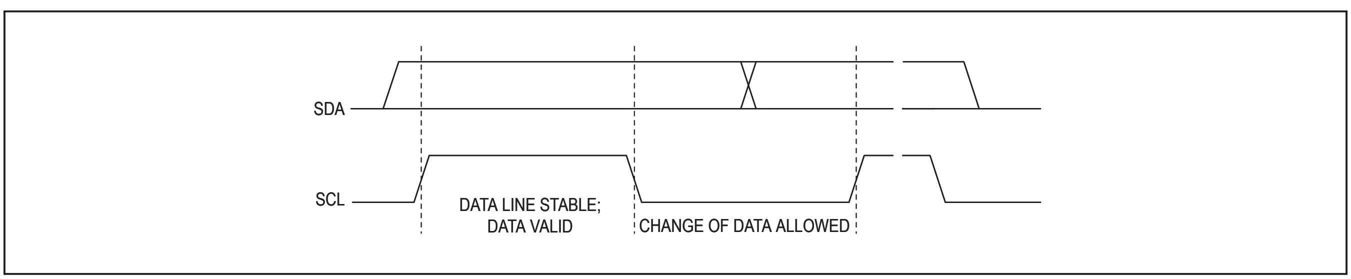


Figure 4. Bit Transfer

finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit, which the recipient uses to handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX6956, the MAX6956 generates the acknowledge bit because the MAX6956 is the

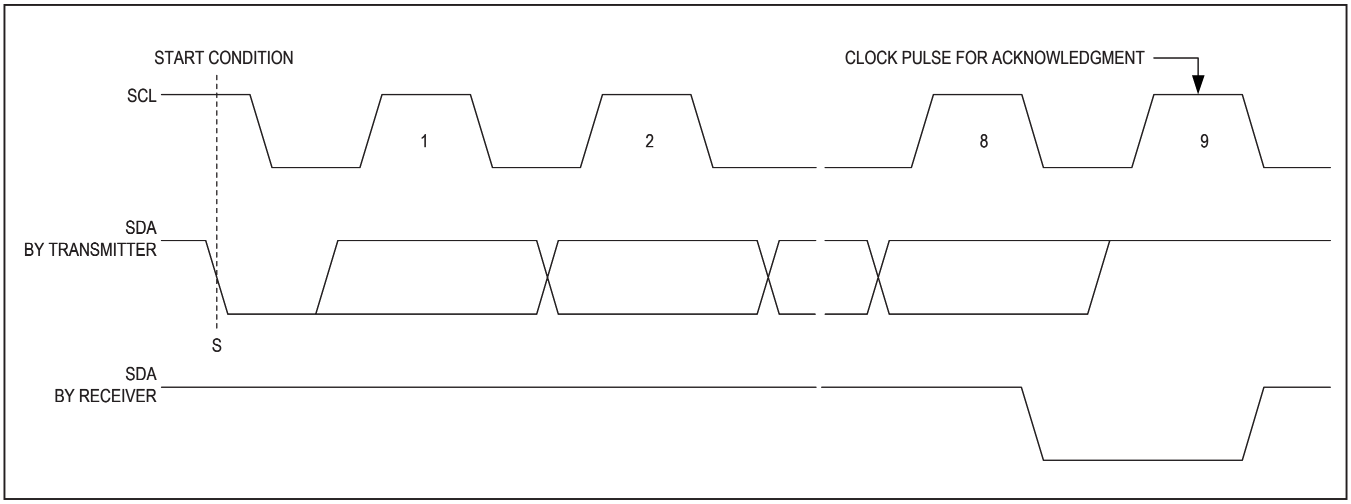


Figure 5. Acknowledge

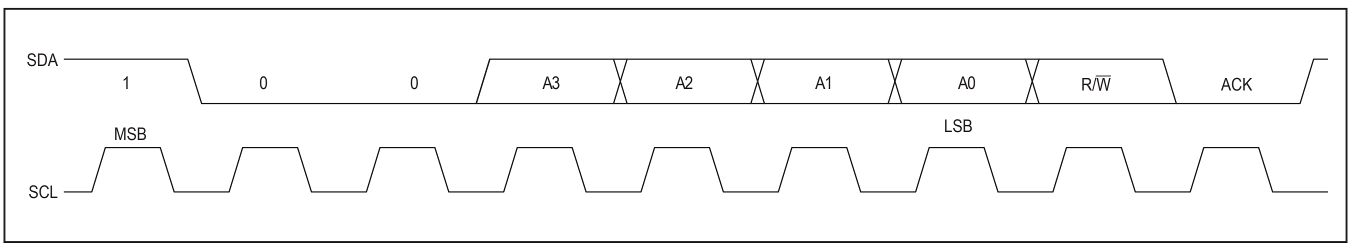


Figure 6. Slave Address

recipient. When the MAX6956 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX6956 has a 7-bit-long slave address (Figure 6). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command, high for a read command.

The first 3 bits (MSBs) of the MAX6956 slave address are always 100. Slave address bits A3, A2, A1, and A0 are selected by address inputs, AD1 and AD0. These two input pins may be connected to GND, V+, SDA, or SCL. The MAX6956 has 16 possible slave addresses (Table 3) and therefore, a maximum of 16 MAX6956 devices may share the same interface.

Message Format for Writing the MAX6956

A write to the MAX6956 comprises the transmission of the MAX6956's slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX6956 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, then the MAX6956 takes no further action (Figure 8) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the MAX6956 selected by the command byte (Figure 9). If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX6956 internal registers because the command byte address generally autoincrements (Table 4).

Message Format for Reading

The MAX6956 is read using the MAX6956's internally stored command byte as address pointer, the same way the stored command byte is used as address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 4). Thus, a read is initiated by first configuring the MAX6956's command byte by performing a write

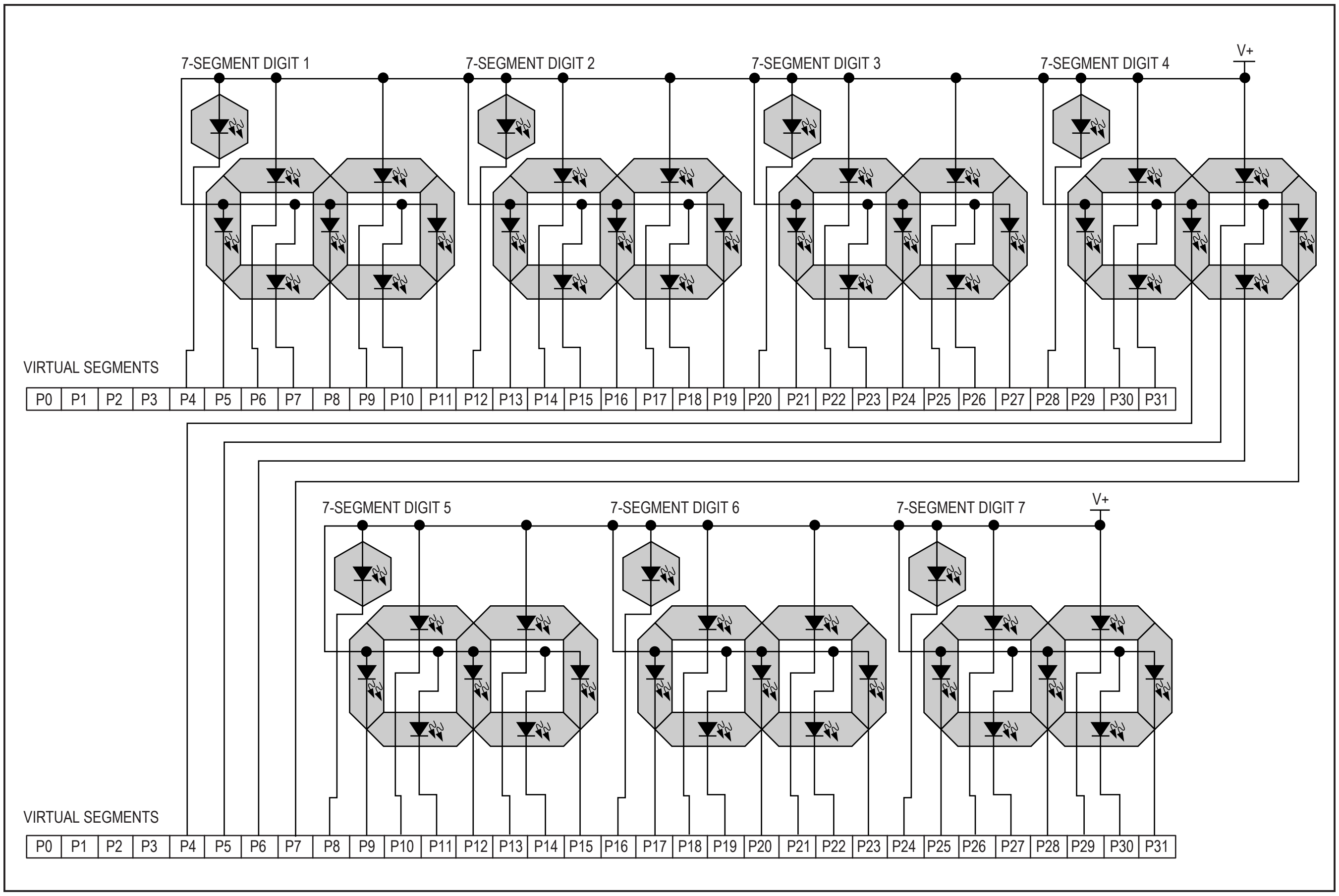


Figure 7. Two MAX6956s Controlling Seven 7-Segment Displays

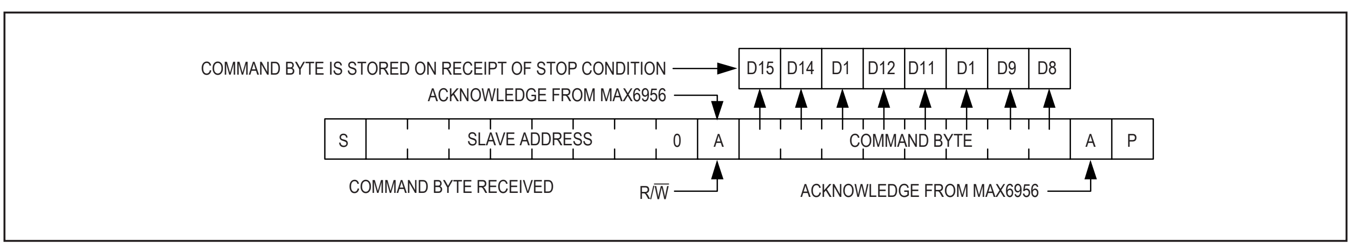


Figure 8. Command Byte Received

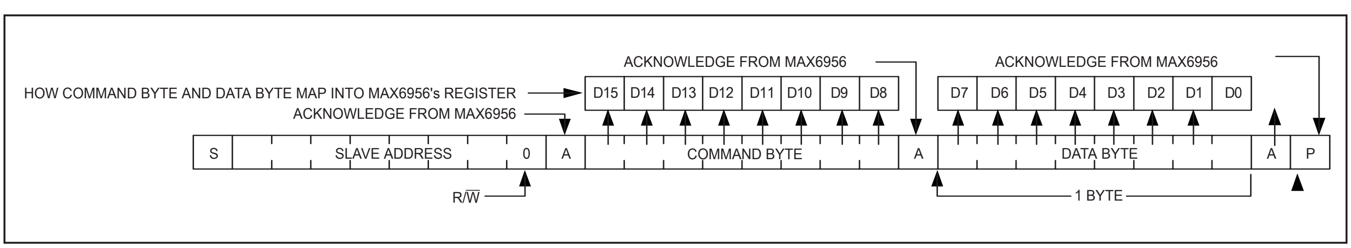


Figure 9. Command and Single Data Byte Received

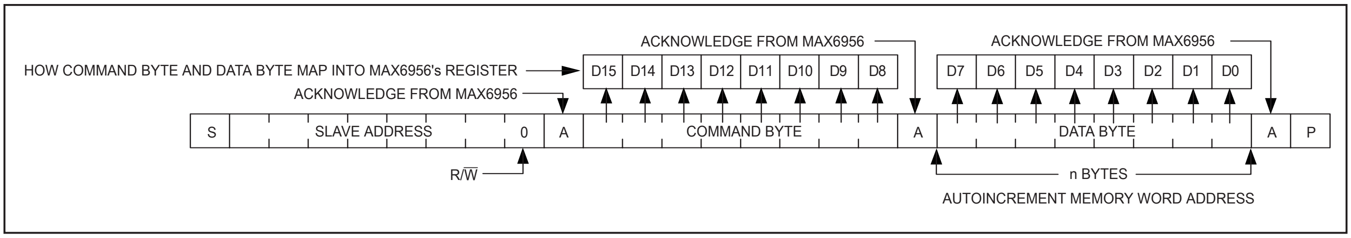


Figure 10. n Data Bytes Received

Table 3. MAX6956 Address Map

PIN CONNECTION		DEVICE ADDRESS						
AD1	AD0	A6	A5	A4	A3	A2	A1	A0
GND	GND	1	0	0	0	0	0	0
GND	V+	1	0	0	0	0	0	1
GND	SDA	1	0	0	0	0	1	0
GND	SCL	1	0	0	0	0	1	1
V+	GND	1	0	0	0	1	0	0
V+	V+	1	0	0	0	1	0	1
V+	SDA	1	0	0	0	1	1	0
V+	SCL	1	0	0	0	1	1	1
SDA	GND	1	0	0	1	0	0	0
SDA	V+	1	0	0	1	0	0	1
SDA	SDA	1	0	0	1	0	1	0
SDA	SCL	1	0	0	1	0	1	1
SCL	GND	1	0	0	1	1	0	0
SCL	V+	1	0	0	1	1	0	1
SCL	SDA	1	0	0	1	1	1	0
SCL	SCL	1	0	0	1	1	1	1

Table 4. Autoincrement Rules

COMMAND BYTE ADDRESS RANGE	AUTO INCREMENT BEHAVIOR
x0000000 to x1111110	Command address autoincrements after byte read or written
x1111111	Command address remains at x1111111 after byte written or read

(Figure 8). The master can now read n consecutive bytes from the MAX6956, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored control byte address generally has been autoincremented after the write (Table 4). Table 5 is the register address map.

Operation with Multiple Masters

If the MAX6956 is operated on a 2-wire interface with multiple masters, a master reading the MAX6956 should use a repeated start between the write, which sets the MAX6956's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX6956's address pointer but before master 1 has read the data. If master 2 subsequently changes, the

Table 5. Register Address Map

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	0	0	0	0x00
Global Current	X	0	0	0	0	0	1	0	0x02
Configuration	X	0	0	0	0	1	0	0	0x04
Transition Detect Mask	X	0	0	0	0	1	1	0	0x06
Display Test	X	0	0	0	0	1	1	1	0x07
Port Configuration P7, P6, P5, P4	X	0	0	0	1	0	0	1	0x09
Port Configuration P11, P10, P9, P8	X	0	0	0	1	0	1	0	0x0A
Port Configuration P15, P14, P13, P12	X	0	0	0	1	0	1	1	0x0B
Port Configuration P19, P18, P17, P16	X	0	0	0	1	1	0	0	0x0C
Port Configuration P23, P22, P21, P20	X	0	0	0	1	1	0	1	0x0D
Port Configuration P27, P26, P25, P24	X	0	0	0	1	1	1	0	0x0E
Port Configuration P31, P30, P29, P28	X	0	0	0	1	1	1	1	0x0F
Current054	X	0	0	1	0	0	1	0	0x12
Current076	X	0	0	1	0	0	1	1	0x13
Current098	X	0	0	1	0	1	0	0	0x14
Current0BA	X	0	0	1	0	1	0	1	0x15
Current0DC	X	0	0	1	0	1	1	0	0x16
Current0FE	X	0	0	1	0	1	1	1	0x17
Current110	X	0	0	1	1	0	0	0	0x18
Current132	X	0	0	1	1	0	0	1	0x19
Current154	X	0	0	1	1	0	1	0	0x1A
Current176	X	0	0	1	1	0	1	1	0x1B
Current198	X	0	0	1	1	1	0	0	0x1C
Current1BA	X	0	0	1	1	1	0	1	0x1D
Current1DC	X	0	0	1	1	1	1	0	0x1E
Current1FE	X	0	0	1	1	1	1	1	0x1F
Port 0 only (virtual port, no action)	X	0	1	0	0	0	0	0	0x20
Port 1 only (virtual port, no action)	X	0	1	0	0	0	0	1	0x21
Port 2 only (virtual port, no action)	X	0	1	0	0	0	1	0	0x22
Port 3 only (virtual port, no action)	X	0	1	0	0	0	1	1	0x23
Port 4 only (data bit D0; D7–D1 read as 0)	X	0	1	0	0	1	0	0	0x24
Port 5 only (data bit D0; D7–D1 read as 0)	X	0	1	0	0	1	0	1	0x25
Port 6 only (data bit D0; D7–D1 read as 0)	X	0	1	0	0	1	1	0	0x26
Port 7 only (data bit D0; D7–D1 read as 0)	X	0	1	0	0	1	1	1	0x27
Port 8 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	0	0	0	0x28
Port 9 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	0	0	1	0x29
Port 10 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	0	1	0	0x2A

Table 5. Register Address Map (continued)

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
Port 11 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	0	1	1	0x2B
Port 12 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	1	0	0	0x2C
Port 13 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	1	0	1	0x2D
Port 14 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	1	1	0	0x2E
Port 15 only (data bit D0; D7–D1 read as 0)	X	0	1	0	1	1	1	1	0x2F
Port 16 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	0	0	0	0x30
Port 17 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	0	0	1	0x31
Port 18 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	0	1	0	0x32
Port 19 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	0	1	1	0x33
Port 20 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	1	0	0	0x34
Port 21 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	1	0	1	0x35
Port 22 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	1	1	0	0x36
Port 23 only (data bit D0; D7–D1 read as 0)	X	0	1	1	0	1	1	1	0x37
Port 24 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	0	0	0	0x38
Port 25 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	0	0	1	0x39
Port 26 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	0	1	0	0x3A
Port 27 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	0	1	1	0x3B
Port 28 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	1	0	0	0x3C
Port 29 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	1	0	1	0x3D
Port 30 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	1	1	0	0x3E
Port 31 only (data bit D0; D7–D1 read as 0)	X	0	1	1	1	1	1	1	0x3F
4 ports 4–7 (data bits D0–D3; D4–D7 read as 0)	X	1	0	0	0	0	0	0	0x40
5 ports 4–8 (data bits D0–D4; D5–D7 read as 0)	X	1	0	0	0	0	0	1	0x41
6 ports 4–9 (data bits D0–D5; D6–D7 read as 0)	X	1	0	0	0	0	1	0	0x42
7 ports 4–10 (data bits D0–D6; D7 reads as 0)	X	1	0	0	0	0	1	1	0x43
8 ports 4–11 (data bits D0–D7)	X	1	0	0	0	1	0	0	0x44
8 ports 5–12 (data bits D0–D7)	X	1	0	0	0	1	0	1	0x45
8 ports 6–13 (data bits D0–D7)	X	1	0	0	0	1	1	0	0x46
8 ports 7–14 (data bits D0–D7)	X	1	0	0	0	1	1	1	0x47
8 ports 8–15 (data bits D0–D7)	X	1	0	0	1	0	0	0	0x48
8 ports 9–16 (data bits D0–D7)	X	1	0	0	1	0	0	1	0x49
8 ports 10–17 (data bits D0–D7)	X	1	0	0	1	0	1	0	0x4A
8 ports 11–18 (data bits D0–D7)	X	1	0	0	1	0	1	1	0x4B
8 ports 12–19 (data bits D0–D7)	X	1	0	0	1	1	0	0	0x4C
8 ports 13–20 (data bits D0–D7)	X	1	0	0	1	1	0	1	0x4D
8 ports 14–21 (data bits D0–D7)	X	1	0	0	1	1	1	0	0x4E
8 ports 15–22 (data bits D0–D7)	X	1	0	0	1	1	1	1	0x4F

Table 5. Register Address Map (continued)

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
8 ports 16–23 (data bits D0–D7)	X	1	0	1	0	0	0	0	0x50
8 ports 17–24 (data bits D0–D7)	X	1	0	1	0	0	0	1	0x51
8 ports 18–25 (data bits D0–D7)	X	1	0	1	0	0	1	0	0x52
8 ports 19–26 (data bits D0–D7)	X	1	0	1	0	0	1	1	0x53
8 ports 20–27 (data bits D0–D7)	X	1	0	1	0	1	0	0	0x54
8 ports 21–28 (data bits D0–D7)	X	1	0	1	0	1	0	1	0x55
8 ports 22–29 (data bits D0–D7)	X	1	0	1	0	1	1	0	0x56
8 ports 23–30 (data bits D0–D7)	X	1	0	1	0	1	1	1	0x57
8 ports 24–31 (data bits D0–D7)	X	1	0	1	1	0	0	0	0x58
7 ports 25–31 (data bits D0–D6; D7 reads as 0)	X	1	0	1	1	0	0	1	0x59
6 ports 26–31 (data bits D0–D5; D6–D7 read as 0)	X	1	0	1	1	0	1	0	0x5A
5 ports 27–31 (data bits D0–D4; D5–D7 read as 0)	X	1	0	1	1	0	1	1	0x5B
4 ports 28–31 (data bits D0–D3; D4–D7 read as 0)	X	1	0	1	1	1	0	0	0x5C
3 ports 29–31 (data bits D0–D2; D3–D7 read as 0)	X	1	0	1	1	1	0	1	0x5D
2 ports 30–31 (data bits D0–D1; D2–D7 read as 0)	X	1	0	1	1	1	1	0	0x5E
1 port 31 only (data bit D0; D1–D7 read as 0)	X	1	0	1	1	1	1	1	0x5F

Note: *Unused bits read as 0.*

MAX6956's address pointer, then master 1's delayed read may be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the MAX6956 to be configured with the shortest number of transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX6956 generally increments after each data byte is written or read (Table 4).

Initial Power-Up

On initial power-up, all control registers are reset, the current registers are set to minimum value, and the MAX6956 enters shutdown mode (Table 6).

LED Current Control

LED segment drive current can be set either globally or individually. Global control simplifies the operation when all LEDs are set to the same current level, because writing just the global current register sets the current for all ports configured as LED segment drivers. It is also possible to individually control the current drive of each LED segment driver. Individual/global brightness control is selected by setting the configuration register I bit (Table 9). The global current register (0x02) data are then ignored, and segment currents are set using register addresses 0x12 through 0x1F (Tables 12, 13, and 14). Each segment is controlled by a nibble of one of the 16 current registers.

Transition (Port Data Change) Detection

Port transition detection allows any combination of the seven ports P24–P30 to be continuously monitored for changes in their logic status (Figure 11). A detected change is flagged on the transition detection mask register INT status bit, D7 (Table 15). If port P31 is configured as an output (Tables 1 and 2), then P31 also automatically becomes an active-high interrupt output (INT), which follows the condition of the INT status bit. Port P31 is set as output by writing bit D7 = 0 and bit D6 = 1 to the port configuration register (Table 1). Note that the MAX6956 does not identify which specific port(s) caused the interrupt, but provides an alert that one or more port levels have changed.

Table 6. Power-Up Configuration

REGISTER FUNCTION	POWER-UP CONDITION	ADDRESS CODE (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Port Register Bits 4 to 31	LED Off; GPIO Output Low	0x24 to 0x3F	X	X	X	X	X	X	X	0
Global Current	1/16 (minimum on)	0x02	X	X	X	X	0	0	0	0
Configuration Register	Shutdown Enabled Current Control = Global Transition Detection Disabled	0x04	0	0	X	X	X	X	X	0
Input Mask Register	All Clear (Masked Off)	0x06	X	0	0	0	0	0	0	0
Display Test	Normal Operation	0x07	X	X	X	X	X	X	X	0
Port Configuration	P7, P6, P5, P4: GPIO Inputs Without Pullup	0x09	1	0	1	0	1	0	1	0
Port Configuration	P11, P10, P9, P8: GPIO Inputs Without Pullup	0x0A	1	0	1	0	1	0	1	0
Port Configuration	P15, P14, P13, P12: GPIO Inputs Without Pullup	0x0B	1	0	1	0	1	0	1	0
Port Configuration	P19, P18, P17, P16: GPIO Inputs Without Pullup	0x0C	1	0	1	0	1	0	1	0
Port Configuration	P23, P22, P21, P20: GPIO Inputs Without Pullup	0x0D	1	0	1	0	1	0	1	0
Port Configuration	P27, P26, P25, P24: GPIO Inputs Without Pullup	0x0E	1	0	1	0	1	0	1	0
Port Configuration	P31, P30, P29, P28: GPIO Inputs Without Pullup	0x0F	1	0	1	0	1	0	1	0
Current054	1/16 (minimum on)	0x12	0	0	0	0	0	0	0	0
Current076	1/16 (minimum on)	0x13	0	0	0	0	0	0	0	0
Current098	1/16 (minimum on)	0x14	0	0	0	0	0	0	0	0
Current0BA	1/16 (minimum on)	0x15	0	0	0	0	0	0	0	0
Current0DC	1/16 (minimum on)	0x16	0	0	0	0	0	0	0	0
Current0FE	1/16 (minimum on)	0x17	0	0	0	0	0	0	0	0
Current110	1/16 (minimum on)	0x18	0	0	0	0	0	0	0	0
Current132	1/16 (minimum on)	0x19	0	0	0	0	0	0	0	0
Current154	1/16 (minimum on)	0x1A	0	0	0	0	0	0	0	0
Current176	1/16 (minimum on)	0x1B	0	0	0	0	0	0	0	0
Current198	1/16 (minimum on)	0x1C	0	0	0	0	0	0	0	0
Current1BA	1/16 (minimum on)	0x1D	0	0	0	0	0	0	0	0
Current1DC	1/16 (minimum on)	0x1E	0	0	0	0	0	0	0	0
Current1FE	1/16 (minimum on)	0x1F	0	0	0	0	0	0	0	0

X = unused bits; if read, zero results.

Table 7. Configuration Register Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Configuration Register	0x04	M	I	X	X	X	X	X	S

Table 8. Shutdown Control (S Data Bit D0) Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown	0x04	M	I	X	X	X	X	X	0
Normal Operation	0x04	M	I	X	X	X	X	X	1

Table 9. Global Current Control (I Data Bit D6) Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Global Constant-current limits for all digits are controlled by one setting in the Global Current register, 0x02	0x04	M	0	X	X	X	X	X	S
Individual Segment Constant-current limit for each digit is individually controlled by the settings in the Current054 through Current1FE registers	0x04	M	1	X	X	X	X	X	S

Table 10. Transition Detection Control (M-Data Bit D7) Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Disabled	0x04	0	I	X	X	X	X	X	S
Enabled	0x04	1	I	X	X	X	X	X	S

The mask register contains 7 mask bits, which select which of the seven ports P24–P30 are to be monitored (Table 15). Set the appropriate mask bit to enable that port for transition detect. Clear the mask bit if transitions on that port are to be ignored. Transition detection works regardless of whether the port being monitored is set to input or output, but generally, it is not particularly useful to enable transition detection for outputs.

To use transition detection, first set up the mask register and configure port P31 as an output, as described above. Then enable transition detection by setting the M bit in the configuration register (Table 10). Whenever the configuration register is written with the M bit set, the MAX6956 updates an internal 7-bit snapshot register, which holds the comparison copy of the logic states of ports P24 through P30. The update action occurs regardless of the previous state of the M bit, so that it is not necessary to clear the M bit and then set it again to update the snapshot register.

When the configuration register is written with the M bit set, transition detection is enabled and remains enabled until either the configuration register is written with the

Table 11. Global Segment Current Register Format

LED DRIVE FRACTION	TYPICAL SEGMENT CURRENT (mA)	ADDRESS CODE (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
1/16	1.5	0x02	X	X	X	X	0	0	0	0	0xX0
2/16	3	0x02	X	X	X	X	0	0	0	1	0xX1
3/16	4.5	0x02	X	X	X	X	0	0	1	0	0xX2
4/16	6	0x02	X	X	X	X	0	0	1	1	0xX3
5/16	7.5	0x02	X	X	X	X	0	1	0	0	0xX4
6/16	9	0x02	X	X	X	X	0	1	0	1	0xX5
7/16	10.5	0x02	X	X	X	X	0	1	1	0	0xX6
8/16	12	0x02	X	X	X	X	0	1	1	1	0xX7
9/16	13.5	0x02	X	X	X	X	1	0	0	0	0xX8
10/16	15	0x02	X	X	X	X	1	0	0	1	0xX9
11/16	16.5	0x02	X	X	X	X	1	0	1	0	0xXA
12/16	18	0x02	X	X	X	X	1	0	1	1	0xXB
13/16	19.5	0x02	X	X	X	X	1	1	0	0	0xXC
14/16	21	0x02	X	X	X	X	1	1	0	1	0xXD
15/16	22.5	0x02	X	X	X	X	1	1	1	0	0xXE
16/16	24	0x02	X	X	X	X	1	1	1	1	0xXF

X = Don't care bit.

M bit clear, or a transition is detected. The INT status bit (transition detection mask register bit D7) goes low. Port P31 (if enabled as INT output) also goes low, if it was not already low.

Once transition detection is enabled, the MAX6956 continuously compares the snapshot register against the changing states of P24 through P31. If a change on any of the monitored ports is detected, even for a short time (like a pulse), the INT status bit (transition detection mask register bit D7) is set. Port P31 (if enabled as INT output) also goes high. The INT output and INT status bit are not cleared if more changes occur or if the data pattern returns to its original snapshot condition. The only way to clear INT is to access (read or write) the transition detection mask register (Table 15). So if the transition detection mask register is read twice in succession after a transition event, the first time reads with bit D7 set (identifying the event), and the second time reads with bit D7 clear.

Transition detection is a one-shot event. When INT has been cleared after responding to a transition event, transition detection is automatically disabled, even though the M bit in the configuration register remains set (unless cleared by the user). Reenable transition detection by writing the configuration register with the M bit set, to take a new snapshot of the seven ports P24 to P30.

Display Test Register

Display test mode turns on all ports configured as LED drivers by overriding, but not altering, all controls and port registers, except the port configuration register (Table 16). Only ports configured as LED drivers are affected. Ports configured as GPIO push-pull outputs do not change state. In display test mode, each port's current is temporarily set to 1/2 the maximum current limit as controlled by R_{ISET}.

Selecting External Component R_{ISET} to Set Maximum Segment Current

The MAX6956 uses an external resistor R_{ISET} to set the maximum segment current. The recommended value, 39kΩ, sets the maximum current to 24mA, which makes the segment current adjustable from 1.5mA to 24mA in 1.5mA steps.

To set a different segment current, use the formula:

$$R_{ISET} = 936k\Omega / I_{SEG}$$

where I_{SEG} is the desired maximum segment current.

Table 12. Individual Segment Current Registers

REGISTER FUNCTION	ADDRESS CODE (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Current054 register	0x12	Segment 5				Segment 4			
Current076 register	0x13	Segment 7				Segment 6			
Current098 register	0x14	Segment 9				Segment 8			
Current0BA register	0x15	Segment 11				Segment 10			
Current0DC register	0x16	Segment 13				Segment 12			
Current0FE register	0x17	Segment 15				Segment 14			
Current110 register	0x18	Segment 17				Segment 16			
Current132 register	0x19	Segment 19				Segment 18			
Current154 register	0x1A	Segment 21				Segment 20			
Current176 register	0x1B	Segment 23				Segment 22			
Current198 register	0x1C	Segment 25				Segment 24			
Current1BA register	0x1D	Segment 27				Segment 26			
Current1DC register	0x1E	Segment 29				Segment 28			
Current1FE register	0x1F	Segment 31				Segment 30			

Table 13. Even Individual Segment Current Format

LED DRIVE FRACTION	SEGMENT CONSTANT CURRENT WITH R_{ISET} = 39kΩ (mA)	ADDRESS CODE (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
1/16	1.5	0x12 to 0x1F	See Table 14.				0	0	0	0	0xX0
2/16	3	0x12 to 0x1F					0	0	0	1	0xX1
3/16	4.5	0x12 to 0x1F					0	0	1	0	0xX2
4/16	6	0x12 to 0x1F					0	0	1	1	0xX3
5/16	7.5	0x12 to 0x1F					0	1	0	0	0xX4
6/16	9	0x12 to 0x1F					0	1	0	1	0xX5
7/16	10.5	0x12 to 0x1F					0	1	1	0	0xX6
8/16	12	0x12 to 0x1F					0	1	1	1	0xX7
9/16	13.5	0x12 to 0x1F					1	0	0	0	0xX8
10/16	15	0x12 to 0x1F					1	0	0	1	0xX9
11/16	16.5	0x12 to 0x1F					1	0	1	0	0xXA
12/16	18	0x12 to 0x1F					1	0	1	1	0xXB
13/16	19.5	0x12 to 0x1F					1	1	0	0	0xXC
14/16	21	0x12 to 0x1F					1	1	0	1	0xXD
15/16	22.5	0x12 to 0x1F					1	1	1	0	0xXE
16/16	24	0x12 to 0x1F					1	1	1	1	0xXF

Table 14. Odd Individual Segment Current Format

LED DRIVE FRACTION	SEGMENT CONSTANT CURRENT WITH R_{ISET} = 39kΩ (mA)	ADDRESS CODE (HEX)	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
1/16	1.5	0x12 to 0x1F	0	0	0	0	See Table 13.				0x0X
2/16	3	0x12 to 0x1F	0	0	0	1					0x1X
3/16	4.5	0x12 to 0x1F	0	0	1	0					0x2X
4/16	6	0x12 to 0x1F	0	0	1	1					0x3X
5/16	7.5	0x12 to 0x1F	0	1	0	0					0x4X
6/16	9	0x12 to 0x1F	0	1	0	1					0x5X
7/16	10.5	0x12 to 0x1F	0	1	1	0					0x6X
8/16	12	0x12 to 0x1F	0	1	1	1					0x7X
9/16	13.5	0x12 to 0x1F	1	0	0	0					0x8X
10/16	15	0x12 to 0x1F	1	0	0	1					0x9X
11/16	16.5	0x12 to 0x1F	1	0	1	0					0xAX
12/16	18	0x12 to 0x1F	1	0	1	1					0xBX
13/16	19.5	0x12 to 0x1F	1	1	0	0					0xCX
14/16	21	0x12 to 0x1F	1	1	0	1					0xDX
15/16	22.5	0x12 to 0x1F	1	1	1	0					0xEX
16/16	24	0x12 to 0x1F	1	1	1	1					0xFX

The recommended value of R_{ISET} is 39kΩ.

The recommended value of R_{ISET} is the minimum allowed value, since it sets the display driver to the maximum allowed segment current. R_{ISET} can be a higher value to set the segment current to a lower maximum value where desired. The user must also ensure that the maximum current specifications of the LEDs connected to the driver are not exceeded.

The drive current for each segment can be controlled through programming either the Global Current register (Table 11) or Individual Segment Current registers (Tables 12, 13, and 14), according to the setting of the Current Control bit of the Configuration register (Table 9). These registers select the LED's constant-current drive from 16 equal fractions of the maximum segment current. The current difference between successive current steps, I_{STEP}, is therefore determined by the formula:

$$I_{STEP} = I_{SEG} / 16$$

If I_{SEG} = 24mA, then I_{STEP} = 24mA / 16 = 1.5mA.

Applications Information

Driving Bicolor and Tricolor LEDs

Bicolor digits group a red and a green die together for each display element, so that the element can be lit red, green (or orange), depending on which die (or both) is lit. The MAX6956 allows each segment's current to be set individually from 1/16th (minimum current and LED intensity) to 16/16th (maximum current and LED intensity), as well as off (zero current). Thus, a bicolor (red-green) segment pair can be set to 289 color/intensity combinations. A discrete or CA tricolor (red-green-yellow or red-green-blue) segment triad can be set to 4913 color/intensity combinations.

Power Dissipation Issues

Each MAX6956 port can sink a current of 24mA into an LED with a 2.4V forward-voltage drop when operated from a supply voltage of at least 3.0V. The minimum voltage drop across the internal LED drivers is therefore (3.0V - 2.4V) = 0.6V. The MAX6956 can sink 28 x 24mA = 672mA when all outputs are operating as LED segment

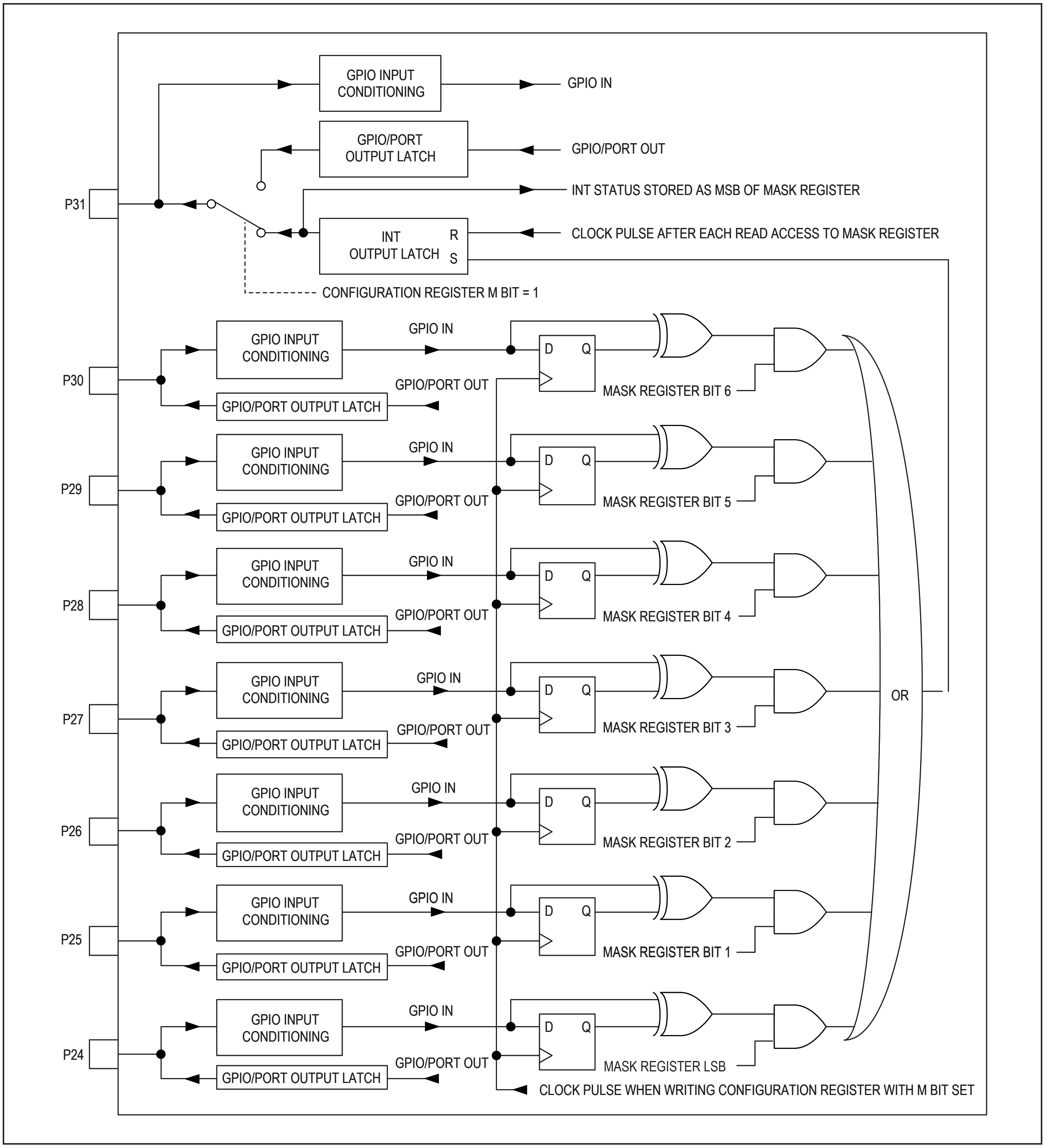


Figure 11. Maskable GPIO Ports P24 Through P31

Table 15. Transition Detection Mask Register

FUNCTION	REGISTER ADDRESS (HEX)	READ/ WRITE	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Mask Register	0x06	Read	INT Status*	Port 30 mask	Port 29 mask	Port 28 mask	Port 27 mask	Port 26 mask	Port 25 mask	Port 24 mask
		Write	Unchanged							

**INT is automatically cleared after it is read.*

Table 16. Display Test Register

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	0x07	X	X	X	X	X	X	X	0
Display Test Mode	0x07	X	X	X	X	X	X	X	1

X = Don't care bit

drivers at full current. On a 3.3V supply, a MAX6956 dissipates (3.3V - 2.4V) x 672mA = 0.6W when driving 28 of these 2.4V forward-voltage drop LEDs at full current. This dissipation is within the ratings of the 36-pin SSOP package with an ambient temperature up to +98°C. If a higher supply voltage is used or the LEDs used have a lower forward-voltage drop than 2.4V, the MAX6956 absorbs a higher voltage, and the MAX6956's power dissipation increases.

If the application requires high drive current and high supply voltage, consider adding a series resistor to each LED to drop excessive drive voltage off-chip. For example, consider the requirement that the MAX6956 must drive LEDs with a 2.0V to 2.4V specified forward-voltage drop, from an input supply range is 5V ±5% with a maximum LED current of 20mA. Minimum input supply voltage is 4.75V. Maximum LED series resistor value is (4.75V - 2.4V - 0.6V)/0.020A = 87.5Ω. We choose 82Ω ±2%. Worst-case resistor dissipation is at maximum toleranced resistance, i.e., $(0.020A)^2$ x (82Ω x 1.02) = 34mW. The maximum MAX6956 dissipation per LED is at maximum input supply voltage, minimum toleranced resistance, minimum toleranced LED forward-voltage drop, i.e., 0.020 x (5.25V - 2.0V - (0.020A x 82Ω x 0.98)) = 32.86mW. Worst-case MAX6956 dissipation is 920mW driving all 28 LEDs at 20mA full current at once, which meets the 941mW dissipation ratings of the 36-pin SSOP package.

Low-Voltage Operation

The MAX6956 operates down to 2V supply voltage (although the sourcing and sinking currents are not guaranteed), providing that the MAX6956 is powered up initially to at least 2.5V to trigger the device's internal reset.

Serial Interface Latency

When a MAX6956 register is written through the I^2C interface, the register is updated on the rising edge of SCL during the data byte's acknowledge bit (Figure 5). The delay from the rising edge of SCL to the internal register being updated can range from 50ns to 350ns.

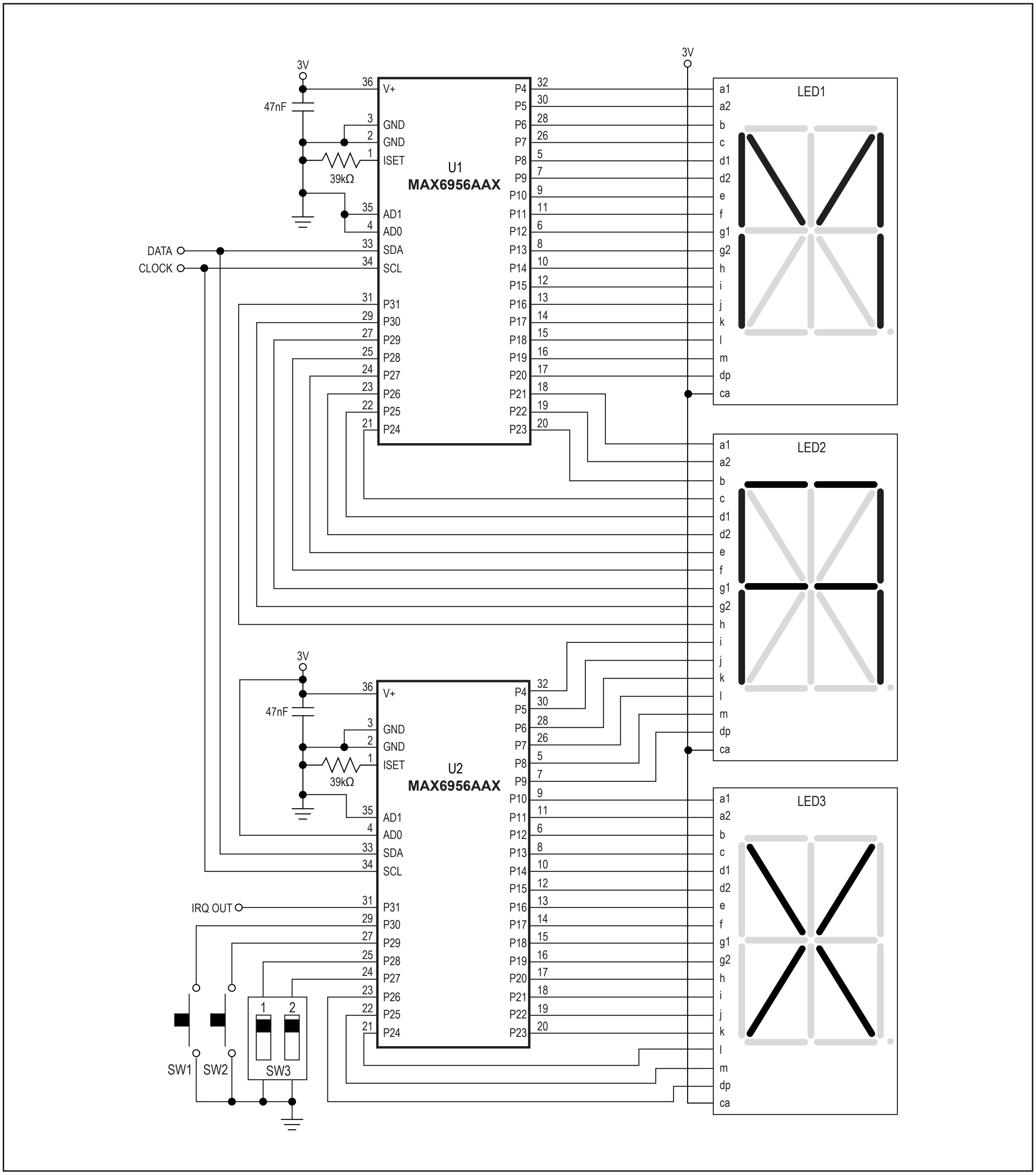
PC Board Layout Considerations

Ensure that all of the MAX6956 GND connections are used. A ground plane is not necessary, but may be useful to reduce supply impedance if the MAX6956 outputs are to be heavily loaded. Keep the track length from the ISET pin to the R_{ISET} resistor as short as possible, and take the GND end of the resistor either to the ground plane or directly to the GND pins.

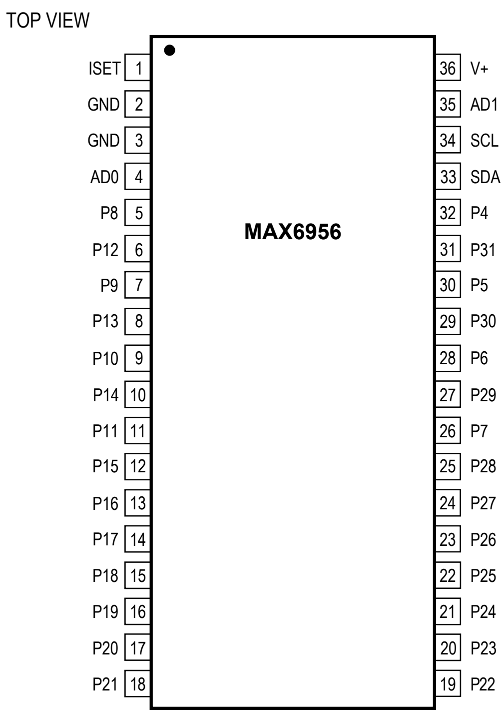
Power-Supply Considerations

The MAX6956 operates with power-supply voltages of 2.5V to 5.5V. Bypass the power supply to GND with a 0.047μF capacitor as close to the device as possible. Add a 1μF capacitor if the MAX6956 is far away from the board's input bulk decoupling capacitor.

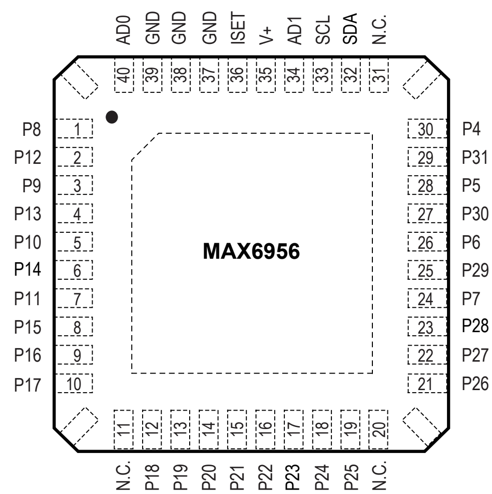
Typical Operating Circuit



Pin Configurations (continued)



SSOP



TQFN

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 DIP	N28+2	21-0043	—
28 SSOP	A28+1	21-0056	90-0095
36 SSOP	A36+4	21-0040	90-0098
40 Thin QFN-EP	T4066+5	21-0141	90-0055

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	11/03	—	—
3	3/09	Added exposed pad information and updated *packaging information*	1, 2, 5, 23
4	6/10	Added lead-free and automotive qualified parts to *Ordering Information*	1
5	2/21	Updated *Package Information*	23

