MAX7317

10-Port SPI-Interfaced I/O Expander with Overvoltage and Hot-Insertion Protection

General Description

The MAX7317 serial-interfaced peripheral provides microprocessors with 10 I/O ports rated to 7V. Each port can be individually configured as either an open-drain output, or an overvoltage-protected Schmitt input.

The MAX7317 supports hot insertion. All port pins remain high impedance in power-down (V+ = 0V) with up to 8V asserted on them.

The MAX7317 is available in 16-pin TQFN and QSOP packages and operates in the -40°C to +125°C range.

For a similar part with constant-current outputs and 8-bit PWM controls, refer to the MAX6966/MAX6967 data sheet.
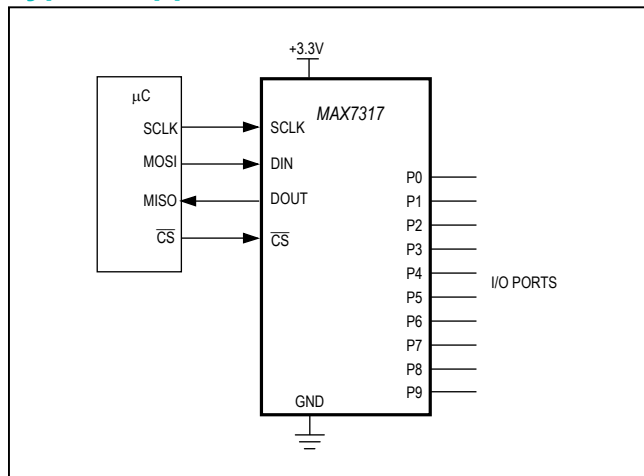
Applications

- Portable Equipment
- Cellular Phones
- White Goods
- Industrial Controllers
- System Monitoring

QSPI is a trademark of Motorola, Inc.

MICROWIRE is a registered trademark of National Semiconductor Corp.

Typical Application Circuit

Benefits and Features

- Industry-Standard 4-Wire Interface Simplifies I/O Ports Expansion Independent of Microprocessor Architecture
  - High-Speed, 26MHz, SPI-/QSPI™-/MICROWIRE®-Compatible Serial Interface
  - 2.25V to 3.6V Operation
- Protection Circuitry Ensures Robust Operation
  - I/O Port Inputs Are Overvoltage Protected to 7V
  - I/O Port Outputs Are 7V-Rated Open Drain
  - I/O Ports Support Hot Insertion
- Low Power Consumption and Small Package Reduce Board Size and Power-Supply Requirements
  - 0.7µA (typ), 1.9µA (max) Standby Current
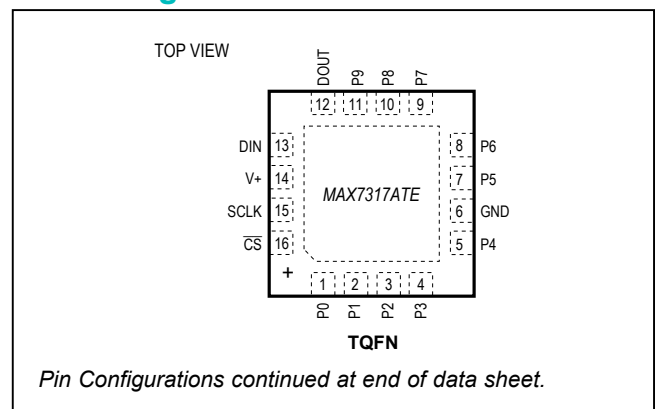 - 3mm x 3mm, 0.8mm High TQFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX7317ATE+	-40°C to +125°C	16 TQFN-EP* 3mm x 3mm x 0.8mm	ACH
MAX7317AEE+	-40°C to +125°C	16 QSOP	—

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Pin Configurations

Pin Configurations continued at end of data sheet.

Absolute Maximum Ratings

Voltage (with respect to GND)
V+ ....-0.3V to +4V
SCLK, DIN, CS, DOUT...............................-0.3V to (V+ + 0.3V)
P_ ....-0.3V to +8V
DC Current into P_ 24mA
DC Current into DOUT 10mA
Total GND Current..200mA

Continuous Power Dissipation (T_A = +70°C)
    16-Pin TQFN (derate 14.7mW/°C above +70°C)......1176mW
    16-Pin QSOP (derate 8.3mW/°C above +70°C)..........667mW
Operating Temperature Range
    (T_{MIN} to T_{MAX})... -40°C to +125°C
Junction Temperature..+150°C
Storage Temperature Range.......................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(*Typical Operating Circuit*, V+ = 2.25V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

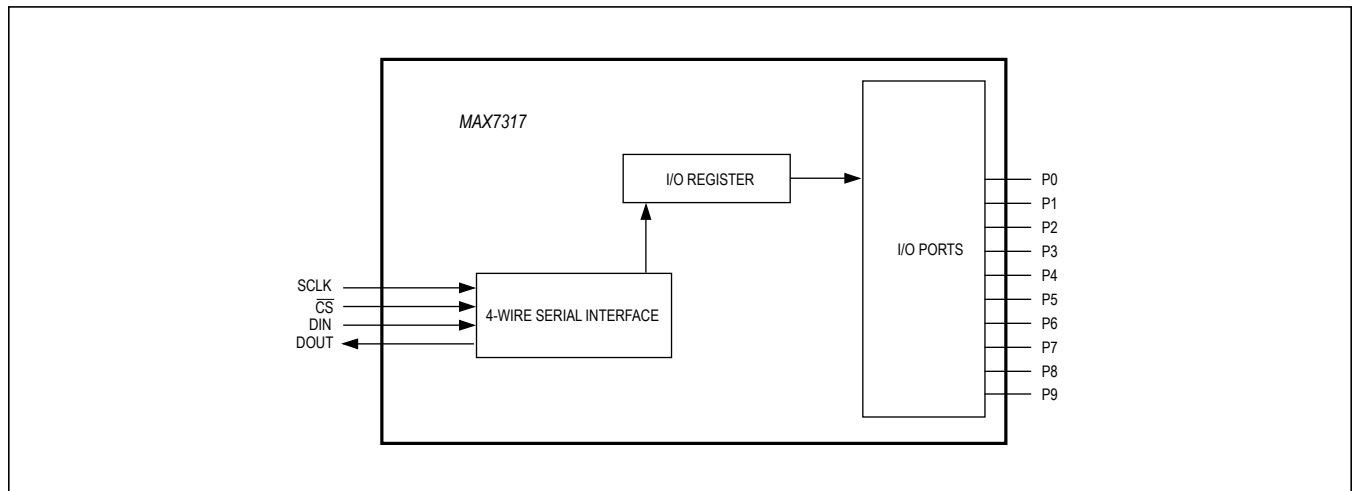| PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.25		3.60	V
Output Load External Supply Voltage P0–P9	V_{EXT}					7	V
Standby Current (Interface Idle)	I_{STBY}	All digital inputs at V+ or GND	T_A = +25°C		0.70	1.5	µA
			T_A = T_{MIN} to +85°C			1.7	
			T_A = T_{MIN} to T_{MAX}			1.9	
Supply Current	I_+	f_{SCLK} = 26MHz; other digital inputs at V+ or GND; DOUT unloaded	T_A = +25°C		385	620	µA
			T_A = T_{MIN} to +85°C			680	
			T_A = T_{MIN} to T_{MAX}			730	
Input High Voltage (P0–P9, DIN, SCLK, $\overline{CS}$)	V_{IH}	P0–P9 output register set to 0x01		0.7 x V+			V
Input Low Voltage (P0–P9, DIN, SCLK, $\overline{CS}$)	V_{IL}	P0–P9 output register set to 0x01				0.3 x V+	V
Input Leakage Current (P0–P9, DIN, SCLK, $\overline{CS}$)	I_{IH}, I_{IL}			-0.2		+0.2	µA
Input Capacitance (P0–P9, DIN, SCLK, $\overline{CS}$		(Note 2)			10		pF
Output Low Voltage (P0–P9)	$V_{OLP\_}$	I_{SINK} = 0.5mA, output register set to 0x00				0.4	V
Output Low Short-Circuit Current (P0–P9)		V_{OLPOUT} = 5V			10.8	20	mA
Output High Voltage (DOUT)	V_{OHDOUT}	I_{SOURCE} = -6mA		V+ - 0.3V			V
Output Low Voltage (DOUT)	V_{OLDOUT}	I_{SINK} = 6mA				0.3	V
Power-On Reset Voltage	V_{POR}			2			V

Timing Characteristics

(*Typical Operating Circuit*, V+ = 2.25V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.)
(Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		38.4			ns
SCLK Pulse-Width High	t_{CH}		19			ns
SCLK Pulse-Width Low	t_{CL}		19			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		9.5			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		2.5			ns
DIN Setup Time	t_{DS}		9.5			ns
DIN Hold Time	t_{DH}		2.5			ns
Output Data Propagation Delay	t_{DO}				19	ns
DOUT Output Rise and Fall Times	t_{FT}	C_{LOAD} = 20pF (Note 2)			10	ns
Minimum $\overline{CS}$ Pulse High	t_{CSW}		38.4			ns

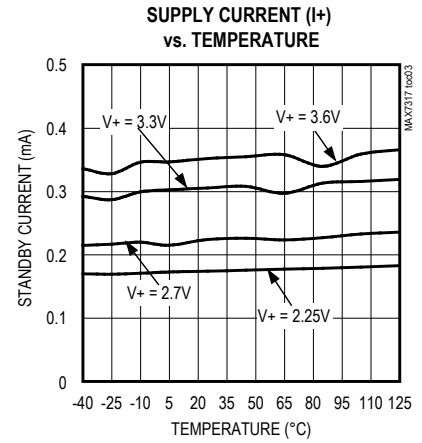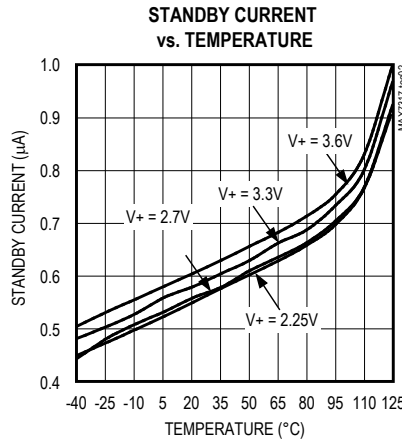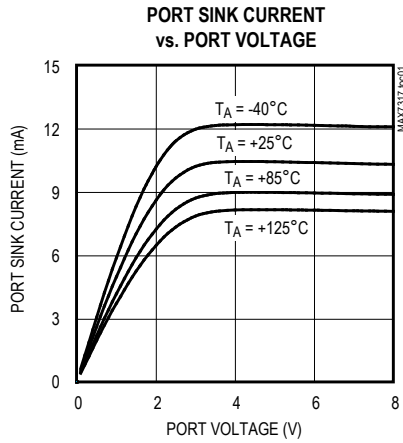**Note 1:** All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.

MAX7317 Block Diagram

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

PORT SINK CURRENT
vs. PORT VOLTAGE

STANDBY CURRENT
vs. TEMPERATURE

SUPPLY CURRENT (I+)
vs. TEMPERATURE

Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN		
1	15	SCLK	Serial-Clock Input. On SCLK's rising edge, data shifts into the internal shift register. On SCLK's falling edge, data is clocked out of DOUT. SCLK is active only while $\overline{CS}$ is low.
2	16	$\overline{CS}$	Chip-Select Input. Serial data is loaded into the shift register while $\overline{CS}$ is low. The most recent 16 bits of data latch on $\overline{CS}$'s rising edge.
3–7, 9–13	1–5, 7–11	P0–P9	I/O Ports. P0 to P9 can be configured as open-drain, current-sink outputs rated at 20mA maximum, or as CMOS inputs, or as open-drain outputs. Loads should be connected to a supply voltage no higher than 7V.
8	6	GND	Ground
14	12	DOUT	Serial-Data Output. The data into DIN is valid at DOUT 15.5 clock cycles later. Use this pin to daisy-chain several devices or allow data readback. Output is push-pull.
15	13	DIN	Serial-Data Input. Data from DIN loads into the internal 16-bit shift register on SCLK's rising edge.
16	14	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047μF ceramic capacitor.
—	PAD	EP	Exposed Pad on Package Underside. Connect to GND.

Detailed Description

The MAX7317 is a general-purpose input/output (GPIO) peripheral that provides 10 I/O ports, P0 to P9, controlled through a high-speed SPI-compatible serial interface. The 10 I/O ports can be used as inputs or open-drain outputs in any combination. Ports withstand 7V independent of the MAX7317's supply voltage whether used as inputs or outputs.

Figure 1 shows the I/O port structure of the MAX7317.

Register Structure

The MAX7317 contains 10 internal registers, addressed as 0x00–0x09, which control the peripheral (Table 2). Two further addresses, 0x0E and 0x0F, do not store data but return the port input status when read. Four virtual addresses, 0x0A–0x0D, allow more than one register to be written with the same data to simplify software. The RAM register provides 1 byte of memory that can be used for any purpose. The no-op address, 0x20, causes no action when written or read, and is used as a dummy register when accessing one MAX7317 out of multiple cascaded devices.

Initial Power-Up

On power-up, all control registers are reset (Table 2). Power-up status sets I/O ports P0 to P9 high impedance, and puts the device into shutdown mode.

RAM Register

The RAM register provides a byte of memory that can be used for any purpose.

GPIO Port Direction Configuration

The 10 I/O ports P0 through P9 can be configured to any combination of inputs and outputs. Ports withstand 7V independent of the MAX7317's supply voltage, whether used as inputs or outputs. Configure a port as an input by setting its output register to 0x01, which sets the port output high impedance (Table 4).

Input Port Registers

Reading an input port register returns the logic levels at the I/O port pins. The input port registers are read only. A write to an input port register is ignored.

Output Registers

The MAX7317 uses one 8-bit register to control each output port (Table 4). Each port can be configured as an input or open-drain output. Write 0x00 to the output register to set the port as a logic-low output, or 0x01 to set the port as a logic-high output or logic input.

The 10 registers, 0x00 through 0x09, control an I/O port each (Table 4). Four pseudo-register addresses, 0x0A through 0x0D, allow groups of outputs to be set to the same value with a single command by writing the same data to multiple output registers.

Serial Interface

The MAX7317 communicates through an SPI-compatible 4-wire serial interface. The interface has three inputs: clock (SCLK), chip select ($\overline{CS}$), and data in (DIN), and one output, data out (DOUT). $\overline{CS}$ must be low to clock data into or out of the device, and DIN must be stable when sampled on the rising edge of SCLK. DOUT is stable on the rising edge of SCLK.

SCLK and DIN can be used to transmit data to other peripherals. The MAX7317 ignores all activity on SCLK and DIN except when $\overline{CS}$ is low.

Note that the SPI protocol expects DOUT to be high impedance when the MAX7317 is not being accessed; DOUT on the MAX7317 is never high impedance. Go to www.maximintegrated.com/an1879 for ways to convert the MAX7317 to tri-state, if required.

Control and Operation Using the 4-Wire Interface

Controlling the MAX7317 requires sending a 16-bit word. The first byte, D15 through D8, is the command, and the second byte, D7 through D0, is the data byte (Table 5).
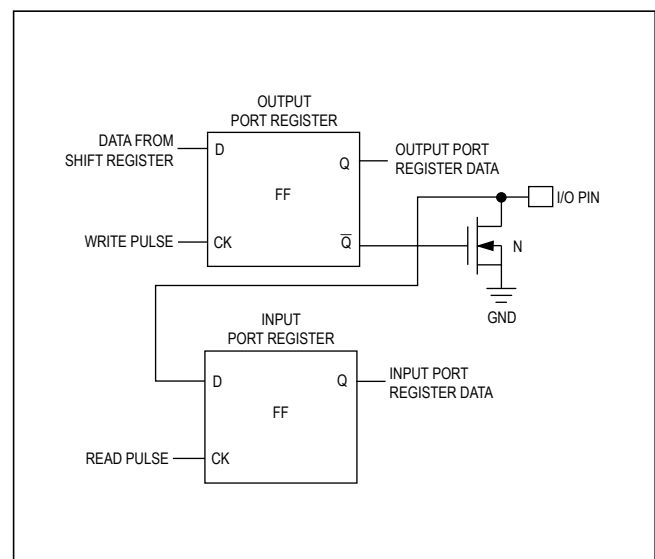

Figure 1. Simplified Schematic of I/O Ports

Table 1. Register Address Map

REGISTER	COMMAND ADDRESS								CODE (hex)
	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	
Port P0 output level	R/$\overline{W}$	0	0	0	0	0	0	0	0x00
Port P1 output level	R/$\overline{W}$	0	0	0	0	0	0	1	0x01
Port P2 output level	R/$\overline{W}$	0	0	0	0	0	1	0	0x02
Port P3 output level	R/$\overline{W}$	0	0	0	0	0	1	1	0x03
Port P4 output level	R/$\overline{W}$	0	0	0	0	1	0	0	0x04
Port P5 output level	R/$\overline{W}$	0	0	0	0	1	0	1	0x05
Port P6 output level	R/$\overline{W}$	0	0	0	0	1	1	0	0x06
Port P7 output level	R/$\overline{W}$	0	0	0	0	1	1	1	0x07
Port P8 output level	R/$\overline{W}$	0	0	0	1	0	0	0	0x08
Port P9 output level	R/$\overline{W}$	0	0	0	1	0	0	1	0x09
Write ports P0 through P9 with same output level	0	0	0	0	1	0	1	0	0x0A
Read port P0 output level	1								
Write ports P0 through P3 with same output level	0	0	0	0	1	0	1	1	0x0B
Read port P0 output level	1								
Write ports P4 through P7 with same output level	0	0	0	0	1	1	0	0	0x0C
Read port P4 output level	1								
Write ports P8 or P9 with same output level	0	0	0	0	1	1	0	1	0x0D
Read port P8 output level	1								
Read ports P7 through P0 inputs	1	0	0	0	1	1	1	0	0x0E
Read ports P9 and P8 inputs	1	0	0	0	1	1	1	1	0x0F
RAM	R/$\overline{W}$	0	0	1	0	0	1	1	0x13
No-op	R/$\overline{W}$	0	1	0	0	0	0	0	0x20
Factory reserved; do not write to this register	R/$\overline{W}$	1	1	1	1	1	0	1	0x7D

Table 2. Initial Power-Up Register Status

REGISTER	POWER-UP CONDITION	ADDRESS CODE (hex)	REGISTER DATA							
			D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Port P0 output level	Port 0 high impedance	0x00	1	1	1	1	1	1	1	1
Port P1 output level	Port 1 high impedance	0x01	1	1	1	1	1	1	1	1
Port P2 output level	Port 2 high impedance	0x02	1	1	1	1	1	1	1	1
Port P3 output level	Port 3 high impedance	0x03	1	1	1	1	1	1	1	1
Port P4 output level	Port 4 high impedance	0x04	1	1	1	1	1	1	1	1
Port P5 output level	Port 5 high impedance	0x05	1	1	1	1	1	1	1	1
Port P6 output level	Port 6 high impedance	0x06	1	1	1	1	1	1	1	1
Port P7 output level	Port 7 high impedance	0x07	1	1	1	1	1	1	1	1
Port P8 output level	Port 8 high impedance	0x08	1	1	1	1	1	1	1	1
Port P9 output level	Port 9 high impedance	0x09	1	1	1	1	1	1	1	1
RAM	0x00	0x13	0	0	0	0	0	0	0	0

Connecting Multiple MAX7317s to the 4-Wire Bus

Multiple MAX7317s can be interfaced to a common SPI bus by connecting DIN inputs together, SCLK inputs together, and providing an individual $\overline{CS}$ per the MAX7317 device (Figure 2). This connection works regardless of the configuration of DOUT/OSC, but does not allow the MAX7317s to be read.

Table 3. Input Ports Register

REGISTER	R/$\overline{W}$	ADDRESS CODE (hex)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Read input ports P7–P0	1	0X0E	Port P7	Port P6	Port P5	Port P4	Port P3	Port P2	Port P1	Port P0
Read input ports P9, P8	1	0X0F	0	0	0	0	0	0	Port P9	Port P8

Table 4. Output Registers Format

REGISTER	R/$\overline{W}$	ADDRESS CODE (hex)	REGISTER DATA								hex
			BINARY								
			D7	D6	D5	D4	D3	D2	D1	D0	
Port P0 level	—	0x00	MSB	Output P0 level and PWM						LSB	
Port P0 is open-drain logic low	—		0	0	0	0	0	0	0	0	0x00
Port P0 is open-drain logic high (high impedance without external pullup) **or** logic input	—		0	0	0	0	0	0	0	1	0x01
Port P1 level	—	0x01	MSB	Port P1 level						LSB	0x00 or 0x01
Port P2 level	—	0x02	MSB	Port P2 level						LSB	
Port P3 level	—	0x03	MSB	Port P3 level						LSB	
Port P4 level	—–	0x04	MSB	Port P4 level						LSB	
Port P5 level	—	0x05	MSB	Port P5 level						LSB	
Port P6 level	—	0x06	MSB	Port P6 level						LSB	
Port P7 level	—	0x07	MSB	Port P7 level						LSB	
Port P8 level	—	0x08	MSB	Port P8 level						LSB	
Port P9 level	—	0x09	MSB	Port P9 level						LSB	
Writes ports P0 through P9 with same level	0	0x0A	MSB	Ports P0 through P9 level						LSB	
Reads port P0 level	1		MSB	Port P0 level						LSB	
Writes ports P0 through P3 with same level	0	0x0B	MSB	Ports P0 through P3 level						LSB	
Reads port P0 level	1		MSB	Port P0 level						LSB	
Writes ports P4 through P7 with same level	0	0x0C	MSB	Ports P4 through P7 level						LSB	
Reads port P4 level	1		MSB	Port P4 level						LSB	
Write ports P8 and P9 with same level	0	0x0D	MSB	Ports P8, P9 level						LSB	
Read port P8 level	1		MSB	Port P8 level						LSB	

Alternatively, MAX7317s can be daisy-chained by connecting the DOUT of one device to the DIN of the next, and driving SCLK and $\overline{CS}$ lines in parallel (Figure 3). This connection allows the MAX7317s to be read. Data at DIN propagates through the internal shift registers and appears at DOUT 15.5 clock cycles later, clocked out on the falling edge of SCLK. When sending commands to daisy-chained MAX7317s, all devices are accessed at the same time. An access requires (16 x n) clock cycles, where n is the number of MAX7317s connected together. The serial interface speed (maximum SCLK) is limited to 10MHz when multiple devices are daisy-chained due to the DOUT propagation delay and DIN setup time.

The MAX7317 is written to using the following sequence (Figure 5):

1) Take SCLK low.

2) Take $\overline{CS}$ low. This enables the internal 16-bit shift register.

3) Clock 16 bits of data into DIN, D15 first to D0 last, observing the setup and hold times. Bit D15 is low, indicating a write command.

4) Take $\overline{CS}$ high (either while SCLK is still high after clocking in the last data bit, or after taking SCLK low).

5) Take SCLK low (if not already low).

If fewer or greater than 16 bits are clocked into the MAX7317 between taking $\overline{CS}$ low and taking $\overline{CS}$ high again, the MAX7317 stores the last 16 bits received, including the previous transmission(s). The general case is when n bits (where n > 16) are transmitted to the MAX7317. The last bits comprising bits {n-15} to {n}, are retained, and are parallel loaded into the 16-bit latch as bits D15 to D0, respectively (Figure 6).

Reading Device Registers

Any register data within the MAX7317 can be read by sending a logic high to bit D15. The sequence is:

1) Take SCLK low.

2) Take $\overline{CS}$ low. This enables the internal 16-bit shift register.

3) Clock 16 bits of data into DIN, D15 first to D0 last. D15 is high, indicating a read command and bits D14 through D8 contain the address of the register to read. Bits D7 to D0 contain dummy data, which is discarded.

4) Take $\overline{CS}$ high (either while SCLK is still high after clocking in the last data bit, or after taking SCLK low). Positions D7 through D0 in the shift register are now loaded with the register data addressed by bits D15 through D8.

5) Take SCLK low (if not already low).

6) Issue another read or write command, and examine the bit stream at DOUT; the second 8 bits are the contents of the register addressed by bits D14 through D8 in step 3.

Table 5. Serial-Data Format

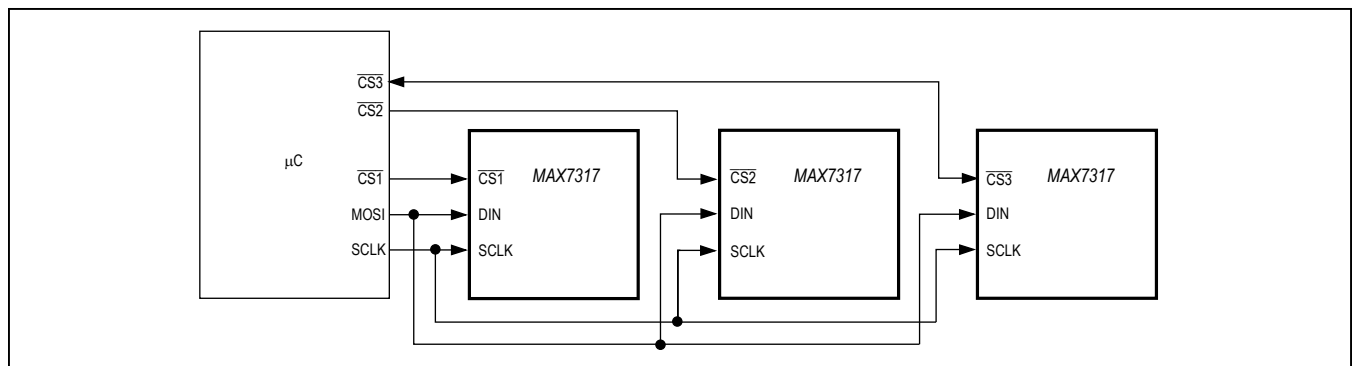| D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R/$\overline{W}$	MSB			ADDRESS			LSB	MSB			DATA				LSB

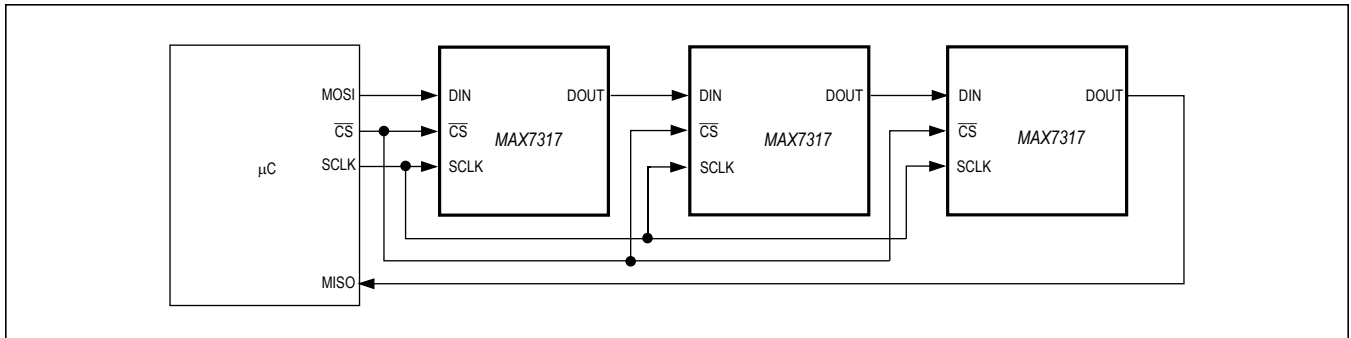*Figure 2. MAX7317 Multiple CS Connection*

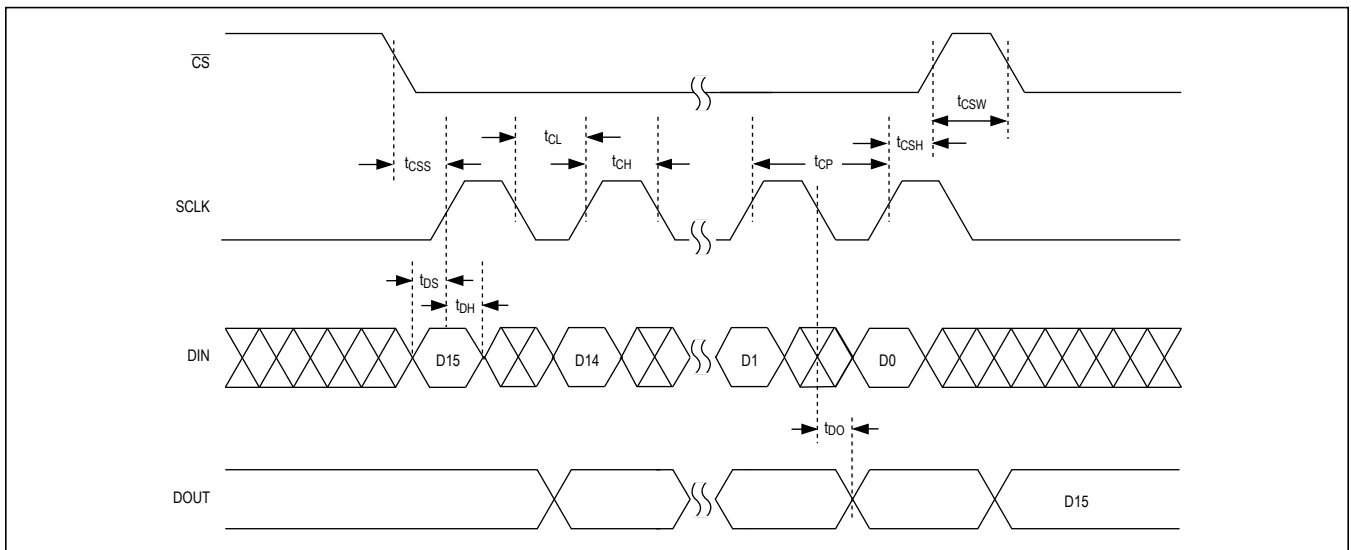*Figure 3. MAX7317 Daisy-Chain Connection*

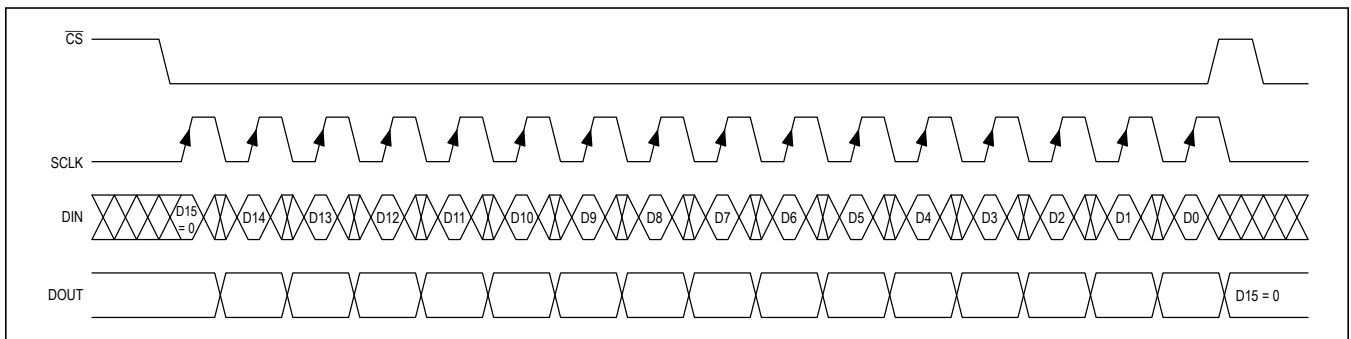*Figure 4. Timing Diagram*

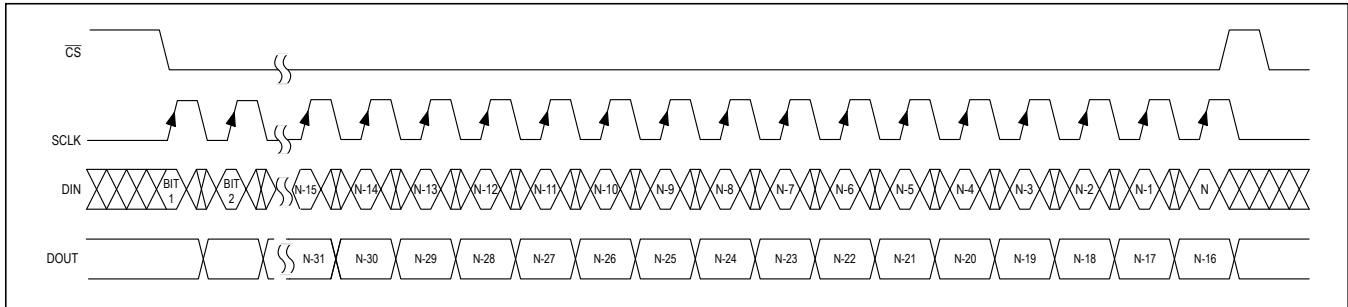

Figure 5. 16-Bit Write Transmission to the MAX7317

Figure 6. Transmission of More than 16 Bits to the MAX7317

Applications Information

Hot Insertion

The I/O ports P0–P9 remain high impedance with up to 8V asserted on them when the MAX7317 is powered down (V+ = 0V). The MAX7317 can therefore be used in hot-swap applications.

SPI Routing Considerations

The MAX7317's SPI interface is guaranteed to operate at 26Mbps on a 2.5V supply, and on a 3.3V supply typically operates at 35Mbps. This means that transmission line issues should be considered when the interface connections are longer than 100mm, particularly with higher supply voltages. Avoid running long adjacent tracks for SCLK, DIN, and $\overline{CS}$ without interleaving GND traces; otherwise, the signals may cross-couple, giving false clock or chip-select transitions. Ringing may manifest itself as communication issues, often intermittent, typically due to double clocking caused by ringing at the SCLK input. Fit a 1kΩ to 10kΩ parallel termination resistor to either GND or V+ at the DIN, SCLK, and $\overline{CS}$ inputs to damp ringing for moderately long interface runs. Use line-impedance-matching terminations when making connections between boards.

Output-Level Translation

The open-drain output architecture allows the ports to level translate the outputs to higher or lower voltages than the MAX7317 supply. An external pullup resistor can be used on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to 7V. When using a pullup on a constant-current output, select the resistor value to sink no more than a few hundred µA in logic-low condition. This ensures that the current-sink output saturates close to GND. For interfacing CMOS inputs, a pullup resistor value of 220kΩ is a good starting point. Use a lower resistance to

improve noise immunity in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.
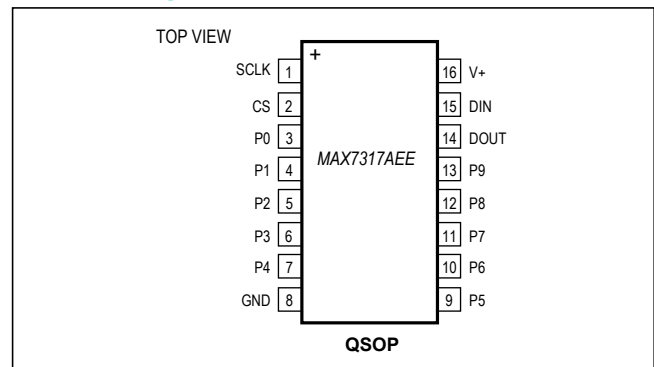
Power-Supply Considerations

The MAX7317 operates with a power-supply voltage of 2.25V to 3.6V. Bypass the power supply to GND with a 0.047µF ceramic capacitor as close to the device as possible. For the TQFN version, connect the underside exposed pad to GND.

Chip Information

PROCESS: BiCMOS

Pin Configurations (continued)

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 QSOP	E16+4	21-0055	90-0167
16 TQFN-EP	T1633+4	21-0136	90-0031

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/05	—	1–17
3	5/14	No /V OPNs; removed automotive reference from *Applications* section; updated *Packaging Information*	1
4	4/15	Updated *Benefits and Features* section	1

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