19-4788; Rev 1; 6/99

8th-Order, Lowpass, Bessel, Switched-Capacitor Filters

General Description

The MAX7401/MAX7405 8th-order, lowpass, Bessel, switched-capacitor filters (SCFs) operate from a single +5V (MAX7401) or +3V (MAX7405) supply. These devices draw only 2mA of supply current and allow corner frequencies from 1Hz to 5kHz, making them ideal for low-power post-DAC filtering and anti-aliasing applications. They feature a shutdown mode that reduces supply current to 0.2µA.

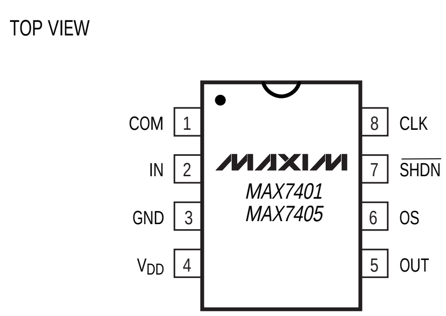
Two clocking options are available on these devices: self-clocking (through the use of an external capacitor) or external clocking for tighter corner-frequency control. An offset adjust pin allows for adjustment of the DC output level.

The MAX7401/MAX7405 Bessel filters provide low overshoot and fast settling. Their fixed response simplifies the design task to selecting a clock frequency.

Applications

ADC Anti-Aliasing	CT2 Base Stations
Post-DAC Filtering	Speech Processing
Air-Bag Electronics	

Pin Configuration



SO/DIP

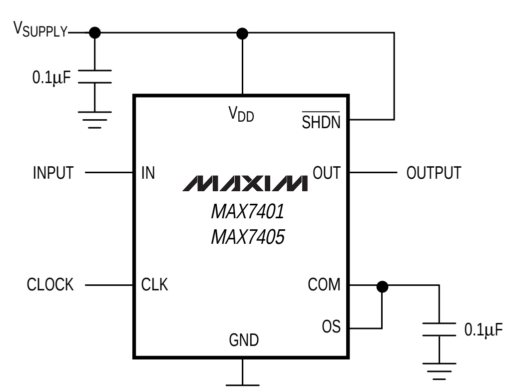
Features

- ♦ **8th-Order, Lowpass Bessel Filters**
- ♦ **Low Noise and Distortion: -82dB THD + Noise**
- ♦ **Clock-Tunable Corner Frequency (1Hz to 5kHz)**
- ♦ **100:1 Clock-to-Corner Ratio**
- ♦ **Single-Supply Operation**
  +5V (MAX7401)
  +3V (MAX7405)
- ♦ **Low Power**
  2mA (Operating Mode)
  0.2µA (Shutdown Mode)
- ♦ **Available in 8-Pin SO/DIP Packages**
- ♦ **Low Output Offset: ±5mV**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX7401CSA	0°C to +70°C	8 SO
MAX7401CPA	0°C to +70°C	8 Plastic DIP
MAX7401ESA	-40°C to +85°C	8 SO
MAX7401EPA	-40°C to +85°C	8 Plastic DIP
MAX7405CSA	0°C to +70°C	8 SO
MAX7405CPA	0°C to +70°C	8 Plastic DIP
MAX7405ESA	-40°C to +85°C	8 SO
MAX7405EPA	-40°C to +85°C	8 Plastic DIP

Typical Operating Circuit



8th-Order, Lowpass, Bessel, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND
- MAX7401 ....-0.3V to +6V
- MAX7405 ....-0.3V to +4V

IN, OUT, COM, OS, CLK ....-0.3V to (V_{DD} + 0.3V)
SHDN...-0.3V to +6V
OUT Short-Circuit Duration.......................................1sec

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin SO (derate 5.88mW/°C above +70°C)................471mW
- 8-Pin DIP (derate 9.09mW/°C above +70°C)..............727mW

Operating Temperature Ranges
- MAX740 _C_A ....0°C to +70°C
- MAX740 _E_A ....-40°C to +85°C

Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX7401

(V_{DD} = +5V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF from COM to GND, SHDN = V_{DD}, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS						
Corner Frequency	f_C	(Note 1)		0.001 to 5		kHz
Clock-to-Corner Ratio	f_{CLK} / f_C			100:1		
Clock-to-Corner Tempco				10		ppm/°C
Output Voltage Range			0.25		V_{DD} - 0.25	V
Output Offset Voltage	V_{OFFSET}	$V_{IN} = V_{COM} = V_{DD} / 2$		±5	±25	mV
DC Insertion Gain with Output Offset Removed		$V_{COM} = V_{DD} / 2$ (Note 2)	-0.1	0.15	0.3	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 4Vp-p, measurement bandwidth = 22kHz		-82		dB
OS Voltage Gain to OUT	A_{OS}			1		V/V
Input Voltage Range at OS	V_{OS}			V_{COM} ±0.1		V
COM Voltage Range	V_{COM}	Input, COM externally driven	V_{DD} / 2 - 0.5	V_{DD} / 2	V_{DD} / 2 + 0.5	V
		Output, COM internally biased	V_{DD} / 2 - 0.2	V_{DD} / 2	V_{DD} / 2 + 0.2	
Input Resistance at COM	R_{COM}		75	125		kΩ
Clock Feedthrough				10		mVp-p
Resistive Output Load Drive	R_L		10	1		kΩ
Maximum Capacitive Load at OUT	C_L		50	500		pF
Input Leakage Current at COM		SHDN = GND, V_{COM} = 0 to V_{DD}		±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to (V_{DD} - 1V) (Note 3)		±0.1	±10	µA
CLOCK						
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF (Note 4)	29	38	48	kHz
Clock Input Current	I_{CLK}	V_{CLK} = 0 or 5V		±15	±30	µA
Clock Input High	V_{IH}		V_{DD} - 0.5			V
Clock Input Low	V_{IL}				0.5	V

ELECTRICAL CHARACTERISTICS—MAX7401 (continued)

(V_{DD} = +5V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	Operating mode, no load, IN = OS = COM		2	3.5	mA
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND, CLK driven from 0 to V_{DD}		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	Measured at DC		60		dB
SHUTDOWN						
$\overline{SHDN}$ Input High	V_{SDH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low	V_{SDL}				0.5	V
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 0 to V_{DD}		±0.1	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7405

(V_{DD} = +3V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS						
Corner Frequency	f_C	(Note 1)		0.001 to 5		kHz
Clock-to-Corner Ratio	f_{CLK}/f_C			100:1		
Clock-to-Corner Tempco				10		ppm/°C
Output Voltage Range			0.25		V_{DD} - 0.25	V
Output Offset Voltage	V_{OFFSET}	V_{IN} = V_{COM} = V_{DD} / 2		±5	±25	mV
DC Insertion Gain with Output Offset Removed		V_{COM} = V_{DD} / 2 (Note 2)	-0.1	0.03	0.3	dB
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 200Hz, V_{IN} = 2.5Vp-p, measurement bandwidth = 22kHz		-84		dB
OS Voltage Gain to OUT	A_{OS}			1		V/V
Input Voltage Range at OS	V_{OS}			V_{COM} ±0.1		V
COM Voltage Range	V_{COM}	COM internally biased or externally driven	V_{DD} / 2 - 0.1	V_{DD} / 2	V_{DD} / 2 + 0.1	V
Input Resistance at COM	R_{COM}		75	125		kΩ
Clock Feedthrough				10		mVp-p
Resistance Output Load Drive	R_L		10	1		kΩ
Maximum Capacitive Load at OUT	C_L		50	500		pF
Input Leakage Current at COM		$\overline{SHDN}$ = GND, V_{COM} = 0 to V_{DD}		±0.1	±10	µA
Input Leakage Current at OS		V_{OS} = 0 to (V_{DD} - 1V) (Note 3)		±0.1	±10	µA

ELECTRICAL CHARACTERISTICS—MAX7405 (continued)

(V_{DD} = +3V, filter output measured at OUT, 10kΩ || 50pF load to GND at OUT, OS = COM, 0.1µF from COM to GND, $\overline{SHDN}$ = V_{DD}, f_{CLK} = 100kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK						
Internal Oscillator Frequency	f_{OSC}	C_{OSC} = 1000pF (Note 4)	26	34	43	kHz
Clock Input Current	I_{CLK}	V_{CLK} = 0 or 3V		±15	±30	µA
Clock Input High	V_{IH}		V_{DD} - 0.5			V
Clock Input Low	V_{IL}				0.5	V
POWER REQUIREMENTS						
Supply Voltage	V_{DD}		2.7		3.6	V
Supply Current	I_{DD}	Operating mode, no load, IN = OS = COM		2	3.5	mA
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND, CLK driven from 0 to V_{DD}		0.2	1	µA
Power-Supply Rejection Ratio	PSRR	Measured at DC		60		dB
SHUTDOWN						
$\overline{SHDN}$ Input High	V_{SDH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low	V_{SDL}				0.5	V
$\overline{SHDN}$ Input Leakage Current		$V_{\overline{SHDN}}$ = 0 to V_{DD}		±0.1	±10	µA

FILTER CHARACTERISTICS—MAX7401/MAX7405

(V_{DD} = +5V for MAX7401, V_{DD} = +3V for MAX7405; filter output measured at OUT; 10kΩ || 50pF load to GND at OUT; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD}/2; f_{CLK} = 100kHz; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

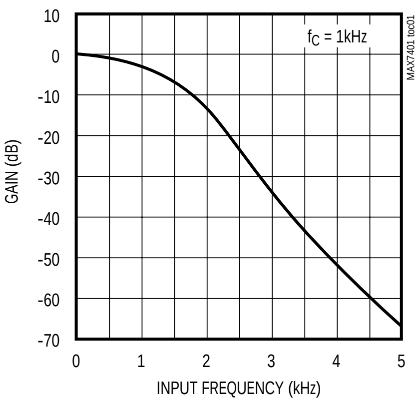
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Gain Relative to DC Gain	f_{IN} = 0.5f_C	-1.0	-0.8	-0.6	dB
	f_{IN} = f_C	-3.3	-3.0	-2.7	
	f_{IN} = 3f_C		-33	-29	
	f_{IN} = 6f_C		-79	-74	

Note 1: The maximum f_C is defined as the clock frequency, f_{CLK} = 100 · f_C, at which the peak SINAD drops to 68dB with a sinusoidal input at 0.2f_C.
Note 2: DC insertion gain is defined as ΔV_{OUT} / ΔV_{IN}.
Note 3: OS voltages above V_{DD} - 1V saturate the input and result in a 75µA typical input leakage current.
Note 4: For MAX7401, f_{OSC} (kHz) ≅ 38 · 10^3 / C_{OSC} (pF). For MAX7405, f_{OSC} (kHz) ≅ 34 · 10^3 / C_{OSC} (pF).

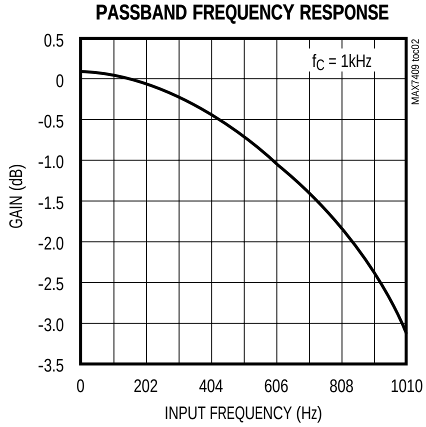
Typical Operating Characteristics

(V_{DD} = +5V for MAX7401, V_{DD} = +3V for MAX7405; f_{CLK} = 100kHz; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; T_A = +25°C; unless otherwise noted.)

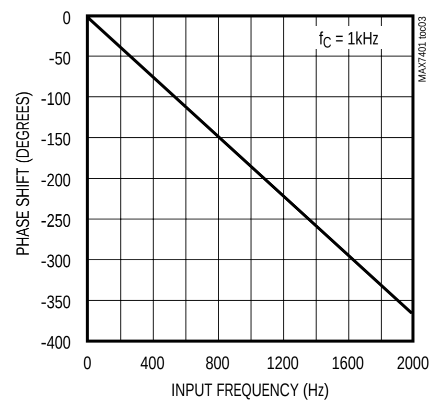
FREQUENCY RESPONSE



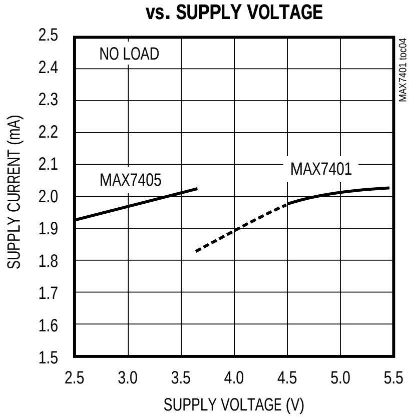
PASSBAND FREQUENCY RESPONSE



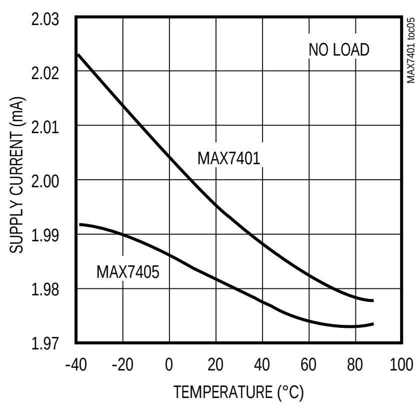
PHASE RESPONSE



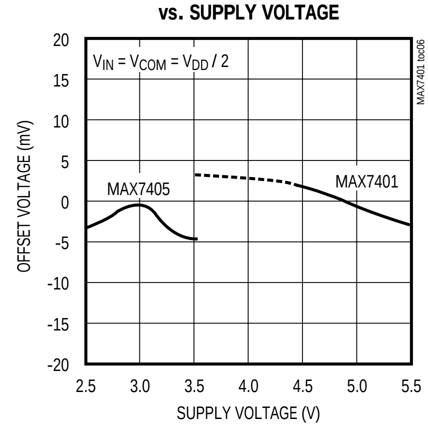
SUPPLY CURRENT vs. SUPPLY VOLTAGE



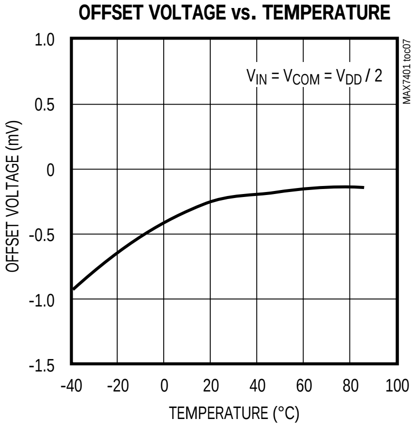
SUPPLY CURRENT vs. TEMPERATURE



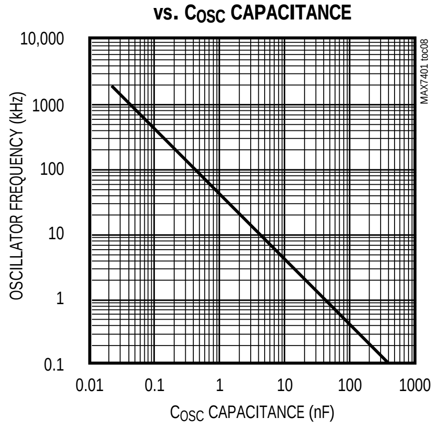
OFFSET VOLTAGE vs. SUPPLY VOLTAGE



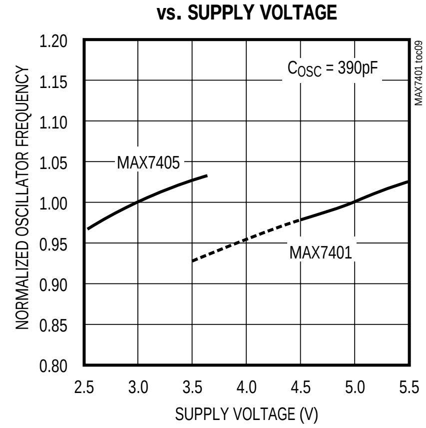
OFFSET VOLTAGE vs. TEMPERATURE



INTERNAL OSCILLATOR FREQUENCY vs. C_{OSC} CAPACITANCE



NORMALIZED OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE

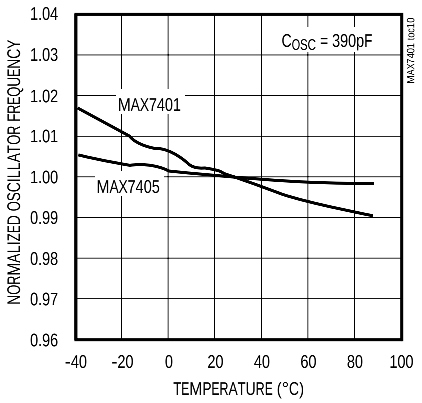


8th-Order, Lowpass, Bessel, Switched-Capacitor Filters

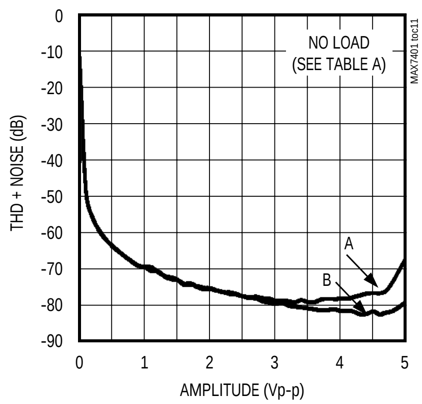
Typical Operating Characteristics (continued)

(V_{DD} = +5V for MAX7401, V_{DD} = +3V for MAX7405; f_{CLK} = 100kHz; $\overline{SHDN}$ = V_{DD}; V_{COM} = V_{OS} = V_{DD} / 2; T_A = +25°C; unless otherwise noted.)

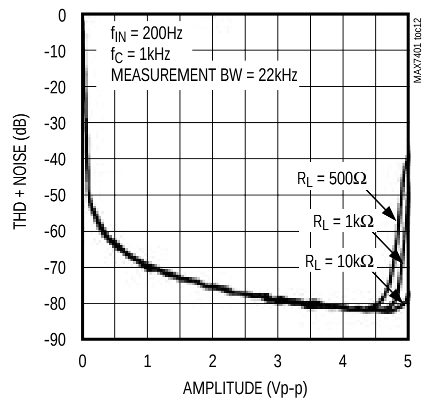
NORMALIZED OSCILLATOR FREQUENCY vs. TEMPERATURE



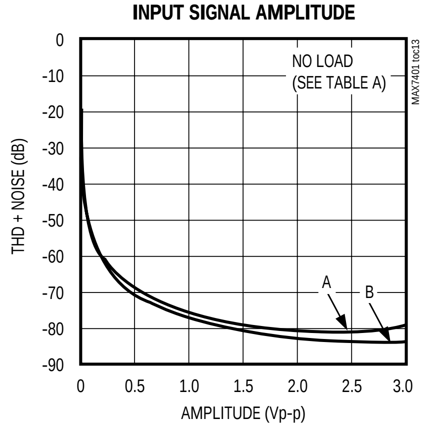
MAX7401 THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE



MAX7401 THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE AND RESISTIVE LOAD



MAX7405 THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE



MAX7405 THD PLUS NOISE vs. INPUT SIGNAL AMPLITUDE AND RESISTIVE LOAD

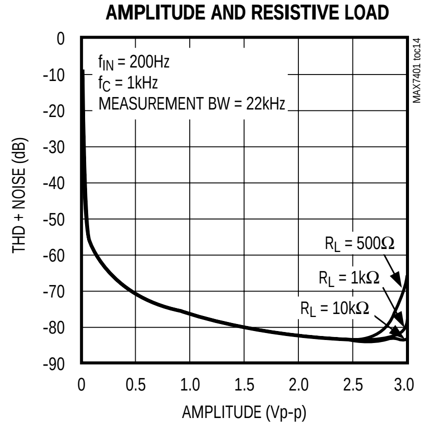


Table A. THD Plus Noise vs. Input Signal Amplitude Test Conditions

TRACE	f_{IN} (Hz)	f_C (kHz)	f_{CLK} (kHz)	MEASUREMENT BANDWIDTH (kHz)
A	1000	5	500	80
B	200	1	100	22

Pin Description

PIN	NAME	FUNCTION
1	COM	Common Input. Biased internally at mid-supply. Bypass externally to GND with a 0.1µF capacitor. To override internal biasing, drive with an external supply.
2	IN	Filter Input
3	GND	Ground
4	V_{DD}	Positive Supply Input: +5V for MAX7401, +3V for MAX7405
5	OUT	Filter Output
6	OS	Offset Adjust Input. To adjust output offset, bias OS externally. Connect OS to COM if no offset adjustment is needed. Refer to *Offset and Common-Mode Input Adjustment* section.
7	$\overline{SHDN}$	Shutdown Input. Drive low to enable shutdown mode; drive high or connect to V_{DD} for normal operation.
8	CLK	Clock Input. To override the internal oscillator, connect to an external clock; otherwise, connect an external capacitor (C_{OSC}) from CLK to GND to set the internal oscillator frequency.

Detailed Description

The MAX7401/MAX7405 Bessel filters provide low overshoot and fast settling responses. Both parts operate with a 100:1 clock-to-corner frequency ratio and a 5kHz maximum corner frequency.

Lowpass Bessel filters such as the MAX7401/MAX7405 delay all frequency components equally, preserving the shape of step inputs (subject to the attenuation of the higher frequencies). Bessel filters settle quickly—an important characteristic in applications that use a multiplexer (mux) to select an input signal for an analog-to-digital converter (ADC). An anti-aliasing filter placed between the mux and the ADC must settle quickly after a new channel is selected.

Figure 1 shows the difference between Bessel and Butterworth filters when a 1kHz square wave is applied to the filter input. With the filter cutoff frequencies set at 5kHz, trace B shows the Bessel filter response and trace C shows the Butterworth filter response.

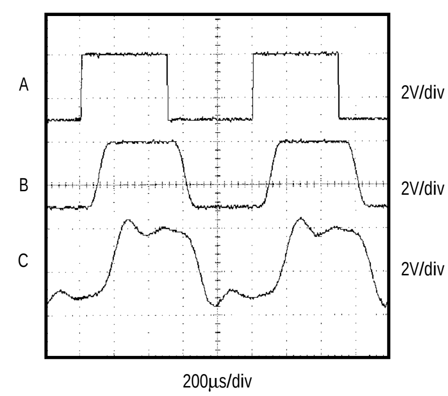


Figure 1. Bessel vs. Butterworth Filter Response

Background Information

Most switched-capacitor filters (SCFs) are designed with biquadratic sections. Each section implements two filtering poles, and the sections are cascaded to produce higher order filters. The advantage to this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high. An alternative approach is to emulate a passive network using switched-capacitor integrators with summing and scaling. Figure 2 shows a basic 8th-order ladder filter structure.

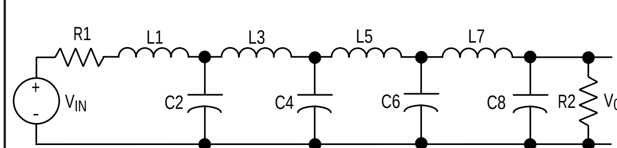


Figure 2. 8th-Order Ladder Filter Network

8th-Order, Lowpass, Bessel, Switched-Capacitor Filters

A switched-capacitor filter such as the MAX7401/MAX7405 emulates a passive ladder filter. The filter's component sensitivity is low when compared to a cascaded biquad design because each component affects the entire filter shape, not just one pole-zero pair. In other words, a mismatched component in a biquad design will have a concentrated error on its respective poles, while the same mismatch in a ladder filter design results in an error distributed over all poles.

Clock Signal

External Clock

The MAX7401/MAX7405 family of SCFs is designed for use with external clocks that have a 40% to 60% duty cycle. When using an external clock with these devices, drive CLK with a CMOS gate powered from 0 to V_{DD}. Varying the rate of the external clock adjusts the corner frequency of the filter as follows:

$$f_C = f_{CLK} / 100$$

Internal Clock

When using the internal oscillator, connect a capacitor (C_{OSC}) between CLK and ground. The value of the capacitor determines the oscillator frequency as follows:

$$f_{OSC}(\text{kHz}) = \frac{K \cdot 10^3}{C_{OSC}} \text{ ; } C_{OSC} \text{ in pF}$$

where K = 38 for MAX7401 and K = 34 for MAX7405.

Minimize the stray capacitance at CLK so that it does not affect the internal oscillator frequency. Vary the rate of the internal oscillator to adjust the filter's corner frequency by a 100:1 clock-to-corner frequency ratio. For example, an internal oscillator frequency of 100kHz produces a nominal corner frequency of 1kHz.

Input Impedance vs. Clock Frequencies

The MAX7401/MAX7405's input impedance is effectively that of a switched-capacitor resistor and is inversely proportional to frequency. The input impedance values determined below represent the average input impedance since the input current is not continuous. As a rule, use a driver with an output impedance less than 10% of the filter's input impedance. Estimate the input impedance of the filter using the following formula:

$$Z_{IN} = \frac{1}{(f_{CLK} \cdot C_{IN})}$$

where f_{CLK} = clock frequency and C_{IN} = 3.37pF.

Low-Power Shutdown Mode

These devices feature a shutdown mode that is activated by driving $\overline{SHDN}$ low. In shutdown mode, the filter's supply current reduces to 0.2µA (typ) and its output becomes high impedance. For normal operation, drive $\overline{SHDN}$ high or connect to V_{DD}.

Applications Information

Offset and Common-Mode Input Adjustment

The voltage at COM sets the common-mode input voltage and is biased at mid-supply with an internal resistor-divider. Bypass COM with a 0.1µF capacitor and connect OS to COM. For applications requiring offset adjustment or DC level shifting, apply an external bias voltage through a resistor-divider network to OS, as shown in Figure 3. (Note: Do not leave OS unconnected.) The output voltage is represented by this equation:

$$V_{OUT} = (V_{IN} - V_{COM}) + V_{OS}$$

with $V_{COM} = V_{DD} / 2$ (typical), and where ($V_{IN} - V_{COM}$) is lowpass filtered by the SCF, and V_{OS} is added at the output stage. See the *Electrical Characteristics* for the voltage range of COM and OS. Changing the voltage on COM or OS significantly from mid-supply reduces the filter's dynamic range.

Power Supplies

The MAX7401 operates from a single +5V supply, and the MAX7405 operates from a single +3V supply. Bypass V_{DD} to GND with a 0.1µF capacitor. If dual supplies are required (±2.5V for MAX7401, ±1.5V for MAX7405), connect COM to system ground and connect

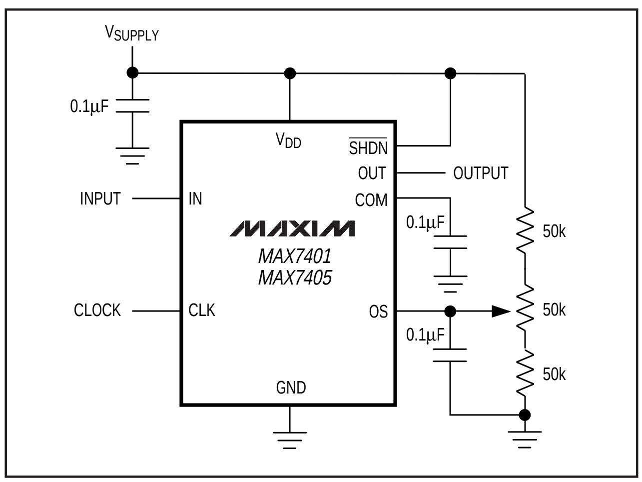


Figure 3. Offset Adjustment Circuit

Table 1. Typical Harmonic Distortion

FILTER	f_{CLK} (kHz)	f_C (kHz)	f_{IN} (Hz)	V_{IN} (Vp-p)	TYPICAL HARMONIC DISTORTION (dB)			
					2nd	3rd	4th	5th
MAX7401	100	1	200	4	-91	-83	-90	-93
	500	5	1000		-89	-79	-92	-92
MAX7405	100	1	200	2	-87	-83	-87	-88
	500	5	1000		-83	-82	-88	-88

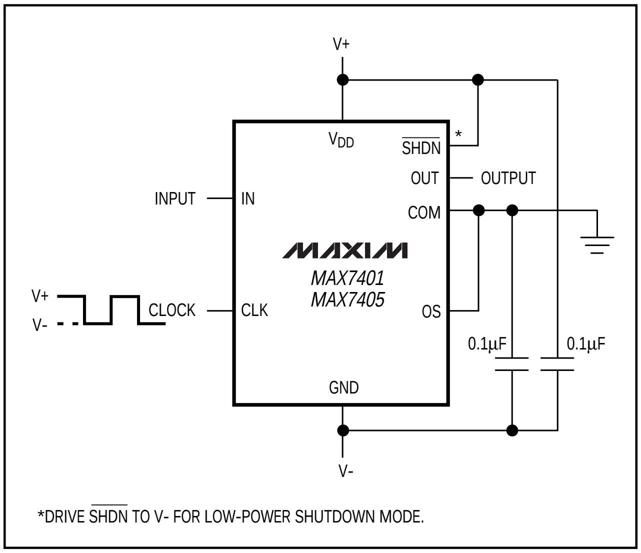


Figure 4. Dual-Supply Operation

GND to the negative supply. Figure 4 shows an example of dual-supply operation. Single- and dual-supply performance are equivalent. For either single- or dual-supply operation, drive CLK and $\overline{SHDN}$ from GND (V- in dual-supply operation) to V_{DD}. For ±5V dual-supply applications, use the MAX291–MAX297.

Input Signal Amplitude Range

The optimal input signal range is determined by observing the voltage level at which the total harmonic distortion plus noise (THD+N) is minimized for a given corner frequency. The *Typical Operating Characteristics* show graphs of the devices' THD+N response as the input signal's peak-to-peak amplitude is varied. These measurements are made with OS and COM biased at mid-supply.

Anti-Aliasing and Post-DAC Filtering

When using the MAX7401/MAX7405 for anti-aliasing or post-DAC filtering, synchronize the DAC and the filter clocks. If the clocks are not synchronized, beat frequencies may alias into the passband.

The high clock-to-corner frequency ratio (100:1) also eases the requirements of pre- and post-SCF filtering. At the input, a lowpass filter prevents the aliasing of frequencies around the clock frequency into the passband. At the output, a lowpass filter attenuates the clock feedthrough.

A high clock-to-corner frequency ratio allows a simple RC lowpass filter, with the cutoff frequency set above the SCF corner frequency, to provide input anti-aliasing and reasonable output clock attenuation.

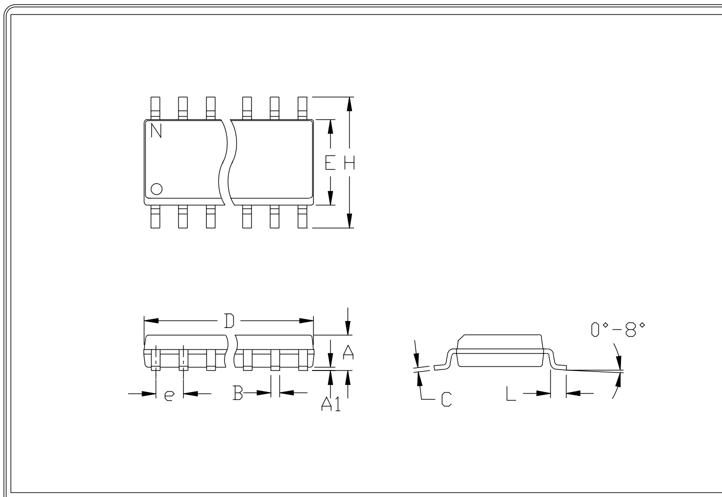
Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. These nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 1 lists the MAX7401/MAX7405's typical harmonic-distortion values with a 10kΩ load at T_A = +25°C.

Chip Information

TRANSISTOR COUNT: 1116

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: SOIC .150"

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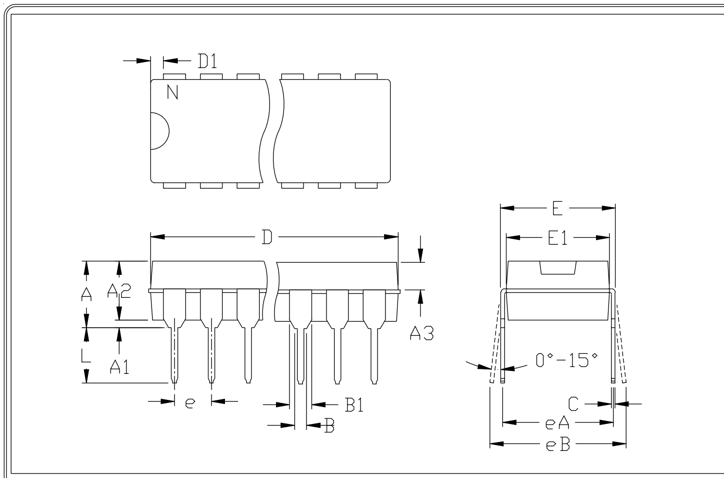
DOCUMENT CONTROL NUMBER: 21-0041 REV: A

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300"

1/1

DOCUMENT CONTROL NUMBER: 21-0043 REV: A

NOTES