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## MAX77504

## 14V Input, 3A High-Efficiency Buck Converter in WLP or QFN

### General Description

The MAX77504 is a synchronous 3A step-down DC-DC converter optimized for portable 2-cell and 3-cell battery-operated applications. The converter operates on an input supply between 2.6V and 14V. Output voltage is adjustable between 0.6V and 6V with external feedback resistors. The device features a low- $I_Q$  SKIP mode that allows excellent efficiency at light loads. The MAX77504 can be synchronized by driving the FPWM pin with an external clock.

Dedicated enable, power-OK, and FPWM pins allow simple hardware control. The SEL input easily configures switching frequency, gain, and output active discharge option. Built-in undervoltage lockout (UVLO), output active discharge, cycle-by-cycle inductor current limit, thermal shutdown, and short-circuit protection ensure safe operation under abnormal operating conditions.

The MAX77504 is offered in a small 1.7mm x 1.7mm, 16-bump, 0.4mm pitch wafer-level package (WLP) or a 2.5mm x 2.5mm, 12-lead, 0.5mm pitch flip-chip QFN (FC2QFN).

### Applications

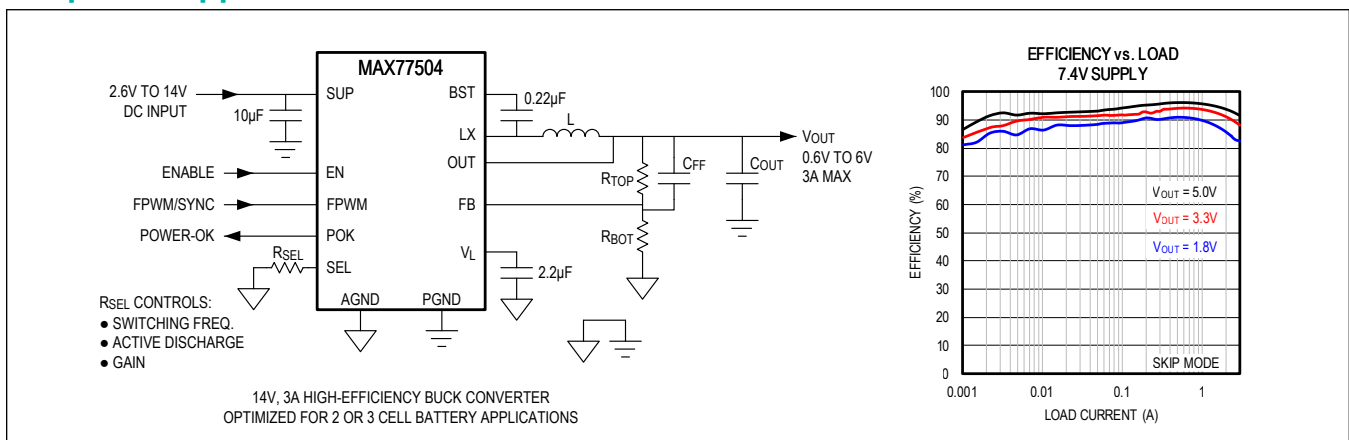
- 1- to 3-Cell Li+/Li-ion Battery-Powered Devices
- Professional Radio, Handheld Computers
- Mirrorless Cameras, DSLR, and Notebook Computers
- Portable Scanners, POS Terminals, Printers
- Space-Constrained Portable Electronics

### Benefits and Features

- 3A Single-Channel Buck Regulator
- 2.6V to 14V Input Voltage
- 0.6V to 6V Output Voltage Range
- 0.5MHz to 1.5MHz Fixed-Frequency Switching Options
- High Efficiency, Low  $I_Q$  Extends Battery Life
  - 94% Peak Efficiency at 7.4V<sub>IN</sub>, 3.3V<sub>OUT</sub> (2520 Inductor)
  - 10 $\mu$ A  $I_{SUP}$  (12V<sub>IN</sub>, 1.8V<sub>OUT</sub>)
  - OUT Powers  $V_L$  Automatically ( $V_{OUT} > 1.7V$ ) for Low  $I_Q$
- Enable Pin (EN) for Direct Hardware Control
- External Clock Synchronization Is Available Through the FPWM/SYNC Pin
- Power-OK Output (POK) Monitors  $V_{OUT}$  Quality (See [Ordering Information](#))
- Protection Features
  - Cycle-by-Cycle Inductor Current Limit
  - Short-Circuit Hiccup Mode, UVLO, and Thermal Shutdown Protection
  - Soft-Start
- FC2QFN or WLP Package Option
  - 2.5mm x 2.5mm (0.6mm max. height) 12-Lead FC2QFN, 0.5mm Pitch
  - 1.7mm x 1.7mm (0.7mm max. height) 16-Bump WLP, 0.4mm Pitch, 4 x 4 Array
- All WLP Package Bumps (Except POK) Routeable on a Non-HDI PCB

[Ordering Information](#) appears at end of data sheet.

### Simplified Application Circuit



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**Absolute Maximum Ratings**

SUP to PGND.....	-0.3V to +16V	AGND to PGND .....	-0.3V to +0.3V
LX to PGND (DC) .....	-0.3V to +16V	OUT Short-Circuit Duration.....	Continuous
EN to PGND .....	-0.3V to $V_{SUP} + 0.3V$	LX Continuous Current (Note 1) .....	3.2A <sub>RMS</sub>
BST to LX .....	-0.3V to +2.2V	Continuous Power Dissipation (Multilayer Board, $T_A = +70^\circ C$ )	
$V_L$ to PGND.....	-0.3V to +2.2V	16 WLP (derate 17.26mW/ $^\circ C$ above +70 $^\circ C$ ).....	1381mW
SEL to AGND .....	-0.3V to $V_L + 0.3V$	12 FC2QFN (derate 14.23mW/ $^\circ C$ above +70 $^\circ C$ ).....	1139mW
POK, FPWM/SYNC to PGND..	-0.3V to $V_{MIN}(V_{SUP} + 0.3V, +6V)$	Operating Junction Temperature Range.....	-40 $^\circ C$ to +125 $^\circ C$
OUT to AGND.....	-0.3V to +8V	Junction Temperature .....	+150 $^\circ C$
FB to AGND.....	-0.3V to +6V	Soldering Temperature (reflow) .....	+260 $^\circ C$

**Note 1:** LX has internal clamp diodes to PGND and SUP. Applications that forward bias these diodes should not exceed the ICs package power dissipation limits.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Package Information

16 WLP

Package Code	W161L1+1
Outline Number	<a href="#">21-100334</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	57.93°C/W

Pin 1 Indicator

1

E

Marking

A

AAAA

D

TOP VIEW

see Note 7

SIDE VIEW

COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	∅0.27 ±0.03
D	1.688 ±0.025
E	1.688 ±0.025
D1	1.20 BASIC
E1	1.20 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

A3

A2

A

FRONT VIEW

A1

S

0.05

E1

SE

e

SD

D

C

B

A

1 2 3 4

D1

∅b

0.05 (M) (S) (AB)

BOTTOM VIEW

NOTES

1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

		TITLE PACKAGE OUTLINE 16 BUMPS WLP PKG. 0.4 mm PITCH, W161L1+1	
APPROVAL	DOCUMENT CONTROL NO. 21-100334	REV. A	1/1

12 FC2QFN

Package Code	F122A2F+2
Outline Number	<a href="#">21-100406</a>
Land Pattern Number	<a href="#">90-100140</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	70.23°C/W

**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.4	---
L/F THICKNESS	A3	0.152 REF		
LEAD WIDTH	b	0.2	0.25	0.3
	b1	0.11	0.16	0.21
BODY SIZE	X	D	2.5 BSC	
	Y	E	2.5 BSC	
LEAD PITCH	e	0.5 BSC		
	e1	0.3 BSC		
LEAD LENGTH	L	0.3	0.4	0.5
	L1	0.35	0.4	0.45
	L2	1.05	1.1	1.15
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
COPLANARITY	eee	0.05		
LEAD OFFSET	bbb	0.1		

**NOTES**

- REFER TO JEDEC MO-220
- COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD
- BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JQET SPECS.
- FINISH: Cu/EP: Sn8~20s
- MAXIM PKG CODE : F122A2F-2
- MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.

**maxim integrated.**

TITLE:  
PACKAGE OUTLINE, 12L FC2QFN  
2.5x2.5x0.55mm

APPROVAL	DOCUMENT CONTROL NO. 21-100406	REV. A	1/1
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-DRAWING NOT TO SCALE-

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).



## Electrical Characteristics

( $V_{SUP} = V_{EN} = 12V$ ,  $V_{FPWM} = 0V$  (SKIP mode),  $V_L = 1.8V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values are at  $T_A = T_J = +25^{\circ}C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>STEP-DOWN CONVERTER</b>							
SUP Valid Voltage Range	$V_{SUP}$			2.6		14	V
SUP Undervoltage Lockout	$V_{SUP-UVLO}$	$V_{SUP}$ rising		2.4	2.5	2.6	V
SUP Undervoltage Lockout Hysteresis					300		mV
SUP Shutdown Current	$I_{SUP-SHDN}$	$V_{EN} = 0V$ (device disabled), $T_J = -40^{\circ}C$ to $+85^{\circ}C$			1.2	3	$\mu A$
Supply Current	$I_{SUP}$	$I_{LOAD} = 0mA$ , SKIP mode	$V_{OUT} = 1.2V$ , $R_{TOP} = 49.9k\Omega$ , $R_{BOT} = 49.9k\Omega$		33		$\mu A$
			$V_{OUT} = 1.8V$ , $R_{TOP} = 46.4k\Omega$ , $R_{BOT} = 23.2k\Omega$		12		
			$V_{OUT} = 3.3V$ , $R_{TOP} = 459k\Omega$ , $R_{BOT} = 102k\Omega$		14		
		$I_{LOAD} = 0mA$ , FPWM mode, no switching		1	1.5	mA	
$V_L$ Regulator Voltage	$V_L$	$V_{SUP} = 2.3V$ to $14V$			1.8		V
$V_L$ Power Input Switch-Over Threshold	$V_{SWO}$	$V_{OUT}$ rising, 100mV hysteresis, POK = 1, $V_L$ input switches from SUP to OUT above this threshold		1.6	1.7	1.75	V
FB Voltage Accuracy	$V_{FB}$	FPWM mode	$V_{SUP} = 12V$ , $I_{LOAD} = 250mA$ , $T_J = 25^{\circ}C$	0.594	0.6	0.606	V
			$V_{SUP} = 2.6V$ to $14V$ , $I_{LOAD} = 0mA$ to $3A$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$	0.588	0.6	0.612	
FB Input Current	$I_{FB}$	$V_{FB} = 0.6V$			0.02		$\mu A$
Total Startup Time	$t_{TSU}$	Measured from EN rising edge to POK rising edge	$SFT\_STRT = 0$ (1ms ramp)		1.25	1.5	ms
High-Side DMOS On-Resistance	$R_{ON-HS}$	$V_L = 1.8V$ , $I_{LX} = 180mA$ , $V_{SUP} = 4.5V$			50	100	m $\Omega$
Low-Side DMOS On-Resistance	$R_{ON-LS}$	$V_L = 1.8V$ , $I_{LX} = 180mA$ , $V_{SUP} = 4.5V$			27	54	m $\Omega$
High-Side DMOS Peak Current Limit	$I_{LX-PLIM}$			3.6	4	4.4	A
Low-Side DMOS Valley Current Threshold	$I_{LX-VALLEY}$	Output overloaded ( $V_{OUT} < 67\%$ of target), threshold below where on-times are allowed to start			2		A

**Electrical Characteristics (continued)**

( $V_{SUP} = V_{EN} = 12V$ ,  $V_{FPWM} = 0V$  (SKIP mode),  $V_L = 1.8V$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , typical values are at  $T_A = T_J = +25^\circ C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
High-Side DMOS Minimum Current Threshold	$I_{LX-PK-MIN}$	Inductor current ramps to at least $I_{LX-PK-MIN}$ in SKIP mode		500		mA	
Low-Side DMOS Zero-Crossing Threshold	$I_{ZX}$	SKIP mode		40		mA	
Low-Side DMOS Negative Current Limit Threshold	$I_{NEG}$	mFPWM Mode		-1.5		A	
Maximum Duty Cycle	$D_{MAX}$	Dropout condition ( $V_{SUP} < V_{OUT}$ target); on-times extend for 16 clocks before LX drives low for 200ns to refresh $C_{BST}$		99		%	
Switching Frequency	$f_{SW}$	FPWM mode, $T_J = -40^\circ C$ to $+85^\circ C$	FSW[1:0] = 0b00	0.475	0.5	0.525	MHz
			FSW[1:0] = 0b01	0.7125	0.75	0.7875	
			FSW[1:0] = 0b10	0.95	1	1.05	
			FSW[1:0] = 0b11	1.425	1.5	1.575	
Minimum Switching Frequency	$F_{SW-MIN}$	SKIP mode	1.2	1.43	1.7	kHz	
Soft-Short Output Voltage Monitor Threshold	$V_{OUT-OVRLD}$	Expressed as a percentage of target $V_{OUT}$		66.7		%	
Output-Overloaded Retry Timer	$t_{RETRY}$	Switching stopped because output voltage has fallen to less than 67% of target and 15 LX cycles ended by current limit; time before converter attempts to soft-start again		15		ms	
Active Discharge Resistor	$R_{AD}$	Between OUT and PGND, buck output disabled, ADEN = 1		100		$\Omega$	
<b>POWER-OK OUTPUT (POK)</b>							
POK Threshold	$V_{POK\_RISE}$	$V_{OUT}$ rising, expressed as a percentage of $V_{OUT-REG}$	90	92	94	%	
	$V_{POK\_FALL}$	$V_{OUT}$ falling, expressed as a percentage of $V_{OUT-REG}$	88	90	92		
POK Debounce Timer	$t_{POK-DB}$	$V_{OUT}$ rising or falling		12		$\mu s$	
POK Leakage Current	$I_{POK}$	POK = high (high impedance), $V_{POK} = 5V$ , $T_A = 25^\circ C$			1	$\mu A$	
POK Low Voltage	$V_{POK}$	POK = low, sinking 1mA			0.4	V	
<b>ENABLE INPUT (EN)</b>							
EN Logic-High Threshold	$V_{EN\_HI}$		1.1			V	
EN Logic-Low Threshold	$V_{EN\_LO}$				0.4	V	
EN Leakage Current	$I_{EN}$	$V_{EN} = V_{SUP} = 14V$		0.1	1	$\mu A$	

**Electrical Characteristics (continued)**

( $V_{SUP} = V_{EN} = 12V$ ,  $V_{FPWM} = 0V$  (SKIP mode),  $V_L = 1.8V$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , typical values are at  $T_A = T_J = +25^\circ C$ , unless otherwise noted.) (Note 2)

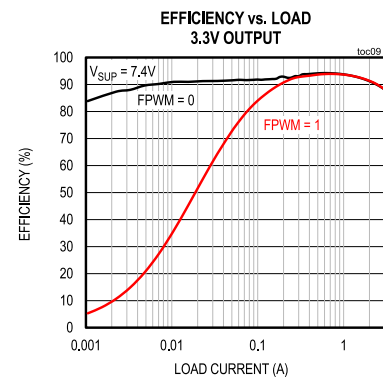
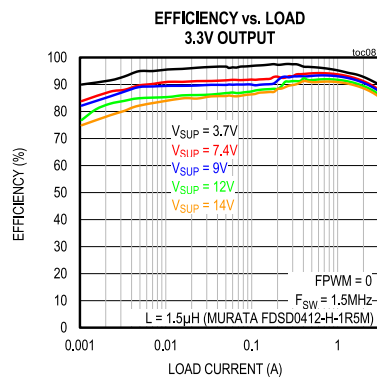
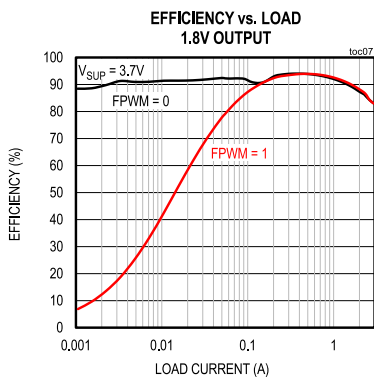
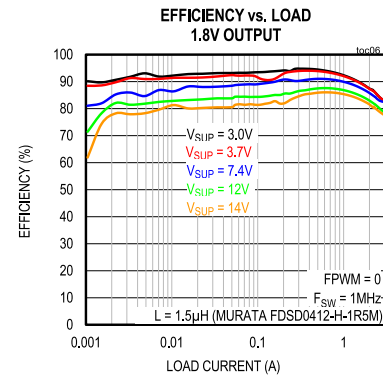
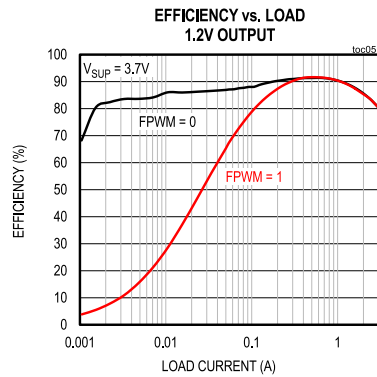
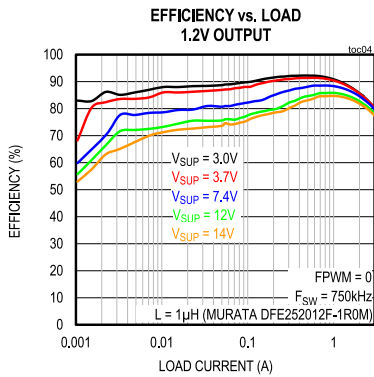
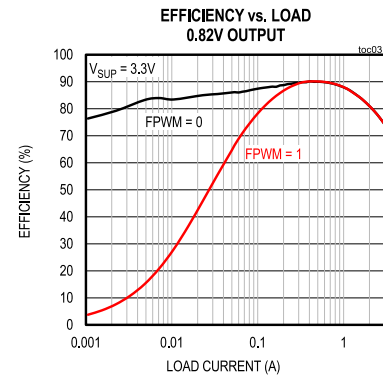
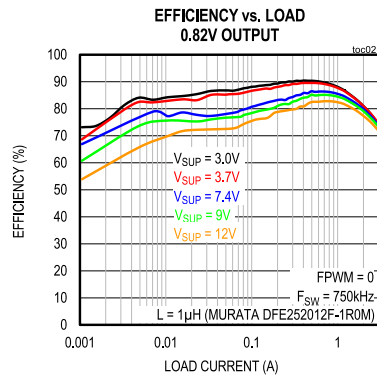
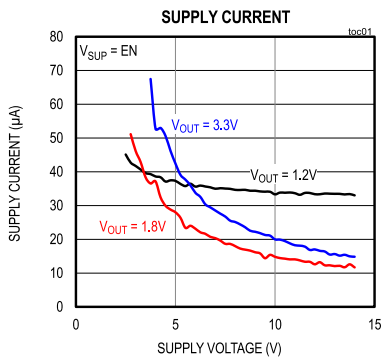
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>FPWM/SYNC</b>							
FPWM/SYNC Logic-High Threshold	$V_{FPWM\_HI}$			1.1			V
FPWM/SYNC Logic-Low Threshold	$V_{FPWM\_LO}$					0.4	V
Valid Synchronization Range (Note 3)	$F_{SYNC-VALID}$	$T_J = -40^\circ C$ to $+85^\circ C$	$FSW[1:0] = 0b00$ (0.5MHz)	0.394		0.690	MHz
			$FSW[1:0] = 0b01$ (0.75MHz)	0.526		0.920	
			$FSW[1:0] = 0b10$ (1.0MHz)	0.789		1.38	
			$FSW[1:0] = 0b11$ (1.5MHz)	1.05		1.84	
<b>THERMAL PROTECTION</b>							
Thermal Shutdown	$T_{SHDN}$	Junction temperature rising			+165		$^\circ C$
Thermal Shutdown Hysteresis					+15		$^\circ C$

**Note 2:** The MAX77504 is tested under pulsed load conditions such that  $T_A \approx T_J$ . Min/Max limits are 100% production tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range are guaranteed by design and characterization using statistical quality control methods. Note that the maximum ambient temperature consistent with this specification is determined by specific operating conditions, board layout, rated package thermal impedance, and other environmental factors.

**Note 3:** Synchronization specifications are only valid for product variants that include the feature. See the [Ordering Information](#) table to find the availability of synchronization for each orderable part number.

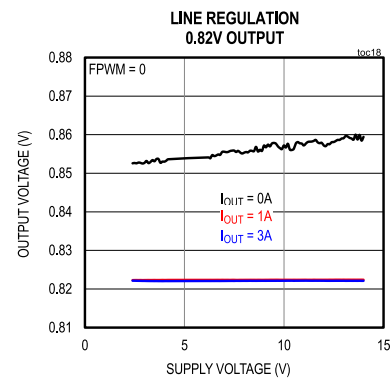
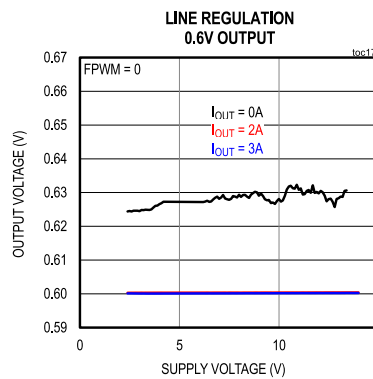
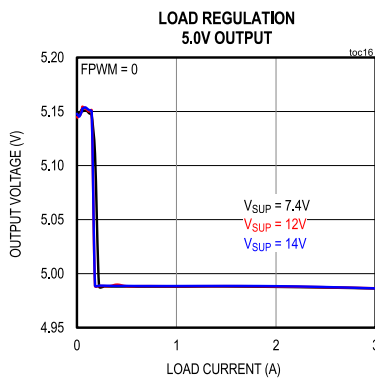
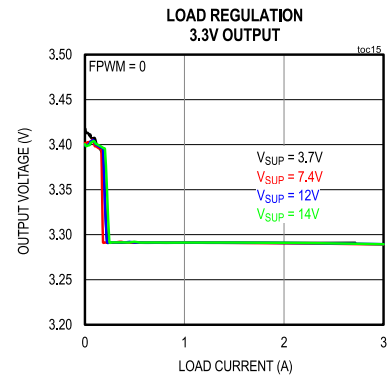
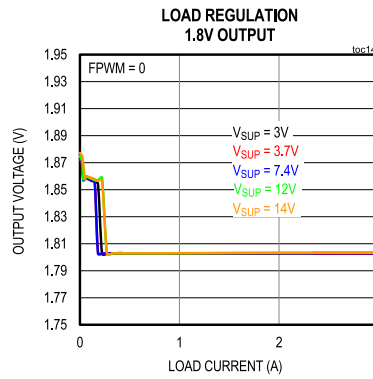
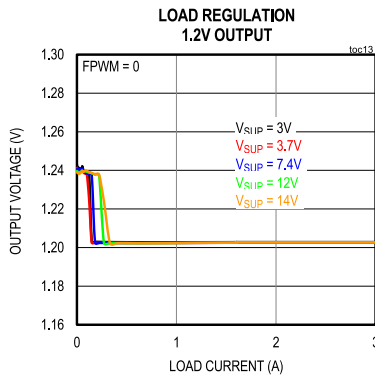
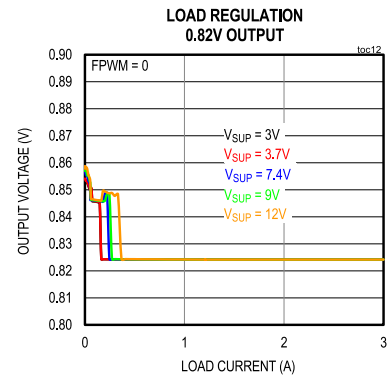
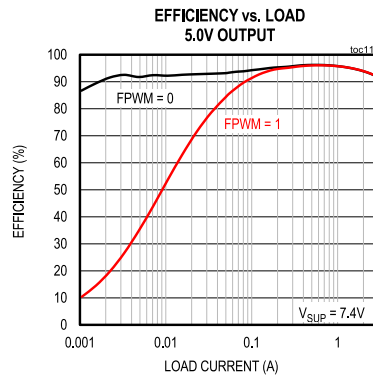
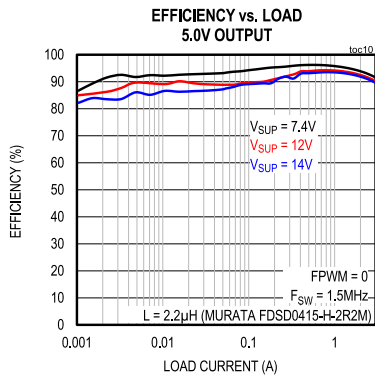
Typical Operating Characteristics

( $V_{SUP} = 7.4V$ ,  $V_{OUT} = 3.3V$ ,  $FPWM = 0$ ,  $I_{LX-PLIM} = 4A$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. See the [Typical Application Circuits](#) section for each  $V_{OUT}$  configuration.)



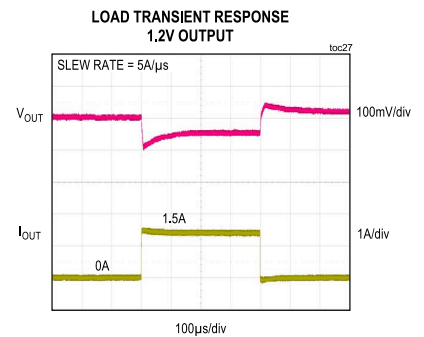
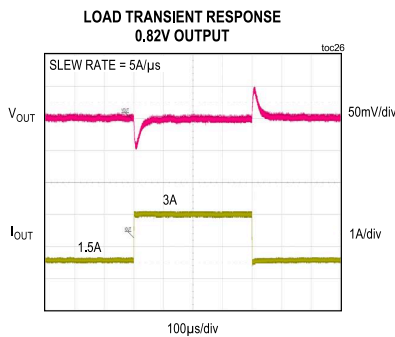
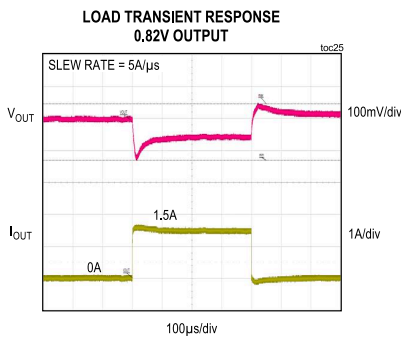
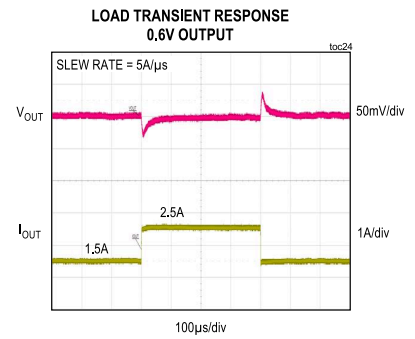
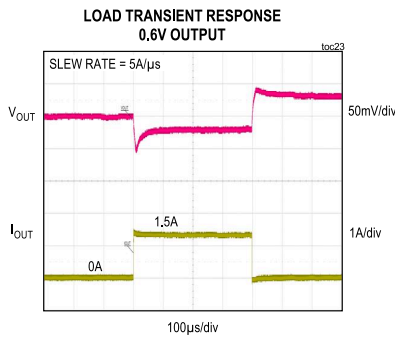
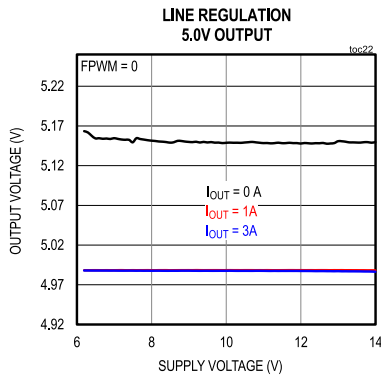
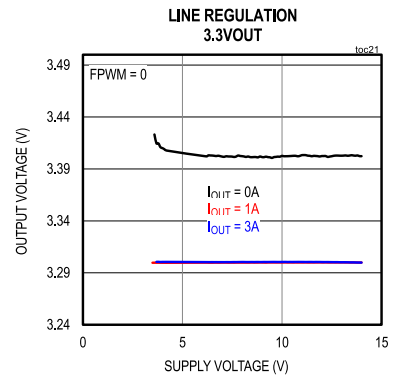
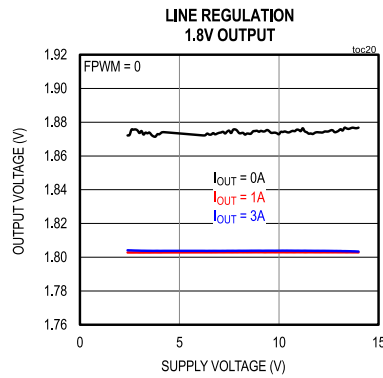
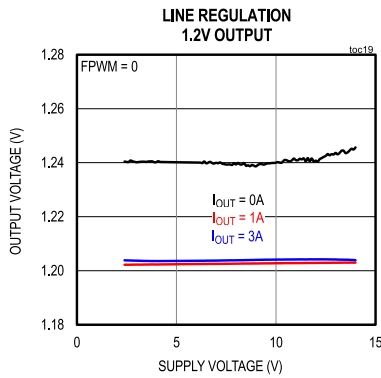
Typical Operating Characteristics (continued)

( $V_{SUP} = 7.4V$ ,  $V_{OUT} = 3.3V$ ,  $FPWM = 0$ ,  $I_{LX-PLIM} = 4A$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. See the [Typical Application Circuits](#) section for each  $V_{OUT}$  configuration.)



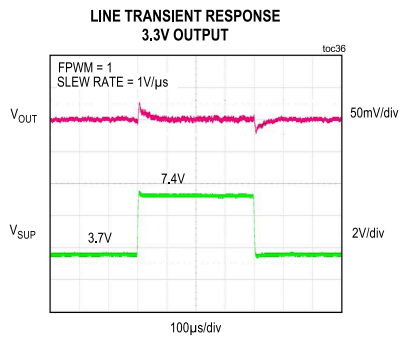
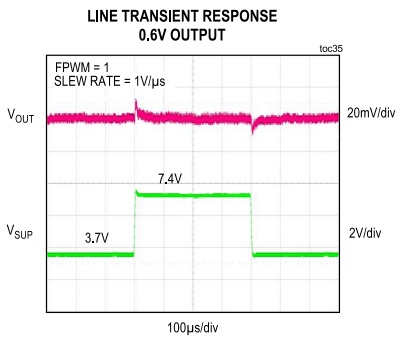
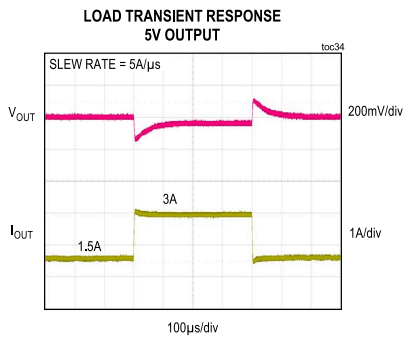
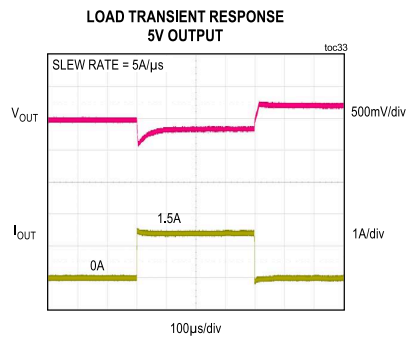
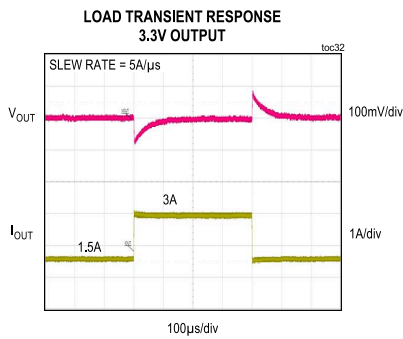
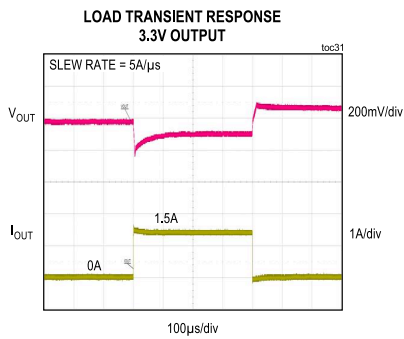
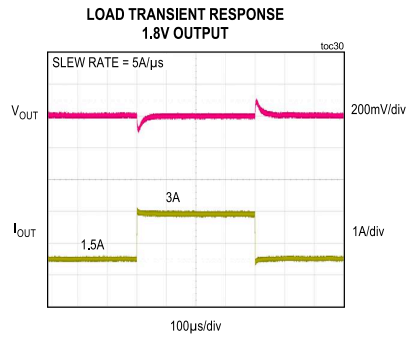
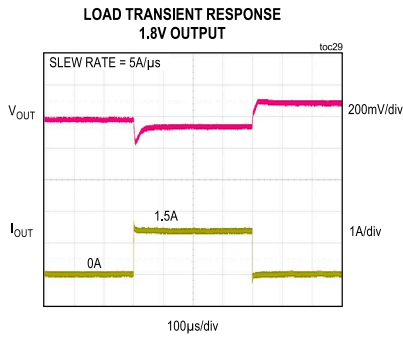
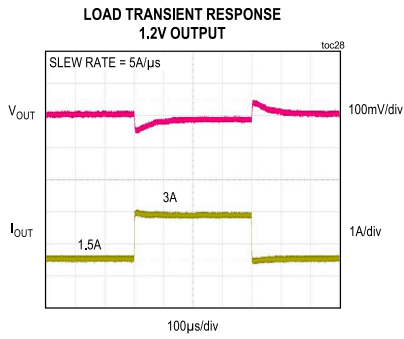
Typical Operating Characteristics (continued)

( $V_{SUP} = 7.4V$ ,  $V_{OUT} = 3.3V$ ,  $FPWM = 0$ ,  $I_{LX-PLIM} = 4A$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. See the [Typical Application Circuits](#) section for each  $V_{OUT}$  configuration.)



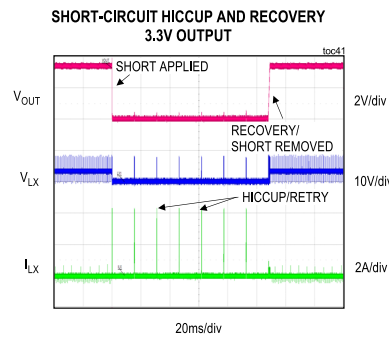
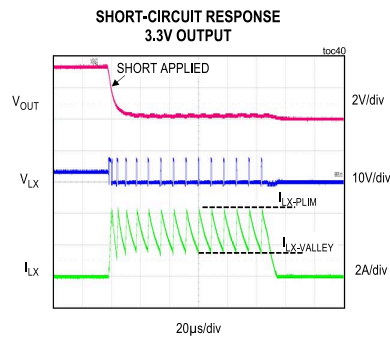
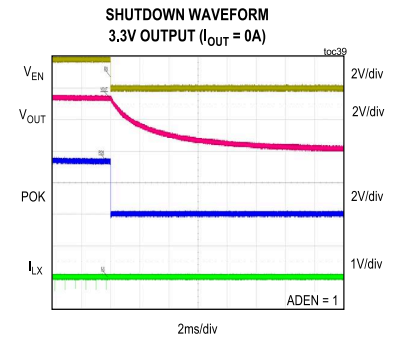
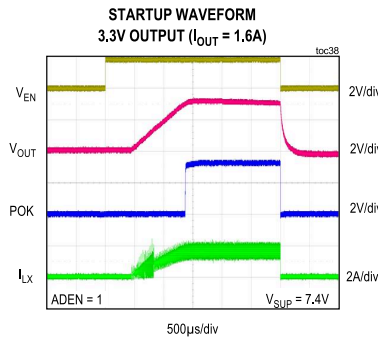
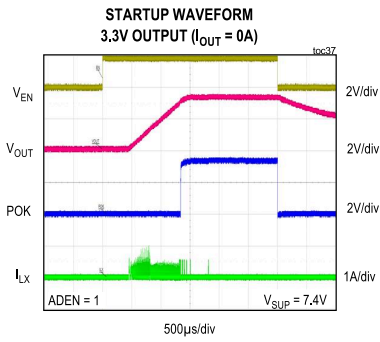
Typical Operating Characteristics (continued)

( $V_{SUP} = 7.4V$ ,  $V_{OUT} = 3.3V$ ,  $FPWM = 0$ ,  $I_{LX-PLIM} = 4A$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. See the [Typical Application Circuits](#) section for each  $V_{OUT}$  configuration.)



Typical Operating Characteristics (continued)

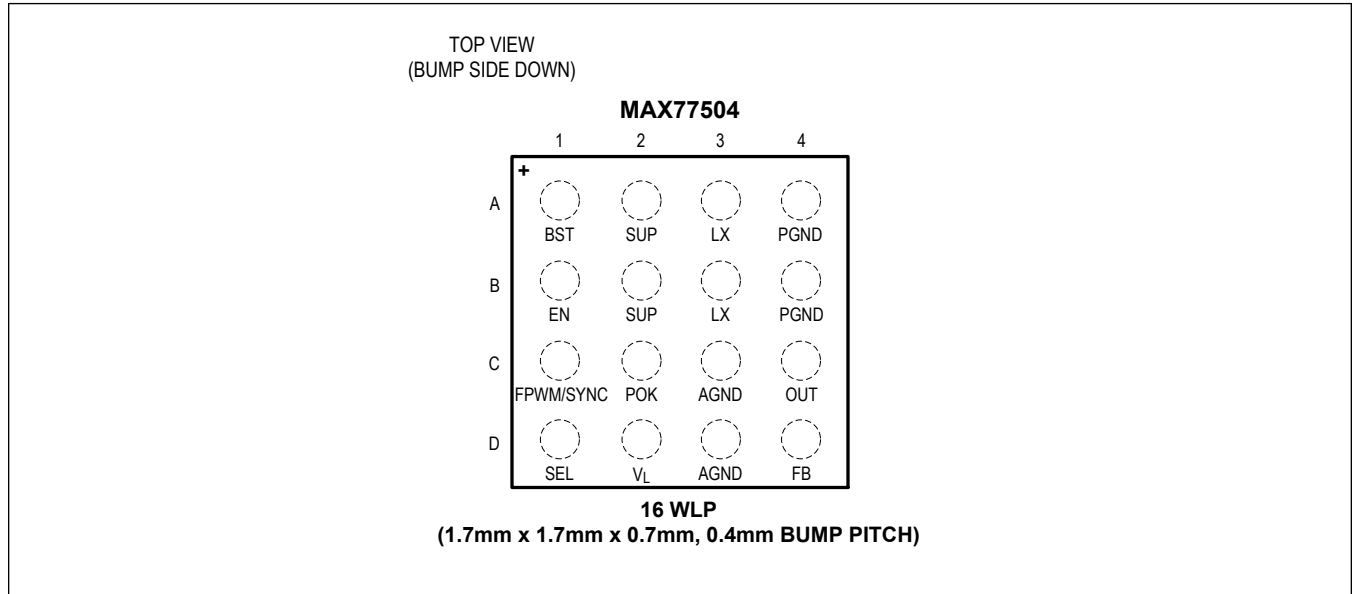
( $V_{SUP} = 7.4V$ ,  $V_{OUT} = 3.3V$ ,  $FPWM = 0$ ,  $I_{LX-PLIM} = 4A$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. See the [Typical Application Circuits](#) section for each  $V_{OUT}$  configuration.)



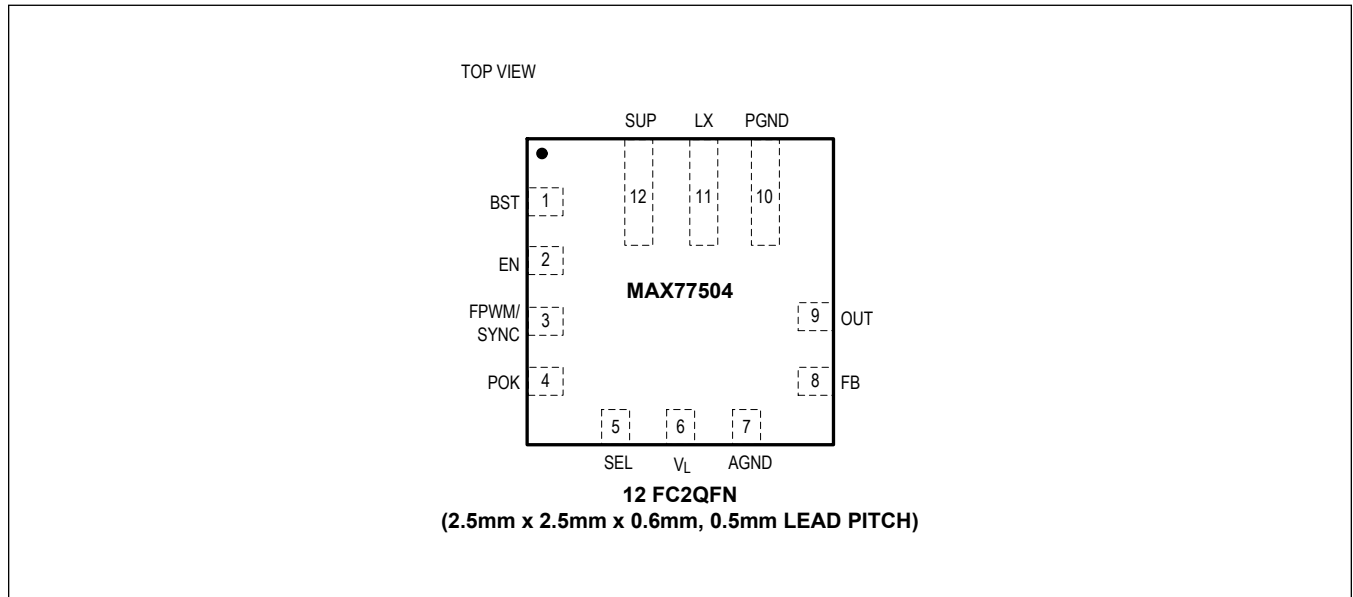


Bump/Pin Configurations

16 WLP



12 FC2QFN



## Bump/Pin Descriptions

PIN		NAME	FUNCTION
16 WLP	12 FC2QFN		
A1	1	BST	High-Side FET Driver Supply. Connect a 0.22 $\mu$ F ceramic capacitor between BST and LX.
A2, B2	12	SUP	Buck Supply Input. Bypass to PGND with a 10 $\mu$ F ceramic capacitor as close to the IC as possible.
A3, B3	11	LX	Switching Node. LX is high-impedance when the converter is disabled.
A4, B4	10	PGND	Power Ground. Connect to AGND on the PCB.
C3, D3	7	AGND	Quiet Ground. Connect to PGND on the PCB.
C2	4	POK	Open-Drain, Power-OK Output. An external pullup resistor (10k $\Omega$ to 100k $\Omega$ ) is required to use this pin. Leave this pin unconnected if unused.
D2	6	V <sub>L</sub>	Low-Voltage Internal IC Supply Output. Powered from SUP or OUT depending on V <sub>OUT</sub> . Bypass to AGND with a 2.2 $\mu$ F ceramic capacitor. Do not load this pin externally.
D4	8	FB	Feedback Sense Input. Connect a resistor voltage divider between the converter's output and AGND to set the output voltage. Do not route FB close to sources of EMI or noise.
B1	2	EN	Enable Input. Drive EN above V <sub>EN_HI</sub> to enable the buck output. Drive EN to PGND to disable. EN is compatible with the SUP voltage domain.
C1	3	FPWM/SYNC	<p>Buck Mode Control and External Clock Synchronization Input. Drive FPWM/SYNC above V<sub>FPWM_HI</sub> to enable forced-PWM mode. Connect to ground to enable SKIP mode. See the <a href="#">Mode Control (FPWM)</a> section for more information.</p> <p>Provide an external clock signal with a frequency inside the valid range (f<sub>SYNC-VALID</sub>) to enable externally synchronized forced-PWM mode while the buck is enabled. See the <a href="#">External Clock Synchronization (SYNC)</a> section for more information.</p> <p>Not all MAX77504 versions include the synchronization feature. Consult the <a href="#">Ordering Information</a>.</p>
C4	9	OUT	Output Voltage Sense Input. Connect to the buck output capacitor. Do not connect anywhere else.
D1	5	SEL	Configuration Selection Input. Connect a $\pm$ 1% selection resistor (R <sub>SEL</sub> ) between SEL and AGND to configure MAX77504 options. See the <a href="#">Configuration Selection Resistor (SEL)</a> section for more information.

Detailed Description

The MAX77504 is a small, high-efficiency 3A step-down (buck) DC-DC converter. The step-down converter uses synchronous rectification and internal current-mode compensation. The buck operates on a supply voltage between 2.6V and 14V. Output voltage is set by external feedback resistors between 0.6V and 6V. The buck utilizes an ultra-low quiescent current ( $I_Q$ ) SKIP mode ( $10\mu A$  typ for  $1.8V_{OUT}$ ) that maintains very high efficiency at light loads.

Buck Regulator Control Scheme

The step-down converter uses a PWM peak current-mode control scheme with a high-gain architecture. Peak current-mode control provides precise control of the inductor current on a cycle-by-cycle basis and inherent compensation for supply voltage variation.

On-times (MOSFET Q1 on) are started by a fixed-frequency clock and terminated by a PWM comparator. See Figure 1. When an on-time ends (starting an off-time) current conducts through the low-side MOSFET (Q2 on). Shoot-through current from SUP to PGND is avoided by introducing a brief period of dead time between switching events when neither MOSFET is on. The inductor current is conducted through Q2's intrinsic body diode during dead time.

The PWM comparator regulates  $V_{OUT}$  by controlling duty cycle. The negative input of the PWM comparator is a voltage proportional to the actual output voltage error. The positive input is the sum of the current-sense signal through MOSFET Q1 and a slope-compensation ramp. The PWM comparator ends an on-time when the error voltage becomes less than the slope-compensated current-sense signal. On-times begin again due to a fixed-frequency clock pulse. The controller's compensation components and current-sense circuits are integrated. This reduces the risk of routing sensitive control signals on the PCB.

A high-gain architecture is present in the controller design. The feedback uses an integrator to eliminate steady-state output voltage error while the converter is conducting heavy loads. See the *Typical Operating Characteristics* sections for information about the converter's typical voltage regulation behavior versus load.

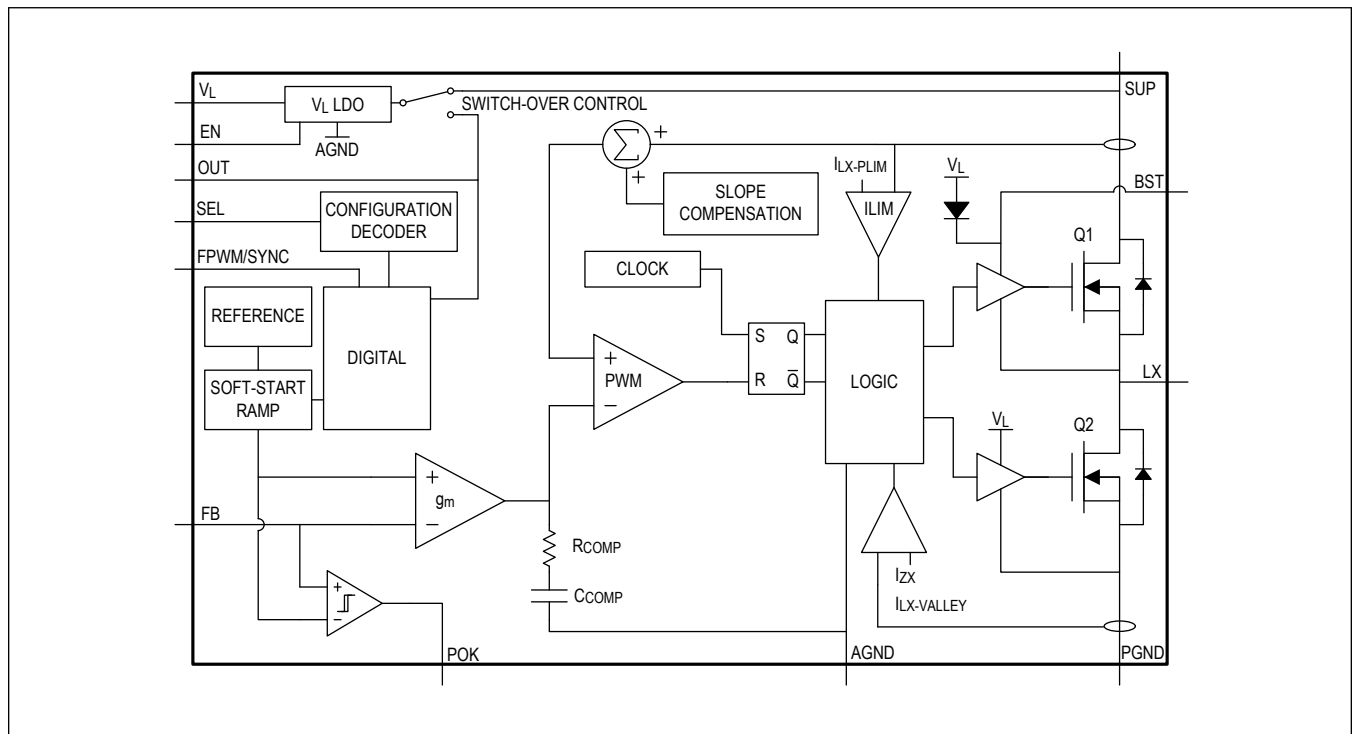


Figure 1. Buck Control Scheme Diagram

### Mode Control (FPWM)

FPWM is an active-high digital input that controls the buck converter's mode. Raise FPWM above  $V_{FPWM\_HI}$  to enable forced-PWM (FPWM) mode. Lower FPWM to AGND to enable SKIP mode. Always drive this pin to prevent mode chatter.

Some MAX77504 versions use the FPWM input for external clock synchronization (FPWM/SYNC). See the [Ordering Information](#) to find which MAX77504 part numbers include the synchronization feature. See the [External Clock Synchronization \(SYNC\)](#) section of the data sheet for a functional description of this feature.

### SKIP Mode

SKIP mode causes discontinuous inductor current at light loads by forcing the low-side MOSFET (Q2) off if inductor current falls below  $I_{ZX}$  (40mA typ) during an off-time. This prevents inductor current from sourcing back to the input (SUP) and enables high-efficiency by reducing the total number of switching cycles required to regulate the output voltage.

When the load is very light and the output voltage is in regulation, then the converter automatically transitions to standby mode. In this mode, the LX node is high-impedance and the converter's internal circuit blocks are deactivated to reduce  $I_Q$  consumption. Output voltage typically rests 2.5% above the regulation target in standby mode. A low-power comparator monitors the output voltage during standby. The converter reactivates and starts switching again when  $V_{OUT}$  drops below 102% of regulation target. Inductor current ramps to at least  $I_{LX-PK-MIN}$  (500mA typ) upon every switching cycle.

### FPWM Mode

The low-side MOSFET (Q2) current-limit threshold is  $I_{NEG}$  (-1.5A typ) in FPWM mode, which allows the converter to switch at constant frequency at light loads. The buck has the best possible load-transient response in this mode at the cost of higher  $I_Q$  consumption. Use FPWM for applications that do not require low- $I_Q$  and/or when heavy load transients are expected. Switching frequency is fixed by an internal oscillator in FPWM mode. See [Table 1](#).

**Table 1. Buck Switching Frequency**

FSW[1:0]	SWITCHING FREQUENCY ( $f_{SW}$ ) (MHz)
00	0.5
01	0.75
10	1.0
11	1.5

A configuration resistor between SEL and AGND programs FSW[1:0]. See the [Configuration Selection Register \(SEL\)](#) section and [Table 2](#).

### External Clock Synchronization (SYNC)

Select MAX77504 versions use the FPWM/SYNC input for external clock synchronization. See the [Ordering Information](#) to find which MAX77504 part numbers include the synchronization feature.

Provide an external clock signal to FPWM/SYNC with a frequency inside the valid range ( $f_{SYNC-VALID}$ ) to enable externally synchronized forced-PWM (FPWM) mode. The valid lockable range shifts depending on the chosen internal switching frequency (FSW[1:0] programmed by  $R_{SEL}$ ). See the FPWM/SYNC section of the [Electrical Characteristics](#) table for the guaranteed valid lock ranges versus FSW[1:0] choice. External synchronization can only happen after the converter enables, soft-start finishes, and the external signal's frequency is valid.

An internal digital state machine (drawn in [Figure 2](#)) evaluates the external clock frequency on a cycle-by-cycle basis to determine if the signal's frequency is within the valid range. If the logic detects 16 consecutive cycles within the valid range then the buck immediately synchronizes the beginning of the next on-time with the rising edge of the external clock on FPWM/SYNC. The converter maintains on-time synchronization as long as each subsequent external clock cycle remains within the valid range. If the logic detects a single invalid external clock cycle (a rising edge that comes too fast or too slow), then the converter immediately reverts back to its internal oscillator (FSW[1:0] programmed by  $R_{SEL}$ ). The converter returns to SKIP mode when FPWM/SYNC asserts low for the debounce time,  $t_{DB-SKIP}$  (5 $\mu$ s typ).

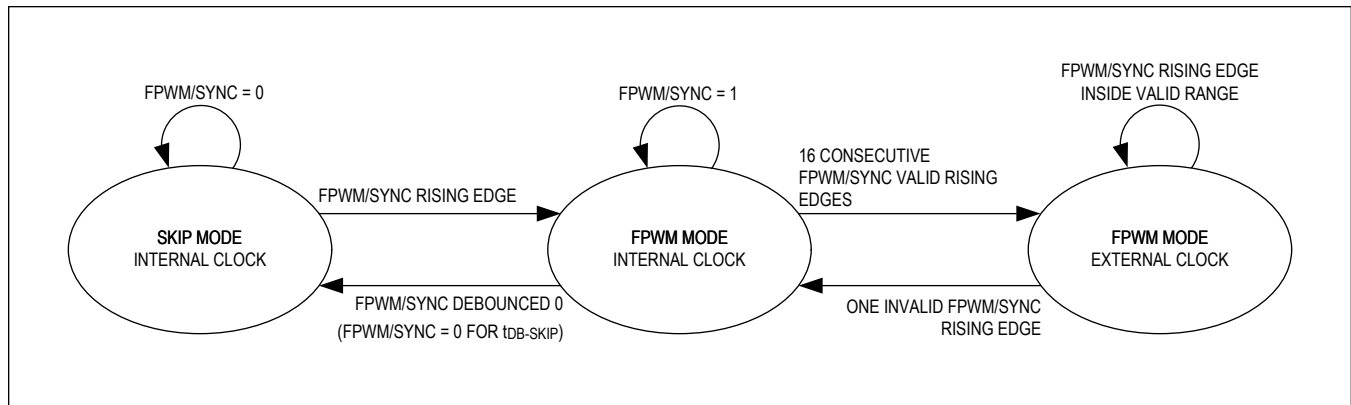


Figure 2. External Clock Synchronization Behavioral State Machine

Applications using the external synchronization function must consider minimum on-time restrictions when providing the external clock. The [Switching Frequency Selection](#) section details these restrictions. Minimum on-time restrictions are valid regardless of whether the switching frequency is controlled with an internal or external clock.

### Buck Enable Control (EN)

Raise the EN pin voltage above  $V_{EN\_HI}$  (or tie to SUP) to enable the buck output. Lower EN to PGND to disable.

### $V_L$ Regulator

An integrated 1.8V linear regulator ( $V_L$ ) provides power to low-voltage internal circuit blocks and switching FET gate drivers.

SUP powers  $V_L$  when  $V_{OUT}$  is set less than the switch-over threshold ( $V_{SWO}$ , 1.7V typical). If  $V_{OUT} > V_{SWO}$ , then the  $V_L$  regulator power input switches from SUP to OUT after the buck soft-start ramp finishes and POK = 1. Switching  $V_L$ 's input to OUT utilizes the buck's high-efficiency to power the linear regulator (as opposed to SUP) and improves the device's total power efficiency.

Do not load  $V_L$  externally. The  $V_L$  regulator activates whenever EN is high. Connect a 2.2 $\mu$ F ceramic capacitor from  $V_L$  to ground on the PCB.

### Soft-Start

The device has an internal soft-start timer ( $t_{SS}$ ) that controls the ramp time of the output as the converter is starting. Soft-start limits inrush current during buck startup. The converter soft-starts every time the buck enables, exits a UVLO condition, and/or retries from an overcurrent (hiccup) or overtemperature condition. 1ms ramp time is available and only programmable at the factory.

### Power-OK (POK) Output

The device features an active-high, open-drain POK output to monitor the output voltage. POK requires an external pullup resistor (typically 10k $\Omega$  to 100k $\Omega$ ). POK goes high (high-impedance) after the buck converter output increases above 92% ( $V_{POK\_RISE}$ ) of the target regulation voltage and the soft-start ramp is done. POK goes low when the output drops below 90% ( $V_{POK\_FALL}$ ) of target or when the buck is disabled.

### Output Voltage Connection (OUT)

OUT is an analog power input used to sense the buck's output voltage and optionally power the dedicated internal  $V_L$  regulator.

- The buck adjusts its own internal compensation ramp based on  $V_{OUT}$ .
- The  $V_L$  regulator's power input switches to OUT when  $V_{OUT} > V_{SWO}$ . See the [V<sub>L</sub> Regulator](#) section.
- The active discharge resistor ( $R_{AD}$ ) discharges the buck's output through the OUT pin when the buck is disabled and ADEN = 1. See the [Active Discharge Resistor](#) section.

Connect OUT to the buck converter's nearest output capacitor. Do not connect OUT anywhere else. See the [PCB Layout Guidelines](#) section for a layout example.

### Configuration Selection Resistor (SEL)

Connect a  $\pm 1\%$  tolerance (or better) configuration selection resistor ( $R_{SEL}$ ) between SEL and AGND to configure five bits of options decoded in [Table 2](#). See the [Design Procedure \(Choosing R<sub>SEL</sub>\)](#) section for the procedure to select the best configuration options for the buck converter's intended application.

The device evaluates the resistance between SEL and AGND whenever SUP is valid and EN transitions from logic 0 to 1. The decoded value of  $R_{SEL}$  latches until the next EN rising edge.

### Active Discharge Resistor

The device integrates a  $100\Omega$  active discharge resistor ( $R_{AD}$ ) between OUT and PGND that discharges the output capacitor when the buck is disabled. This function is enabled/disabled using the ADEN bit. Use a configuration resistor between SEL and AGND to program ADEN. See [Table 2](#).

$R_{AD}$  discharges the output capacitor for 15ms when ADEN = 1 and the buck is disabled. The OUT pin returns to a high-impedance state after this time.

### Short-Circuit Protection and Hiccup Mode

The device has fault protection designed to protect itself from abnormal conditions. If the output is overloaded, cycle-by-cycle current limit prevents inductor current from increasing beyond  $I_{LX-PLIM}$ .

The buck stops switching if  $V_{OUT}$  falls to less than 67% of target and 15 consecutive on-times are ended by current limit. After switching stops, the buck waits for  $t_{RETRY}$  before attempting to soft-start again (hiccup mode). While  $V_{OUT}$  is less than 67% of target, the converter prevents new on-times if the inductor current has not fallen below  $I_{LX-VALLEY}$ . This prevents inductor current from increasing uncontrollably due to the short-circuited output.

### Thermal Shutdown

The device has an internal thermal protection circuit that monitors die temperature. The temperature monitor disables the buck if the die temperature exceeds  $T_{SHDN}$  ( $165^\circ\text{C}$  typ). The buck soft-starts again after the die temperature cools by approximately  $15^\circ\text{C}$ .

## Applications Information

### Buck Enable Options

The MAX77504 offers two control options using the EN pin. See [Figure 3](#) for suggested methods of controlling the buck converter.

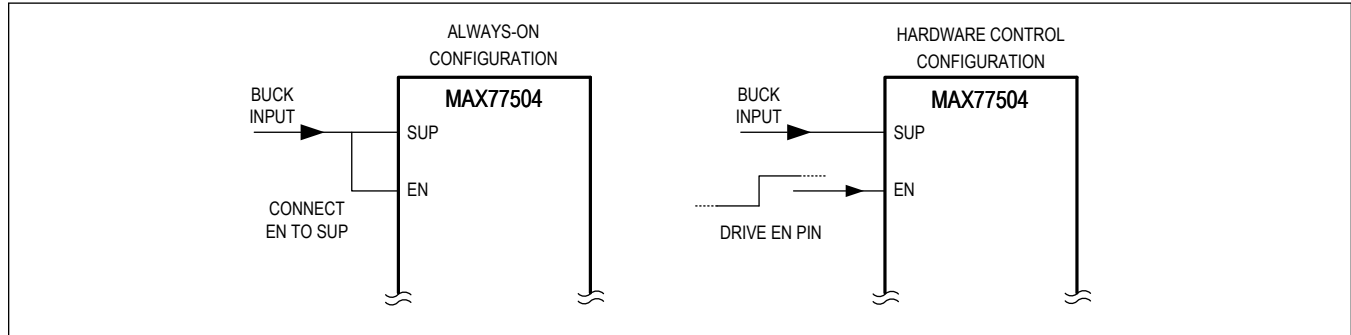


Figure 3. Buck Enable Options

#### Always-On

Strap the EN pin to SUP to configure the device in an always-on configuration. See [Figure 3](#) (left). The buck converter activates whenever  $V_{SUP}$  is valid and  $T_J < T_{SHDN}$ .

#### Hardware Control

Drive the EN pin externally to control the buck. See [Figure 3](#) (right). The buck converter activates whenever  $V_{EN} > V_{EN\_HI}$  (1.1V min),  $T_J < T_{SHDN}$ , and  $V_{SUP}$  is valid.

#### FPWM/SYNC Clock Pulse Width Requirements

Applications using an external clock should choose a clock with close to 50% duty cycle. Keep clock duty cycles within  $\pm 25\%$  of the clock period. For example, if the input clock has a period of  $1\mu\text{s}$  (i.e., 1MHz), a 50% duty cycle has a 500ns pulse width and the clock should not exceed  $\pm 250\text{ns}$  away from this. Valid on times in this specific case include 250ns to 750ns within the  $1\mu\text{s}$  period.

**Design Procedure (Choosing R<sub>SEL</sub>)**

The configuration selection resistor (R<sub>SEL</sub>) sets five bits of configuration options decoded in [Table 2](#). Choose R<sub>SEL</sub>[4:0] carefully by following the procedure outlined in this section. See the [Typical Application Circuits](#) section for a list of known good R<sub>SEL</sub> choices for common applications. [Contact Maxim](#) for help or questions with this procedure.

**Table 2. Resistor-Set Configuration Bits**

RSEL[4:0]		NAME	DESCRIPTION	DECODE
MSB	Bit 4	FSW[1:0]	Switching Frequency Control. Sets f <sub>SW</sub> . Lower f <sub>SW</sub> requires more C <sub>OUT</sub> to maintain stability.	00 = 0.5MHz 01 = 0.75MHz 10 = 1.0MHz 11 = 1.5MHz
	Bit 3			
	Bit 2	GAIN[1:0]	Mid-band Gain Control. Sets R <sub>COMP</sub> . Higher R <sub>COMP</sub> increases gain and improves transient response, but requires more C <sub>OUT</sub> to maintain stability.	00 = 75kΩ 01 = 100kΩ 10 = 150kΩ 11 = 200kΩ
	Bit 1			
LSB	Bit 0	ADEN	Active discharge resistor enable.	0 = Disabled 1 = Enabled

Program these bits by choosing a configuration selection resistor (R<sub>SEL</sub>) with a tolerance of ±1% or better using lookup [Table 3](#).

Follow the design procedure to determine R<sub>SEL</sub>[4:0]. Use [Table 3](#) to choose the corresponding R<sub>SEL</sub> value.

**Table 3. Configuration Selection Resistor (R<sub>SEL</sub>) Lookup Table**

R <sub>SEL</sub> (Ω) → RSEL[4:0]		
95.3Ω or SHORT → 0x00	1620Ω → 0x0B	30900Ω → 0x16
200Ω → 0x01	1870Ω → 0x0C	36500Ω → 0x17
309Ω → 0x02	2150Ω → 0x0D	42200Ω → 0x18
422Ω → 0x03	2490Ω → 0x0E	48700Ω → 0x19
536Ω → 0x04	2870Ω → 0x0F	56200Ω → 0x1A
649Ω → 0x05	3740Ω → 0x10	64900Ω → 0x1B
768Ω → 0x06	8060Ω → 0x11	75000Ω → 0x1C
909Ω → 0x07	12400Ω → 0x12	86600Ω → 0x1D
1050Ω → 0x08	16900Ω → 0x13	100000Ω → 0x1E
1210Ω → 0x09	21500Ω → 0x14	115000Ω or OPEN → 0x1F
1400Ω → 0x0A	26100Ω → 0x15	

For example, choose a 30.9kΩ (±1% TOL) resistor to program R<sub>SEL</sub>[4:0] to 0x16. 0x16 (0b10110) decodes with the following configuration:

- FSW[1:0] = 0b10 (1MHz switching frequency)
- GAIN[1:0] = 0b11 (200kΩ R<sub>COMP</sub>)
- ADEN = 0b0 (active discharge disabled)

[Table 3](#) indicates that a 30.9kΩ selection resistor selects code 0b10110 (0x16).

The device evaluates R<sub>SEL</sub> whenever SUP is valid and EN transitions from logic 0 to 1. The decoded value of R<sub>SEL</sub> is latched until the next EN rising edge.



**Switching Frequency Selection**

See the [Typical Application Circuits](#) section of the data sheet for a list of known good switching frequency choices for common output voltages.

Program the converter's switching frequency ( $f_{SW}$ ) using the external selection resistor ( $R_{SEL}$ ) to set the bits in FSW[1:0]. See [Table 2](#), bits 3 and 4.

The converter's minimum on-time ( $t_{ON-MIN}$ ) limits the maximum  $f_{SW}$  choice. The required on-time ( $t_{ON(REQ)}$ ) to regulate a desired output voltage must be greater than the converter's minimum on-time to ensure stable operation.

$$t_{ON(REQ)} \geq t_{ON-MIN}$$

Large step-down ratios (high  $V_{IN}$ , low  $V_{OUT}$ ) result in low duty cycles and require short on-times. High  $F_{SW}$  (short switching period) results in shorter on-times compared to lower  $F_{SW}$  (long switching period). Generally, fast switching frequency converters are desired due to their low output voltage ripple, small external component size, and high closed-loop bandwidth.

Determine the application's target output voltage ( $V_{OUT}$ ) and maximum expected input voltage ( $V_{IN(MAX)}$ ). Start with the highest  $F_{SW}$  option (1.575MHz with tolerance) and compute the on-time required for stable operation ( $t_{ON(REQ)}$ ) using Equation 1.

**Equation 1:**

$$t_{ON(REQ)} = \frac{V_{OUT}}{V_{IN(MAX)} \times F_{SW}}$$

Compare  $t_{ON(REQ)}$  with  $t_{ON-MIN}$  (100ns max). If  $t_{ON(REQ)}$  is less than 100ns, then reduce the  $F_{SW}$  to the next slowest option and recompute. Always consider  $f_{SW}$  with tolerance using the guaranteed upper limit. See the [Electrical Characteristics](#) table for more information.

If the slowest  $f_{SW}$  choice (525kHz with tolerance) results in a required on-time that is less than  $t_{ON-MIN}$ , then reduce the application's maximum expected input voltage using external methods.

**Example A (9V<sub>IN</sub> to 3.3V<sub>OUT</sub>)**

Choose  $f_{SW}$  for a 3.3V power supply operating from a 2s Li+ battery stack (9V max).

- Target  $V_{OUT} = 3.3V$
- $V_{IN(MAX)} = 9V$

Try the highest switching frequency first (1.5MHz typ, 1.575MHz max). Use Equation 1 to compute required on-time ( $t_{ON(REQ)}$ ):

$$t_{ON(REQ)} = \frac{3.3V}{9V \times 1.575MHz} = 232.8ns \text{ (OK)}$$

The choice of 1.5MHz typical switching frequency is OK because  $t_{ON(REQ)}$  is greater than the upper limit of  $t_{ON-MIN}$  (100ns max).

**Example B (12V<sub>IN</sub> to 1.8V<sub>OUT</sub>)**

Choose  $f_{SW}$  for a 1.8V power supply operating from a 12V ( $\pm 5\%$ ) supply rail.

- Target  $V_{OUT} = 1.8V$
- $V_{IN(MAX)} = 12V + 5\% = 12.6V$

Try the highest switching frequency first (1.5MHz typ, 1.575MHz max). Use Equation 1 to compute required on-time ( $t_{ON(REQ)}$ ):

$$t_{ON(REQ)} = \frac{1.8V}{12.6V \times 1.575MHz} = 90.7ns \text{ (not OK)}$$

The choice of 1.5MHz typical switching frequency is not OK because  $t_{ON(REQ)}$  is shorter than the upper limit of  $t_{ON-MIN}$  (100ns). Choose the next slowest  $f_{SW}$  (1MHz typ, 1.05MHz max) and recompute Equation 1.

$$t_{ON(REQ)} = \frac{1.8V}{12.6V \times 1.05MHz} = 136.1ns \text{ (OK)}$$

The choice of 1MHz typical switching frequency is OK because  $t_{ON(REQ)}$  is greater than 100ns.

### Gain Selection

See the [Typical Application Circuits](#) section of the data sheet for a list of known good gain choices for common output voltages and  $C_{OUT}$  values.

Program the converter's mid-band gain by changing  $R_{COMP}$  using the GAIN[1:0] bitfield. Program GAIN[1:0] using the external selection resistor ( $R_{SEL}$ ). See [Table 2](#), bits 1 and 2.

The converter's mid-band gain is limited by the switching frequency ( $f_{SW}$ ) choice and effective output capacitance ( $C_{OUT}$ ) requirement. High gain (large  $R_{COMP}$ ) results in better transient performance but requires additional  $C_{OUT}$  for stability. Low gain (small  $R_{COMP}$ ) requires less  $C_{OUT}$  at the expense of transient performance. Generally, converters with higher gain are desired due to their fast transient response and high  $V_{OUT}$  regulation quality versus disturbances.

The choice of  $R_{COMP}$  and  $C_{OUT}$  must not allow the closed-loop unity-gain bandwidth ( $f_{BW}$ ) of the converter to exceed 20% of the switching frequency.

$$f_{BW} \leq 0.2 \times f_{SW}$$

### SUP Capacitor Selection

Choose the input capacitor ( $C_{SUP}$ ) to be a 10 $\mu$ F nominal ceramic decoupling capacitor and place it as close to the SUP pin as possible. Larger values improve the decoupling of the buck converter, but increase inrush current from the voltage supply when connected.  $C_{SUP}$  reduces the current peaks drawn from the input power source during buck operation and reduces switching noise in the system. The ESR/ESL of  $C_{SUP}$  and its series PCB trace should be very low. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to Application Note 5527: [Temperature and Voltage Variation of Ceramic Capacitors, or Why Your 4.7 \$\mu\$ F Capacitor Becomes a 0.33 \$\mu\$ F Capacitor](#) for more information.

### Output Capacitor Selection

Choose an output capacitance ( $C_{OUT}$ ) based on the transient performance requirements with a minimum of 8 $\mu$ F effective capacitance for stable operation.

Effective  $C_{OUT}$  is the actual capacitance value seen by the buck output during operation. Choose effective  $C_{OUT}$  carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias.

See the [Typical Application Circuits](#) section for recommended output capacitors for each use case.

Larger values of  $C_{OUT}$  (above the required effective minimum) improve load transient performance, but increase the input surge currents during soft-start and output voltage changes. The output filter capacitor must meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. Calculate output voltage ripple ( $V_{RIPPLE(P-P)}$ ) to ensure the requirements are met:

$$V_{RIPPLE(P-P)} = (LIR) / (8 \times f_{SW} \times C_{OUT})$$

where LIR is the inductor current ripple. Compute LIR with Equation 2.

Equation 2:

$$LIR = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where  $V_{IN}$  is the application's input voltage and  $f_{SW}$  is the switching frequency. See [Table 1](#).

After taking careful consideration of the output voltage ripple, finalize the selection of the output capacitance based on the transient performance requirements. See the [Typical Application Circuits](#) section for recommended output capacitors for each use case that have a load transient performance of  $\pm 5\%$  overshoot and undershoot with a 1.5A load step (5A/ $\mu$ s slew rate).

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

### Inductor Selection

Choose an inductor with a saturation current greater than or equal to the maximum peak current limit ( $I_{LX-PLIM}$ ). Inductors with lower saturation current and higher DCR ratings tend to be physically small. Higher values of DCR reduce buck efficiency. Choose the RMS current rating of the inductor (the current at which temperature rises appreciably) based on the system's expected load current.

Choose an inductor value based on the  $V_{OUT}$  setting. See [Table 4](#).

**Table 4. Inductor Value vs. Output Voltage**

$V_{OUT}$ RANGE	INDUCTOR VALUE ( $\mu$ H)	SUGGESTED COMPONENT PART NUMBERS*
$V_{OUT} \leq 1.3V$	1	MURATA DFE252012F-1R0M MURATA DFE252010F-1R0M SAMSUNG CIGT252010EH1R0MNE COILCRAFT XGL4020-102ME
$1.3V < V_{OUT} \leq 4.5V$	1.5	MURATA DFE252012F-1R5M MURATA FDSD0412-H-1R5M TDK SPM3015T-1R5M-LR COILCRAFT XGL4020-152ME
$V_{OUT} > 4.5V$	2.2	MURATA FDSD0415-H-2R2M COILCRAFT XGL4020-222ME

\*List compiled circa 2019. Always consider the most recent inductor offerings for new designs to achieve best possible MAX77504 circuit performance.

The chosen inductor value (L) should ensure that the peak inductor ripple current ( $I_{PEAK}$ ) is below the high-side MOSFET peak current limit ( $I_{LX-PLIM}$ , 4A typ) so that the buck can maintain voltage regulation over load.

Use Equation 3 and Equation 4 to compute  $I_{PEAK}$ . If  $I_{PEAK}$  is greater than the limit ( $I_{LX-PLIM}$ ), then increase the inductor value.

#### Equation 3:

$$I_{P-P} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

#### Equation 4:

$$I_{PEAK} = I_{LOAD} + \frac{I_{P-P}}{2}$$

where  $I_{LOAD}$  is the buck's output current in the particular application (3A max),  $V_{IN(MAX)}$  is the application's largest expected input voltage (up to 14V), and  $f_{SW}$  is the chosen switching frequency. See the [Switching Frequency Selection](#) section.

**Setting the Output Voltage**

The IC uses external feedback resistors (R<sub>TOP</sub> and R<sub>BOT</sub>) to set V<sub>OUT</sub> between 0.6V and 6V. Connect a resistor divider between V<sub>OUT</sub>, FB, and AGND as shown in Figure 4. One percent tolerance resistors (or better) are recommended to maintain high output accuracy. Choose R<sub>BOT</sub> to be 10kΩ or greater. Calculate the value of R<sub>TOP</sub> for a desired output voltage with Equation 5.

**Equation 5:**

$$R_{TOP} = R_{BOT} \times \left[ \frac{V_{OUT}}{V_{FB}} - 1 \right]$$

where V<sub>FB</sub> is 0.6V and V<sub>OUT</sub> is the desired output voltage.

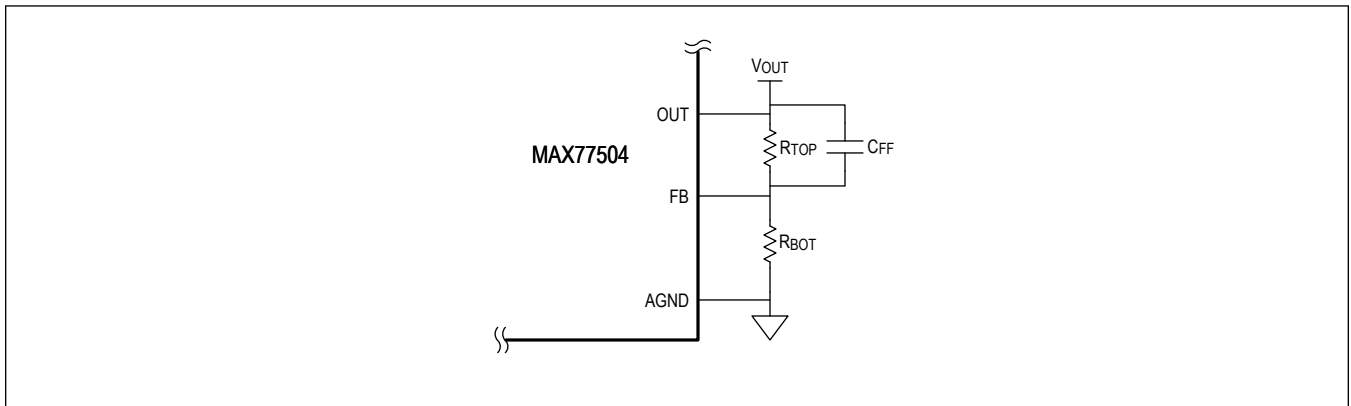


Figure 4. External Feedback Network

[Table 5](#) lists common feedback resistor combinations for various output voltages. For voltages not listed, see the closest output voltage in the table and take the RBOT value as a starting point. Then calculate RTOP using Equation 5.

See the [Typical Application Circuits](#) section of the data sheet for a list of known configurations for these output voltages.

**Table 5. Common Feedback Resistor Values**

OUTPUT VOLTAGE TARGET (V)	RTOP (kΩ)	RBOT (kΩ)
0.6	SHORT	OPEN
0.7	1.84	11.1
0.82	4.07	11.1
1.0	75	49.9
1.2	49.9	49.9
1.5	34.8	23.2
1.8	46.4	23.2
1.85	48.1	23.2
2.05	56.2	23.2
2.5	73.2	23.2
3.0	44.2	11.1
3.3	49.9	11.1
3.6	55.6	11.1
5.0	459	62.6
5.6	167	20
6.0	180	20

[Table 6](#) suggests which typical application circuit corresponds to which range of output voltages. Use this table to determine the CFF, RSEL, and COUT values.

**Table 6. Typical Application Circuit Reference**

OUTPUT VOLTAGE TARGET (V)	TYPICAL APPLICATION CIRCUIT REFERENCE
0.6	<a href="#">0.6V</a>
$0.6 < V_{OUT} \leq 0.9$	<a href="#">0.82V</a>
$0.9 < V_{OUT} \leq 1.1$	<a href="#">1.0V</a>
$1.1 < V_{OUT} \leq 1.4$	<a href="#">1.2V</a>
$1.4 < V_{OUT} \leq 2.1$	<a href="#">1.8V</a>
$2.1 < V_{OUT} \leq 2.9$	<a href="#">2.5V</a>
$2.9 < V_{OUT} \leq 4.0$	<a href="#">3.3V</a>
$4.0 < V_{OUT} \leq 5.5$	<a href="#">5.0V</a>
$5.5 < V_{OUT} \leq 6.0$	<a href="#">6.0V</a>

**PCB Layout Guidelines**

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. [Figure 5](#) shows an example PCB top-metal layout for the WLP version device, and [Figure 6](#) shows an example PCB top-metal layout for the FC2QFN version of the device.

Follow these guidelines when designing the PCB:

1. Place the SUP capacitor immediately next to the SUP pin of the device. Since the device can operate up to 1.5MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the SUP pin.
2. Place the inductor and output capacitor close to the device and keep the loop area of switching current small.
3. Make the trace between LX and the inductor short and wide. Do not take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
4. The trace between BST and C<sub>BST</sub> should be as short as possible.
5. Connect PGND and AGND together on the PCB. They must be the same net. Connect them together through a low-impedance inner PCB ground layer close to the IC.
6. Keep the power traces and load connections short and wide. Use both top and inner PCB copper floods to reduce trace impedance. This practice is essential for high-efficiency.
7. Place the V<sub>L</sub> capacitor ground next to the AGND pin.
8. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and sizes carefully. See the [Output Capacitor Selection](#) section and refer to Application Note 5527: [Temperature and Voltage Variation of Ceramic Capacitors, or Why Your 4.7µF Capacitor Becomes a 0.33µF Capacitor](#) for more information.

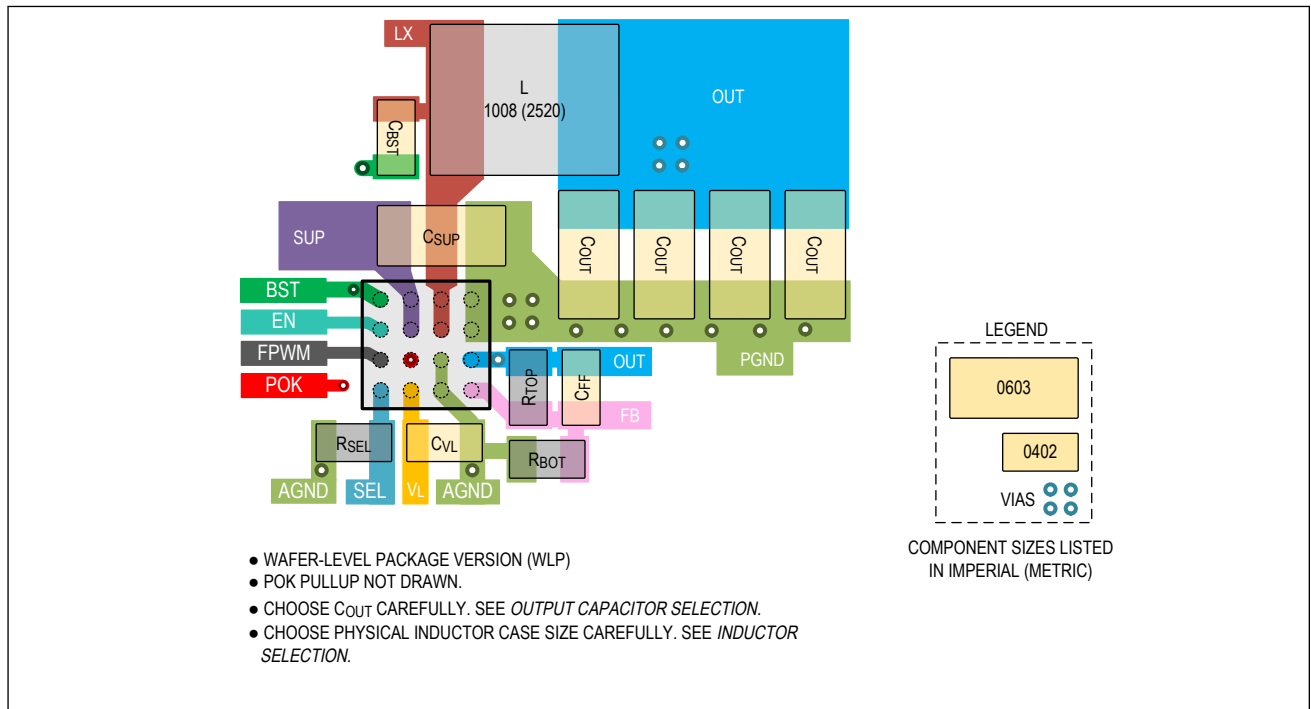


Figure 5. PCB Top-Metal and Component Layout Example (WLP Version)

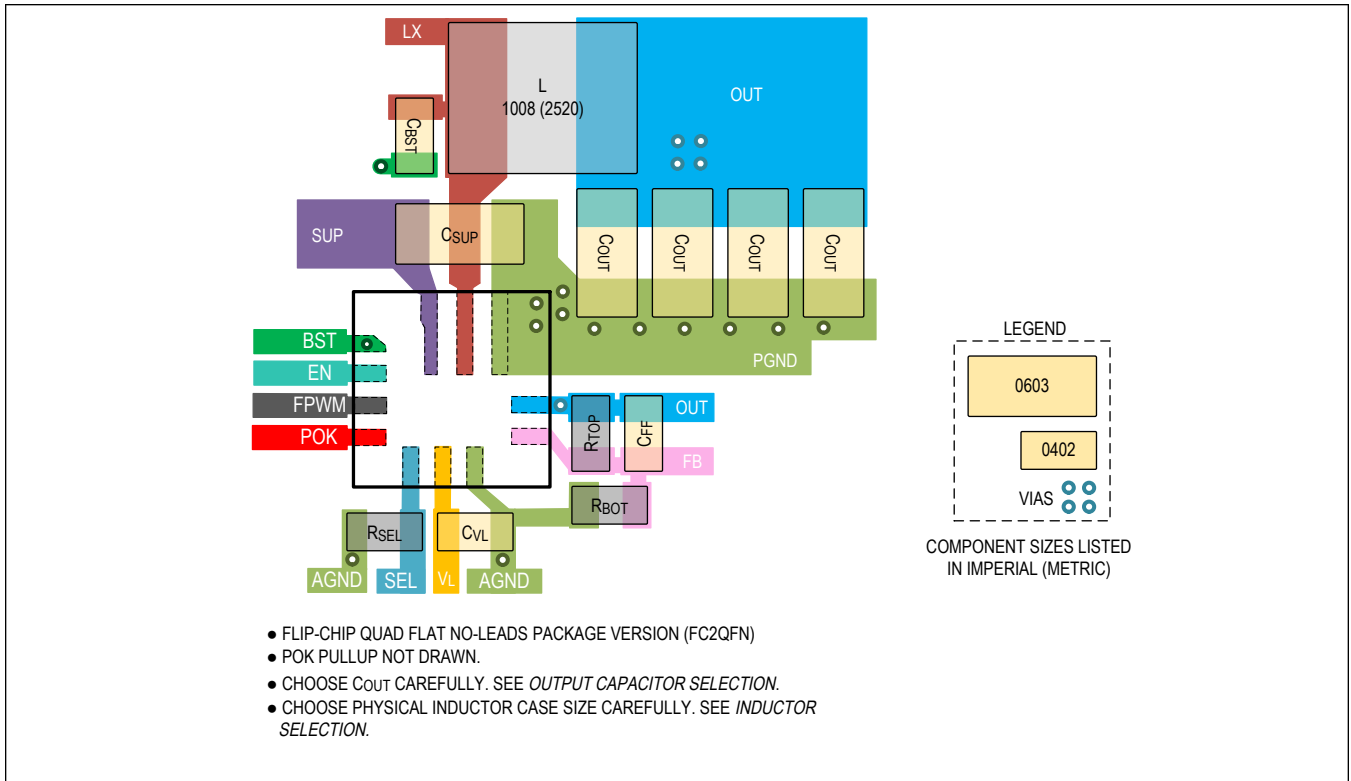


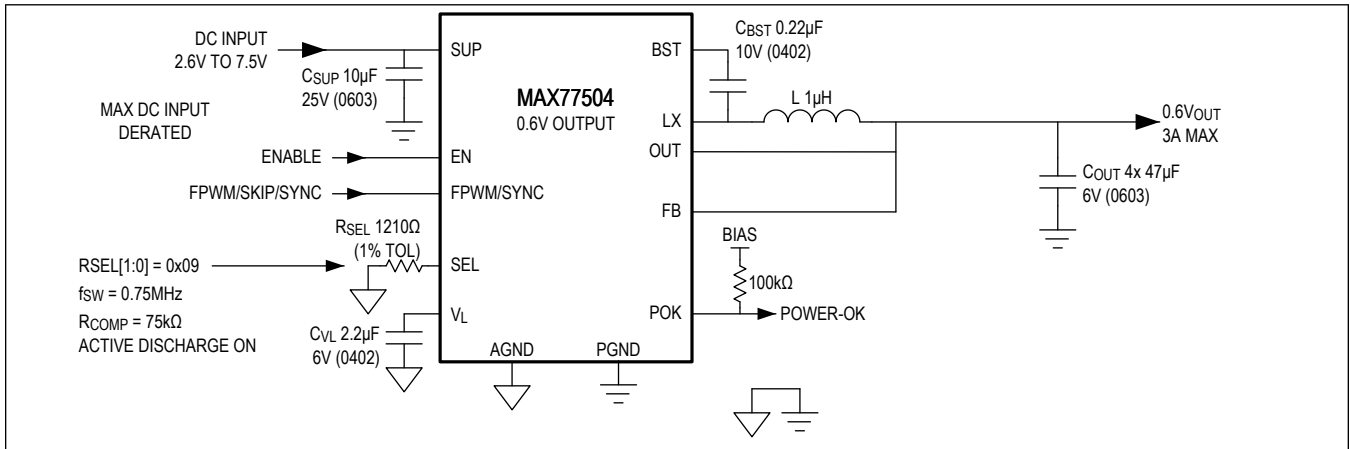
Figure 6. PCB Top-Metal and Component Layout Example (FC2QFN Version)

Typical Application Circuits

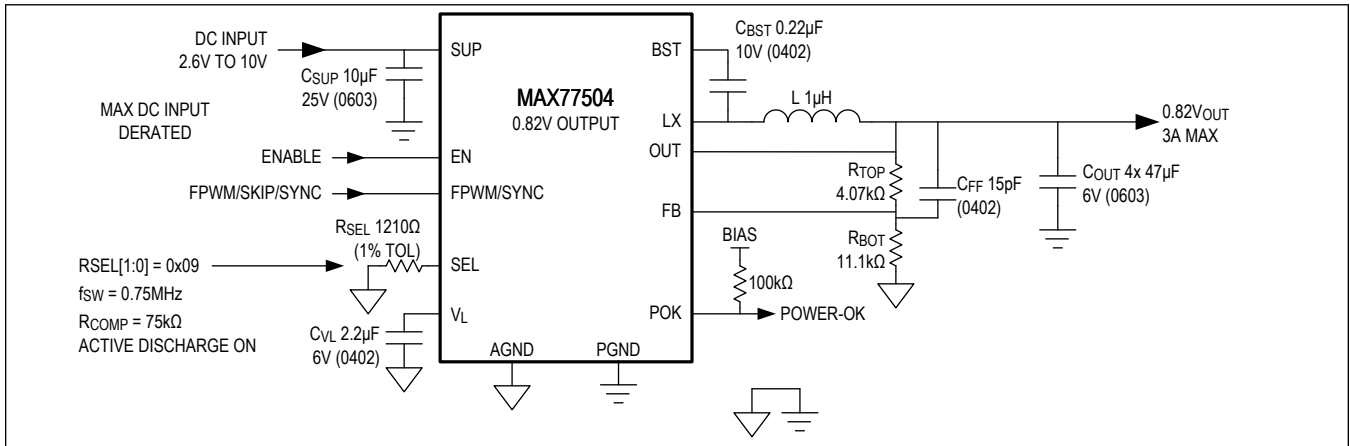
Typical Application Circuits

All output voltage use cases are configured to optimize load transient performance ( $\pm 5\%$  overshoot and undershoot at a  $5A/\mu s$  slew rate) and phase margin of at least  $45^\circ$  across the entire input voltage range specified.

0.6V Output, 0.75MHz



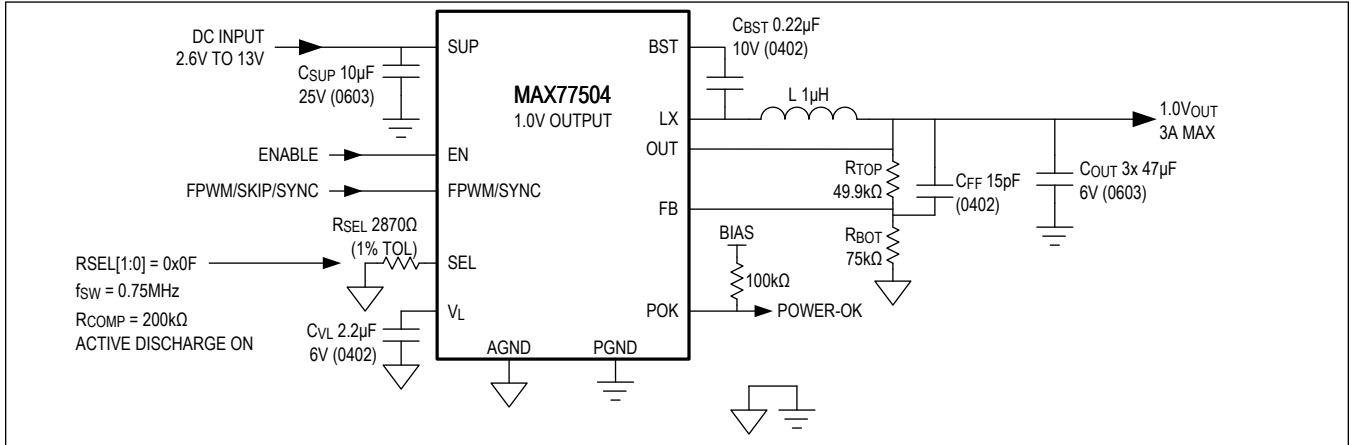
0.82V Output, 0.75MHz



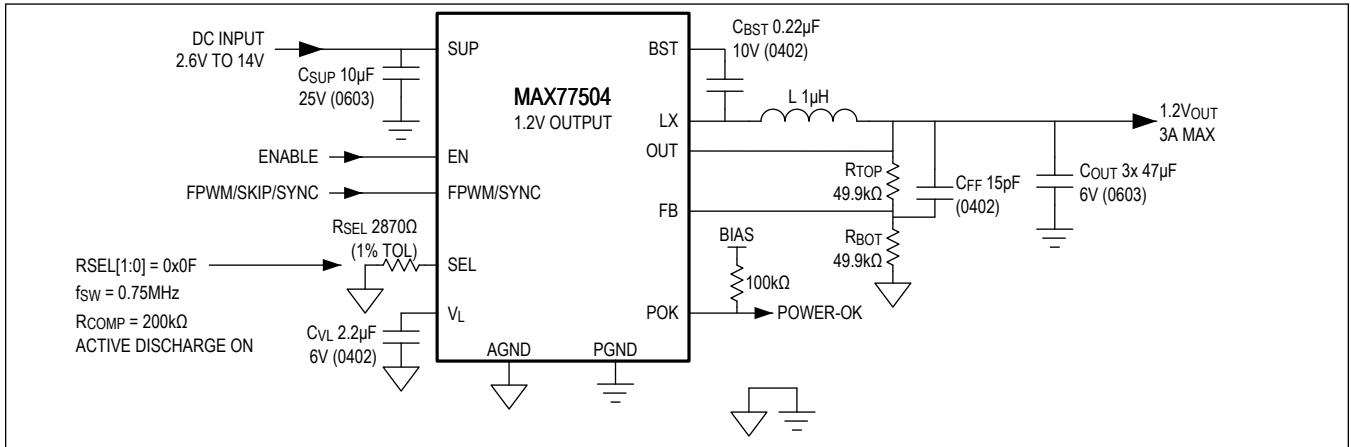


Typical Application Circuits (continued)

1.0V Output, 0.75MHz

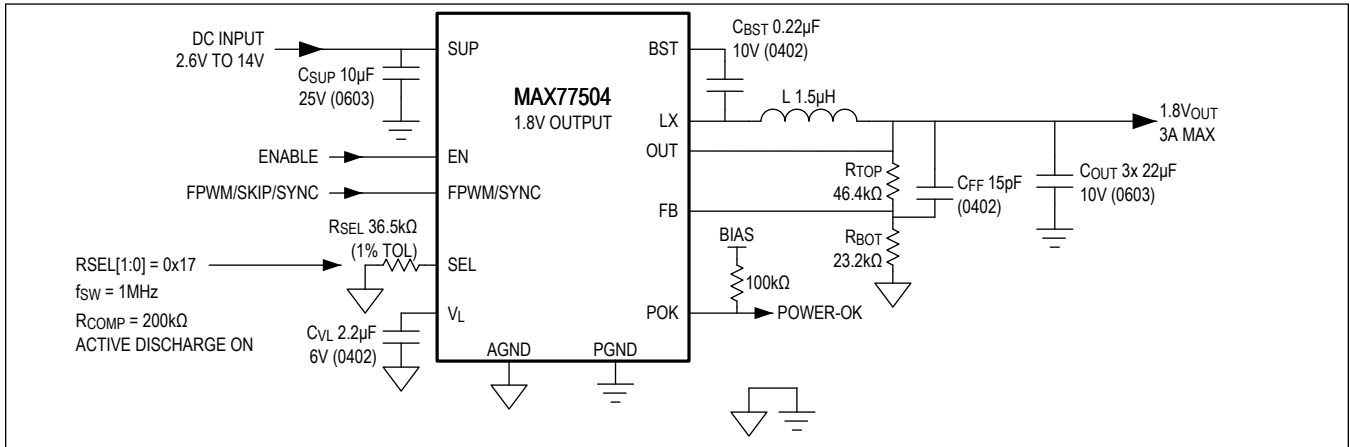


1.2V Output, 0.75MHz

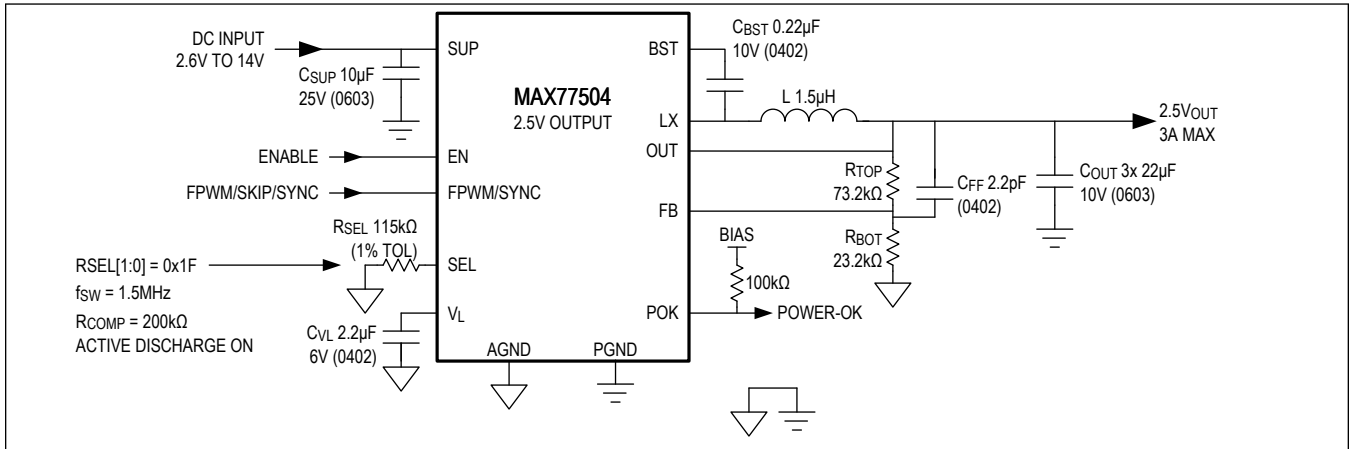


Typical Application Circuits (continued)

1.8V Output, 1MHz

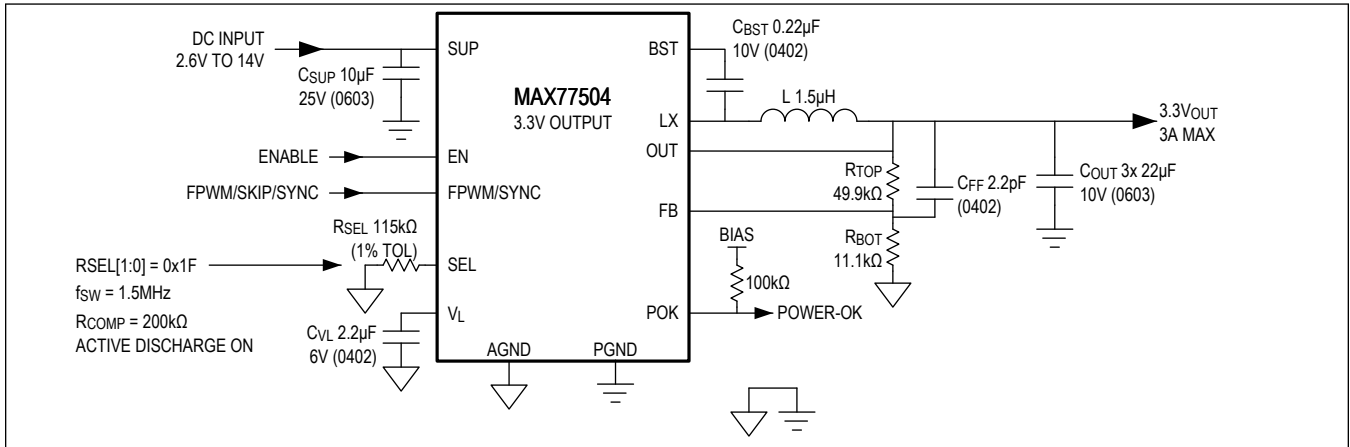


2.5V Output, 1.5MHz

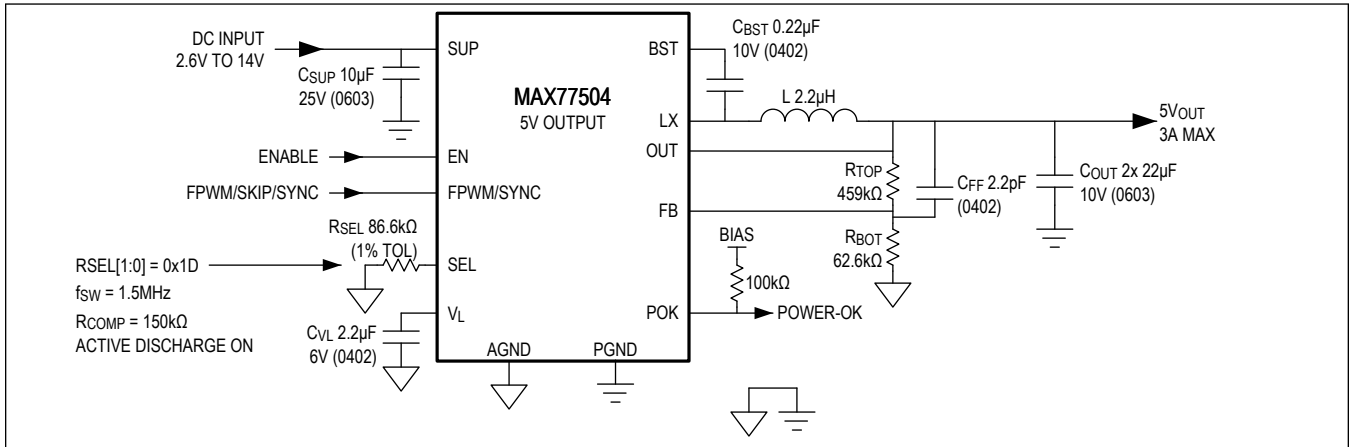


Typical Application Circuits (continued)

3.3V Output, 1.5MHz

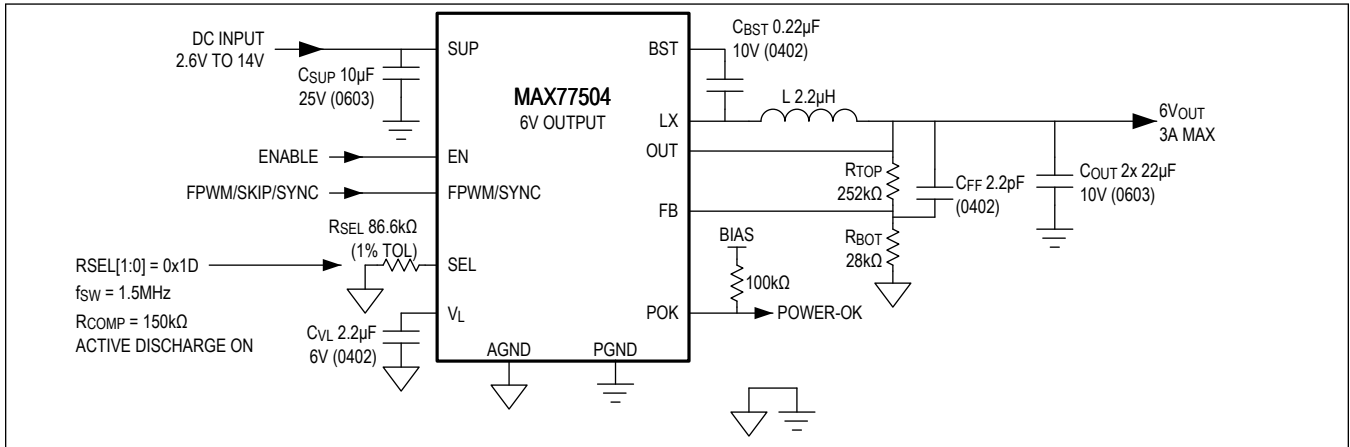


5V Output, 1.5MHz



Typical Application Circuits (continued)

6V Output, 1.5MHz



Ordering Information

PART NUMBER	<u>SOFT-START RAMP TIME</u> (ms)	<u>EXTERNAL CLOCK SYNC</u>	PIN-PACKAGE
MAX77504AAFC+T	1	Available	12 FC2QFN
MAX77504AAWE+T	1	Unavailable	16 WLP
MAX77504BAWE+T	1	Available	16 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/19	Initial release	—
1	3/20	Updated the <i>Electrical Characteristics</i> table, <i>Bump/Pin Descriptions</i> table, <i>Configuration Selection Resistor (SEL)</i> section, <i>Design Procedure (Choosing <math>R_{SEL}</math>)</i> section, <i>Output Capacitor Selection</i> section, <i>Setting the Output Voltage</i> section, <i>PCB Layout Guidelines</i> section, Figure 5, <i>Typical Application Circuits</i> section, and the <i>Ordering Information</i> table; added <i>FPWM/SYNC Clock Pulse Width Requirements</i> section, Table 6, and Figure 6	9, 11, 18, 22–24, 26, 29–34, 36
2	7/20	Updated the <i>Ordering Information</i> table	36

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