Click here for production status of specific part numbers.

MAX77818

Dual Input, Power Path, 3A Switch Mode Charger with Fuel Gauge

General Description

The MAX77818 integrates a high-performance 3A switching charger and proprietary ModelGauge™ m5 fuel gauge in a space saving WLP package, ideal for USB powered portable devices. The smart power path charger supports two inputs with reverse blocking and USB On-the-Go (OTG), integrates all power switches, operates at high-switching frequency with high efficiency, enabling low heat designs with small external components. The ModelGauge m5 algorithm combines the excellent short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. The device also integrates two high voltage input LDOs and is highly programmable with I²C interface.

Applications

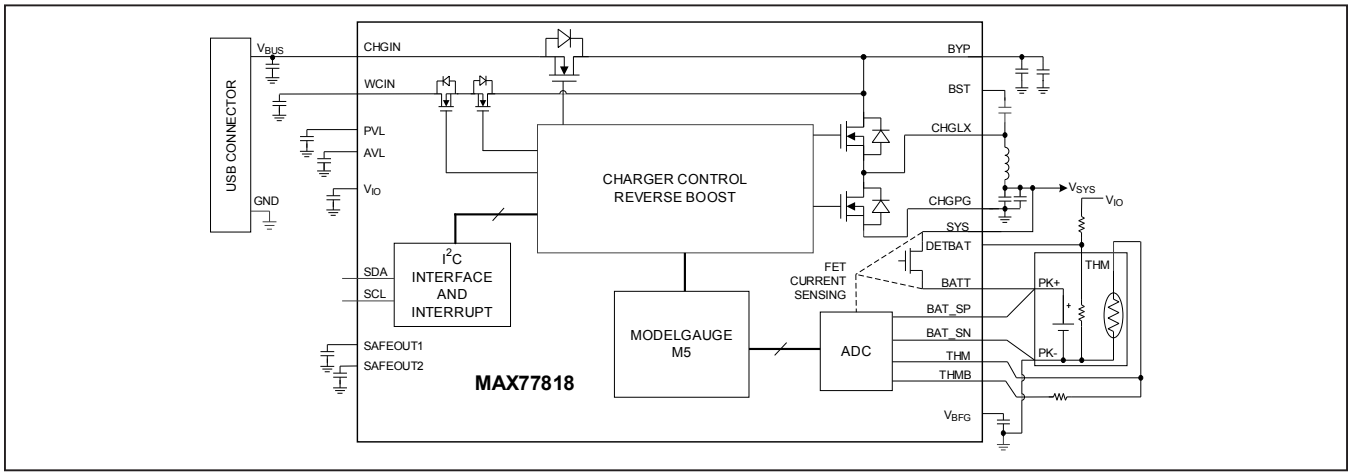
- Industrial PCs
- Portable Medical Devices
- Wearable, Smart Watches
- Handheld Devices
- Wireless Speakers
- Bluetooth Headsets
- Smart Home Automation, Sensors
- Internet of Things (IoT)

Benefits and Features

- Smart Power Path, Dual Input Switching Charger
  - Up to 13.4V Operating/16V Withstand/4A (CHGIN)
  - Up to 6V Operating/1.26A (WCIN)
  - Reverse Leakage Blocking
  - Reverse Boost with up to 5.1V/1.5A (OTG)
  - Integrated Low-Loss FETs for 3A Charging/4.5A Discharging
  - 95.6% Peak Efficiency at 5V/4.35V
  - Full Feature Charger with Protection
  - Thermal Regulation and JEITA Compliance
- ModelGauge m5 Fuel Gauge
  - Time-to-Empty and Time-to-Full Prediction
  - Accurate Battery Capacity (SOC) and Time-to-Empty Readings
    - Temperature, Age, and Discharge Rate Compensated
    - No Calibration
    - Integrated FET Current Sensing
    - Maintains Accuracy without Empty, Full, or Idle States
  - Low Quiescent Current (IQ)
- Two High Voltage Input LDOs
- I²C Serial Interface
- 72-Bump, 3.867mm x 3.608mm, 0.4mm Pitch WLP

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuit



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Absolute Maximum Ratings

Switching Charger
CHGIN to GND .....-0.3V to +16V
BYP to GND .....-0.3V to +16V
WCIN, PVL, AVL, BAT_SP, BATT, SYS,
DETBATB to GND .....-0.3V to +6V
BST to PVL.....-0.3V to +16V
BST to CHGLX.....-0.3V to +6V
WCINOKB, INOKB to GND.....-0.3V to SYS+0.3V
BAT_SN, CHGPG to GND .....-0.3V to +0.3V
CHGLX, CHGPG Continuous Current .....3.5A_{RMS}
SYS, BATT Continuous Current.....4.5A_{RMS}
CHGIN, BYP Continuous Current .....4.0A_{RMS}
WCIN Continuous Current.....1.5A_{RMS}
Fuel Gauge
V_{BFG}, to GND .....-0.3V to +2.2V
THMB, THM to GND ..... -0.3V to V_{AVL} + 0.3V
Safeout LDOs
SAFEOUT1, SAFEOUT2 to GND .....-0.3V to 6V
SAFEOUT1, SAFEOUT2 Continuous Current.....100mA
I²C and Interface Logic
V_{IO} to GND.....-0.3V to +6V
SDA, SCL to GND.....-0.3V to V_{IO}+0.3V
INTB to GND .....-0.3V to V_{SYS_A} + 0.3V
TEST_, V_{CCTEST}, SYS_ to GND.....-0.3V to +6V
GND_ to GND .....-0.3V to +0.3V
Thermal Ratings
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C
Continuous Power Dissipation (T_A = +70°C)
(derate 28.9mW/°C with 4L board, above 70°C).....2.31W

CHGLX has internal clamp diodes to CHGPG and BYP. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....34.6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

General Electrical Characteristics

(V_{SYS} = +3.7V, V_{CHGIN} = 0V , V_{IO} = 1.8V, T_A =-40°C to +85°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current (BATT)		All circuits off V_{BATT} = 3.6V		23	50	µA
No Load Supply Current (BATT)		Fuel gauge is on All other circuits off, V_{BATT} = 3.6V		50	100	µA
SYS INPUT RANGE						
SYS Operating Voltage	V_{SYS}	Guaranteed by $V_{SYSUVLO}$ and $V_{SYSOVLO}$	2.8		5	V
SYS Undervoltage Lockout Threshold	V_{SYS_UVLO}	V_{SYS} falling, 200mV hysteresis	2.45	2.5	2.55	V
SYS Overvoltage Lockout Threshold	V_{SYS_OVLO}	V_{SYS} rising, 200mV hysteresis	5.2	5.36	5.52	V

Switching Charger Electrical Characteristics

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN INPUT						
CHGIN Operating Voltage Range		Operating voltage	3.2		V_{OVLO}	V
WCIN Operating Voltage Range		Operating voltage	3.2		V_{OVLO}	V
CHGIN Overvoltage Threshold (Note 4)	$V_{CHGIN-OVLO}$	V_{CHGIN} rising	13.4	13.7	14	V
WCIN Overvoltage Threshold (Note 4)	$V_{WCIN-OVLO}$	V_{WCIN} rising	5.9		6	V
WCIN Overvoltage Threshold Hysteresis	$V_{WCINH-OVLO}$	V_{WCIN} falling		100		mV
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGINH-OVLO}$	V_{CHGIN} falling		300		mV
WCIN/CHGIN Overvoltage Delay	T_{D-OVLO}	V_{WCIN/BUS_DET} rising, 100mV overdrive, not production tested		10		us
		V_{WCIN/BUS_DET} falling, 100mV overdrive, not production tested		20		us
WCIN/CHGIN to GND Minimum Turn-On Threshold Range (Note 4)	V_{WCIN_UVLO}/ V_{CHGIN_UVLO}	V_{CHGIN} rising, 100mV hysteresis, programmable at 4.5V, 4.9V, 5.0V, 5.1V, WCIN input is disabled when valid CHGIN input is detected	4.5		5.1	V
WCIN/CHGIN to GND Minimum Turn-On Threshold Accuracy	V_{WCIN_UVLO}/ V_{CHGIN_UVLO}	$V_{WCIN/CHGIN}$ rising, 4.5V setting	4.4	4.5	4.6	V
WCIN/CHGIN to SYS Minimum Turn-On Threshold (Note 4)	$V_{WCIN2SYS}$/ $V_{CHGIN2SYS}$	V_{CHGIN} rising, 50mV hysteresis, WCIN input is disabled when valid CHGIN input is detected	V_{SYS} + 0.12	V_{SYS} + 0.20	V_{SYS} + 0.28	V
WCIN/CHGIN Turn-On Threshold Delay	T_{D-UVLO}	Not production tested		10		us
WCIN/CHGIN Adaptive Current Regulation Threshold Range (Note 5)	V_{WCIN_REG}/ V_{CHGIN_REG}	Programmable at 4.3V, 4.7V, 4.8V, 4.9V	4.3		4.9	V
WCIN/CHGIN Adaptive Voltage Regulation Threshold Accuracy	V_{WCIN_REG}/ V_{CHGIN_REG}	4.9V setting	4.8	4.9	5	V
CHGIN Current-Limit Range		Programmable, 500mA default, factory programmable option of 100mA, production tested at 100mA, 500mA, 1000mA, 1800mA, 4000mA settings only	0.1		4	A
WCIN Current-Limit Range		Programmable, 500mA default, factory programmable option of 100mA, production tested at 100mA, 250mA, 500mA, 1000mA settings only	0.06		1.26	A

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WCIN or CHGIN Supply Current	I_{IN}	$V_{WCIN/CHGIN}$ = 2.4V, the input is undervoltage and R_{INSD} is the only loading		0.075		mA
		$V_{WCIN/CHGIN}$ = 5.0V, charger disabled		0.17	0.5	
		$V_{WCIN/CHGIN}$ = 5.0V, charger enabled, V_{SYS} = V_{BATT} = 4.5V, (no switching, battery charged)		2.7	4	
VWCIN or VCHGIN Input Current Limit	$I_{INLIMIT}$	V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 100mA input current setting, T_A = +25°C	90	102	108	mA
		V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 500mA Input current setting, T_A = +25°C	462.5	487.5	500	
		V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1000mA Input current setting, T_A = +25°C	950	975	1000	
		V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1000mA input current setting, T_A = 0°C to +85°C	926	975	1024	
VCHGIN Input Current Limit	$I_{INLIMIT}$	V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = +25°C	1710	1755	1800	mA
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = 0°C to +85°C	1667	1755	1843	
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = +25°C	3800	3900	4000	
		V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = 0°C to +85°C	3705	3900	4095	
WCIN, CHGIN Self-Discharge Down to UVLO Time	t_{INSD}	Time required for the charger input to cause a 10µF input capacitor to decay from 6.0V to 4.3V.		100		ms
WCIN, CHGIN Input Self-Discharge Resistance	R_{INSD}	For CHGIN, this resistor is disconnected from the CHGIN pin during MUIC microphone mode		35		kΩ
WCINOK/CHGINOK to Start Switching	t_{START}			150		ms

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH IMPEDANCES AND LEAKAGE CURRENTS							
CHGIN to BYP Resistance	R_{IN2BYP}	Bidirectional			0.0144	0.04	Ω
WCIN to BYP Resistance	$R_{WCIN2BYP}$				0.093	0.26	Ω
CHGLX High-Side Resistance	R_{HS}				0.0327	0.1	Ω
CHGLX Low-Side Resistance	R_{LS}				0.0543	0.14	Ω
BATT to SYS Dropout Resistance	$R_{BAT2SYS}$				0.0128	0.04	Ω
CHGIN to BATT Dropout Resistance	R_{IN2BAT}	Calculation estimates a 0.04Ω inductor resistance (R_L) $R_{IN2BAT} = R_{IN2BYP} + R_{HS} + R_L + R_{BAT2SYS}$			0.0999		Ω
CHGLX Leakage Current		CHGLX = CHGPG or BYP	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
BST Leakage Current		V_{BST} = 5.5V	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
BYP Leakage Current		V_{BYP} = 5.5V, V_{CHGIN} = 0V, V_{CHGLX} = 0V, charger disabled	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
WCIN Leakage Current		V_{BYP} = 0V, V_{CHGIN} = 0V, V_{WCIN} = 5.5V	T_A = +25°C		0.01		µA
			T_A = +85°C		1		µA
SYS Leakage Current		V_{SYS} = 0V, V_{BATT} = 4.2V, charger disabled	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BATT Quiescent Current (I_{SYS} = 0A, I_{BYP} = 0A)	I_{MBAT}	V_{CHGIN} = 0V, V_{SYS} = 0V, V_{BATT} = 4.2V, QBAT is off	T_A = +25°C		20	30	µA
			T_A = +85°C		20		µA
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, QBAT is on, main-battery overcurrent protection disabled	T_A = +25°C		15.3		µA
			T_A = +85°C		15.3		µA
		V_{CHGIN} = 0V, V_{BATT} = 4.2V, QBAT is on, main-battery overcurrent protection enabled	T_A = +25°C		20		µA
			T_A = +85°C		20		µA
		V_{SYS} = 4.2V, V_{BATT} = 0V, charger disabled	T_A = +25°C		0.01	10	µA
			T_A = +85°C		1		µA
	I_{MBDN}	V_{CHGIN} = 5V, V_{BATT} = 4.2V, QBAT is off, main-battery overcurrent protection disabled, Charger is enabled but in its done mode	T_A = +25°C		3	10	µA
			T_A = +85°C		3		µA
CHARGER DC-DC BUCK							
Minimum On-Time	t_{ON-MIN}				75		ns
Minimum Off-Time	t_{OFF}				75		ns
Current Limit (Note 6)	I_{LIM}	T_A = 0°C to +85°C I_{ND} = 0 (0.47µH inductor option) Production tested at I_{LIM} = 00 setting (Note 7)	I_{LIM} = 00 (3.00A out)	4.15	5.05	5.95	A
			I_{LIM} = 01 (2.75A out)		4.75		
			I_{LIM} = 10 (2.50A out)		4.45		
			I_{LIM} = 11 (2.25A out)		4.15		
		T_A = 0°C to +85°C I_{ND} = 1 (1.0µH inductor option) Production tested at I_{LIM} = 11 setting (Note 7)	I_{LIM} = 00 (3.00A out)		4.60		A
			I_{LIM} = 01 (2.75A out)		4.30		
			I_{LIM} = 10 (2.50A out)		4.00		
			I_{LIM} = 11 (2.25A out)	3.00	3.70	4.40	

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REVERSE BOOST							
BYP Voltage Adjustment Range		2.5V < V_{BATT} < 4.5V. Adjustable from 3V to 5.75V, production tested at 3V, 5.0V and 5.75V settings		3		5.75	V
Reverse Boost Quiescent Current	I_{BYP}	Not switching: output forced 200mV above its target regulation voltage			1150		µA
Reverse Boost BYP Voltage in OTG Mode	$V_{BYP.OTG}$	5.1V setting		4.94	5.1	5.26	V
CHGIN Voltage in OTG Mode	$V_{CHGIN.OTG}$	Mode = 0x05 or 0x0F, WCIN switch is on, VCHGIN_REG = 4.9V, RIN2WCIN + RDSCHGIN < 300ml, OTG load current ≤ 450mA		4.75			V
CHGIN Output Current Limit	$I_{CHGIN.OTG.LIM}$	3.4V < V_{BATT} < 4.5V, T_A = +25°C	OTG_ILIM = 00	500		550	mA
			OTG_ILIM = 01	900		990	mA
			OTG_ILIM = 10	1200		1320	mA
			OTG_ILIM=11	1500		1650	mA
Reverse Boost Output Voltage Ripple		Discontinuous inductor current (i.e., skip mode)			±150		mV
		Continuous inductor current			±150		mV
CHARGER							
BATT Regulation Voltage Range	V_{BATREG}	Programmable in 25mV steps (4 bits), production tested at 3.65V and 4.4V only.		3.65		4.7	V
BATT Regulation Voltage Accuracy		3.65V and 4.7V settings	T_A = +25°C	-0.75		+0.75	%
			T_A = 0°C to +85°C	-1		+1	%
Fast-Charge Current Program Range		0A to 3.0A in 50mA steps, production tested at 500,1000, 2000 and 3000mA settings		0		3	A
Fast-Charge Current Accuracy		Programmed currents ≥ 500mA, V_{BATT} > V_{SYSMIN} (short mode), production tested at 500mA, 800mA, 1000mA, 2000mA, 3000mA settings	T_A = +25°C	-2.5		+2.5	%
			T_A = 0°C to +85°C	-5		+5	%
		Programmed currents ≥ 500mA, V_{BATT} < V_{SYSMIN} (LDO mode), production test at 800mA		-10		+10	%

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Fast-Charge Currents	I_{FC}	T_A = +25°C, V_{BATT} > V_{SYSMIN}	Programmed for 3.0A	2925	3000	3075	mA
			Programmed for 2.0A	1950	2000	2050	mA
			Programmed for 1.0A	975	1000	1025	mA
			Programmed for 0.5A	487.5	500	512.5	mA
Low-Battery Prequalification Threshold	V_{PQLB}	V_{BATT} rising		2.8	2.9	3	V
Dead-Battery Prequalification Threshold	V_{PQDB}	V_{BATT} rising		1.9	2	2.1	V
Prequalification Threshold Hysteresis	V_{PQ-H}	Applies to both V_{PQLB} and V_{PQDB}			100		mV
Low-Battery Prequalification Charge Current	I_{PQLB}	Default setting = disabled		75	100	140	mA
Dead-Battery Prequalification Charge Current	I_{PQDB}			40	55	80	mA
Charger Restart Threshold Range	V_{RSTRT}	Adjustable, 100, 150, and 200; it can also be disabled		100	150	200	mV
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time			130		ms
Top-Off Current Program Range		Programmable from 100 to 350mA in 8 steps.		100		350	mA
Top-Off Current Accuracy (Note 8)		Gain				5	%
		Offset				20	mA
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time			30		ms
Charger State Change Interrupt Deglitch Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state			30		ms
Charger Soft-Start Time	t_{SS}				1.5		ms

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SMART POWER SELECTOR							
BATT to SYS Reverse Regulation Voltage	V_{BSREG}	I_{BATT} = 10mA			30		mV
		I_{BATT} = 1A			60		mV
		Load regulation during the reverse regulation mode			30		mV/A
Minimum SYS Voltage Accuracy	V_{SYSMIN}	Programmable from 3.4V to 3.7V in 100mV steps, V_{BATT} = 2.8V, tested at 3.4V and 3.7V settings		-3		3	%
Maximum SYS Voltage	V_{SYSMAX}	The maximum system voltage: V_{SYSMAX} = V_{BATREG} + $R_{BAT2SYS}$ x I_{BATT}	V_{BATREG} = 4.2V, I_{BATT} = 3.0A		4.245	4.32	V
		The maximum system voltage: V_{SYSMAX} = V_{BATREG} + $R_{BAT2SYS}$ x I_{BATT}.	V_{BATREG} = 4.7V, I_{BATT} = 3.0A		4.745	4.82	V
WATCHDOG TIMER							
Watchdog Timer Period	t_{WD}			80			s
Watchdog Timer Accuracy				-20	0	+20	%
CHARGE TIMER							
Prequalification Time	t_{PQ}	Applies to both low-battery prequalification and dead-battery prequalification modes			35		min
Fast-Charge Constant Current + Fast-Charge Constant Voltage Time	t_{FC}	Adjustable from 4hrs to 16hrs in 2 hour steps including a disable setting			8		hrs
Top-Off Time	t_{TO}	Adjustable from 0min to 70min in 10min steps			30		min
Timer Accuracy				-20		+20	%
AVL FILTER							
Internal AVL Filter Resistance					12.5		Ω

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL FOLDBACK						
Junction Temperature Thermal Regulation Loop Setpoint Program Range	T_{JREG}	Junction temperature when charge current is reduced. Programmable from +85°C to +130°C in 15°C steps, default value is +100°C	85		130	°C
Thermal Regulation Gain	A_{TJREG}	The charge current is decreased 6.7% of the fast charge current setting for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3.0A is reduced to 0A by the time the junction temperature is 20°C above the programmed loop set point. For lower programmed charge currents such as 500mA, this slope is valid for charge current reductions down to 100mA; below 100mA the slope becomes shallower but the charge current still reduced to 0A if the junction temperature is 20°C above the programmed loop set point.		-150		mA/°C
BATTERY OVERCURRENT PROTECTION						
Battery Overcurrent Threshold Range	I_{BOVCR}	Programmable from 3.0A to 4.5A in 0.25A steps, can be disabled	3		4.5	A
Battery Overcurrent Debounce Time	t_{BOVRC}	This is the response time for generating the overcurrent interrupt flag	3	6	10	ms
Battery Overcurrent Protection Quiescent Current	I_{BOVRC}			3 + I_{BATT} /22000		µA
System Power-Up Current	I_{SYSPU}		35	50	80	mA
System Power-Up Voltage	V_{SYSPU}	V_{SYS} rising, 100mV hysteresis	2	2.1	2.2	V
System Power-Up Response Time	t_{SYSPU}	Time required for circuit to activate from an unpowered state (i.e., main-battery hot insertion)		1		µs
SYSTEM SELF DISCHARGE WITH NO POWER						
BATT Self-Discharge Resistor				600		Ω
SYS Self-Discharge Resistor				600		Ω
Self-Discharge Latch Time				300		ms

Switching Charger Electrical Characteristics (continued)

(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DETBATB, INOKB, WCINOKB							
DETBATB Logic Threshold	V_{IH}	4% hysterisis			0.8 x V_{IO}		V
Logic Input Leakage Current	$I_{DETBATB}$				0.1	1	µA
Output Low Voltage INOKB, WCINOKB		I_{SINK} = 1mA				0.4	V
Output High Leakage INOKB, WCINOKB		V_{SYS} = 5.5V	T_A = +25°C	-1	0	+1	µA
			T_A = +85°C		0.1		µA

Safeout LDOs Electrical Characteristics

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAFEOUT1						
Output Voltage (Default On)		5V < V_{CHGIN} < 5.5V, I_{OUT} = 10mA, SAFEOUT1 = 0x01 (default)	4.8	4.9	5	V
		SAFEOUT1 = 0x00		4.85		V
		SAFEOUT1 = 0x10		4.95		V
		SAFEOUT1 = 0x11		3.3		V
Maximum Output Current		When LDO output is regulated	60			mA
Output Current Limit		When LDO output may be out of regulation	60	150	320	mA
Dropout Voltage		V_{CHGIN} = 5V, I_{OUT} = 60mA		120		mV
Load Regulation		V_{CHGIN} = 5.5V, 30µA < I_{OUT} < 30mA		50		mV
Quiescent Supply Current		Not production tested		72		µA
Output Capacitor for Stable Operation (Note 9)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ		1		µF
Minimum Output Capacitor for Stable Operation (Note 9)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ		0.7		µF
Internal Off-Discharge Resistance				1200		Ω

Safeout LDOs Electrical Characteristics (continued)

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAFEOUT2						
Output Voltage (Default Off)		5V < V_{CHGIN} < 5.5V, I_{OUT} = 10mA, SAFEOUT2 = 0x01 (default)	4.8	4.9	5	V
		SAFEOUT2 = 0x00		4.85		V
		SAFEOUT2 = 0x10		4.95		V
		SAFEOUT2 = 0x11		3.3		V
Maximum Output Current		When LDO output is regulated	60			mA
Output Current Limit		When LDO output may be out of regulation	60	150	320	mA
Dropout Voltage		V_{CHGIN} = 5V, I_{OUT} = 60mA		120		mV
Load Regulation		V_{CHGIN} = 5.5V, 30µA < I_{OUT} < 30mA		50		mV
Quiescent Supply Current		Not production tested		72		µA
Output Capacitor for Stable Operation (Note 9)		0µA < I_{OUT} < 30mA, MAX ESR = 50mΩ		1		µF
Minimum Output Capacitor for Stable Operation (Note 9)		0FA < I_{OUT} < 30mA, MAX ESR = 50mΩ		0.7		µF
Internal Off-Discharge Resistance				1200		Ω

Fuel Gauge Electrical Characteristics

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD0}	Fuel gauge shut down (Note 10)		0.5		µA
	I_{DD1}	Fuel gauge active, average with 7.5% ADC duty cycle (Note 10)		35	70	µA
ADC Duty Cycle	Duty			7.5		%
Parameter Capture Rate	t_{ACQ}	Period of ADC activation loop		0.1758		s
Regulator Output	V_{BFG}		1.5	1.8	1.98	V
VOLTAGE CHANNEL						
V_{BATT} Measurement Error	V_{GERR}	V_{BATT} = 2.8V to 4.5V, T_A = +25°C	-7.5		+7.5	mV
		T_A = -40°C to +85°C	-20		+20	mV
V_{BATT} Measurement Resolution	V_{LSB}			1.25		mV
V_{BATT} Measurement Range	V_{RANGE}		2.8		4.98	V

Fuel Gauge Electrical Characteristics (continued)

(V_{SYS} = 2.8V to 4.5V, T_A = -40°C to 85°C, typical values are at T_A = +25°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT CHANNEL							
Current Measurement Resolution	I_{LSB}				1.25		mA
Current Measurement Range	I_{RANGE}			-3.6		+3.6	A
Current Measurement Offset	I_{OERR}	Long term average at zero input current			±0.25		mA
Current Measurement Symmetrical Error	I_{SERR}	(Notes 11, 12, 13)			2%		%
Current Measurement Asymmetrical Error	I_{AERR}	±3000mA	(Notes 12, 13, 14)	-150		+150	mA
		±1000mA		-20		+20	
		±300mA		-9.5		+9.5	
Linear Regulator Mode Current Measurement Error	I_{LRERR}	+1500mA	(Note 15)	-225		+225	mA
		+100mA		-40		+40	
Time-Base Accuracy	t_{ERR}	V_{SYS} = 3.7V at T_A = +25°C			±1		%
		T_A = -40°C to +85°C		-3.5		+3.5	
THERMAL CHANNEL							
Ratiometric Measurement Accuracy, THM	T_{GERR}	(Note 13)		-0.5		+0.5	% of full scale
Ratiometric Measurement Resolution, THM	T_{LSB}				0.0244		% of full scale
THMB Output Drive	V_{OH_THMB}	I_{OH_THMB} = -0.5mA		V_{AVL} - 0.1			V
THMB Precharge Time	t_{PRE_THMB}				12.7		ms
THMB Operating Range	V_{THMB}			2.8		V_{AVL}	V
THMB Input Leakage	I_{IN_THMB}	V_{THMB} = 5V		-1		+1	µA
THM Input leakage	I_{IN_THM}			-1		+1	µA

I²C Electrical Characteristics

(V_{SYS} = +3.7V, V_{CHGIN} = 0V , V_{IO} = 1.8V, T_A =-40°C to +85°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND CONTROL INPUT						
SCL, SDA Input Low Level		T_A = +25°C			0.3 x V_{IO}	V
SCL, SDA Input High Level		T_A = +25°C	0.7 x V_{IO}			V
SCL, SDA Input Hysteresis		T_A = +25°C		0.05 x V_{IO}		V
SCL, SDA Logic Input Current		V_{IO} = 3.6V	-10		+10	µA
SCL, SDA Input capacitance				10		pF
SDA Output Low Voltage		Sinking 20mA			0.4	V
Output Low Voltage INTB		I_{SINK} = 1mA			0.4	V
I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS (Note 2)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that Must Be Suppressed by the Input Filter		(Note 3)		50		ns

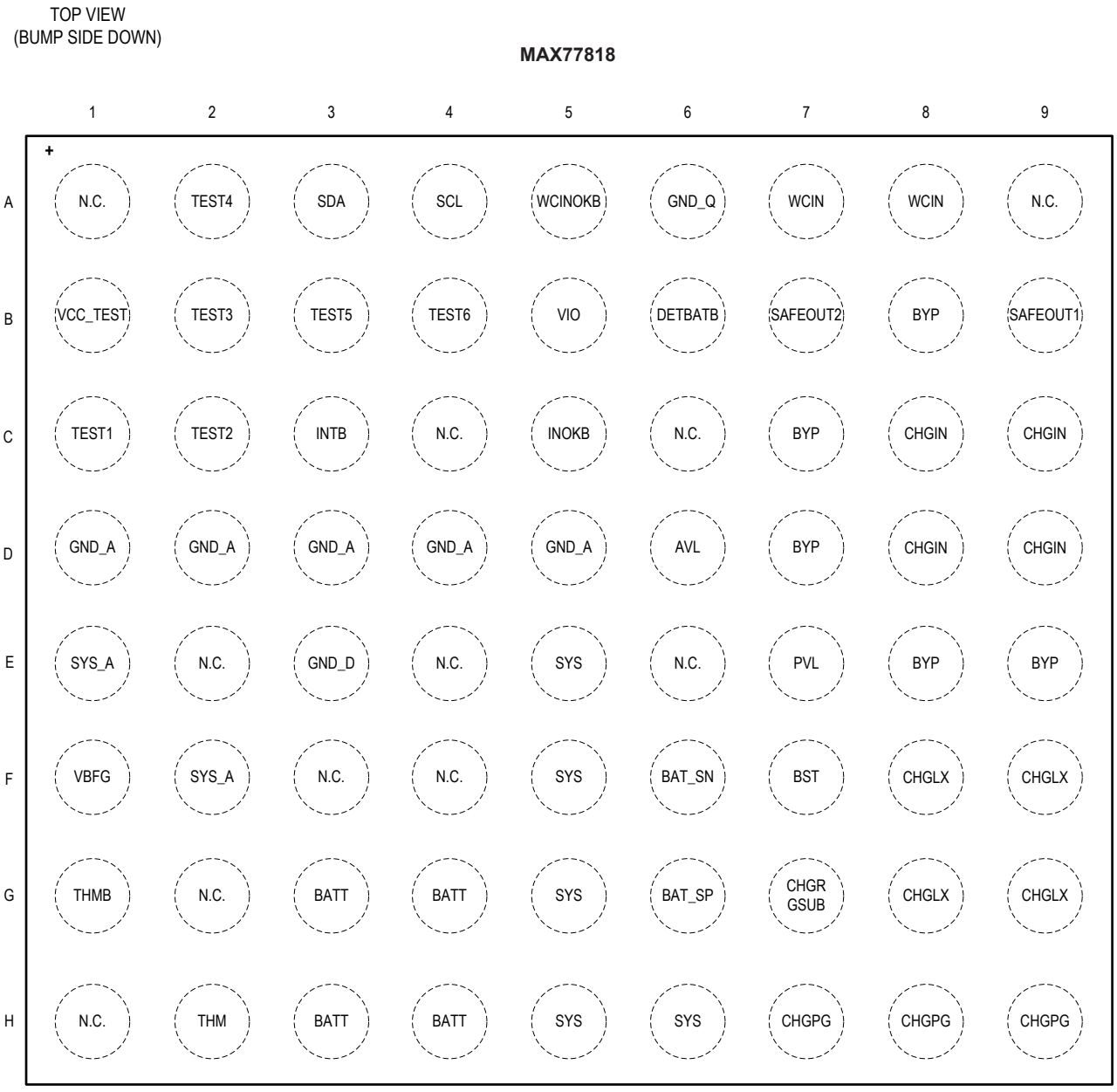
I²C Electrical Characteristics (continued)

(V_{SYS} = +3.7V, V_{CHGIN} = 0V , V_{IO} = 1.8V, T_A =-40°C to +85°C, unless otherwise noted. Limits are 100% production tested at T_A = +25°C . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF			UNITS
			MIN	TYP	MAX	
I²C-COMPATIBLE INTERFACE TIMING FOR HS MODE (Note 2)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
SCL Rise Time	t_{RCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal After a Repeated START condition and After an Acknowledge Bit	t_{RCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{FDA}	T_A = +25°C			80	ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns

Note 2: Design guidance only, not tested during final test.
Note 3: Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.
Note 4: The CHGIN input must be less than V_{OVLO} and greater than both V_{CHGIN_UVLO} and $V_{CHGIN2SYS}$ for the charger to turn-on.
Note 5: The input voltage regulation loop decreases the input current to regulate the input voltage at V_{CHGIN_REG}. If the input current is decreased to $I_{CHGIN\_REG\_OFF}$ and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off.
Note 6: Production tested to ¼ of the threshold with LPM bit = 1 (¼ FET configuration).
Note 7: Production tested in charger DC-DC low-power mode.
Note 8: Not production tested.
Note 9: Not production tested.
Note 10: The total chip supply current includes the charger supply current in addition to the supply current for the fuel gauge.
Note 11: Symmetrical error is the sum of odd order errors in the measured values at two inputs symmetrical around zero; for example, ISERR_0.3A = (Error 0.3A - Error -0.3A)/2/0.3A x 100.
Note 12: Total current measurement error is the sum of the symmetrical and asymmetrical errors. Fuel gauge accuracy is sensitive to asymmetrical error but insensitive to symmetrical error.
Note 13: Current and ratiometric measurement errors are production tested at V_{SYS} = 3.7V and guaranteed by design at V_{SYS} = 2.8V and 4.5V.
Note 14: Asymmetrical error is the sum of even order errors in the measured values at two inputs symmetrical around zero; for example IAERR_0.3A = (Error 0.3A + Error -0.3A)/2.
Note 15: Total linear regulator mode current measurement error is simply the total error with respect to the input. This mode exists for a short duration when charging an empty battery, hence this error has limited consequence.

Pin Configuration



WLP
(72 BUMPS WLP 9X8 BUMP ARRAY 0.4MM PITCH)

N/C PINS ARE FLOATING AND CAN BE CONNECTED AT BOARD-LEVEL IF NEEDED.

ALL TEST PINS (TEST1-6 AND VCCTEST) SHOULD BE GROUNDED IN THE END-USE APPLICATION.

*TOP VIEW = WAFER BACK-SIDE VIEW (BUMPS NOT VIEWABLE)

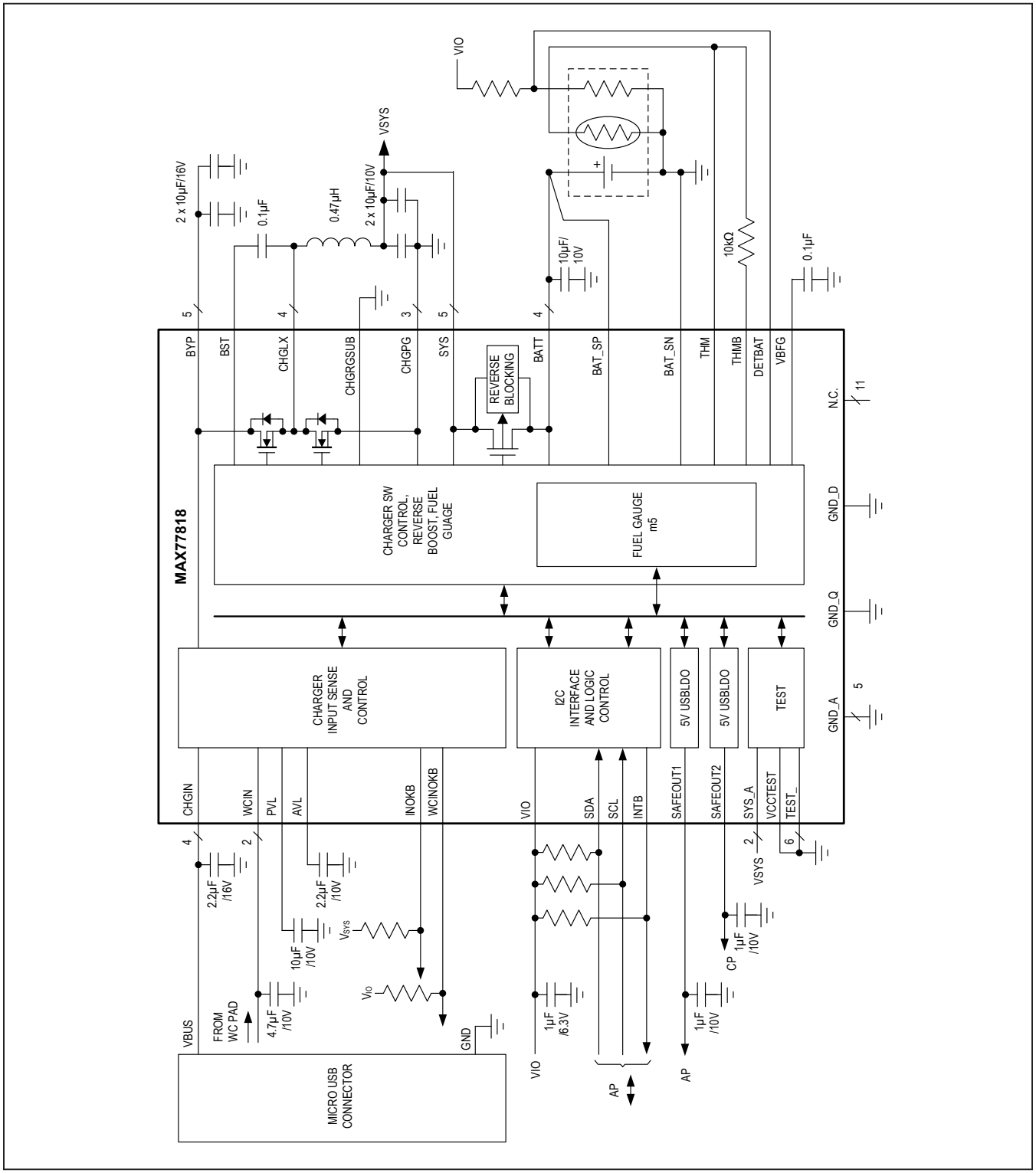
Pin Description

PIN	NAME	FUNCTION
A1, A9, C4, C6, E2, E4, E6, F3, F4, G2, H1	N.C.	No Connection
A2	TEST4	Test I/O Pin. Ground this pin in the application.
A3	SDA	I²C Serial Data. Add an external 2.2kΩ pullup resistor to V_{IO}.
A4	SCL	I²C Serial Clock. Add an external 2.2kΩ pullup resistor to V_{IO}.
A5	WCINOKB	Open-Drain, Active-Low WCIN Input Valid Indication Output. Pulls low when a valid WCIN is available and SYS is in the valid range. Pulls high with an off-chip pullup resistor to V_{IO} when WCIN is invalid.
A6	GND_Q	Quiet Ground. Short to GND_A and GND_D.
A7, A8	WCIN	6 V_{DC} Protected Input for USB or Wireless Charging. Bypass with 4.7µF/10V ceramic capacitor to GND.
B1	V_{CCTEST}	Test Mux Supply. Ground this pin in the application.
B2	TEST3	Test I/O. Ground this pin in the application.
B3	TEST5	Test I/O. Ground this pin in the application.
B4	TEST6	Test I/O. Ground this pin in the application.
B5	V_{IO}	Digital I/O Supply Input for I²C Interface.
B6	DETBATB	Active-Low Battery Detection Input. Connected to V_{IO} through an off-chip pullup resistor or left unconnected disables charging. Pulled low below 80% of V_{IO} enables charging.
B7	SAFEOUT2	High-Voltage Input LDO SAFEOUT2 Output. Default off. Bypass with 1µF/10V ceramic capacitor to GND.
B8, C7, D7, E8, E9	BYP	Switching Charger Buck Input and Reverse Boost Output. Bypass with 2x10µF/25V ceramic capacitors to CHGPG.
B9	SAFEOUT1	High-Voltage Input LDO SAFEOUT1 Output. Default 4.9V, on when CHGIN is valid. Bypass with 1µF/10V ceramic capacitor to GND.
C1	TEST1	Test I/O. Ground this pin in the application.
C2	TEST2	Test I/O. Ground this pin in the application.
C3	INTB	Interrupt Output. Active-low, open-drain output. Add a 200kΩ pullup resistor to V_{IO}.
C5	INOKB	Open-Drain, Active-Low CHGIN Input Valid Indication Output. Pulls low when a valid CHGIN is available and SYS is in the valid range. Pulls high with an off-chip pullup resistor to V_{IO} when CHGIN is invalid.
C8, C9, D8, D9	CHGIN	High Voltage Input for USB or Wireless Charging. Bypass with 2.2µF/25V ceramic capacitor to GND.
D1–D5	GND_A	Analog Ground. Short to GND_D and GND_Q.

Pin Description (continued)

PIN	NAME	FUNCTION
D6	AVL	Output of an integrated 5V LDO powering on-chip, low noise circuits. Powering external loads other than pullup resistors is not recommended. Bypass with 2.2µF/10V ceramic capacitor to GND.
E1, F2	SYS_A	Analog SYS Input
E3	GND_D	Digital Ground. Short to GND_A and GND_Q.
E5, F5, G5, H5, H6	SYS	System Power Connection, Output of Charger Buck. Bypass with 2x10µF/10V ceramic capacitors to CHGPG.
E7	PVL	Output of an Integrated 5V LDO Powering On-Chip, High Current Circuits. Powering external loads is not recommended. Bypass with 10µF/10V ceramic capacitor to GND.
F1	V_{BFG}	Output of an Integrated 1.8V Power Supply for Fuel Gauge. Powering external load is not recommended. Bypass with 0.1µF/6.3V ceramic capacitor to GND.
F6	BAT_SN	Battery Negative Differential Sense Connection. Connect to the negative or ground terminal close to the battery.
F7	BST	High-Side FET Driver Supply. Bypass BST to LX with a 0.1µF ceramic capacitor.
F8, F9, G8, G9	CHGLX	Charger Switching Node. Connect the inductor between CHGLX and SYS.
G1	THMB	Pullup Voltage for THM Pin Pullup Resistor. Can be switched to save power.
G3, G4, H3, H4	BATT	Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li Ion battery. Bypass BATT to CHGPG ground plane with a 10µF/10V ceramic capacitor.
G6	BAT_SP	Battery Positive Differential Sense Connection. Connect to the positive terminal close to the battery.
G7	CHGRGSUB	Substrate Charger Ground Connection. Connect with GND_A.
H2	THM	Thermistor Connection. Determines battery temperature using ratiometric measurement.
H7–H9	CHGPG	Charger Power Ground Connection.

Functional Block Diagram



Detailed Description

Switching Charger

The MAX77818 includes a full-featured switch-mode charger for a one-cell lithium ion (Li+) or lithium polymer (Li-poly) battery. Figure 2 shows the detailed functional diagram. One high voltage input (CHGIN) and one low voltage input (WCIN) can be enabled or disabled independently with I^2C. When enabled, the input powers the system and charges the battery. Both inputs have programmable current limit and under-/over-voltage protections. The reverse leakage blocking feature prevents back powering from the battery or between the two inputs.

The synchronous switch-mode DC-DC converter utilizes a high 4.0MHz switching frequency which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When a valid input is available (CHGIN or WCIN), the DC-DC operates as a buck, delivering energy to the system and charge the battery. When no valid inputs are available and boost mode or OTG mode is enabled, the DC-DC operates in reverse mode, and outputs a boosted voltage at BYP powered by battery. CHGIN can be used to power USB On-the-Go (OTG) devices when OTG mode is enabled.

Maxim's Smart Power Selector™ architecture makes the best use of the limited adapter power and the battery's power at all times to supply up to 3.0A continuous (4A peak) from the buck to the system. Additionally, supplement mode provides additional current from the battery to the system up to $4.5A_{RMS}$. Adapter power that is not used for the system goes to charge the battery. All power switches for charging and switching the system load between battery and adapter power are integrated on chip. No external MOSFETs are required.

Maxim's proprietary process technology allows for low-R_{DSON} devices in a small solution size. The total dropout resistance from CHGIN to BATT is 0.0599Ω excluding inductor DCR, allowing high-efficiency and low heat operation.

A multitude of safety features ensures reliable charging. Features include charge timers, watchdog, junction thermal regulation, over-/under-voltage protection, and short-circuit protection.

ModelGauge m5 Fuel Gauge

The MAX77818 is the latest high-performance battery charger that integrates the Maxim proprietary ModelGauge m5 algorithm in the same chip. Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated, causing the reported capacity error to increase over time, which requires periodic corrections. The ModelGauge m5 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time. The ModelGauge m5 adopts a mixing algorithm that combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, canceling the coulomb-counter drift.

The MAX77818 includes improved age adaptation, improved SOC accuracy to empty, and increased temperature measurement. The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer. Moreover, the device provides precision measurements of current, voltage, and temperature. Details are discussed in the *ModelGauge m5 Details* section.

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

Charger Details

Smart Power Selector (SPS)

The Smart Power Selector architecture includes a network of internal switches and control loops that distributes energy among CHGIN, WCIN, BYP, SYS, and BATT.

Figure 2 shows the Smart Power Selector switches: Q_{CHGIN}, Q_{WCIN}, Q_{HS}, Q_{LS}, and Q_{BAT}.

Switch and Control Loop Descriptions:

CHGIN Input Switch: QCHGIN is used for input current sensing. It turns completely on when a valid CHGIN is available and does not provide forward blocking. SPS control loops regulate CHGIN input current and voltage.

DC-DC Switches: Q_{HS} and Q_{LS} are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is delivered from BYP to SYS. When operating as a boost, energy is delivered from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.

Battery-to-System Switch: Q_{BAT} controls the battery charging and discharging. Additionally, Q_{BAT} allows the battery to be isolated from the system (SYS). SPS control loops regulate battery current and voltage.

Control Bits

MODE[3:0] configures the Smart Power Selector.

MINVSYS[1:0] sets the minimum system voltage.

VBYPSET[6:0] sets the BYP regulation voltage target.

B2SOVRC[2:0] sets the battery overcurrent protection threshold.

Energy Distribution Priority:

With a valid external power source (buck operation):

- The external power source is the primary source of energy.
- The battery is the secondary source of energy.
- Energy delivery to SYS is the highest priority.
- Any energy that is not required by SYS is available to the battery charger.

With no valid external power source:

- The battery is the source of energy.
- Energy delivery to SYS is the highest priority.
- Any energy not required by SYS is available for BYP or CHGIN (when boost or OTG is enabled).

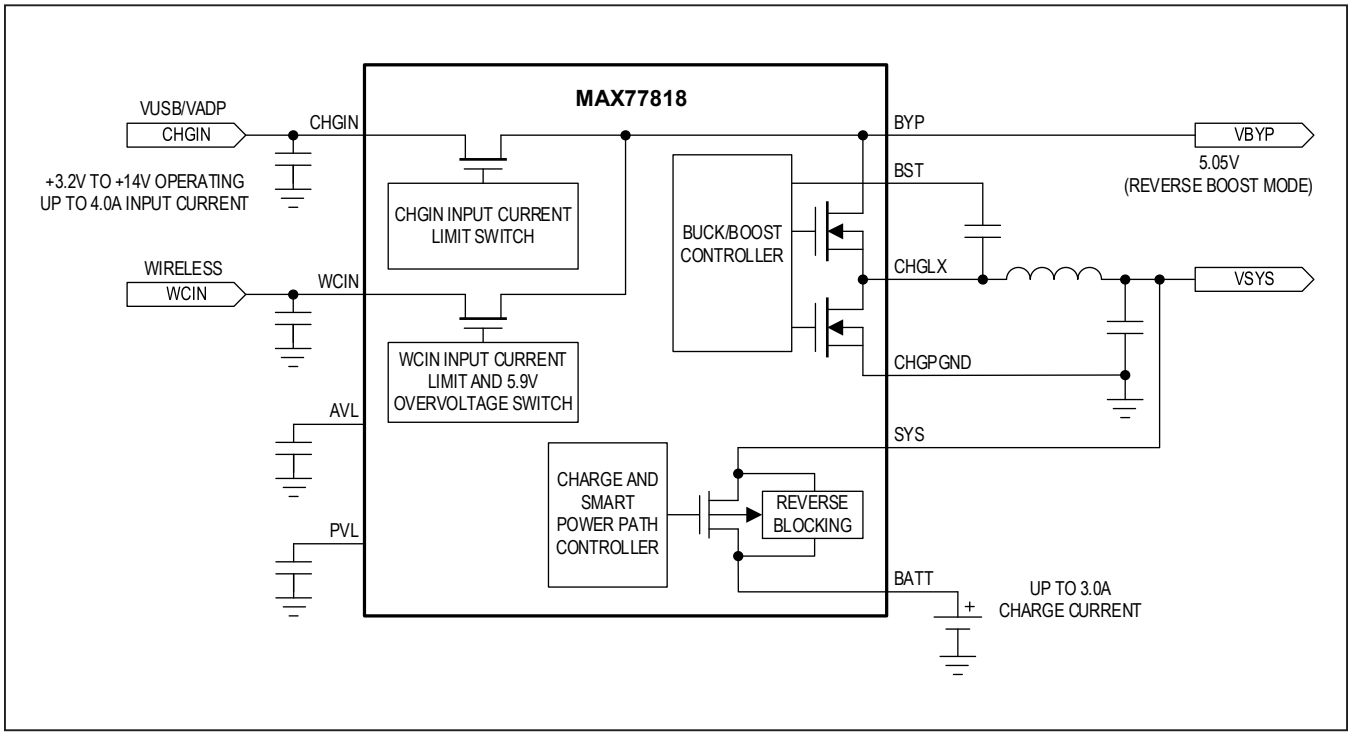


Figure 1. Simplified Charger Functional Diagram

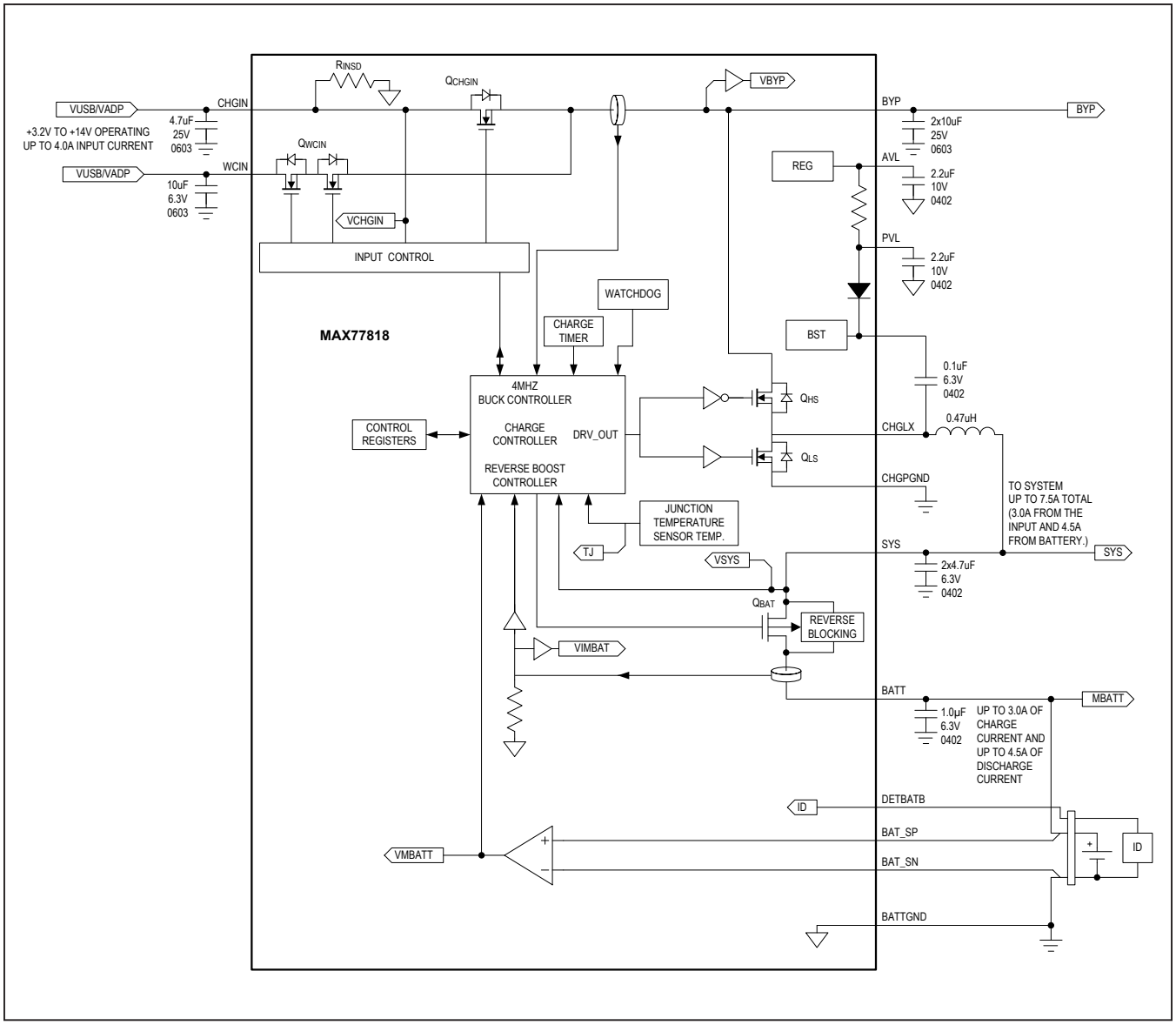


Figure 2. Battery Charger Detailed Functional Diagram

BYP Regulation Voltage

When the DC-DC is enabled in boost only mode (MODE[3:0] = 0x08), the voltage from BYP to ground (V_{BYP}) is regulated to VBYPSET[6:0].

When the DC-DC is enabled in one of its USB OTG modes (MODE[3:0] = 0x0A or 0x0E or 0x0F), V_{BYP} is set for 5.1V ($V_{BYP.OTG}$).

When the DC-DC is off or in one of its buck modes (MODE[3:0] = 0x00 or 0x04 or 0x05) and there is a valid power source at CHGIN, $V_{BYP} = V_{CHGIN} - I_{CHGIN} \times R_{QCHGIN}$. When the DC-DC is off and there is no valid power source at CHGIN, BYP is connected to SYS with an internal 200Ω resistor. This 200Ω resistor keeps BYP biased at V_{SYS} and allows for the system to draw very light loads from BYP. If the system loading on BYP is more than 1.0mA then the DC-DC should be operated in boost mode. Note that the inductor and the high-side switch's body diode are in parallel with the 200Ω from SYS to BYP.

SYS Regulation Voltage

When the DC-DC is enabled as a buck and the charger is disabled (MODE[3:0] = 0x04), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and Q_{BAT} is off.

When the DC-DC is enabled as a buck and the charger is enabled but in a non-charging state such as done, watchdog suspend or timer fault (MODE[3:0] = 0x05 and not charging), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and Q_{BAT} is off.

When the DC-DC is enabled as a buck and charging in prequalification, fast-charge, or top-off modes (MODE[3:0] = 0x05 and charging), V_{SYS} is regulated to V_{SYSMIN} when the $V_{BATT} < V_{SYSMIN}$; in this mode the Q_{BAT} switch acts like a linear regulator and dissipates power [$P = (V_{SYSMIN} - V_{BATT}) \times I_{BATT}$]. When $V_{BATT} > V_{SYSMIN}$, then $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$; in this mode the Q_{BAT} switch is closed.

In all of the above modes, if the combined SYS and BYP loading exceeds the input current limit, then the battery provides supplemental current to the system, and V_{SYS} regulates to $V_{BATT} - V_{BSREG}$. If the fuel gauge requests battery information (voltage and current) during supplement mode, then the Q_{BAT} switch is closed ($V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$) during the fuel gauge sampling period. If the fuel gauge requests continuous samples from the battery during supplement mode, then the Q_{BAT} switch eventually opens when I_{BATT} decreases below 40mA.

When the DC-DC is enabled in boost or OTG modes (MODE[3:0] = 0x08, 0x0A, 0x0C, 0x0D, 0x0E, or 0x0F), then the QBAT switch is closed and $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$.

Battery Detect Input Pin (DETBATB)

Utilize the DETBATB pin to disable charging until the host processor configures the charger, or connect the DETBATB pin to the ID pin of the battery pack and allow charging to automatically start when a valid charging source is available (Figure 3).

Input Validation

As shown in Figure 4, the charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following three criteria to be valid:

1) CHGIN must be above V_{CHGIN_UVLO} to be valid.
2) CHGIN must be below its overvoltage-lockout threshold ($V_{CHGIN-OVLO}$).
3) CHGIN must be above the system voltage by $V_{CHGIN2SYS}$.

CHGIN input generates a CHGIN_I interrupt when its status changes. The input status can be read from CHGIN_OK and CHGIN_DTLS register bits. Interrupts can be masked with CHGIN_M.

The WCIN input validation is similar.

Input Current Limit

Set CHGIN and WCIN input current regulation thresholds with CHGIN_ILIM[6:0] and WCIN_ILIM[5:0] register bits. The default settings of the CHGIN_ILIM[6:0], WCIN_ILIM[5:0] and MODE[3:0] register bits are such that when a charge source is applied to CHGIN or WCIN, the MAX77818 turns its DC-DC converter on in BUCK mode, limits V_{SYS} to V_{BATREG}, and limits the charge source current to 500mA. All control bits are reset on global shutdown.

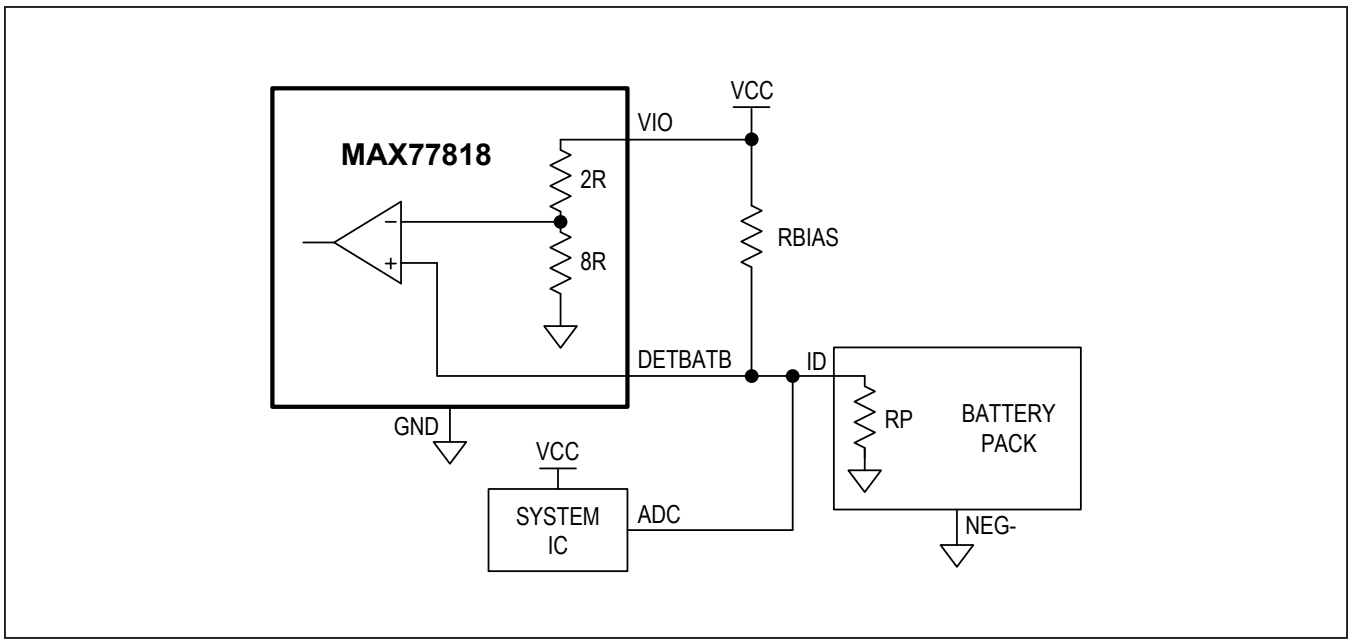


Figure 3. DETBATB Internal Circuitry and System Diagram

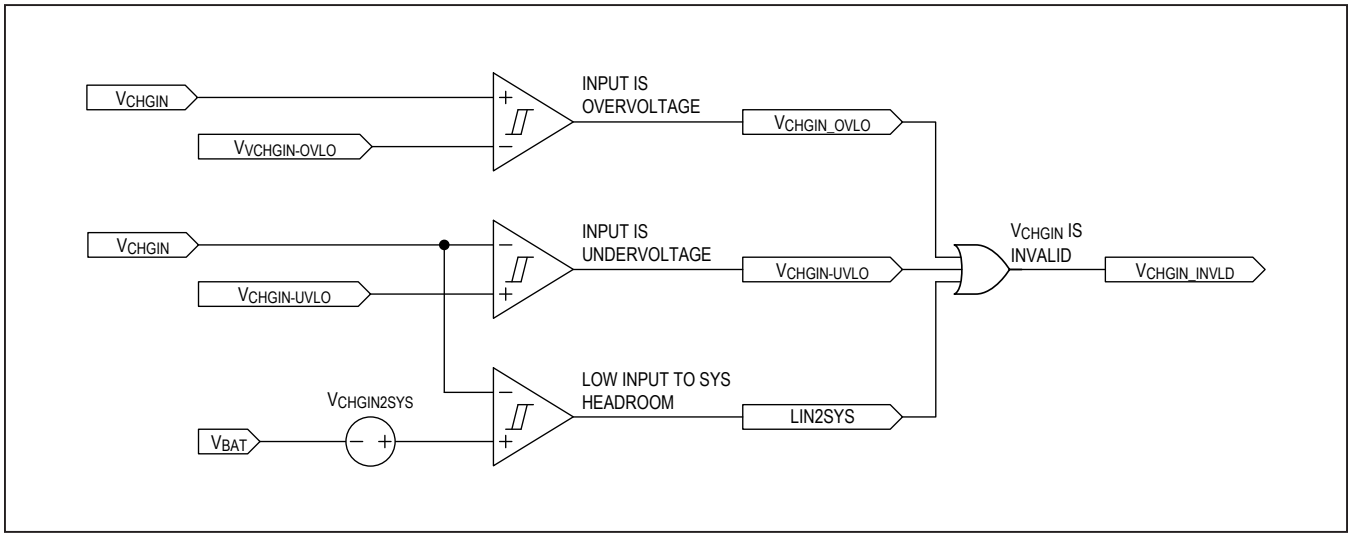


Figure 4. Charger Input Validation

Input-Voltage Regulation (V_{CHGIN_REG})

The input-voltage regulation loop allows the charger to extract maximum input power while avoiding input source overload when it is attached to a poor quality power source (CHGIN) or wireless charger (WCIN). The loop improves performance with relatively high-resistance charge sources that exist when long cables are used or devices are charged with noncompliant USB hub configurations. Additionally, this input-voltage regulation loop improves performance with current limited adapters. If the MAX77818's input current limit is programmed above the current limit threshold of given adapter, the input voltage loop allows the MAX77818 to regulate at the current limit of the adapter. Finally, the input-voltage regulation loop allows the MAX77818 to perform well with adapters that have poor transient load response times.

The input-voltage regulation loop automatically reduces the input current in order to regulate the input voltage at V_{CHGIN_REG} or V_{WCIN_REG}. If the input current is reduced to $I_{CHGIN\_REG\_OFF}$ (50mA typ) and the input voltage is below V_{CHGIN_REG}, then Q_{CHGIN} is turned off. V_{CHGIN_REG} and V_{WCIN_REG} are programmable with $V_{CHGIN\_REG[1:0]}$ and $V_{WCIN\_REG[1:0]}$ register bits.

After input-voltage regulation is activated, a BYP_I interrupt is generated, BYP_OK is cleared and BYP_DTLS[3:0] = 0b1xxx. To optimize input power when working with a current limited charge source, monitor BYP_DTLS[3:0] while decreasing the input current limit with CHGIN_ILIM[6:0]. When the input current limit is set below the current limit of the adapter, the input voltage rises. Although the input current limit is lowered, more power can be extracted from the input source when the input voltage is allowed to rise.

Example 1: Optimum use of the input-voltage regulation loop along with a current limited adapter.

Sequence of Events

V_{BATT} = 3.2V, the system is operating normally.

A 5.0V 1.2A current limited dedicated USB charger is applied to CHGIN.

The system detects that the charge source is a dedicated USB charger and enables the battery charger (MODE = 0x05) and programs an input current limit to 1.8A (CHGIN_ILIM = 0x36 = 1.8A).

The input current starts to ramp up from 100mA to 1.8A, but at the input current limit of the adapter (1.2A), the adapter voltage collapses. The MAX77818's input-voltage regulation loop prevents the adapter voltage from falling below 4.3V (V_{CHGIN_REG} = 4.3V). A BYP_I interrupt is generated.

With the input-voltage regulation loop active, the adapter provides 1.2A at 4.3V, which is a total of 5.04W being delivered to the system.

The system software detects that the input-voltage regulation loop is active and it begins to ramp down the programmed input current limit. When the current limit ramps down to 1.167A (CHGIN_ILIM[6:0]), the adapter is no longer in current limit and the adapter voltage increases from 4.3V to 5.0V.

When the adapter operates just below its current limit, it provides 1.167A at 5.0V which is a total of 5.84W to the system. This is 800mW more than when the adapter was in current limit.

Input Self-Discharge for Reliable Charger Input Interrupt

To ensure that a rapid removal and reinsertion of a charge source always results in a charger input interrupt, the charger input presents loading R_{INSD} to the input capacitor to ensure that when the charge source is removed, the input voltage decays below the UVLO threshold in a reasonable time.

System Self-Discharge with No Power

To ensure a timely, complete, repeatable, and reliable reset behavior when the system has no power, the MAX77818 actively discharges the BATT and SYS nodes when the battery is removed and V_{SYS} is less than $V_{SYSUVLO}$. As shown in Figure 5, the BATT and SYS discharge resistors are both 600Ω.

Charge States

The MAX77818 utilizes several charging states to safely and quickly charge batteries as shown in Figure 6 and Figure 7. Figure 6 shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and battery are close to room temperature: daed battery/low battery prequalification ➔ fast-charge ➔ top-off ➔ done.

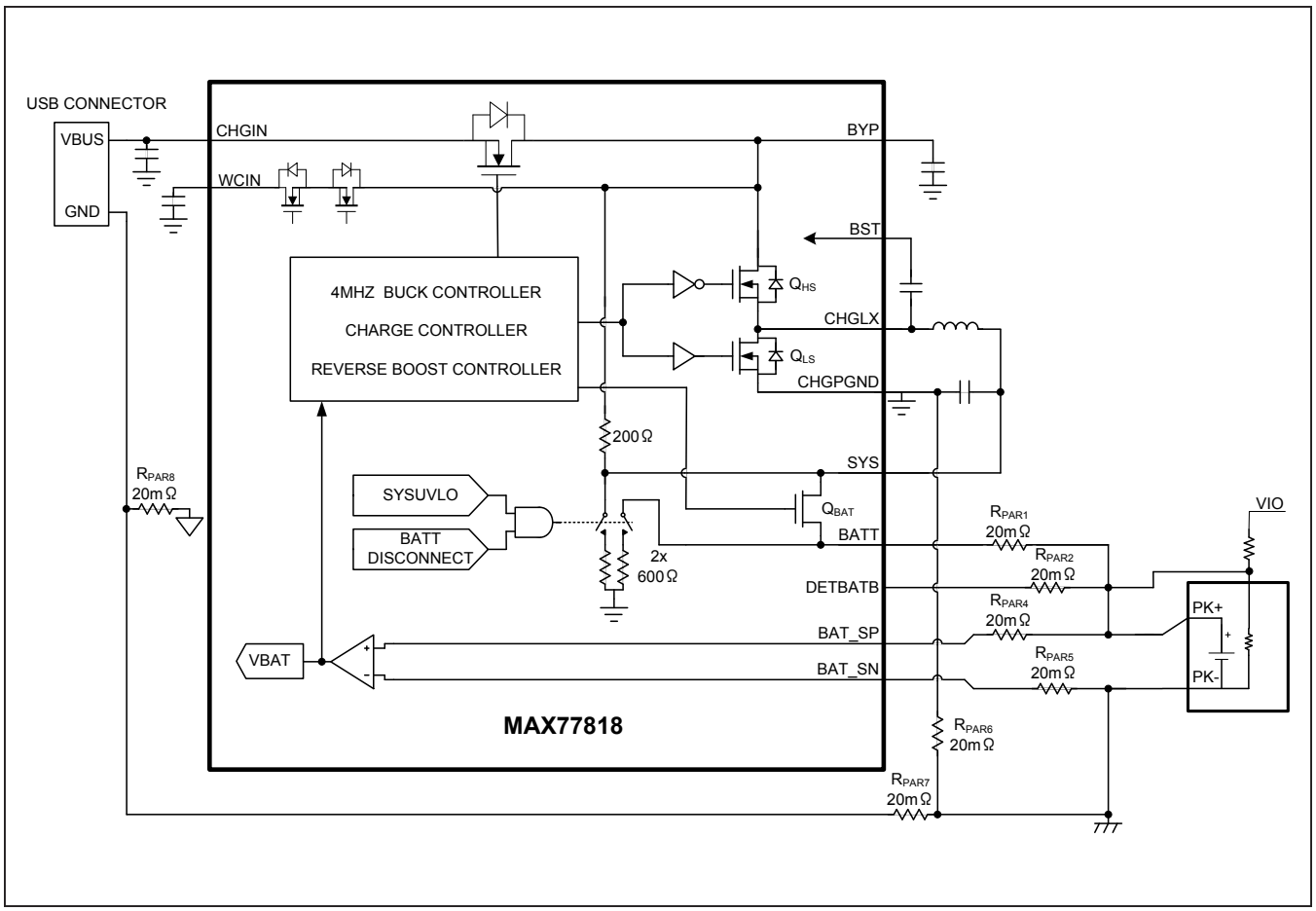
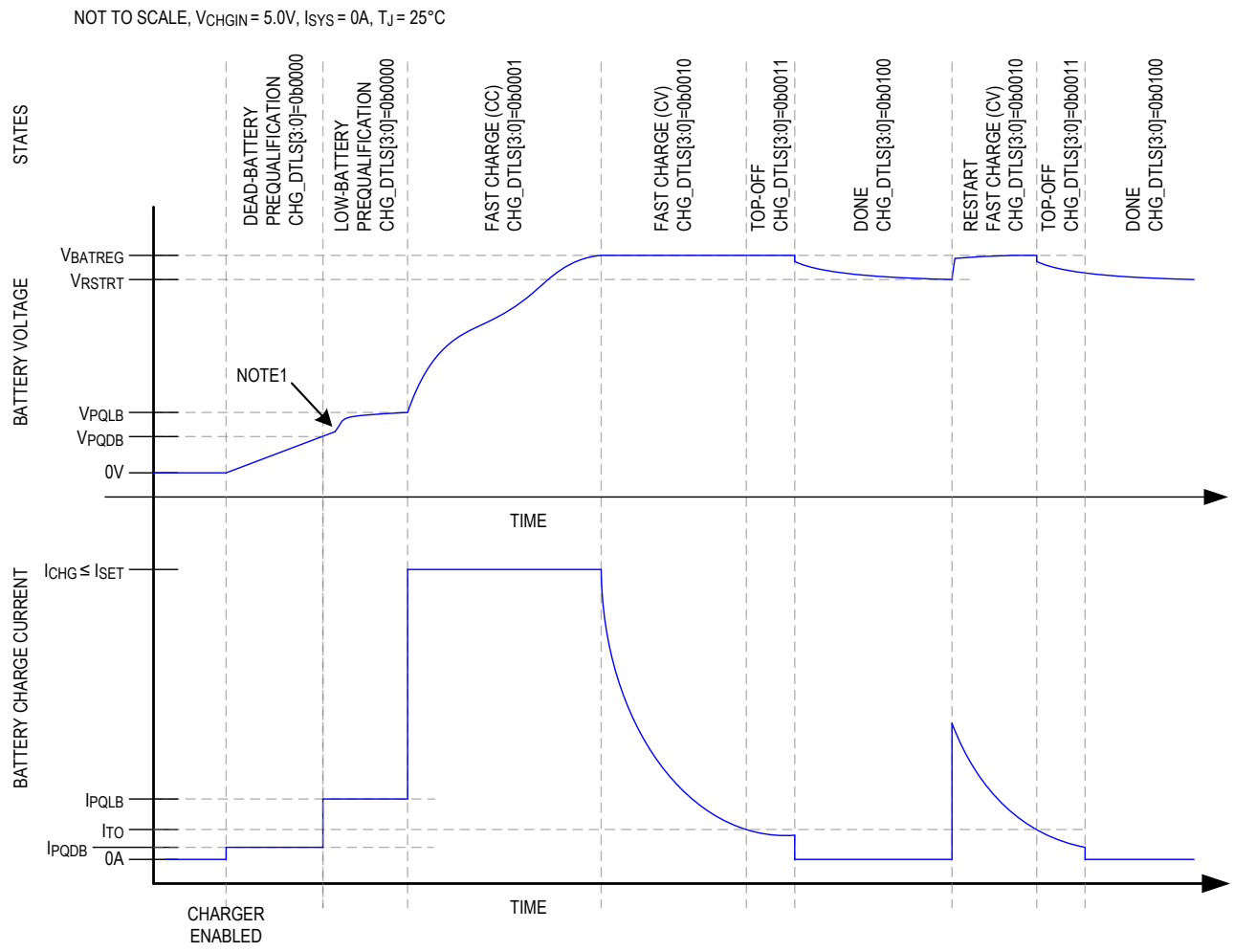


Figure 5. Battery Charger High-Current Paths with Typical Parasitic Resistances and Self-Discharging Resistors



NOTE 1: A TYPICAL LI+/LI-POLY HAS AN INTERNAL BATTERY PACK PROTECTION CIRCUIT THAT WILL OPEN THE BATTERY CONNECTION WHEN THE BATTERY'S CELL VOLTAGE IS LOWER THAN A DEAD BATTERY THRESHOLD ($V_{DB.FALLING}$~2.5V). TO GET THE PACK PROTECTION TO CLOSE AGAIN, THE CHARGER CHARGES THE BATTERY CAPACITOR WITH I_{PQDB} UNTIL THE VOLTAGE EXCEEDS V_{PQDB}. THEN THE CHARGER CHARGES THE BATTERY CAPACITOR WITH I_{PQLB}. WHEN THE BATTERY CAPACITOR'S VOLTAGE EXCEEDS $V_{DB.RISING}$~2.6V, THEN THE BATTERY PACK PROTECTION CIRCUIT CLOSES WHICH CONNECTS THE CELL TO THE CHARGER. $V_{DB.FALLING}$ AND $V_{DB.RISING}$ ARE NOT DETERMINED BY THE CHARGER – THEY ARE PROPERTIES OF THE BATTERY.

Figure 6. Li+/Li-Poly Charge Profile

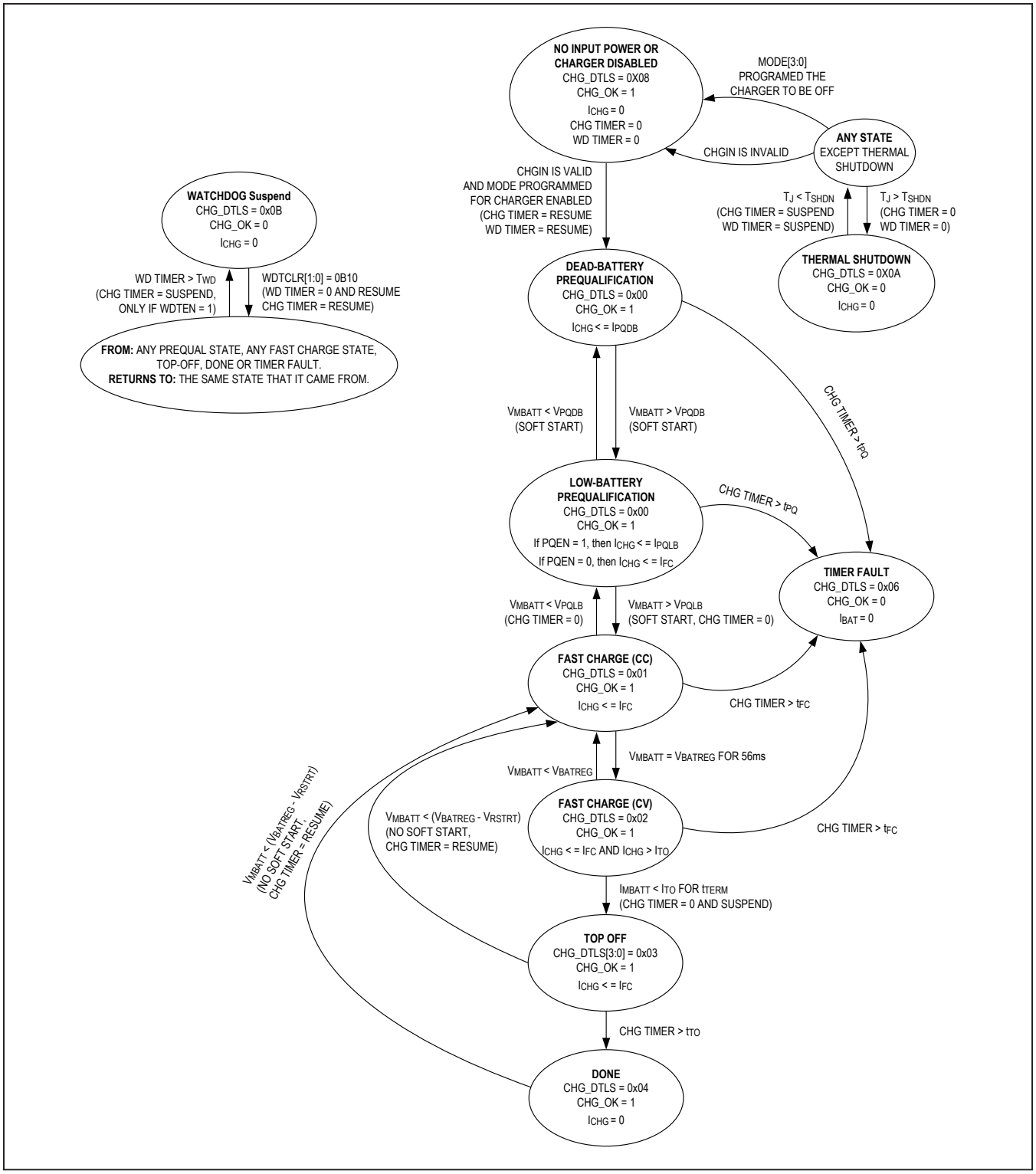


Figure 7. Charger State Diagram

No Input Power or Charger Disabled State

From any state shown in Figure 7 except thermal shutdown, the no input power or charger disabled state is entered whenever the charger is programmed to be off or the charger input CHGIN is invalid. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS[3:0] is set to 0x08.

While in the no input power or charger disabled state, the charger current is 0mA, the watchdog and charge timers are forced to 0, and the power to the system is provided by either the battery or the adapter. When both battery and adapter power are available, the adapter provides primary power to the system and the battery contributes supplemental energy to the system if necessary.

To exit the no input power or charger disabled state, the charger input must be valid and the charger must be enabled.

Dead Battery Prequalificiation State

As shown in Figure 7, the dead battery prequalification state occurs when the main battery voltage is less than V_{PQDB}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS[3:0] is set to 0x00. In the dead battery prequalification state, charge current into the battery is I_{PQDB}.

The following events cause the state machine to exit this state:

The main battery voltage rises above V_{PQDB} and the charger enters the next state in the charging cycle: low battery prequalification.

If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the timer fault state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

Note that the dead battery prequalification state works with battery voltages down to 0V. The low 0V operation typically allows this battery charger to recover batteries that have an open internal pack protector. Typically, a packs internal protection circuit opens if the battery has seen an over current, undervoltage, or overvoltage. When a battery with an open internal pack protector is used with this charger, the low battery prequalification mode current flows into the 0V battery. This current raises the pack's terminal voltage to the point where the internal pack protection switch closes.

Note that a normal battery typically stays in the low battery prequalification state for several minutes or less. Therefore, a battery that stays in low battery prequalification for longer than t_{PQ} may be experiencing a problem.

Fast-Charge Constant Current State

As shown in Figure 7, the fast-charge constant current (CC) state occurs when the main battery voltage is greater than the low battery prequalification threshold and less than the battery regulation threshold ($V_{PQLB} < V_{BATT} < V_{BATREG}$). After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set and CHG_DTLS[3:0] = 0x01.

In the fast-charge CC state, the current into the battery is less than or equal to I_{FC}. Charge current can be less than I_{FC} for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.

The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

When the main battery voltage rises above V_{BATREG}, the charger enters the next state in the charging cycle: fast charge (CV).

If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the timer fault state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds T_{REG}, I_{FC} is reduced.

Fast-Charge Constant Voltage State

As shown in Figure 7, the fast-charge constant voltage (CV) state occurs when the battery voltage rises to V_{BATREG} from the fast-charge CC state. After being in the fast-charge CV state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS[3:0] = 0x02.

In the fast-charge CV state, the battery charger maintains V_{BATREG} across the battery and the charge current is less than or equal to I_{FC}. As shown in Figure 6, charger current decreases exponentially in this state as the battery becomes fully charged.

The Smart Power Selector control circuitry may reduce the charge current lower than the battery may otherwise consume for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.

The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

When the charger current is below I_{TO} for t_{TERM}, the charger enters the next state in the charging cycle: TOP OFF.

If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the timer fault state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

Top-Off State

As shown in Figure 7, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the top-off state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is set, and CHG_DTLS[3:0] = 0x03. In the top-off state, the battery charger tries to maintain V_{BATREG} across the battery and typically the charge current is less than or equal to I_{TO}.

The Smart Power Selector control circuitry can reduce the charge current lower than the battery is able to. Otherwise, consume for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.

The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Following events causes the state machine to exit this state:

After being in this state for the top-off time (t_{TO}), the charger enters the next state in the charging cycle: DONE.

If $V_{BATT} < V_{BATREG} - V_{RSTRT}$, the charger goes back to the FAST CHARGE (CC) state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

Done State

As shown in Figure 7, the battery charger enters its done state after the charger has been in the top-off state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is cleared, and CHG_DTLS[3:0] = 0x04.

The following events cause the state machine to exit this state:

If $V_{BATT} < V_{BATREG} – V_{RSTRT}$, the charger goes back to the fast charge (CC) state.

If the watchdog timer is not serviced, the charger state machine transitions to the watchdog suspend state.

In the done state, the charge current into the battery (I_{CHG}) is 0A. In the done state, the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low (<< 100µA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the restart threshold (V_{RSTRT}) and the charger state machine transitions back into the fast-charge CV state. There is no soft-start (di/dt limiting) during the done to fast-charge state transition.

Timer-Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 7, the charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of its prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC and CV states is t_{FC}, which is programmable with FCHGTIME. Finally, the time that the charger is in the top-off state is t_{TO}, which is programmable with TO_TIME. Upon entering the timer-fault state, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x06.

In the timer-fault state the charger is off. The charger can exit the timer-fault state by programming the charger to be off and then programming it to be on again through the MODE bits. Alternatively, the charger input can be removed and reinserted to exit the timer-fault state. See the any state bubble in the upper right of Figure 7.

Watchdog Timer

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 7, the watchdog timer protects the battery from charging indefinitely in the event that the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature, enable the feature by setting WDTEN. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.

If the watchdog timer expires while the charger is in dead-battery prequalification, low-battery prequalification, fast-charge CC or CV, top-off, done, or timer fault, the charging stops, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS[3:0] indicates that the charger is off because the watchdog timer expired. Once the watchdog timer has expired, the charger can be restarted by programming WDTCLR = 0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer is expired.

Thermal-Shutdown State

As shown in Figure 7, the thermal-shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device's thermal-shutdown threshold (T_{SHDN}). When T_J is close to T_{SHDN}, the charger has folded back the input current limit to 0A so the charger and inputs are effectively off. Upon entering this state, CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS[3:0] = 0x0A.

In the thermal-shutdown state the charger is off and timers are suspended. The charger exits the temperature suspend state and returns to the state it came from once the die temperature has cooled. The timers resume once the charger exits this state.

Battery Differential Voltage Sense

As shown in Figure 2, BAT_SP and BAT_SN are differential remote sense voltage inputs for the battery. To improve accuracy and decrease charging time, the battery charger voltage sense is based on the differential voltage between BAT_SP and BAT_SN.

Figure 5 shows the high-current paths of the battery charger along with some example parasitic resistances. With the parasitics described in Figure 5, a charge current of 1A measuring from BATT to GND leads to a V_{BATT} that is 40mV higher than the real voltage because of R_{PAR1} and R_{PAR7} (I_{CHG} x (R_{PAR1} + R_{PQR7}) = 1A x 40mΩ = 40mV).

Since the charger thinks the battery voltage is higher than it actually is, it enters its fast-charge CV state sooner and the effective charge time may be extended by 10 minutes (based on real lab measurements). This charger with differential remote sensing does not experience this type of problem because BAT_SP and BAT_SN sense the battery voltage directly. To get the maximum benefit from these sense lines, connect them as close as possible to the battery connector.

OTG Mode

The DC-DC converter topology of the MAX77818 allows it to operate as a forward buck converter or as a reverse-boost converter. The operating modes of the DC-DC converter are controlled with MODE[3:0] register bits. When MODE[3:0] = 0x0A, 0x0E or 0x0F the OTG mode is enabled, the DC-DC converter provides power to CHGIN pin, commonly known as USB On-the-Go (OTG).

When OTG mode is enabled, the DC-DC converter operates in reverse-boost mode and regulates V_{BYP} to $V_{BYP.OTG}$ (5.1V, typ) and the switch from BYP to CHGIN is closed. The current through the BYP to CHGIN switch is limited to the value programmed by OTG_ILIM[1:0].

If the external OTG load at CHGIN exceeds $I_{CHGIN.OTG.ILIM}$, then a BYP_I interrupt is generated, BYP_OK = 0, and BYP_DTLS[3:0] = 0bxxx1. In response to an overload at CHGIN during OTG mode operation, the BYP to CHGIN switch is latched off. The BYP to CHGIN switch automatically tries to retry in ~300ms. If the overload at CHGIN persists, then the switch toggles on and off with ~30ms on and ~300ms off.

Battery Overcurrent Protection During System Power-Up

The main battery overcurrent protection during system power-up feature limits the main battery to system current to I_{SYSPU} as long as V_{SYS} is less than V_{SYSPU}. This feature limits the surge current that typically flows from the main battery to the device's low-impedance system bypass capacitors during a system power-up. System power-up is anytime that energy from the battery is supplied to SYS when V_{SYS} < V_{SYSPU}. This system power-up condition typically occurs when a battery is hot-inserted into an otherwise unpowered device. Similarly, the system power-up condition could occur when the DISIBS bit is driven low.

When system power-up occurs due to hot insertion into an otherwise unpowered device, a small delay of (t_{SYSPU}) is required in order for this feature's control circuits to activate. A current spike over I_{SYSPU} can occur during this time.

Battery Overcurrent Protection Due to Fault

The MAX77818 protects itself, the battery, and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current may occur in a smartphone for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit. The main battery overcurrent protection feature is enabled with B2SOVRC; disabling this feature reduces the main battery current consumption by I_{MBOVRC}.

When the battery (BATT) to system (SYS) discharge current (I_{BATT}) exceeds the programmed overcurrent threshold for at least t_{MBOVRC}, a BAT_I interrupt is generated, BAT_OK is cleared, and BAT_DTLS reports and overcurrent condition. Typically when the system's processor detects this overcurrent interrupt, it executes a housekeeping routine that tries to mitigate the overcurrent situation. If the processor cannot correct the overcurrent, then it can disable the BATT to SYS discharge path (B2S switch) by driving DISIBS bit to a logic high.

There are different scenarios of how the MAX77818 responds to setting the DISIBS bit high depending on the available power source and the state of the charger.

The MAX77818 is only powered from BATT and DISIBS bit is set.

SYS collapses and is allowed to go to 0V.

DISIBS holds state.

To exit from this state, plug in a valid input charger, then SYS is powered up, and the system wakes up.

The MAX77818 is powered from BATT and CHGIN, and the charger buck is not switching and DISIBS bit is set.

To exit from this state, plug in a valid input charger, then SYS is powered up and the system wakes up.

The MAX77818 is powered from BATT and CHGIN and the charger buck is switching and DISIBS bit is set.

The DISIBIS bit is ignored.

Thermal Management

The MAX77818 charger uses several thermal management techniques to prevent excessive battery and die temperatures.

Thermal Monitor

The user can monitor thermistor temperature using the fuel gauge and adjust the charger voltage/current as needed.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the MAX77818 junction temperature. As shown in Figure 8, when the die temperature exceeds the value programmed by REGTEMP (T_{JREG}), a thermal limiting circuit reduces the battery charger's target current by 105mA/°C (A_{TJREG}). The target charge current reduction is achieved with an analog control loop (i.e., not a digital reduction in the input current). When the thermal foldback loop changes state, a CHG_I interrupt is generated and the system's microprocessor may want to read the status of the thermal regulation loop through the TREG status bit. Note that the thermal foldback loop being active is not considered to be abnormal operation and the thermal foldback loop status does not affect the CHG_OK bit (only information contained within CHG_DTLS affects CHG_OK).

Analog Low-Noise Power Input (AVL) and PVL

As shown in Figure 2, AVL is a regulated output from BYPC node. AVL is the power input for the MAX77818 charger's analog circuitry. PVL has a 12.5Ω resistor internal to the MAX77818 and a 10µF ceramic capacitor external bypass capacitor to isolate noises from AVL.

Power States

The MAX77818 transitions between power states as input/battery and load conditions dictate; see Figure 9.

The MAX77818 provides seven power states and one no power state. Under power-limited conditions, the power path feature maintains SYS and USB-OTG loads at the expense of battery charge current. In addition, the battery supplements the input power when required. As shown, transitions between power states are initiated by detection/removal of valid power sources, OTG events, and under-voltage conditions. Details of the BYP and SYS voltages are provided for each state.

No Input Power, MODE = undefined: No input adapter or battery is detected. The charger and system is off. Battery is disconnected and charger is off.

Battery Only, MODE = 0x00: Adapter and wireless charger are invalid, outside the input voltage operating range (QCHGIN = off, QWCIN = off). Battery is connected to power the SYS load (QBAT = on), and boost is ready to power OTG (Boost=standby), see Figure 10**. Battery Only.**

Battery Boost, MODE = 0x08: Adapter and wireless inputs are invalid, outside the input voltage operating range (QCHGIN = off, QWCIN = off). Battery is connected to power the SYS load (QBAT = on), and charger is operating in Boost mode (Boost = on). See Figure 11.

Battery Boost (OTG), MODE = 0x0A: Wireless input is turned off (QWCIN = off) and OTG is active (QCHGIN = on). Battery is connected to support SYS and OTG loads (QBAT = on), and charger is operating in boost mode (boost = on). See Figure 12.

No Charge Buck, MODE = 0x0C: Adapter or wireless charger are detected, within the input voltage operating range (QCHGIN = on or QWCIN = on). Battery is disconnected (QBAT = off), and charger is operating in buck mode powering the SYS node. See Figure 13.

Charge Buck, MODE = 0x0D: Adapter or wireless charger are detected, within the input voltage operating range (QCHGIN = on or QWCIN = on). Battery is connected in charge mode (QBAT = on), and charger is operating in buck mode. See Figure 14.

No Change Buck (OTG), MODE = 0x0E: Wireless charger is detected within the input voltage operating range (QWCIN = on) and OTG is active (QCHGIN = of). Battery is connected in charge mode (QBAT = on), and charger is operating in buck mode. See Figure 15.

Charge Buck (OTG), MODE = 0x0F: Wireless charger is detected within the input voltage operating range (QWCIN = on) and OTG is active (QCHGIN = on). Battery is connected in charge mode (QBAT = on), and charger is operating in buck mode powering the SYS node. See Figure 16.

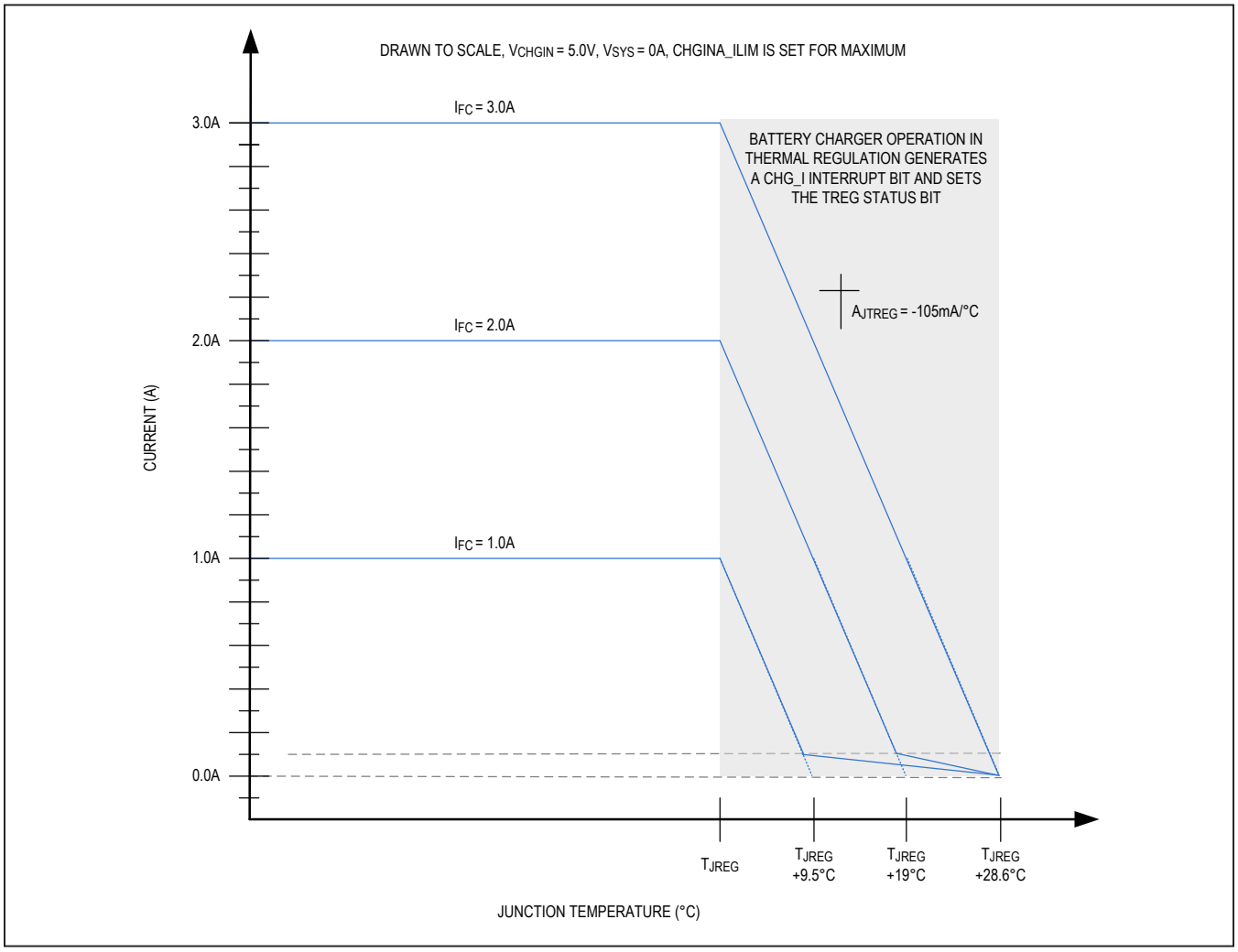


Figure 8. Charge Currents vs. Junction Temperature

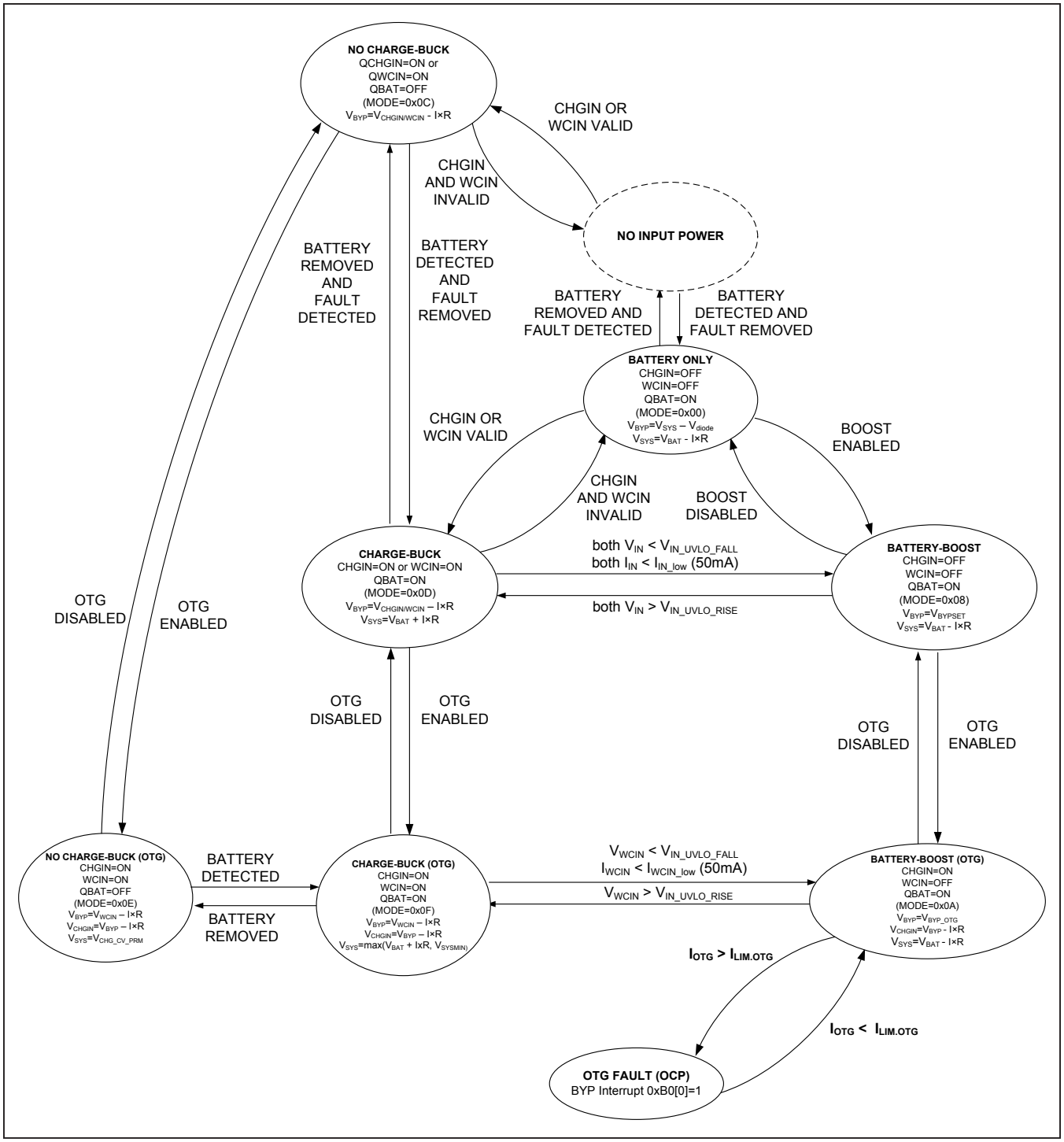


Figure 9. Power State Diagram

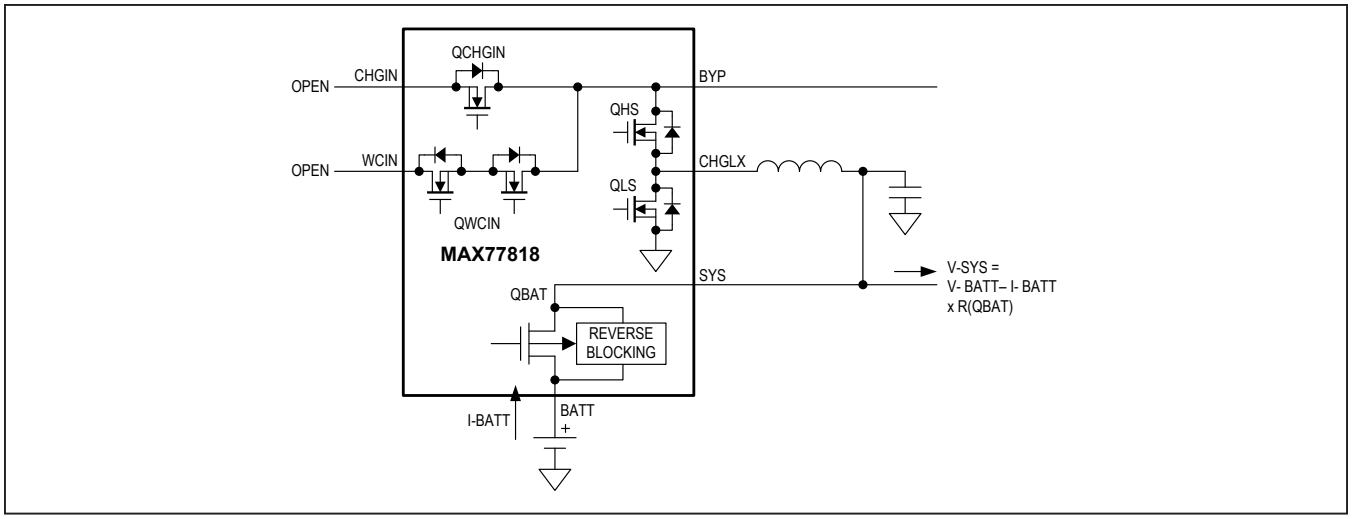


Figure 10. Battery-Only

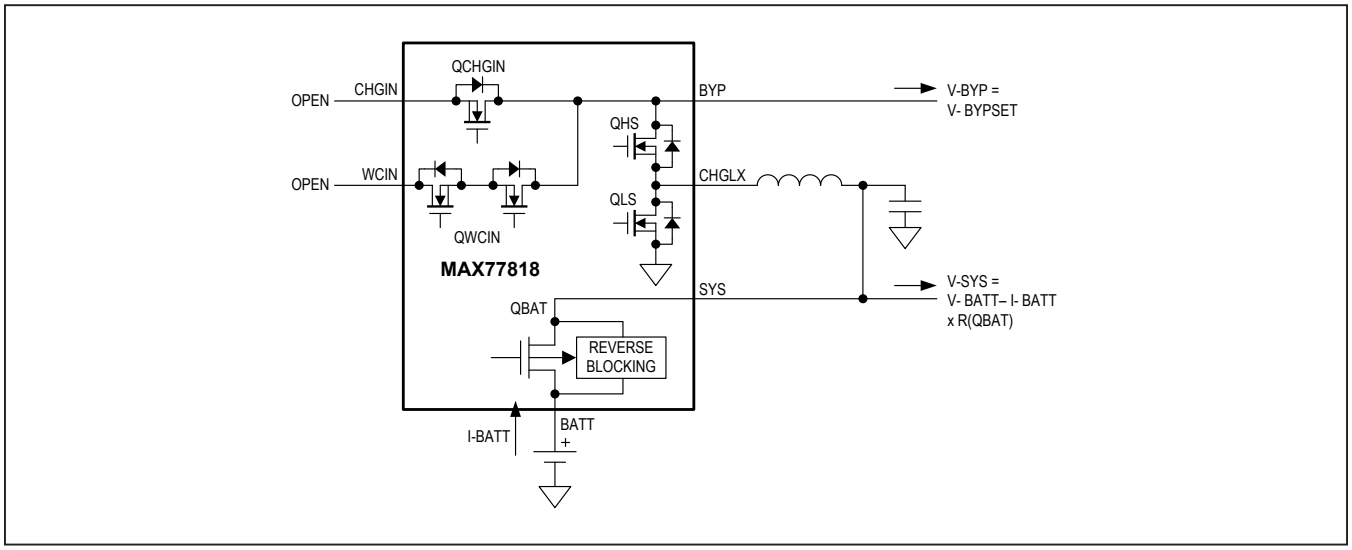


Figure 11. Battery-Boost

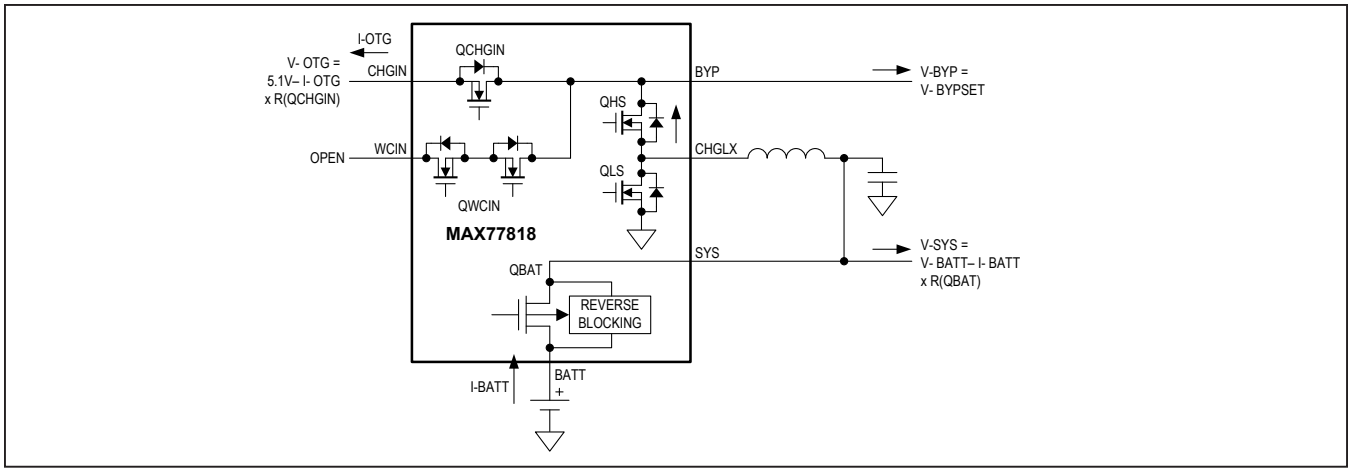


Figure 12. Battery Boost (OTG)

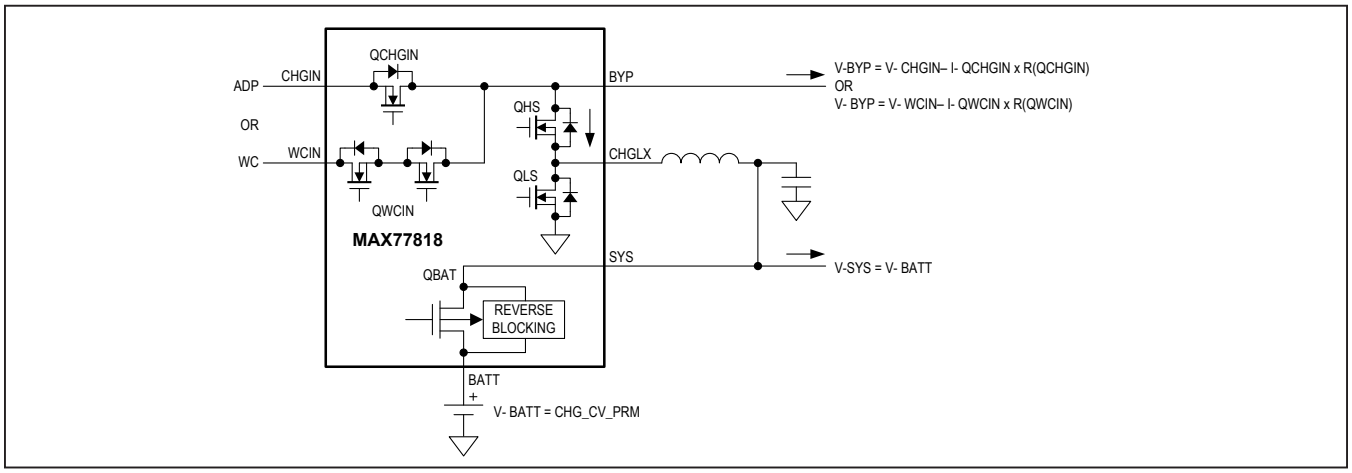


Figure 13. No Charge Buck

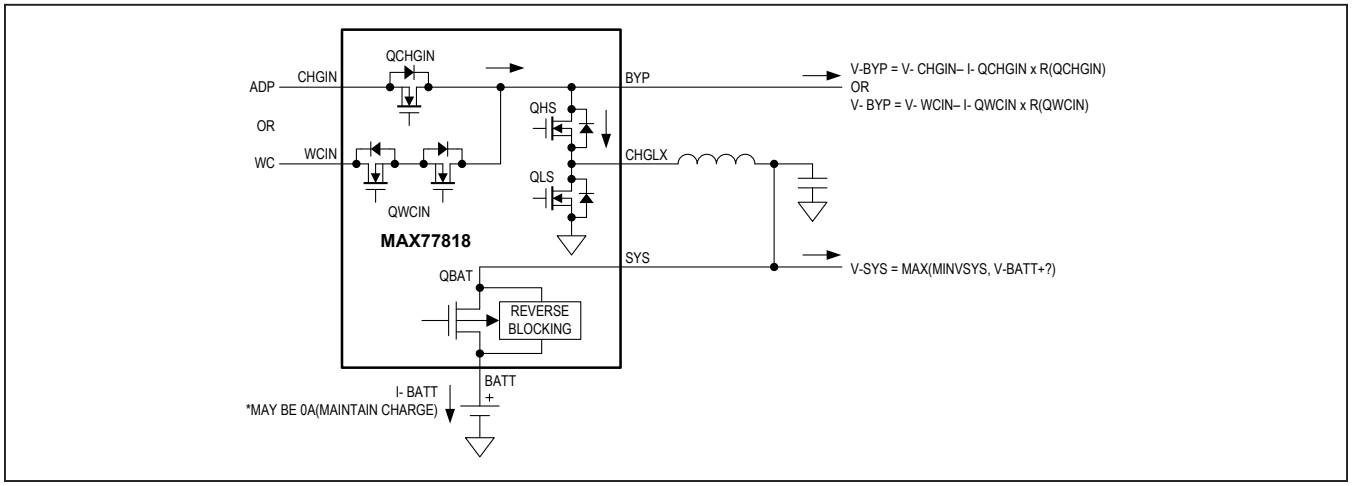


Figure 14. Charge Buck

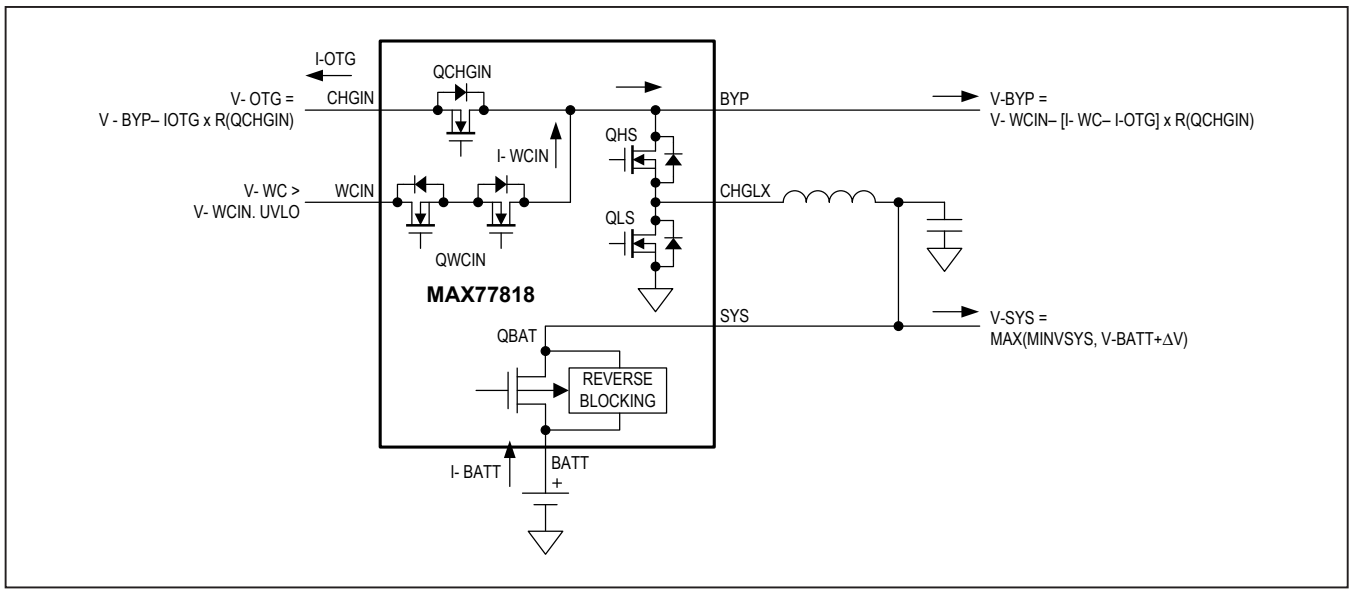


Figure 15. No Charge Buck (OTG)

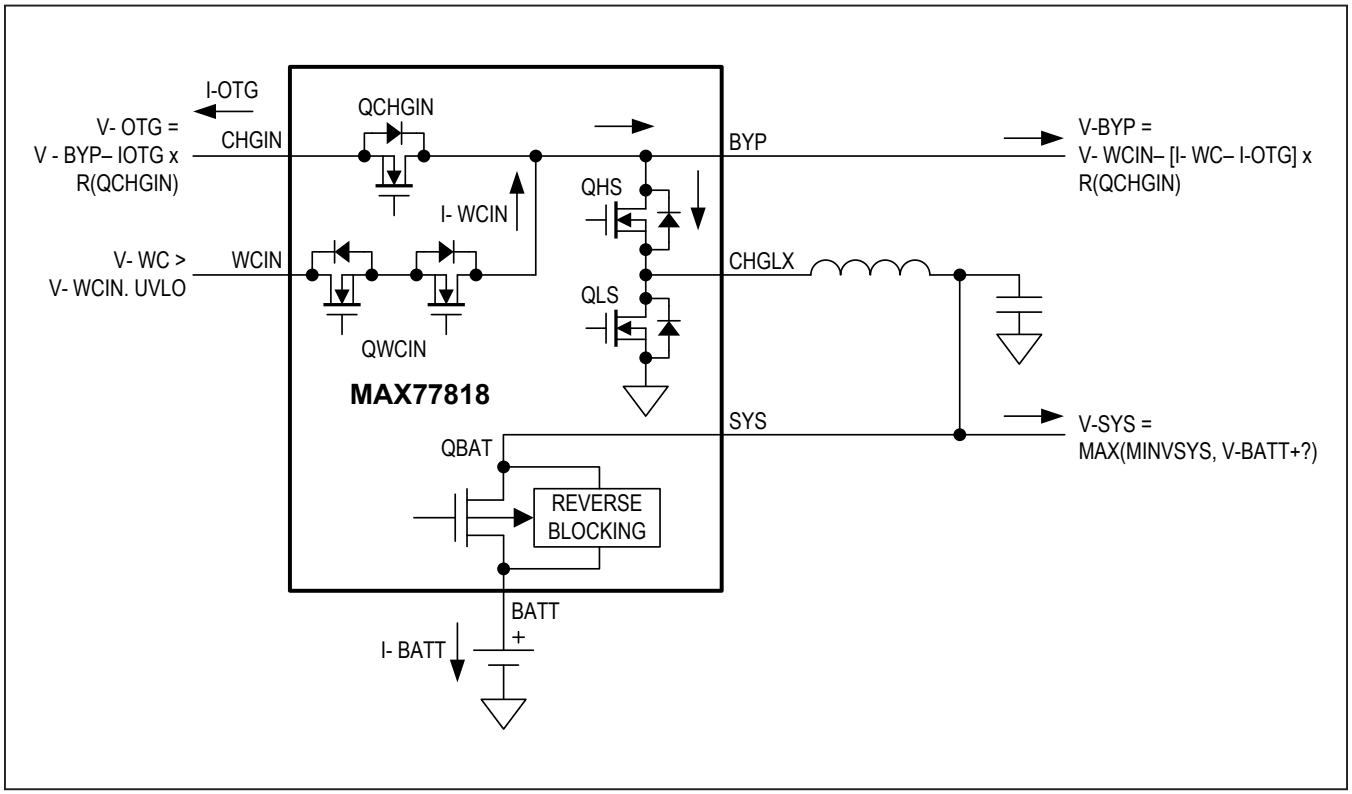


Figure 16. Charge-Buck (OTG)

ModelGauge m5 Details

The MAX77818 incorporates the Maxim ModelGauge m5 algorithm that combines the excellent short-term accuracy and linearity of a coulomb counter with the excellent long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel-gauge accuracy. The device also includes Cycle+ charger control, improved aged adaptation, improved state-of-charge (SOC) accuracy to empty, and increased temperature measurement accuracy. ModelGauge m5 cancels offset accumulation error in the coulomb counter, while providing better short-term accuracy than any purely voltage-based fuel gauge. Additionally, the ModelGauge m5 algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time. The device automatically compensates for aging, temperature, and discharge rate and provides accurate SOC in mAh or % over a wide range of operating conditions. The device provides two methods for reporting the age of the battery: reduction in capacity and cycle odometer. The device provides precision measurements of current, voltage, and temperature. Temperature of the battery pack is measured using an external thermistor supported by ratiometric measurements on an auxiliary input. A 2-wire (I^2C) interface provides access to data and control registers.

ModelGauge m5 Algorithm

The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a voltage fuel gauge (VFG), as described in Figure 17. Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated, causes the reported capacity error to increase over time, and requires periodic corrections. Corrections are usually performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the SOC based on the battery voltage after a long time of no current flow. Both have the same limitation: if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Classical voltage-measurement-based SOC estimation has poor accuracy due to inadequate cell modeling, but does not accumulate offset error over time. The device includes an advanced VFG, which estimates open-circuit voltage (OCV), even during current flow, and simulates the nonlinear internal dynamics of a lithium-ion (Li+) battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC based on table lookup. This SOC estimation does not accumulate offset error over time. The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a VFG. The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG, while providing the strengths of both. A mixing algorithm combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, canceling the coulomb-counter drift. The ModelGauge m5 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. The ModelGauge m5 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated, and the VFG dynamics adapt based on cell voltage behavior in the application.

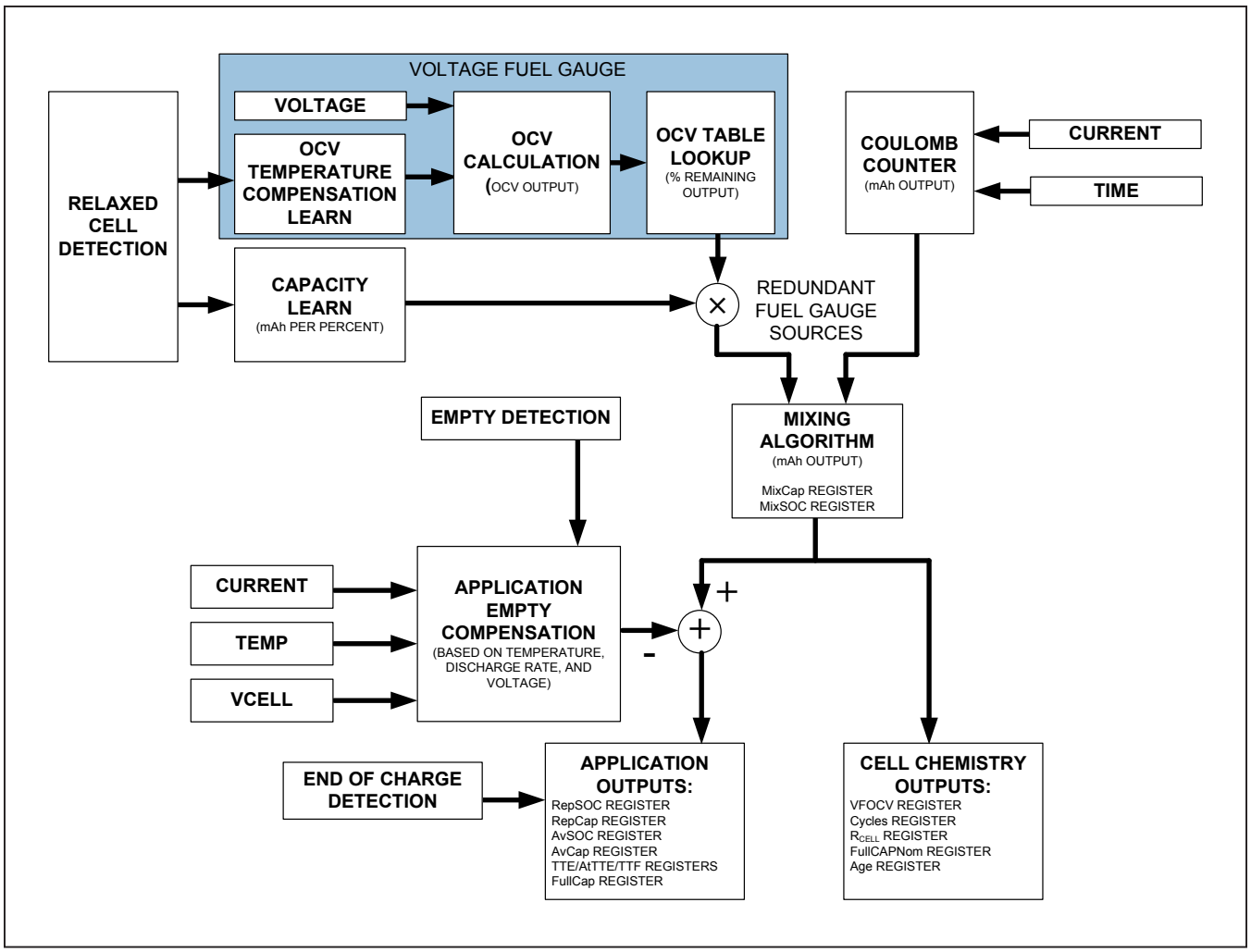


Figure 17. ModelGauge m5 Block Diagram

OCV Estimation and Coulomb-Count Mixing

The core of the ModelGauge m5 algorithm is a mixing algorithm that combines the OCV state estimation with the coulomb counter. After power-on reset of the IC, coulomb-count accuracy is unknown. The OCV state estimation is weighted heavily compared to the coulomb-count output. As the cell progresses through cycles in the application, coulomb-counter accuracy improves and the mixing algorithm alters the weighting so that the coulomb-counter result is dominant. From this point forward, the IC switches to servo mixing. Servo mixing provides a fixed magnitude continuous error correction to the coulomb count, up or down, based on the direction of error from the OCV estimation. This allows differences between the coulomb count and OCV estimation to be corrected quickly. The resulting output from the mixing algorithm does not suffer drift from current measurement offset error and is more stable than a stand-alone OCV estimation algorithm. Initial accuracy depends on the relaxation state of the cell. The highest initial accuracy is achieved with a fully relaxed cell.

Fuel-Gauge Empty Compensation

As the temperature and discharge rate of an application changes, the amount of charge available to the application also changes. The ModelGauge m5 algorithm distinguishes between remaining capacity of the cell (RemCapMIX), and remaining capacity of the application (RemCapAV), and reports both results to the user.

Fuel-Gauge Learning

The device periodically makes internal adjustments to cell characterization and application information to remove initial error and maintain accuracy as the cell ages. These adjustments always occur as small under corrections to prevent instability of the system and prevent any noticeable jumps in the fuel-gauge outputs. Learning occurs automatically without any input from the host. To maintain learned accuracy through power loss, the host must periodically save learned information and then restore after power is returned. See the *Power-Up and Power-On Reset* section for details:

- **Full Capacity Available to Application (FullCAP):** This is the total capacity available to the application at full. FullCAP is updated near the end of charging when termination is detected. See the *End-of-Charge Detection* section.
- **Cell Capacity (FullCapNom):** This is the total cell capacity at full, according to the VFG. This includes some capacity that is not available to the application at high loads and/or low temperature. The device periodically compares percent change based on OCV measurement vs. coulomb-count change as the cell charges and discharges. This information allows the device to maintain an accurate estimation of the cell's capacity in mAh as the cell ages.
- **Voltage Fuel-Gauge Adaptation:** The device observes the battery's relaxation response and adjusts the dynamics of the VFG. This adaptation adjusts the RCOMP0 register during qualified cell relaxation events.
- **Empty Compensation:** The device updates internal data whenever cell empty is detected (VCELL < V_empty) to account for cell age or other cell deviations from the characterization information.

Determining Fuel-Gauge Accuracy

To determine the true accuracy of a fuel gauge, as experienced by end users, the battery should be exercised in a dynamic manner. The end-user accuracy cannot be understood with only simple cycles. To challenge a correction-based fuel gauge, such as a coulomb counter, test the battery with partial loading sessions. For example, a typical user can operate the device for 10 minutes and then stop use for an hour or more. A robust test method includes these kinds of sessions many times at various loads, temperatures, and duration.

Initial Accuracy

The device uses the first voltage reading after power-up or after cell insertion to determine the starting output of the fuel gauge. It is assumed that the cell is fully relaxed prior to this reading; however, this is not always the case. If the cell was recently charged or discharged, the voltage measured by the device may not represent the true state of charge of the cell, resulting in initial error in the fuel-gauge outputs. In most cases, this error is minor and is quickly removed by the fuel-gauge algorithm during normal operation.

Cycle+ Charger Control

ModelGauge m5 is paired internally with a programmable, high voltage, high current charger. The charger has adjustable JEITA thresholds and works with the Cycle+ scheme to control the charge current vs. state-of-charge. In addition, Cycle+ provides smart-full charge termination, which can control charger charge-termination according to the OCV prediction of the fuel gauge. This helps to support more accurate charge termination and is less sensitive to system load transients at the end of charging.

End-of-Charge Detection

The device detects the end of a charge cycle when the application current falls into the band set by the ICHGTerm register value. By monitoring both the current and average current registers, the device can reject false end-of-charge events such as application load spikes or early charge-source removal. When a proper end-of-charge event is detected, the device learns a new FullCAP register value based on the RemCapREP output. If the old FullCAP value was too high, it is adjusted downward after the last valid end-of-charge detection. If the old FullCAP was too low, it is adjusted upward to match RemCapREP. This prevents the calculated state of charge from ever reporting a value greater than 100%.

Power-Up and Power-On Reset

Any power-on reset (POR) of the device resets all memory locations to their default POR value. This removes any custom cell characterization and application data, affects ALRT interrupt and shutdown mode settings, and resets all learned adjustments made by the fuel gauge. To maintain accuracy of the fuel gauge and reset operation settings of the device, the host must reload all application memory data and restore all learned fuel gauge information. Note that the device can take up to 445ms to completely reset operation after a POR event occurs. Saved data should not be restored until after this period is over. The following procedure is recommended:

- Read Status register. If POR = 0, exit.
- Wait 600ms for POR operation to fully complete.
- Restore all application register values.
- Restore fuel gauge learned-value information (see the *Save and Restore Registers* section).
- Clear POR bit.

Save and Restore Registers

The device is designed to operate outside the battery pack and can therefore be exposed to power loss when in the application. To prevent the loss of learned information during power cycles, a save-and-restore procedure can be used to maintain register values in nonvolatile memory external to the device. The registers (see Table 1) must be stored externally and then rewritten to the device after power-up to maintain a learned state of operation. Note that some registers are application outputs, some registers are for internal calculations, and some are characterization setup registers. Registers that are not internal are described in their own sections. These values should be stored by the application at periodic intervals. Some recommended back-up events are:

- End-of-charge
- End-of-discharge
- Prior to application entering shutdown state

The host is responsible for loading the default characterization data at first power-up of the device, and restoring the default characterization data, plus learned information on subsequent power-up events.

Battery Removal and Insertion

The device detects when a cell has been removed or inserted into the application. This allows the device to adjust to the new cell to maintain accuracy. The removal detection feature also allows the device to quickly warn the host processor through interrupt of impending power loss if enabled. Detection occurs by monitoring the AIN pin voltage compared to the THRM pin. Whenever a cell is present, the external resistor-divider network sets the voltage of AIN. When the cell is removed, the remaining external resistor pulls AIN to the THRM pin voltage level. Whenever VAIN < VTHRM - VDETF, the device determines that a cell is present in the application. If VAIN > VTHRM - VDETR, the device determines that no cell is present at that time.

Cell Insertion (IC Already Powered)

The device is ready to detect a cell insertion if either the ETHRM or FTHRM bits of the CONFIG register are set to enable the THRM pin output. When a cell insertion is detected, the fuel gauge is reset and all fuel-gauge outputs are updated to reflect the SOC of the newly inserted cell. This process can take up to 1.845s (FTHRM = 0) or 620ms (FTHRM = 1) from time of insertion. Note that the device uses the cell voltage as a starting point for the fuel gauge. If the cell voltage is not fully relaxed at time of insertion, the fuel gauge begins with some initial error. See the *Fuel-Gauge Learning* section for details. The host can disable this feature by clearing the enBi1 bit in the MiscCFG register. The device can also be configured to alert the host when cell insertion occurs. When Bei = 1 in the CONFIG register, the device generates an interrupt on the ALRT pin at the start of the first temperature conversion after insertion. This could take up to 1.4s to occur. This feature is useful if the application uses more than one cell type and the device must be reconfigured at each insertion.

Cell Removal

The device detects a cell removal if either the ETHRM or FTHRM bits of the CONFIG register are set to enable the THRM pin output. Cell removal does not affect IC operation. The device continues to update fuel-gauge outputs. The host should monitor the Br and Bst bits of the Status register to determine if the fuel-gauge outputs are valid. The device can also be configured to alert the host when cell removal occurs. When Ber = 1 in the CONFIG register, the device generates an interrupt on the ALRT pin at the start of the first temperature conversion after removal. This could take up to 1.4s to occur. This feature is useful if the application uses more than one cell type and the device must be reconfigured at each insertion.

Fast Detection of Cell Removal

The device can be configured to quickly alert the host of impending power loss on cell removal. This fast response allows the system to quickly and gracefully hibernate to prevent power loss during battery swap. When Ber = 1, FTHRM = 1, and ALRTp = 0 in the CONFIG register, an interrupt on the ALRT pin is generated within 100Fs after VAIN becomes greater than VTHRM - VDETR. If fast detection is used, it is recommended that all other IC interrupts are disabled to prevent the host from spending time determining the cause of the interrupt. Fast detection of cell removal has no effect on fuel-gauge operation, but leaving the external resistor-divider active increases current consumption of the application.

Modes of Operation

The device operates in one of two power modes: active and shutdown. While in active mode, the device operates as a high-precision battery monitor with temperature, voltage, auxiliary inputs, current, and accumulated current measurements acquired continuously, and the resulting values updated in the measurement registers. READ and WRITE access is allowed only in active mode. In shutdown mode, the LDO is disabled and all activity stops, **although volatile RAM contents remain preserved**. All A/D register and fuel-gauge output values are maintained. There are several options for entering shutdown:

Entering shutdown:

- **SHUTDOWN Command**—Write the CONFIG register SHDN = 1 through the I2C interface; wait for longer than the SHDNTIMER register value.
- **Pack Removal**—Pack removal detection is valid for longer than the SHDNTIMER register value and the CONFIG register AINSH = 1.
- **I2C Shutdown**—I2C lines both persist low for longer than the SHDNTIMER register value and the CONFIG register I2CSH = 1.
- **ALRT Shutdown**—Shutdown occurs when the ALRT line is externally driven low for longer than the SHDNTIMER register value (ALSH = 1 and ALRTp = 0), or the ALRT line is externally driven high for longer than the SHDNTIMER register value (ALSH = 1 and ALRTp = 1). See the CONFIG Register (1Dh) section.

These shutdown entry modes are all programmable according to application. Shutdown events are gated by the SHDNTIMER register, which allows a long delay between the shutdown event and the actual shutdown. By behaving this way, the device takes the best reading of the relaxation voltage.

Exiting shutdown:

- **I2C Wakeup**—Any edge on SCL/SDA.
- **ALRT Wakeup**—Any edge on ALRT line and (ALSH = 1 or I2CSH = ALSH = 0).
- **Reset**—IC is power cycled.

See the *Status and Configuration Registers* section for detailed descriptions of the SHDNTIMER and CONFIG registers. The state of the device when returning to active mode differs depending on the triggering event. Host software can monitor the POR and Bi status bits to determine what type of event has occurred.

ALRT Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, a high or low temperature, or a high or low SOC. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup is required to generate a logic-high signal. Note that if the pin is configured to be logic-low when inactive, the external pullup increases current drain. The ALRTp bit in the CONFIG register sets the polarity of the ALRT pin output. Alerts can be triggered by any of the following conditions:

- **Battery Removal**—(VAIN > VTHRM - VDETR) and battery removal detection enabled (Ber = 1).
- **Battery Insertion**—(VAIN < VTHRM - VDETF) and battery insertion detection enabled (Bei = 1).
- **Over/Under Voltage**—VALRT threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **Over/Under Temperature**—TALRT threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **Over/Under SOC**—SALRT threshold violation (upper or lower) and alerts enabled (Aen = 1).
- **dSOC**— 1% change in SOC (Config.dSOC = 1)
- **Charger Communication Failure**—Set when FG fails to communicate with the charger. Controlled by Config.FCFE and Config.ICFE.

To prevent false interrupts, the threshold registers should be initialized before setting the Aen bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the status register. Alerts generated by a threshold-level violation can be configured to be cleared only by software, or cleared automatically when the threshold level is no longer violated. See the CONFIG (1Dh) register description for details of the alert function configuration.

IC Memory Map

The device has a 256-word linear memory space containing all user-accessible registers. All registers are 16 bits wide and are read and written as 2-byte values. When the MSB of a register is read, the MSB and LSB are latched simultaneously and held for the duration of the Read Data command. This prevents updates to the LSB during the read, ensuring synchronization between the 2 register bytes. All locations are volatile RAM and lose their data in the event of power loss. Data is retained during device shutdown. Each register has a power-on-reset value that it defaults to at power-up. Word addresses designated as reserved return an undetermined when read. These locations should not be written.

ModelGauge m5 Registers

All ModelGauge m5 registers are shown in Table 1. The register address is composed by two HEX digits shown given by first row and first column. All the registers are grouped by their functions and described in the *ModelGauge m5 Output Registers* section.

Table 1. ModelGauge m5 Registers

0X6C I²C COMMAND ADDRESS	0X0_	0X1_	0X2_	0X3_	0X4_	0X5_ 0X7_	0X8_	0X9_	0XA_	0XB_	0XC_	0XD_	0XE_	0XF_
0x0_0	STATUS	FullCAP	TTF	Reserved	Reserved	Reserved	OCV	CAP	RCOMP seg	Status2	Reserved	Reserved	Reserved	Reserved
0x0_1	VALRT_Th	TTE	DevName	Reserved	Reserved					Reserved		ChargeState0		Reserved
0x0_2	TALRT_Th	QRtable00	QRtable10	QRtable20	QRtable30					TALRT_Th2		ChargeState1		Reserved
0x0_3	SALRT_Th	FullSOCthr	FullCAPNom	AtTTF	Reserved					Reserved		ChargeState2		Reserved
0x0_4	AtRate	RSLOW	TempNom	Reserved	Reserved					Reserved		ChargeState3		Reserved
0x0_5	RepCap	Reserved	TempLim	FullCapRep	dQ_acc					TTF_CFG		ChargeState4		Reserved
0x0_6	RepSOC	AvgTA	Reserved	Iavg_empty	dP_acc					CV_MixCap		ChargeState5		Reserved
0x0_7	Age	Cycles	AIN0	FCTC	Reserved					CV_HalfTime		ChargeState6		Reserved
0x0_8	TEMP	DesignCap	LearnCFG	RCOMP0	Reserved					CGTempCo		ChargeState7		Reserved
0x0_9	VCELL	AvgVCELL	FilterCFG	TempCo	ConvgCfg					Curve		JEITA_Volt		Reserved
0x0_A	Current	MaxMinTemp	RelaxCFG	V_empty	VFRemCap					Reserved		JEITA_Curr		Reserved
0x0_B	AvgCurrent	MaxMinVolt	MiscCFG	Reserved	Reserved					Config2		SmartChgCfg		VFOCV
0x0_C	Qresidual	MaxMinCurr	TGAIN	Reserved	Reserved					Vripple		AtQresidual		Reserved
0x0_D	MixSOC	CONFIG	TOFF	Reserved	QH					RippleCfg		AtTTE		Reserved
0x0_E	AvSOC	ICHGTerm	CGAIN	TIMER	Reserved					TIMERH		AtAvSOC		Reserved
0x0_F	MixCap	AvCap	COFF	SHDNTIMER	Reserved					MaxError		AtAvCap		VFSOC

System Protections

V_{SYS} Undervoltage Lockout ($V_{SYSUVLO}$)

When SYS voltage falls below $V_{SYSUVLO}$, the device's type O registers are reset.

When the charger input is valid and battery is present and:

$$V_{PQDB}<V_{SYS}<V_{SYS\_UVLO}$$

Q_{BAT} is on and SYS is shorted to BATT.

When:

$$0 < V_{SYS} < V_{PQDB}$$

Q_{BAT} is off, but the charger pulls up SYS from BAT with a constant current of 50mA.

When charger input is invalid and battery is present and:

$$V_{PQDB}<V_{SYS}<V_{SYSUVLO}$$

Q_{BAT} is on and SYS is shorted to BAT.

When:

$$0 < V_{SYS} < V_{PQDB}$$

Q_{BAT} is off.

V_{SYS} Overvoltage Lockout ($V_{SYSOVLO}$)

Ideally, V_{SYS} should not exceed the battery charge termination threshold. Systems must be designed so that V_{SYS} never exceeds 4.8V (transient and steady-state). If the V_{SYS} exceeds $V_{SYSOVLO}$ during a fault, the MAX77818 resets the charger and fuel gauge O type registers.

Safeout LDO

The MAX77818 integrates two high voltage input LDOs, with I²C programmable on/off control, active discharge and programmable output voltages, ideal for powering low voltage rated USB systems. Refer to the register 0xC6: SAFEOUT LDO Control detailed description. SAFEOUT1 is enabled by default once charger detection is completed and CHGIN is valid. SAFEOUT1 is off by default.

I²C Interface

The MAX77818 acts as a slave transmitter/receiver. The MAX77818 has the following slave addresses:

Slave Addresses

Charger: 0xD2/D3h

Clogic, GTEST and Safeout LDOs: 0xCCh/0xCDh

Fuel Gauge: 0x6C/0x6D. See the Fuel Gauge I²C Protocol for details in the *Fuel Gauge Electrical Characteristics* section.

I²C Bit Transfer

One data bit is transferred for each clock pulse. The data on SDA must remain stable during the high portion of the clock pulse as changes in data during this time are interpreted as a control signal.

I²C Start and Stop Conditions

Both SDA and SCL remain high when the bus is not busy. A high-to-low transition of SDA, while SCL is high is defined as the start (S) condition. A low-to-high transition of SDA while SCL is high is defined as the stop (P) condition.

I²C System Configuration

A device on the I²C bus that generates a message is called a transmitter and a device that receives the message is a receiver. The device that controls the message is the master. The devices that are controlled by the master are called slaves.

I²C Acknowledge

The number of data bytes between the start and stop conditions for the transmitter and receiver are unlimited.

Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a high-level signal put on SDA by the transmitter during the time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge clock pulse (set-up and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a stop condition.

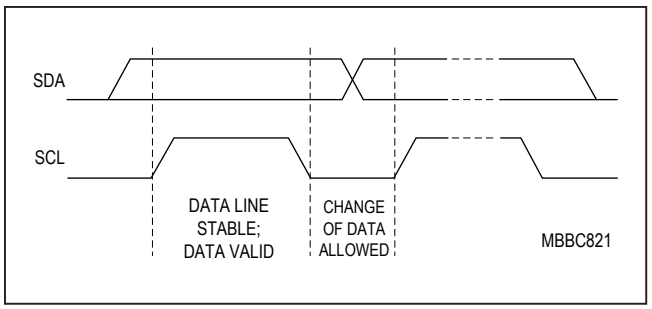


Figure 18. I²C Bit Transfer

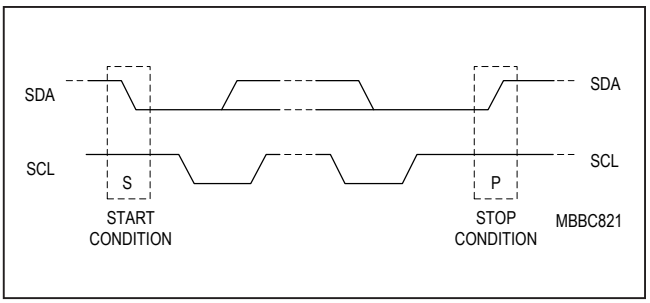


Figure 19. I²C Start and Stop

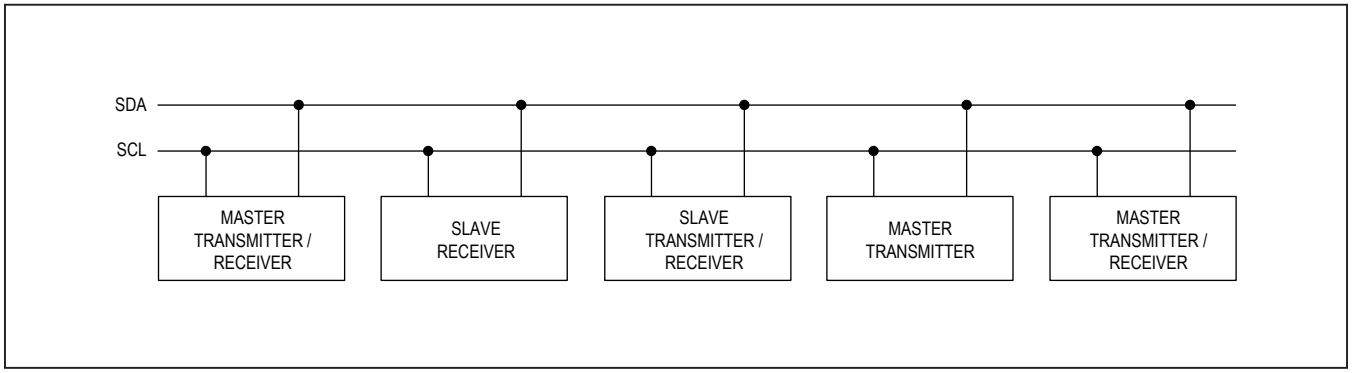


Figure 20. I²C System Configuration

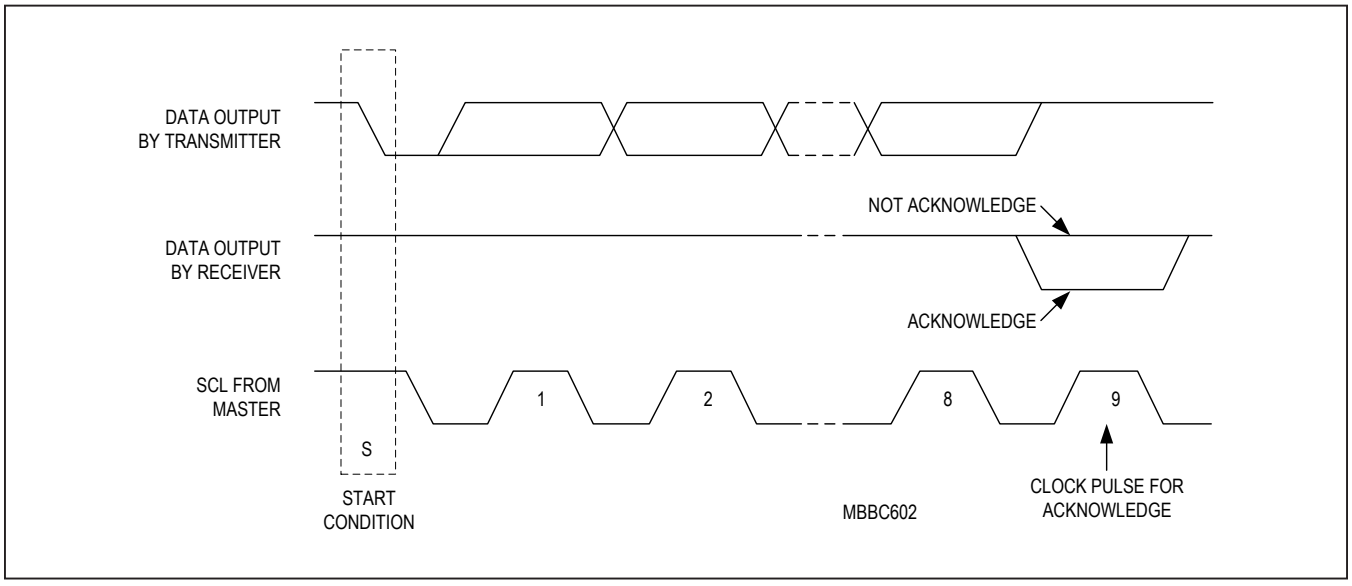
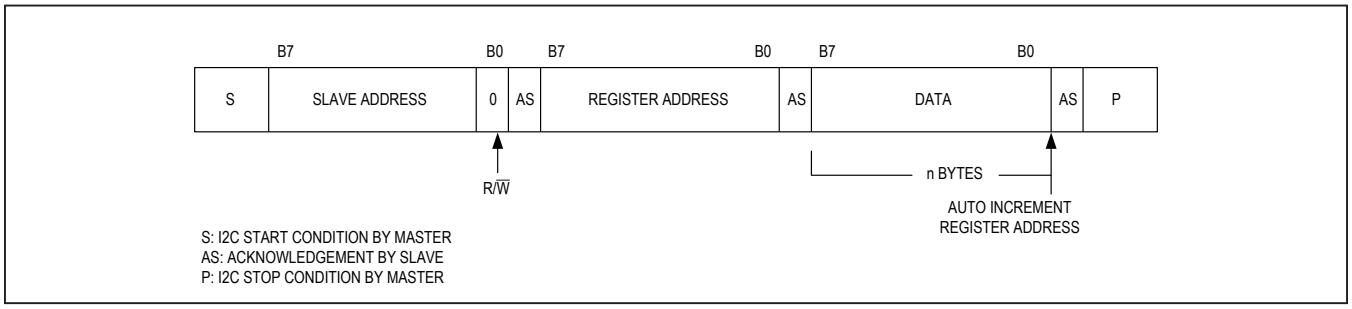


Figure 21. I²C Acknowledge

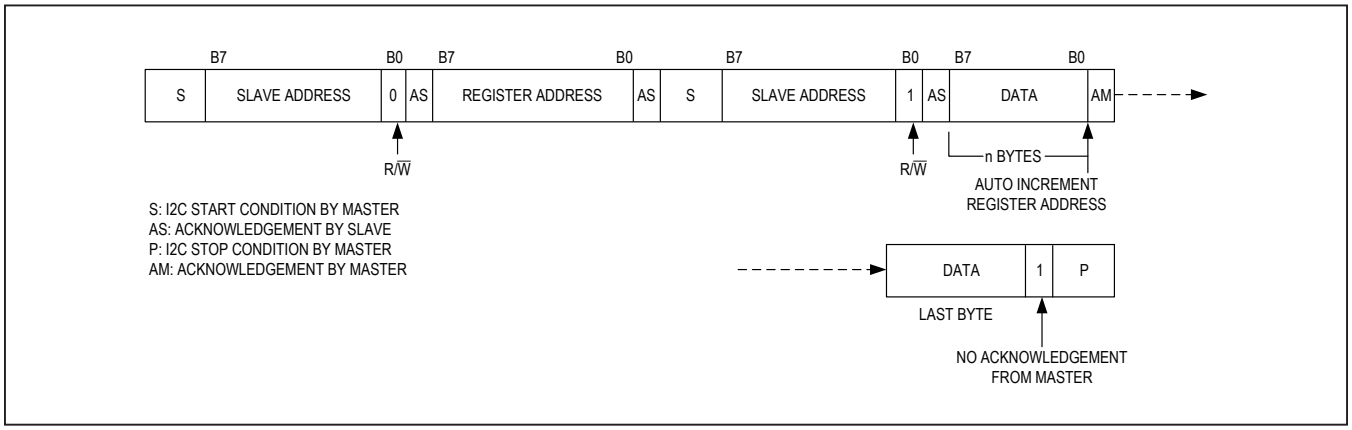
Master Transmits (Write Mode)

When master writes to slave, use the following format:



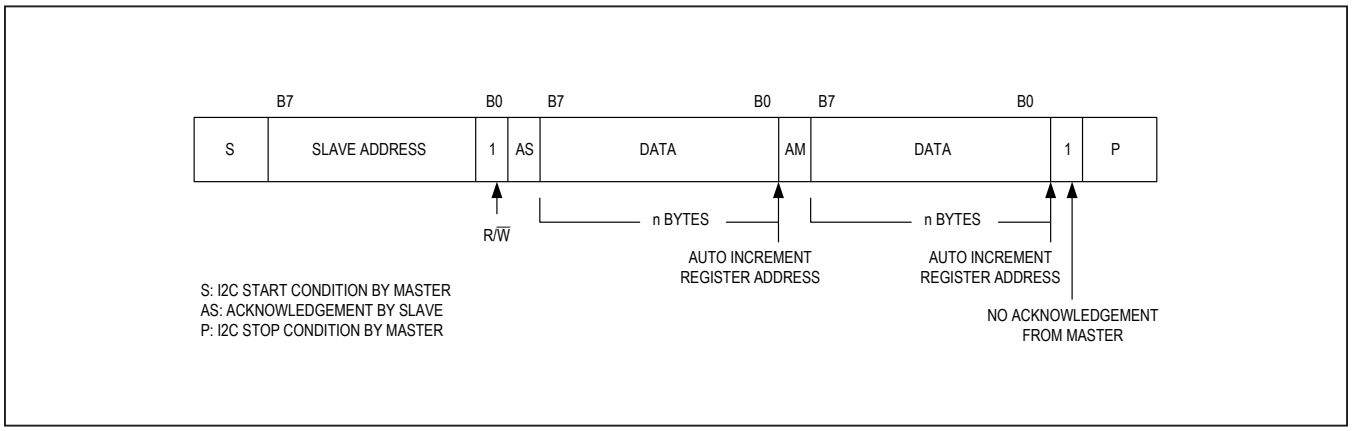
Master Reads After Setting Register Address (Write Register Address and Read Data)

When reading a specific register, use the following format:



Master Reads Register Data Without Setting Register Address (Read Mode)

When reading registers from the first address, use the following format:



I²C Register Map and Detailed Descriptions

INTB

The INTB is the hardware pin used to notify the host processor that one or more of the unmasked interrupt bits toggled. Masking the interrupt by setting INT_MASK_ bit to '1' prevents the INTB from asserting. The INTB pin deasserts (pulled high by off-chip pullup) as soon as the read sequence of the last INT_ register that contains an active interrupt starts. FG interrupts are cleared by setting new threshold values.

The application processor reads the interrupts in two steps. First, the AP reads the INTSRC register. This is a read-only register that indicates which functional block is generating the interrupt (i.e., charger and FG). Depending on the result of the read, the next step is to read the actual interrupt registers pertaining to the functional block.

For example, if the application processor reads 0x02 from register 0x22: INTSRC, it means the top-level MAX77818 block has an interrupt generated. The next step is to read register 0x24: SYSTEM Interrupt in order to understand the source of the interrupt.

Register Type and Reset Conditions

Type S: Registers are reset each time when SYS < SYS POR (~1.55V).

Type O: Registers are reset each time when SYS < SYS UVLO (2.55V max) or SYS > SYS OVLO or Die temp > 165° (or MAX77818 transitions from on to off state).

Top Level I²C Registers

The MAX77818 acts as a slave transmitter/receiver. The slave address of the MAX77818 top is 0xCCh/0xCDh (OTP option for 0xDC/0xDDh). The least significant bit is the read/write indicator.

The MAX77818's tope level has the following registers:

0x20: PMIC ID Register

NAME	FUNCTION	ADDR	TYPE	RESET
PMICID	PMIC ID	0x20	O	0x23

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R	ID	0011	ID of MAX77818
7:4	R	ID	0010	

0x21: PMIC Version/Rev Register

NAME	FUNCTION	ADDR	TYPE	RESET
PMICREV	PMIC revision	0x21	O	0x80

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R	REV	—	Pass 0b000 = pass 1 0b001 = pass 2 0b010 = pass 3
7:3	R	VERSION	—	Version 0b00000 = zmo 0b00001 = ymo … Null Trim Version 0b10000 = tmo 0b10001 = umo

0x22: Interrupt Source

NAME	FUNCTION	ADDR	TYPE	RESET
INTSRC	Interrupt source	0x22	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	CHGR_INT	0	0: No charger interrupt. 1: Charger interrupt is detected.
1	R	FG_INT	0	0 = No interrupt pending from FG block. 1 = interrupt from FG block is detected .
2	R	SYS_INT	0	0: No SYS INT 1: SYS interrupt is detected.
3	R	RSVD	0	Reserved
4	R	RSVD	0	Reserved
5	R	RSVD	0	Reserved
6	R	RSVD	0	Reserved
7	R	RSVD	0	Reserved

0x23: Interrupt Source Mask

NAME	FUNCTION	ADDR	TYPE	RESET
INTSRCMASK	Interrupt source mask	0x23	S	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/W	CHGR_INT_MASK	1	1: Charger interrupt is masked.
1	R/W	FG_INT_MASK	1	1: FG interrupt is masked.
2	R/W	SYS_INT_MASK	1	1: SYS interrupt is masked.
3	R/W	RSVD	1	Reserved
4	R/W	RSVD	1	Reserved
5	R/W	RSVD	1	Reserved
6	R/W	RSVD	1	Reserved
7	R/W	RSVD	1	Reserved

0x24: SYSTEM Interrupt

NAME	FUNCTION	ADDR	TYPE	RESET
SYSINTSRC	SYS interrupt source	0x24	S	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	SYSUVLO_INT	0	0: No SYSUVLO INT. 1: SYSUVLO interrupt is detected (falling).
1	R	SYSOVLO_INT	0	0: No SYSOVLO interrupt. 1: SYSOVLO interrupt is detected (rising and falling).
2	R	TSHDN_INT		0: No TSHDN interrupt. 1: TSHDN interrupt is detected.
3	R	RSVD	0	Reserved
4	R	RSVD	0	Reserved
5	R	RSVD	0	Reserved
6	R	RSVD	0	Reserved
7	R	TM_INT	0	0: Test mode interrupt is not set. 1: Test mode interrupt is set.

0x26: SYSTEM Interrupt Source Mask

NAME	FUNCTION	ADDR	TYPE	RESET
SYSINTMASK	System interrupt mask	0x26	S	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/W	SYSUVLO_INT_MASK	1	1: SYSUVLO interrupt is masked.
1	R/W	SYSOVLO_INT_MASK	1	1: SYSUVLO interrupt is masked.
2	R/W	TSHDN_INT_MASK	1	1: Thermal shutdown interrupt is masked.
3	R/W	RSVD	1	Reserved
4	R/W	RSVD	1	Reserved
5	R/W	RSVD	1	Reserved
6	R/W	RSVD	1	Reserved
7	R/W	TM_INT_MASK	0	1: INT test mode interrupt is masked.

0xC6: SAFEOUT LDO Control

NAME	FUNCTION	ADDR	TYPE	RESET
SAFEOUTCTRL	SAFEOUT linear regulator control	0xC6	O	0x75

BIT	MODE	NAME	RESET	DESCRIPTION
1:0	R/W	SAFEOUT1[1:0]	01	SAFEOUT1 output voltage 00: 4.85V 01: 4.90V (default) 10: 4.95V 11: 3.3V.
3:2	R/W	SAFEOUT2[3:2]	01	SAFEOUT2 output voltage 00: 4.85V 01: 4.90V (default) 10: 4.95V 11: 3.3V
4	R/W	ACTDISSAFEO1	1	0: No active discharge 1: Active discharge
5	R/W	ACTDISSAFEO2	1	0: No active discharge 1: Active discharge
6	R/W	ENSAFEOUT1	1	SAFEOUTLDO1 enable bit 0: Disable SAFEOUT1. 1: Enable SAFEOUT1.
7	R/W	ENSAFEOUT2	0	SAFEOUTLDO2 enable bit 0: Disable SAFEOUT2. 1: Enable SAFEOUT2.

Charger I²C Registers

The MAX77818's charger has convenient default register settings and a complete charger state machine that allow it to be used with minimal software interaction. Software interaction with the register map enhances the charger by allowing a high degree of configurability. An easy-to-navigate interrupt structure and in-depth status reporting allows software to quickly track the changes in the charger's status.

Register Protection

The CHG_CNFG_01, CHG_CNFG_02, CHG_CNFG_03, CHG_CNFG_04, CHG_CNFG_05, and CHG_CNFG07 registers contain settings for static parameters that are associated with a particular system and battery. These static settings are typically set once each time the system's microprocessor runs its boot-up initialization code; then they are not changed again until the microprocessor reboots. CHGPROT allows for blocking the "write" access to these static settings to protect them from being changed unintentionally. This protection is particularly useful for critical parameters such as the battery charge current CHG_CC and the battery charge voltage CHG_CV_PRM.

Determine the following registers bit settings by considering the characteristics of the battery. Maxim recommends that CHG_CC be set to the maximum acceptable charge rate for your battery – there is typically no need to actively adjust the CHG_CC setting based on the capabilities of the source at CHGIN, system load, or thermal limitations of the PCB; the Smart Power Selector intelligently manages all these parameters to optimize the power distribution.

Charger Restart Threshold ➔ CHG_RSTRT

Fast-Charge Timer (t_{FC}) ➔ FCHGTIME

Fast-Charge Current ➔ CHG_CC

Top-Off Time ➔ TO_TIME

Top-Off Current ➔ TO_ITH

Battery Regulation Voltage ➔ CHG_CV_PRM

Determine the following register bit settings by considering the characteristics of the system:

Low Battery Prequalification Enable ➔ PQEN

Minimum System Regulation Voltage ➔ MINVSYS

Junction Temperature Thermal Regulation Loop Setpoint ➔ REGTEMP

Interrupt, Mask, OK, and Detail Registers

The battery charger section of the MAX77818 provides detailed interrupt generation and status for the following subblocks:

- Charger Input
- Charger State Machine
- Battery
- Bypass Node

State changes on any subblock report interrupts through the CHG_INT register. Interrupt sources are masked from affecting the hardware interrupt pin when bits in the CHG_INT_MASK register are set. The CHG_INT_OK register provides a single-bit status indication of whether the interrupt generating subblock is okay or not. The full status of interrupt generating subblock is provided in the CHG_DETAILS_00, CHG_DETAILS_01, CHG_DETAILS_02, and CHG_DETAILS_03 registers.

Note that CHG_INT, CHG_INT_MASK, and CHG_INT_OK use the same bit position for each interrupt generating block to simplify software development.

Interrupt bits are automatically cleared upon reading a given interrupt register. When all pending CHG_INT interrupts are cleared, the top level interrupt bit deasserts.

CHG_INT Register Bit Description (0xB0)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_INT	Charger interrupt	0xB0	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/C	BYP_I	0	Bypass Node Interrupt 0 = The BYP_OK bit has not changed since the last time this bit was read. 1 = The BYP_OK bit has changed since the last time this bit was read.
1	R/C	RSVD	0	Reserved
2	R/C	BATP_I	0	Battery Presence Interrupt. 0 = The BATP_OK bit has not changed since the last time this bit was read. 1 = The BATP_OK bit has changed since the last time this bit was read.s
3	R/C	BAT_I	0	Battery Interrupt 0 = The BAT_OK bit has not changed since the last time this bit was read. 1 = The BAT_OK bit has changed since the last time this bit was read.
4	R/C	CHG_I	0	Charger Interrupt 0 = The CHG_OK bit has not changed since the last time this bit was read. 1 = The CHG_OK bit has changed since the last time this bit was read.
5	R/C	WCIN_I	0	WCIN Interrupt. 0 = The WCIN_OK bit has not changed since the last time this bit was read. 1 = The WCIN_OK bit has changed since the last time this bit was read.
6	R/C	CHGIN_I	0	CHGIN Interrupt. 0 = The CHGIN_OK bit has not changed since the last time this bit was read. 1 = The CHGIN_OK bit has changed since the last time this bit was read.
7	R/C	AICL_I	0	AICL interrupt 0=The AICL_OK bit has not changed since the last time this bit was read. 1=The AICL_OK bit has changed since the last time this bit was read.

CHG_INT_MASK Register Bit Description (0xB1)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_INT_MASK	Charger interrupt mask	0xB1	O	0xFF

BIT	MODE	NAME	RESET	DESCRIPTION
0	R/W	BYP_M	1	Bypass Interrupt Mask 0 = Unmasked 1 = Masked
1	R/W	RSVD	1	Reserved
2	R/W	BATP_M	1	Battery Presence Interrupt Mask 0 = Unmasked 1 = Masked
3	R/W	BAT_M	1	Battery Interrupt Mask 0 = Unmasked 1 = Masked
4	R/W	CHG_M	1	Charger Interrupt Mask 0 = Unmasked 1 = Masked
5	R/W	WCIN_M	1	WCIN Interrupt Mask 0 = Unmasked 1 = Masked
6	R/W	CHGIN_M	1	CHGIN Interrupt Mask 0 = Unmasked 1 = Masked
7	R/W	AICL_M	1	AICL Interrupt Mask 0 = Unmasked 1 = Masked

CHG_INT_OK Register Bit Description (0xB2)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_INT_OK	Charger status	0xB2	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	BYP_OK	0	Single-Bit Bypass Status Indicator. See BYP_DTLS for more information. 0 = Something powered by the bypass node has hit current limit. i.e., BYP_DTLS ≠ 0x00. 1 = The bypass node is okay. i.e., BYP_DTLS = 0x00.
1	R	RSVD	0	Reserved
2	R	BATP_OK	0	BAT present status indicator. 0 = Main Battery is not present 1 = Main Battery is present.
3	R	BAT_OK	0	Single-Bit Battery Status Indicator. See BAT_DTLS for more information. 0 = The battery has an issue or the charger has been suspended, i.e., BAT_DTLS ≠ 0x03 or 0x04 1 = The battery is okay. i.e., BAT_DTLS = 0x03 or 0x04
4	R	CHG_OK	0	Single-Bit Charger Status Indicator. See CHG_DTLS for more information. 0 = The charger has suspended charging or TREG = 1 i.e., CHG_DTLS ≠ 0x00 or 0x01 or 0x02 or 0x03 or 0x05 or 0x08 1 = The charger is okay or the charger is off i.e., CHG_DTLS = 0x00 or 0x01 or 0x02 or 0x03 or 0x05 or 0x08
5	R	WCIN_OK	0	Single-Bit WCIN Input Status Indicator. See WCIN_DTLS for more information. 0 = The WCIN input is invalid. i.e., WCIN_DTLS ≠ 0x03. 1 = The WCIN input is valid. i.e., WCIN_DTLS = 0x03.
6	R	CHGIN_OK	0	Single-Bit CHGIN Input Status Indicator. See CHGIN_DTLS for more information. 0 = The CHGIN input is invalid. i.e., CHGIN_DTLS ≠ 0x03. 1 = The CHGIN input is valid. i.e., CHGIN_DTLS = 0x03.
7	R	AICL_OK	0	AICL_OK 0 = AICL mode 1 = Not in AICL mode

CHG_DETAILS_00 Register Bit Description (0xB3)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_00	Charger details 00	0xB3	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
0	R	BATP_DTLS	0	Battery Detection 0 = Battery presence 1 = No battery presence
2:1	R	RSVD	00	Reserved
4:3	R	WCIN_DTLS	00	WCIN Details 0x00 = VWCIN is invalid. $V_{WCIN} < V_{WCIN\_UVLO}$ 0x01 = VWCIN is invalid. $V_{WCIN} < V_{MBAT} + V_{WCIN2SYS}$ and $V_{WCIN} > V_{WCIN\_UVLO}$ 0 x 02 = VWCIN is invalid. $V_{WCIN} > V_{WCIN\_OVLO}$ 0 x 03 = VWCIN is valid. $V_{WCIN} > V_{WCIN\_UVLO}$, $V_{WCIN} > V_{MBAT} + V_{WCIN2SYS}$, $V_{WCIN} < V_{WCIN\_OVLO}$
6:5	R	CHGIN_DTLS	00	CHGIN Details 0x00 = VBUS is invalid. $V_{CHGIN} < V_{CHGIN\_UVLO}$ 0x01 = VBUS is invalid. $V_{CHGIN} < V_{MBAT} + V_{CHGIN2SYS}$ and $V_{CHGIN} > V_{CHGIN\_UVLO}$ 0x02 = VBUS is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0x03 = VBUS is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$, $V_{CHGIN} > V_{MBAT} + V_{CHGIN2SYS}$, $V_{CHGIN} < V_{CHGIN\_OVLO}$
7	R	RSVD	0	Reserved

CHG_DETAILS_01 Register Bit Description (0xB4)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_01	Charger details 01	0xB4	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R	CHG_DTLS	0000	Charger Details 0x00 = Charger is in dead-battery prequalification or low-battery prequalification mode, CHG_OK = 1, $V_{MBATT} < V_{PQLB}$, $T_J < T_{JSHDN}$ 0x01 = Charger is in fast-charge constant current mode, CHG_OK = 1, $V_{MBATT} < V_{BATREG}$, $T_J < T_{JSHDN}$ 0x02 = Charger is in fast-charge constant voltage mode, CHG_OK = 1, $V_{MBATT} = VBATREG$, $T_J < T_{JSHDN}$ 0x03 = Charger is in top-off mode, CHG_OK = 1, $V_{MBATT} \geq V_{BATREG}$, $T_J < TJ_{SHDN}$ 0x04 = Charger is in done mode, CHG_OK=0, $V_{MBATT} > V_{BATREG} - V_{RSTRT}$, $T_J < T_{JSHDN}$ 0x06 = Charger is in timer fault mode, CHG_OK = 0, $V_{MBATT} < V_{BATOV}$, if BAT_DTLS = 0b001 then $V_{MBATT} < V_{BATPQ}$, $T_J < T_{JSHDN}$ 0x07 = Charger is in DETBAT = High suspend mode, CHG_OK = 0, $V_{MBATT} < V_{BATOV}$, if BAT_DTLS = 0b001 then $V_{MBATT} < V_{PQLB}$, $T_J < T_{JSHDN}$ 0x08 = Charger is off, charger input invalid and/or charger is disabled, CHG_OK = 1. 0x09 = Reserved 0x0A = Charger is off and the junction temperature is > T_{JSHDN}, CHG_OK = 0. 0x0B = Charger is off because the watchdog timer expired, CHG_OK = 0. 0x0C-0x0F = Reserved
6:4	R	BAT_DTLS	000	Battery Details 0x00 = No battery and the charger is suspended. 0x01 = $V_{MBATT} < V_{PQLB}$. This condition is also reported in the CHG_DTLS as 0x00 0x02 = The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery or something else. Charging has suspended and the charger is in its timer fault mode. This condition is also reported in the CHG_DTLS as 0x06. 0x03 = The battery is okay and its voltage is greater than the minimum system voltage ($V_{SYSMIN} < V_{MBATT}$), QBAT is on and V_{SYS} is approximately equal to V_{MBATT}. 0x04 = The battery is okay but its voltage is low: $V_{PQLB} < V_{MBATT} < V_{SYSMIN}$. Q_{BAT} is operating like an LDO to regulate V_{SYS} to V_{SYSMIN}. 0x05 = The battery voltage is greater than the battery overvoltage flag threshold (V_{BATOVF}) or it has been greater than this threshold within the last 37.5ms. V_{BATOVF} is set to a percentage above the V_{BATREG} target as programmed by CHG_CV_PRM. Note that this flag is only be generated when there is a valid input or when the DC-DC is operating as a boost. 0x06 = The battery is overcurrent or it has been overcurrent for at least 6ms since the last time this register has been read. 0x07 = Reserved In the event that multiple faults occur within the battery details category, overcurrent has priority followed by no battery, then overvoltage, then timer fault, then below prequel.

CHG_DETAILS_01 Register Bit Description (0xB4) (continued)

BIT	MODE	NAME	RESET	DESCRIPTION
7	R	TREG	0	Temperature Regulation Status 0 = The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 1 = The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation.

CHG_DETAILS_02 Register Bit Description (0xB5)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_DTLS_02	Charger details 02	0xB5	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R	BYP_DTLS	0000	Bypass Node Details. All bits in this family are independent from each other. They are grouped together only because they all relate to the health of the BYP node and any change in these bits generates a BYP_I interrupt. BYP_DTLS0 = OTGILIM = **0bxxx1** BYP_DTLS1 = BSTILIM = **0bxx1x** BYP_DTLS2 = BCKNegILIM = **0bx1xx** ********** 0x00=The bypass node is okay. 0bxxx1=The BYP to CHGIN switch (OTG switch) current limit was reached within the last 37.5ms. 0bxx1x=The BYP reverse boost converter has hit its current limit -- this condition persists for 37.5ms. 0bx1xx= The BYP buck converter has hit the max negative demand current limit.
7:4	R	RSVD	00	Reserved

CHG_CNFG_00 Register Bit Description (0xB7)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_00	Charger configuration 00	0xB7	O	0x05

BIT	MODE	NAME	RESET	DESCRIPTION
3:0	R/W	MODE	0101	Smart Power Selector Configuration 0x00 = 0b0000 = charger = off, OTG = off, buck = off, boost = off. The QBAT switch is on to allow the battery to support the system. BYP may or may not be biased based on the CHGIN availability. 0x01 = 0b0001 = same as 0b0000 0x02 = 0b0010= same as 0b0000 0x03 = 0b0011= same as 0b0000 0x04 = 0b0100 = charger = off, OTG = off, **buck = on**, boost = off. When there is a valid input, the buck converter regulates the system voltage to be V_{BATREG}. 0x05 = 0b0101 = **charger = on**, OTG = off, **buck = on**, boost = off. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS}$. 0x06 = 0b0110 = same as 0b101 0x07 = 0b0111 = same as 0b101 0x08 = 0b1000 = charger = off, OTG = off, buck = off, **boost = on.** The Q_{BAT} switch is on to allow the battery to support the system and the charger's DC-DC operates as a boost converter. The BYP voltage is regulated to VBYPSET. Q_{CHGIN} is off. 0x09 = 0b1001= same as 0b1000 0x0A = 0b1010 = charger = off, **OTG = on**, buck = off, **boost = on**. The Q_{BAT} switch is on to allow the battery to support the system, the charger's DC-DC operates as a boost converter. **Q_{CHGIN} is on** allowing it to source current up to $I_{CHGIN.OTG.MAX}$. The boost target voltage is 5.1V ($V_{BYP.OTG}$) . 0x0B = reserved 0x0C = 0b1100 = charger = off, OTG = off, **buck = on**, **boost = on**. When there is a valid input, the system is supported from that input: V_{SYS} = 4.2V. When input is invalid, the boost is on with a target voltage that is VBYPSET. 0x0D = 0b1101 = **charger = on**, OTG = off, **buck = on**, **boost = on**. When there is a valid input, the system is supported from that input: V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS}$. When input is invalid, the boost is on with a target voltage that is VBYPSET. 0x0E = 0b1110=charger=off, **OTG = on**, **buck = on**, **boost = on**. When there is a valid WCIN input, the system is supported from that input: V_{SYS} = 4.2V and **Q_{CHGIN} is on**, allowing it to source current up to $I_{CHGIN.OTG.MAX}$. When WCIN input is invalid the boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$). 0x0F = 0b1111 = **charger = on**, **OTG = on**, **buck = on**, **boost = on**. When there is a valid WCIN input, the system is supported from that input: V_{SYS} is the larger of V_{SYSMIN} and ~V_{MBATT} + I_{MBATT} x $R_{BAT2SYS}$. **Q_{CHGIN} is on** allowing it to source current up to $I_{CHGIN.OTG.MAX}$. When WCIN input is invalid, the boost is on with a target voltage of 5.1V ($V_{BYP.OTG}$).

CHG_CNFG_00 Register Bit Description (0xB7) (continued)

BIT	MODE	NAME	RESET	DESCRIPTION
4	R/W	WDTEN	0	Watchdog Timer Enable Bit. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01. 0 = Watchdog timer disabled 1 = Watchdog timer enabled
5	R/W	SPREAD	0	Spread Spectrum Feature Feature is operational both for 9V and 12V CHGIN input voltage. Feature is not guaranteed to be operational for 5V CHGIN/WCIN input voltage. When feature is not operational, it can be kept enabled without side effect. 0: Disabled 1: Enabled
6	R/W	DISIBS	0	MBATT to SYS FET Disable Control 0 = MBATT to SYS FET is controlled by the power path state machine. 1 = MBATT to SYS FET is forced off.
7	R/W	OTG_ CTRL	0	OTG FET Control 0 = Forces the CHGIN input switch to be on when in Mode = 0x0E or 0x0F. 1 = The CHGIN turns off anytime power switches between WCIN and BATT.

CHG_CNFG_01 Register Bit Description (0xB8)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_01	Charger details 01	0xB8	O R/W (protected with CHGPROT)	0x10

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R/W	FCHGTIME	001	Fast-Charge Timer Duration (t_{FC}) 0x00 = disable 0x01 = 4hrs 0x02 = 6hrs 0x03 = 8hrs 0x04 = 10hrs 0x05 = 12hrs 0x06 = 14hrs 0x07 = 16hrs
3	R/W	FSW	0	Switching Frequency Option 0: 4MHz 1: 2MHz
5:4	R/W	CHG_RSTRT	01	Charger Restart Threshold 0x00 = 100mV below the value programmed by CHG_CV_PRM 0x01 = 150mV below the value programmed by CHG_CV_PRM 0x02 = 200mV below the value programmed by CHG_CV_PRM 0x03 = Disabled
6	R/W	LSEL	0	Inductor Selection 0:0.47µH (for 4MHz without restriction) 2MHz/0.47µH option can be used only in the charge mode and is forbidden in following use cases: Boost mode Buck mode 1:1µH (for 2MHz and 4MHz option)
7	R/W	PQEN	0	Low Battery Prequalification Mode Enable 0 = Low battery prequalification mode is disabled. 1 = Low battery prequalification mode is enabled.

CHG_CNFG_02 Register Bit Description (0xB9)

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_02	Charger configuration 02	0xB9	O R/W (protected with CHGPROT)	0x09

BIT	MODE	NAME	RESET	DESCRIPTION
5:0	R/W	CHG_CC	001001 (450mA)	Fast-Charge Current Selection. When the charger is enabled, the charge current limit is set by these bits. These bits range from 0.10A (0x00) to 3.0A (0x3C) in 50mA step. **Note that the first 3 codes are all 100mA**
7:6	R/W	OTG_ILIM	00	CHGIN Output Current Limit in OTG Mode ($I_{CHGIN.OTG.LIM}$) When MODE = 0x09 or 0x0A the CHGIN current limit is set at the following current limit: 00 = 500mA 01 = 900mA 10 =1200mA 11 = 1500mA

Bits	(mA)	Bits	(mA)	Bits	(mA)	Bits	(mA)
0x00	100	0x10	800	0x20	1600	0x30	2400
0x01	100	0x11	850	0x21	1650	0x31	2450
0x02	100	0x12	900	0x22	1700	0x32	2500
0x03	150	0x13	950	0x23	1750	0x33	2550
0x04	200	0x14	1000	0x24	1800	0x34	2600
0x05	250	0x15	1050	0x25	1850	0x35	2650
0x06	300	0x16	1100	0x26	1900	0x36	2700
0x07	350	0x17	1150	0x27	1950	0x37	2750
0x08	400	0x18	1200	0x28	2000	0x38	2800
0x09	**450**	0x19	1250	0x29	2050	0x39	2850
0x0A	500	0x1A	1300	0x2A	2100	0x3A	2900
0x0B	550	0x1B	1350	0x2B	2150	0x3B	2950
0x0C	600	0x1C	1400	0x2C	2200	0x3C	3000
0x0D	650	0x1D	1450	0x2D	2250	0x3D	3000
0x0E	700	0x1E	1500	0x2E	2300	0x3E	3000
0x0F	750	0x1F	1550	0x2F	2350	0x3F	3000

Note that the thermal foldback loop can reduce the battery charger's target current by A_{TJREG}

CHG_CNFG_03 Register Bit Description (0xBA):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_03	Charger configuration 03	0xBA	O R/W (protected with CHGPROT)	0xDA

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R/W	TO_ITH	010 (150mA)	Top-Off Current Threshold. The charger transitions from its fast-charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report top-off mode. This transition also starts the top-off time as programmed by TO_TIME. 0x00 = 0.1A 0x01 = 0.125A 0x02 = 0.15A 0x03 = 0.175A 0x04 = 0.2A 0x05 = 0.25A 0x06 = 0.3A 0x07 = 0.35A
5:3	R/W	TO_TIME	011 (30min)	Top-Off Timer Setting 0x00 = 0min 0x01 = 10min 0x02 = 20min 0x03 = 30min 0x04 = 40min 0x05 = 50min 0x06 = 60min 0x07 = 70min
7:6	R/W	ILIM	11	Program Buck Peak Current Limit 00: support ICHG=3.00A 01: support ICHG=2.75A 10: support ICHG= 2.50A 11: support ICHG=2.25A

CHG_CNFG_04 Register Bit Description (0xBB):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_04	Charger configuration 04	0xBB	O R/W (protected with CHGPROT)	0x96

BIT	MODE	NAME	RESET	DESCRIPTION
5:0	R/W	CHG_CV_PRM	010110 (4.2V)	Primary Charge Termination Voltage Setting When the charger is enabled and the main-battery temperature is < T3 if JEITA = 1 or < T4 if JEITA = 0, then, the charger's battery regulation voltage (V_{BATREG}) is set by CHG_CV_PRM.
7:6	R/W	MINVSYS	10 (3.6V)	Minimum System Regulation Voltage (V_{SYSMIN}) 0x00 = 3.4V 0x01 = 3.5V 0x02 = 3.6V 0x03 = 3.7V

BITS	V	BITS	V	BITS	V
0x00	3.650	0x10	4.050	0x20	4.425
0x01	3.675	0x11	4.075	0x21	4.450
0x02	3.700	0x12	4.100	0x22	4.475
0x03	3.725	0x13	4.125	0x23	4.500
0x04	3.750	0x14	4.150	0x24	4.525
0x05	3.775	0x15	4.175	0x25	4.550
0x06	3.800	0x16	4.200	0x26	4.575
0x07	3.825	0x17	4.225	0x27	4.600
0x08	3.850	0x18	4.250	0x28	4.625
0x09	3.875	0x19	4.275	0x29	4.650
0x0A	3.900	0x1A	4.300	0x2A	4.675
0x0B	3.925	0x1B	4.325	0x2B	4.700
0x0C	3.950	0x1C	4.340		
0x0D	3.975	0x1D	4.350		
0x0E	4.000	0x1E	4.375		
0x0F	4.025	0x1F	4.400		

CHG_CNFG_06 Register Bit Description (0xBD):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_06	Charger configuration 06	0xBD	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
1:0	R/W	WDTCLR	00	Watchdog Timer Clear Bits Writing 01 to these bits clears the watchdog timer when the watchdog timer is enabled. 0x00 = the watchdog timer is not cleared 0x01 = the watchdog timer is cleared 0x02 = the watchdog timer is not cleared 0x03 = the watchdog timer is not cleared
3:2	R/W	CHGPROT	00	Charger Settings Protection Bits Writing 11 to these bits unlocks the write capability for the registers who are protected with CHGPROT writing any value besides 11 locks these registers. 0x00 = write capability is locked 0x01 = write capability is locked 0x02 = write capability is locked 0x03 = write capability is unlocked
7:4	R/W	RSVD	0000	Reserved

CHG_CNFG_07 Register Bit Description (0xBE):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_07	Charger configuration 07	0xBE	O R/W (protected with CHGPROT)	0x40

BIT	MODE	NAME	RESET	DESCRIPTION
4:0	R/W	RSVD	00000	Reserved
6:5	R/W	REGTEMP	10	Junction Temperature Thermal Regulation Loop Set point. The charger's target current limit starts to foldback and the TREG bit is set if the junction temperature is greater than the REGTEMP setpoint. 0x00 = 85°C 0x01 = 100°C 0x02 = 115°C 0x03 = 130°C
7	R/W	RSVD	0	Reserved

CHG_CNFG_09 Register Bit Description (0xC0):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_09	Charger configuration 09	0xC0	O	0x0F

BIT	MODE	NAME	RESET	DESCRIPTION
6:0	R/W	CHGIN_ILIM	0x0F (0.50A)	Maximum Input Current Limit Selection 7-bit adjustment from 100mA to 4.0A in 33mA steps. Note that the first 4 codes are all 100mA:
7	R/W	RSVD	0	Reserved

Bits	Unit (mA)	Bits	Unit (mA)	Bits	Unit (mA)	Bits	Unit (mA)
0x00	100	0x20	1067	0x40	2133	0x60	3200
0x01	100	0x21	1100	0x41	2167	0x61	3233
0x02	100	0x22	1133	0x42	2200	0x62	3267
0x03	100	0x23	1167	0x43	2233	0x63	3300
0x04	133	0x24	1200	0x44	2267	0x64	3333
0x05	167	0x25	1233	0x45	2300	0x65	3367
0x06	200	0x26	1267	0x46	2333	0x66	3400
0x07	233	0x27	1300	0x47	2367	0x67	3433
0x08	267	0x28	1333	0x48	2400	0x68	3467
0x09	300	0x29	1367	0x49	2433	0x69	3500
0x0A	333	0x2A	1400	0x4A	2467	0x6A	3533
0x0B	367	0x2B	1433	0x4B	2500	0x6B	3567
0x0C	400	0x2C	1467	0x4C	2533	0x6C	3600
0x0D	433	0x2D	1500	0x4D	2567	0x6D	3633
0x0E	467	0x2E	1533	0x4E	2600	0x6E	3667
0x0F	**500**	0x2F	1567	0x4F	2633	0x6F	3700
0x10	533	0x30	1600	0x50	2667	0x70	3733
0x11	567	0x31	1633	0x51	2700	0x71	3767
0x12	600	0x32	1667	0x52	2733	0x72	3800
0x13	633	0x33	1700	0x53	2767	0x73	3833
0x14	667	0x34	1733	0x54	2800	0x74	3867
0x15	700	0x35	1767	0x55	2833	0x75	3900
0x16	733	0x36	1800	0x56	2867	0x76	3933
0x17	767	0x37	1833	0x57	2900	0x77	3967
0x18	800	0x38	1867	0x58	2933	0x78	4000
0x19	833	0x39	1900	0x59	2967	0x79	4000
0x1A	867	0x3A	1933	0x5A	3000	0x7A	4000
0x1B	900	0x3B	1967	0x5B	3033	0x7B	4000
0x1C	933	0x3C	2000	0x5C	3067	0x7C	4000
0x1D	967	0x3D	2033	0x5D	3100	0x7D	4000
0x1E	1000	0x3E	2067	0x5E	3133	0x7E	4000
0x1F	1033	0x3F	2100	0x5F	3167	0x7F	4000

CHG_CNFG_10 Register Bit Description (0xC1):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_10	Charger configuration 09	0xC1	O	0x19

BIT	MODE	NAME	RESET	DESCRIPTION
5:0	R/W	WCIN_ILIM	0x19 (0.50A)	Maximum Input Current Limit Selection 6bit adjustment from 60mA to 1.260A in 20mA steps. Note that the first 4 codes are all 60mA:

Bits	(mA)	Bits	(mA)
0x00	60	0x20	640
0x01	60	0x21	660
0x02	60	0x22	680
0x03	60	0x23	700
0x04	80	0x24	720
0x05	100	0x25	740
0x06	120	0x26	760
0x07	140	0x27	780
0x08	160	0x28	800
0x09	180	0x29	820
0x0A	200	0x2A	840
0x0B	220	0x2B	860
0x0C	240	0x2C	880
0x0D	260	0x2D	900
0x0E	280	0x2E	920
0x0F	300	0x2F	940
0x10	320	0x30	960
0x11	340	0x31	980
0x12	360	0x32	1000
0x13	380	0x33	1020
0x14	400	0x34	1040
0x15	420	0x35	1060
0x16	440	0x36	1080
0x17	460	0x37	1100
0x18	480	0x38	1120
0x19	500	0x39	1140
0x1A	520	0x3A	1160
0x1B	540	0x3B	1180
0x1C	560	0x3C	1200
0x1D	580	0x3D	1220
0x1E	600	0x3E	1240
0x1F	620	0x3F	1260

7:6	R/W	RSVD	00	Reserved

CHG_CNFG_11 Register Bit Description (0xC2):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_11	Charger configuration 11	0xC2	O	0x00

BIT	MODE	NAME	RESET	DESCRIPTION
6:0	R/W	VBYPSET	0x00 (3V)	Bypass Target Output Voltage in Boost Mode 3V (0x00) to 5.8V (0x70) in 0.025V steps. This setting is valid for the “boost only” mode (MODE = 0x08).
7	R/W	RSVD	0	Reserved

Bits	Unit (mA)	Bits	Unit (mA)	Bits	Unit (mA)	Bits	Unit (mA)
0x00	3.000	0x20	3.800	0x40	4.600	0x60	5.400
0x01	3.025	0x21	3.825	0x41	4.625	0x61	5.425
0x02	3.050	0x22	3.850	0x42	4.650	0x62	5.450
0x03	3.075	0x23	3.875	0x43	4.675	0x63	5.475
0x04	3.100	0x24	3.900	0x44	4.700	0x64	5.500
0x05	3.125	0x25	3.925	0x45	4.725	0x65	5.525
0x06	3.150	0x26	3.950	0x46	4.750	0x66	5.550
0x07	3.175	0x27	3.975	0x47	4.775	0x67	5.575
0x08	3.200	0x28	4.000	0x48	4.800	0x68	5.600
0x09	3.225	0x29	4.025	0x49	4.825	0x69	5.625
0x0A	3.250	0x2A	4.050	0x4A	4.850	0x6A	5.650
0x0B	3.275	0x2B	4.075	0x4B	4.875	0x6B	5.675
0x0C	3.300	0x2C	4.100	0x4C	4.900	0x6C	5.700
0x0D	3.325	0x2D	4.125	0x4D	4.925	0x6D	5.725
0x0E	3.350	0x2E	4.150	0x4E	4.950	0x6E	5.750
0x0F	3.375	0x2F	4.175	0x4F	4.975		
0x10	3.400	0x30	4.200	0x50	5.000		
0x11	3.425	0x31	4.225	0x51	5.025		
0x12	3.450	0x32	4.250	0x52	5.050		
0x13	3.475	0x33	4.275	0x53	5.075		
0x14	3.500	0x34	4.300	0x54	5.100		
0x15	3.525	0x35	4.325	0x55	5.125		
0x16	3.550	0x36	4.350	0x56	5.150		
0x17	3.575	0x37	4.375	0x57	5.175		
0x18	3.600	0x38	4.400	0x58	5.200		
0x19	3.625	0x39	4.425	0x59	5.225		
0x1A	3.650	0x3A	4.450	0x5A	5.250		
0x1B	3.675	0x3B	4.475	0x5B	5.275		
0x1C	3.700	0x3C	4.500	0x5C	5.300		
0x1D	3.725	0x3D	4.525	0x5D	5.325		
0x1E	3.750	0x3E	4.550	0x5E	5.350		
0x1F	3.775	0x3F	4.575	0x5F	5.375		

CHG_CNFG_12 Register Bit Description (0xC3):

NAME	FUNCTION	ADDR	TYPE	RESET
CHG_CNFG_12	Charger configuration 12	0xC3	O	0x67

BIT	MODE	NAME	RESET	DESCRIPTION
2:0	R/W	B2SOVRC	111	BAT to SYS Overcurrent Threshold 0x00 = Disabled 0x01 = 3.00A 0x02 = 3.25A 0x03 = 3.50A 0x04 = 3.75A 0x05 = 4.00A 0x06 = 4.25A 0x07 = 4.50A
4:3	R/W	VCHGIN_REG	00	CHGIN Voltage Regulation Threshold (V_{CHGIN_REG}) Adjustment The CHGIN to GND Minimum Turn-On Threshold (V_{CHGIN_UVLO}) also scales with this adjustment. 0x00 = V_{CHGIN_REG} = 4.3V and V_{CHGIN_UVLO} = 4.5V 0x01 = V_{CHGIN_REG} = 4.7V and V_{CHGIN_UVLO} = 4.9V 0x02 = V_{CHGIN_REG} = 4.8V and V_{CHGIN_UVLO} = 5.0V 0x03 = V_{CHGIN_REG} = 4.9V and V_{CHGIN_UVLO} = 5.1V
5	R/W	CHGINSEL	1	CHGIN/USB Input Channel Select 0 = Disabled 1 = Enabled
6	R/W	WCINSEL	1	WCIN Input Channel Select 0 = Disabled 1 = Enabled
7	R/W	Reserved	0	Reserved

Model Gauge m5 Register Map

TAlrtTh2 (0xB2)

BITFIELD	BITS	DESCRIPTION	DECODE
TempWarm	15:8	Temperature threshold used for smart charging as T4	Units of LSB are 1°C. Set to 0x7F to disable.
TempCool	7:0	Temperature threshold used for smart charging as T1	Units of LSB are 1°C. Set to 0x80 to disable.

SmartChgCfg (0xDB)

BITFIELD	BITS	DESCRIPTION	DECODE
DisJEITA	5	Set 1 to disable JEITA battery temperature monitor adjusts	
UseVF	4		0x0: MixSOC is an input SOC for SmartCharging 0x1: VFSOC is an input SOC for SmartCharging
EnsC	1	Set 1 to enable SmartCharing	
EnSF	0	Set 1 to enable SmartFull	

Status and Configuration Registers

Register Details

Status (0x00)

Interrupt status register for the FG block.

BITFIELD	BITS	DESCRIPTION	DECODE
Br	15	Battery Removal	This bit is set to 1 when the device detects that a battery has been removed from the system. This bit must be cleared by system software to detect the next removal event. Br is set to 0 at power-up.
Smx	14	Maximum SOCALRT Threshold Exceeded	This bit is set to 1 whenever SOC rises above the maximum SOCALRT value. This bit may or may not need to be cleared by system software to detect the next event. See SS in the CONFIG register and SACFG in the MiscCFG register. Smx is set to 0 at power-up.
Tmx	13	Maximum TALRT Threshold Exceeded	This bit is set to 1 whenever a Temperature register reading is above the maximum TALRT value. This bit may or may not need to be cleared by system software to detect the next event. See TS in the CONFIG register. Tmx is set to 0 at power-up.
Vmx	12	Maximum VALRT Threshold Exceeded	This bit is set to 1 whenever a VCELL register reading is above the maximum VALRT value. This bit may or may not need to be cleared by system software to detect the next event. See VS in the CONFIG register. Vmx is set to 0 at power-up.
Bi	11	Battery Insertion	This bit is set to 1 when the device detects that a battery has been inserted into the system by monitoring the AIN pin. This bit must be cleared by system software to detect the next insertion event. Bi is set to 0 at power-up.

BITFIELD	BITS	DESCRIPTION	DECODE
Smn	10	Minimum SOCALRT Threshold Exceeded	This bit is set to 1 whenever SOC falls below the minimum SOCALRT value. This bit may or may not need to be cleared by system software to detect the next event. See SS in the CONFIG register and SACFG in the MiscCFG register. Smn is set to 0 at power-up.
Tmn	9	Minimum TALRT Threshold Exceeded	This bit is set to 1 whenever a Temperature register reading is below the minimum TALRT value. This bit may or may not need to be cleared by system software to detect the next event. See TS in the CONFIG register. Tmn is set to 0 at power-up.
Vmn	8	Minimum VALRT Threshold Exceeded	This bit is set to 1 whenever a VCELL register reading is below the minimum VALRT value. This bit may or may not need to be cleared by system software to detect the next event. See VS in the CONFIG register. Vmn is set to 0 at power-up.
dSOCi	7	1% SOC Change Alert	This bit is set to 1 to indicate a 1% SOC change alert. dSOCi is set to 0 at power-up.
ThmHot	6	FG Control Charger Input Current Limit	Set to 1 to indicate a Thermistor Hot to allow FG control charger input current limit. ThmHot is set to 0 at power-up.
SPR_5	5		
Isysmx	4	SYS current is over OCP limit.	Maximum SYS current threshold exceeded.
Bst	3	Battery Status	This bit is set to 0 when a battery is present in the system and set to 1 when the battery is removed. Bst is set to 0 at power-up.
SPR_2	2		
POR	1	Power-On Reset	This bit is set to 1 when the device detects that a software or hardware POR event has occurred. If the host detects that the POR bit has been set, the device should be reconfigured. See the *Power-Up and Power-On Reset* section. This bit must be cleared by system software to detect the next POR event. POR is set to 1 at power-up.
Imn	0	Minimum Isys Threshold Exceeded	

VAlrtTh (0x01)

BITFIELD	BITS	DESCRIPTION	DECODE
MaxVoltageAlrt	15:8	Sets an alert threshold for maximum voltage.	Set Max = 0xFF to disable. Units of LSB are 20mV.
MinVoltageAlrt	7:0	Sets an alert threshold for minimum voltage.	Set Min = 0x00 to disable. Units of LSB are 20mV.

TAlrtTh (0x02)

BITFIELD	BITS	DESCRIPTION	DECODE
MaxTempAlrt	15:8	Sets an alert threshold for maximum temperature.	Set Max = 0x7F to disable. Units of LSB are 1˚C.
MinTempAlrt	7:0	Sets an alert threshold for minimum temperature.	Set Min = 0x80 to disable. Units of LSB are 1˚C.

SAlrtTh (0x03)

BITFIELD	BITS	DESCRIPTION	DECODE
MaxSocAlrt	15:8	Sets an alert for maximum SOC.	This may be used for charge/discharge termination, or for power-management near empty. Set Max = 0xFF to disable. Units of LSB are 1%.
MinSocAlrt	7:0	Sets an alert for minimum SOC.	This may be used for charge/discharge termination, or for power-management near empty. Set Min = 0x00 to disable. Units of LSB are 1%.

AtRate (0x04)

BITFIELD	BITS	DESCRIPTION
AtRate	15:0	Host software should write the AtRate register with a negative two's-complement 16-bit value of a theoretical load current prior to reading any of the at-rate output registers (AtTTE, AtAvSOC, AtAvCap).

QRTable00 (0x12)

BITFIELD	BITS	DESCRIPTION
QRTable00	15:0	QRTable__ is interpreted the same as BT07, using interpolation. However, during empty learning 2 QRTable registers should be modified with interpolation applied.

FullSocThr (0x13)

BITFIELD	BITS	DESCRIPTION	DECODE
FullSOCThr	15:0	FullSOCThr comes from OTP if the OTP register is enabled. Otherwise, it POR's to a default of 95%.	LSB unit is 1/256%.

DesignCap (0x18)

BITFIELD	BITS	DESCRIPTION	DECODE
DesignCap	15:0	DesignCap16 is used to relate to FullCap16 to help measure the age of the battery.	Units are 0.5mAh with 10mΩ sense resistor.

Config (0x1D)

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_15	15	Fuel-Gauge Charger Fail Enable	Set to 1 to enable FGCHGFAIL interrupt to drive the INTB pin. This bit is not accessible by the fuel-gauge firmware.
Ss	14	SOC ALRT Sticky	When SS = 1, SOC alerts can only be cleared through software. When SS = 0, SOC alerts are cleared automatically when the threshold is no longer exceeded. SS is set to 0 at power-up.
Ts	13	Temperature ALRT Sticky	When TS = 1, temperature alerts can only be cleared through software. When TS = 0, temperature alerts are cleared automatically when the threshold is no longer exceeded. TS is set to 1 at power-up.
Vs	12	Voltage ALRT Sticky	When VS = 1, voltage alerts can only be cleared through software. When VS = 0, voltage alerts are cleared automatically when the threshold is no longer exceeded. VS is set to 0 at power-up.
SPR_11	11	Fuel-Gauge Charger Control	Set to 1 to enable MaxCharge (fuel-gauge controlled charging).
AINSH	10	AIN Pin Shutdown	Set to 1 to enable device shutdown when the battery is removed. The IC enters shutdown if the AIN pin remains high (AIN reading > VTHRM - VDETR) for longer than the timeout of the SHDNTIMER register. This also configures the device to wake up when AIN is pulled low on cell insertion. AINSH is set to 0 at power-up. Note that if I2CSH and AINSH are both set to 0, the device wakes up an edge of any of the SDA, SCL, or INTB pins.
Ten	9	Enable Temperature Channel	Set to 1 and set ETHRM or FTHRM to 1 to enable measurements on the AIN pin. Ten is set to 1 at power-up.
Tex	8	Temperature External	When set to 1, the fuel gauge requires external temperature measurements to be written from the host. When set to 0, measurements on the AIN pin are converted to a temperature value and stored in the Temperature register instead. Tex is set to 1 at power-up.
SHDN	7	Shutdown	Write this bit to logic 1 to force a shutdown of the device after timeout of the SHDNTIMER register. SHDN is reset to 0 at power-up and upon exiting shutdown mode

BITFIELD	BITS	DESCRIPTION	DECODE
I2CSH	6	I²C Shutdown	Set to logic 1 to force the device to enter shutdown mode if both SDA and SCL are held low for more than timeout of the SHDNTIMER register. This also configures the device to wake up on a rising edge of either SDA or SCL. Set to 1 at power-up. Note that if I2CSH and AINSH are both set to 0, the device wakes up an edge of any of the SDA, SCL, or INTB pins.
SPR_5	5	I²C Charge Fail Enable	Set to 1 to enable I2CChgFail interrupt to drive the INTB pin. This bit is not accessible by the fuel-gauge firmware.
ETHRM	4	Enable Thermistor	Set to logic 1 to enable the automatic THRM output bias and AIN measurement every 1.4s. This bit is set to 1 at power-up.
FTHRM	3	Force Thermistor Bias Switch. This allows the host to control the bias of the thermistor switch or enable fast detection of battery removal (see the *Fast Detection of Cell Removal* section).	Set FTHRM = 1 to always enable the thermistor bias switch. With a standard 10kΩ thermistor, this adds an additional ~200µA to the current drain of the circuit. This bit is set to 0 at power-up.
Aen	2	Enable alert on fuel-gauge outputs.	When Aen = 1, violation of any of the alert threshold register values by temperature, voltage, or SOC triggers an alert. This bit affects the INTB pin (FG_INT) operation only. The Smx, Smn, Tmx, Tmn, Vmx, and Vmn bits are not disabled. This bit is set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.
Bei	1	Enable alert on battery insertion.	When Bei = 1, a battery-insertion condition, as detected by the AIN pin voltage, triggers an alert. Set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.
Ber	0	Enable alert on battery removal.	When Ber = 1, a battery-removal condition, as detected by the AIN pin voltage, triggers an alert. Set to 0 at power-up. Note that if this bit is set to 1, the ALSH bit should be set to 0 to prevent an alert condition from causing the device to enter shutdown mode.

IChgTerm (0x1E)

BITFIELD	BITS	DESCRIPTION	DECODE
ICHGTerm	15:0	No change from BT07. ICHGTerm restores from OTP if enabled, however it restores according to nDesignCap/10 if OTP is disabled for ICHGTerm.	LSB unit is the same as the register current's LSB unit.

DevName (0x21)

BITFIELD	BITS	DESCRIPTION
DevName	15:0	Firmware version information

QRTable10 (0x22)

BITFIELD	BITS	DESCRIPTION
QRTable10	15:0	QRTable__ is interpreted the same as BT07, using interpolation. However, during empty learning 2 QRTable registers should be modified with interpolation applied.

FullCapNom (0x23)

BITFIELD	BITS	DESCRIPTION	DECODE
FullCapNom	15:0	FullCapNom is the internally measured value of the nominal full capacity estimated for room temperature. It is measured by one of the 3 defined full capacity learning methods (relax-to-relax, relax-to-relax zigzag, or continual).	0.5mAh per LSB with 10mΩ sense resistor.

TempNom (0x24)

BITFIELD	BITS	DESCRIPTION	DECODE
TempNom	15:6	When Temperature measurements are hotter than TempNom, the VFG is compensated using TempCoHot. When Temperature measurements are colder than TempNom, the VFG is compensated using TempCoCold.	10 bit value in bits D15 through D6. The MSbit in D15 represents sign which is useful for values in degrees C but should always be set to 0 for ratiometric values. The LSB is 0.0039˚C and the upper Byte has units 1°C. This is a signed register.
SPR	5:0		

TempLim (0x25)

BITFIELD	BITS	DESCRIPTION	DECODE
TempHot	15:8	RCOMP0 is learned when TempCold<AvgTA<TempHot. TempCoHot is learned when (TempNom+TempHot)/2<AvgTA<TempHot.	Units are 1°C.
TempCold	7:0	RCOMP0 is learned when TempCold<AvgTA<TempHot.TempCoCold is learned when TempCold<AvgTA,(TempNom+TempCold)/2. Units are 1°C.	Units are 1°C.

LearnCfg (0x28)

The LearnCFG register controls all functions relating to adaptation during operation. The LearnCFG register default values should not be changed unless specifically required by the application.

BITFIELD	BITS	DESCRIPTION	DECODE
Learn-RCOMP	15:13	LearnRCOMP defines the rate to learn RCOMP0.	
LearnTCO	12:10	LearnTCO defines the rate to learn the temperature compensation. Set LearnRCOMP = LearnTCO = 0 to disable learning.	Set to 1 for increment/decrement learning. Otherwise, any non-zero value applies the error signal (VFOCVprerelax – VFOCVpostrelax) to the learn parameter (RCOMP0, TempCoUp, or TempCoDn) by left-shifting the learn level (LearnRCOMP or LearnTCO).
FCLm	9:8	FCLrnMethod defines one of 3 methods for learning FullCAP:0) relax-to-relax (DS2786 style). d%_acc16 and dQacc16 are only calculated at relaxation points, and FullCAP is only calculated at these relax points. However, unlike the DS2786, if the delta-percentage is too small to successfully learn capacity, the measurement is accumulated towards the next relax. Set FCLrnMethod = 1 to enable relax-to-relax learning. This method carries the least error, although it is the least opportunistic. 1) Not applicable. 2) Zigzag. d%_acc16 and dQacc16 are calculated frequently. FullCAP learning only occurs during relax. This improves accuracy of d%_acc16 and reduces error contributed by voltage fuel-gauge. Set FCLrnMethod = 2 to enable ZigZag learning. 3) Continual learning. d%_acc16 and dQacc16 are calculated frequently. FullCAP occurs during any d%_acc16 overflow. Relax criteria not needed. Set FCLrnMethod = 3 to enable continual learning.	FCLrn0 is FCalways. Set FCalways = 1 to enable fullcap learning even when relax is not detected. FCLrn1 is accalways. Set accalways = 1 to enable dQ and dacc accumulation even when relax is not detected. Set accalways = 0 to enable dQ/dAcc accumulation only when relax is detected.
FCx	7	FCx sets the source value to effect FullCAP when charge termination is detected.	Set FCx = 0 (follow RepCap)

BITFIELD	BITS	DESCRIPTION	DECODE
FCLrnStage	6:4	FCLrnStage determines how to best merge-in the usage of the coulomb-counter during the initial cycling of a new battery, since the capacity is not initially known. The host can write the FullCAP and FullCAPNom values and advance the FCLrnStage to 0x7 to shortcut the startup behavior. Writing to 0x7, will enable the full mixing using the normal MixRatio. If RdFCLrn is asserted in the MiscCFG register, then FCLrnStage 7 will also clear the FCLrn bits. At startup, FCLrnStage is reset to 0x0 and the Voltage Fuel-gauge mixing time constant is 5.625 seconds. For each 16% accumulation in Cycles, the time constant is doubled. The maximum allowed mixing time constant is set by NMIX in the SHFTCFG register. For each 32% accumulation in Cycles, the FCLrnStage is incremented. The actual shift applied when mixing VFREMCAP to MixRemCap is the smaller of ((Cycles>>4)+5 or (NMIX+5). For example, with NMIX = 13 (0xD) the maximum time constant is 12.8 hours and the progression looks like the following: %Capacity Learned FCLrnStage >> Mixing Time Constant 0% - 15% 0 5 5.625 seconds - Voltage FG dominant 16% - 31% 0 6 11.25 seconds - " 32% - 47% 1 7 22.5 seconds - " 48% - 63% 1 8 45 seconds - " 64% - 79% 2 9 1.5 minutes - " 80% - 95% 2 10 3 minutes - " 96% - 111% (About 1 cycle) 3 11 6 minutes - " 112% - 127% 3 12 12 minutes - " 128% - 143% 4 13 24 minutes - Coulomb-counter dominant 144% - 159% 4 14 48 minutes - " 160% - 175% 5 15 1.6 hours - " 176% - 191% 5 16 3.2 hours - " 192% - 207% (About 2 cycles) 6 17 6.4 hours - " 208% - 223% (And all future cycles) 6 18 12.8 hours - "	

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_3_3	3		
FillEmpty	2	FiltEmpty chooses whether empty is determined by a filtered or unfiltered voltage.	Set FiltEmpty = 1 to detect empty using AvgV-CELL. Set FiltEmpty = 0 to detect empty using VCELL, which can be only lightly filtered.
MixEn	1	MixEn enables mixing. Setting this to zero forces >>0.	
SPR	0		

FilterCfg (0x29)

BITFIELD	BITS	DESCRIPTION	DECODE
NEMPTY	15:14	Sets the filtering for empty learning for both the I_Avgempty and QRTable registers.	Iavg_empty is learned with(NEMPTY+3) right shifts. QRTable is learned with (NEMPTY + sizeof(Iavgempty) – sizeof(AvgCurrent)) right shifts.
NTEMP	13:11	Sets the time constant for the AverageTempera-ture register. The default POR value of 1h gives a time constant of 12min.	The equation setting the period is: AvergeTempera-ture time constant = 175.8ms x 2^(11 + TEMP)
NMIX	10:7	Sets the time constant for the mixing algorithm. The default POR value of Dh gives a time constant of 12.8 hours.	The equation setting the period is: Mixing Period = 175.8ms × 2(5+NMIX)
NAVGCELL	6:4	Sets the time constant for the AverageVCELL register. The default POR value of 2h gives a time constant of 45.0s.	The equation setting the period is: AverageVCELL time constant = 175.8ms × 2(6+NAVGVCELL)
NCURR	3:0	Sets the time constant for the AverageCurrent register. The default POR value of 4h gives a time constant of 11.25 seconds.	The equation setting the period is: AverageCurrent time constant = 175.8ms × 2^(2+NCURR)

RelaxCfg (0x2A)

The RelaxCFG register defines how the device detects if the cell is in a relaxed state. For a cell to be considered relaxed, current flow through the cell must be kept at a minimum while the change in the cell's voltage over time, dV/dt, shows little or no change. If AverageCurrent remains below the load threshold while VCELL changes less than the dV threshold over two consecutive periods of dt, the cell is considered relaxed.

BITFIELD	BITS	DESCRIPTION	DECODE
LoadThr	15:9	When current magnitude is less than LoadThr, the device is considered to be unloaded. This is used to determine when to latch-load direction and VFSOC_EOL and when to start searching for relaxation. 8 bits. Stopload is detected when (RelaxCFG>>4)&0x0FE0) < |AvgCurrent8|. LoadThr does not include a sign bit.	The LSb is 5mA for 10mΩ sense resistor.
dVThr	8:4	dVThr sets the relaxation criteria between VCELL and OCV. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed;	dVThr5 is 1.25mV per LSB. (1.25mV to 40mV range)
dTThr	3:0	dTThr configures the relaxation timer. Sets the time period over which change in VCELL is compared against dV. If the cell's voltage changes by less than dV over two consecutive periods set by dt, the cell is considered relaxed. The default value is 6 minutes.	The AvgVCELL is sampled at every dTThr interval (2dTThr x 0.1758s), and delta-V is checked by comparing to the previous sample.

MiscCfg (0x2B)

The MiscCFG control register enables various other functions of the device. The MiscCFG register default values should not be changed unless specifically required by the application.

0—Bit must be written 0. Do not write 1.

1—Bit must be written 1. Do not write 0.

X—Don't Care. Bit may read 0 or 1.

BITFIELD	BITS	DESCRIPTION	DECODE
OopsFilter	15:12	OopsFilter default 3 (OopsFilter + 1) defines 0.39%/45s, 4%/6minutes, or 32%/hr rate limitation.	OopsFilter is 8%/hr per LSB.
EnBi1	11	Enable reset on battery-insertion detection. Set this bit to 1 to force a reset of the fuel gauge whenever a battery insertion is detected based on AIN pin monitoring. This bit is written to 1 at power-up.	
InitVFG	10	Setting this bit will cause the fuelgauge to re-initialize	
MixRate	9:5	Mixing Rate. This value sets the strength of the servo mixing rate after the final mixing state has been reached (> 2.08 complete cycles). The units are MR0 = 6.25µV, giving a range up to 19.375mA with a standard 10mΩ sense resistor. Setting this value to 00000b disables servo mixing and the IC continues with time-constant mixing indefinitely. The default setting is 18.75µV or 1.875mA with a standard sense resistor.	
RdFCLrn	4	Setting this bit will cause the FCLrn bits to be automattically cleared to 0 when the fule-gauge reaches FCLrnStage 7. This allows allows a more aggressive FullCapNom learning method to be used initially to quickly get an estimate of the battery capacity. Then the learning method will automatically revert to the most conservative method.	
vttl	3	This bit allows a lower voltage thermistor pullup.	
Vex	2	Set Vex=1 to disable voltage measurements. In this operation VCELL should be periodically written by the host.	
SACFG	1:0	SOC Alert CONFIG.	Set SACFG=0 to manage empty alerts using RepSOC. Set SACFG=1 to manage empty alerts using AvSOC. Set SACFG=10 to manage alerts using MixSOC. Set SACFG=11 to manage alerts using VFSOC.

TGain (0x2C)

The TGAIN and TOFF registers adjust the gain and offset of the temperature measurement A/D on the AIN pin to convert the result to a temperature value by the following equation: Temperature Register = (AIN Register ×TGAIN Register/16384) + (TOFF Register × 2).

Both these registers are signed two's complement. These registers allow for accurate temperature conversions when using a variety of external NTC thermistors.

BITFIELD	BITS	DESCRIPTION
TGAIN	15:0	TGAIN is a signed value with units of °C/64

TOff (0x2D)

The TGAIN and TOFF registers adjust the gain and offset of the temperature measurement A/D on the AIN pin to convert the result to a temperature value by the following equation: Temperature Register = (AIN Register ×TGAIN Register/16384) + (TOFF Register × 2).

Both these registers are signed two's complement. These registers allow for accurate temperature conversions when using a variety of external NTC thermistors.

BITFIELD	BITS	DESCRIPTION
TOFF	15:0	TOFF is a signed value with units of 2^{-7} in the LSb. Note that these units are 2X the TEMP register

CGain (0x2E)

The CGAIN and COFF registers adjust the gain and offset of the current measurement result. The current measurement A/D is factory trimmed to data-sheet accuracy without the need for the user to make further adjustments. The default power-up settings for CGAIN and COFF apply no adjustments to the Current register reading. For specific application requirements, the CGAIN and COFF registers can be used to adjust readings as follows:

Current Register = Current A/D Reading × (CGAIN Register/16384) + (2 × COFF Register)

For easiest software compatibility between systems, configure CGAIN to keep current LSb resolution at 0.15625mA. A minimum sense resistance of 5mΩ is required due to the maximum range of CGAIN. This preserves resolution of current readings and capacities. Both these registers are signed two's complement. The default values of 4000h for CGAIN and 0000h for COFF preserve factory calibration and unit values (1.5625µA/RSENSE).

BITFIELD	BITS	DESCRIPTION
CGAIN	15:0	CGAIN is a signed value with units of 2^{-14}. LSB is 0.0061%.

COff (0x2F)

BITFIELD	BITS	DESCRIPTION	DECODE
COFF	15:0	Current Offset	LSB is 3.15µA

QRTable20 (0x32)

BITFIELD	BITS	DESCRIPTION
QRTable20	15:0	QRTable__ is interpreted the same as BT07, using interpolation. However, during empty learning 2 QRTable registers should be modified with interpolation applied.

IAvgEmpty (0x36)

BITFIELD	BITS	DESCRIPTION	DECODE
Iavg_empty	15:0	This is average of the current sampled at the last several empty events. IavgEmpty is used for defining a "pivot point" during empty learning, for adapting QRTable values. When empty occurs, if the current is much greater than IavgEmpty, then mostly gain is learned. But if the current is much lower than IavgEmpty, then mostly offset is learned.	IavgEmpty is a signed register with a 12.5µV/Rsns (1.25mA with 10mΩsense resistor)LSB in D3.

RComp0 (0x38)

BITFIELD	BITS	DESCRIPTION
SPR	15:8	
RCOMP0	7:0	This is the RCOMP value that is appropriate at Temperature = TempNom Adjust RCOMP0 as you would adjust RCOMP in ModelGauge 1.0 parts.

TempCo (0x39)

BITFIELD	BITS	DESCRIPTION
TempCoHot	15:8	Upper byte holds TempCoHot with units of 0.03125counts/°C.
TempCoCold	7:0	Lower byte holds TempCoCold with units of 0.125counts/°C

VEmpty (0x3A)

BITFIELD	BITS	DESCRIPTION	DECODE
V_Empty	15:7	Empty Voltage. Sets the voltage level for detecting empty.	A 10mV resolution gives a 0 to 5.11V range. This value is written to 3.12V at power-up.
V_Recover	6:0	Recovery Voltage. Sets the voltage level for clearing empty detection. Once the cell voltage rises above this point, empty voltage detection is reenabled.	A 40mV resolution gives a 0 to 5.08V range. This value is written to 3.68V at power-up.

QRTable30 (0x42)

BITFIELD	BITS	DESCRIPTION
QRTable30	15:0	QRTable__ is interpreted the same as BT07, using interpolation. However, during empty learning 2 QRTable registers should be modified with interpolation applied.

ConvgCfg (0x49)

The ConvgCFG register controls the converge to empty function of ModelGauge m5. This feature bends the RepSOC curve to closely match the voltage waveform as the SOC approaches empty, ensuring 0% is reported when V_Empty is reached.

BITFIELD	BITS	DESCRIPTION	DECODE
RepLow	15:12	Sets the threshold below which RepCap begins to bend upwards.	The LSB for RepLow is 2% and the range is 0% to 30%.
VoltLowOff	11:7	When the AvgVCELL drops below VoltLow, RepCap is bent downwards according to the ratio ((VCELL-Vempty)/VoltLowOff). The LSB for VoltLowOff is 20mV as the value here is a positive differential value to V_empty. Note that once this condition is reached, the RepLow math is replaced by this math.	
MinSlopeX	6:3	Sets the amount of slope-shallowing which occurs when RepSOC falls below RepLow.	MinSlopeX=1 corresponds to a 1/16 ratio, and MinSlopeX=15 corresponds to 15/16 ratio.
RepL_per_stage	2:0	Adjusts the RepLow threshold by: RepL_per_stage*1%*(7-LearnStage). This allows the earlier learn-stages to effectively use a higher RepLow setting, while the final learn-stages are just set to RepLow.	The LSB for Rep_per_stage is 1% and the range is 0% to 7%.

Status2 (0xB0)

The Status 2 register indicates when the battery is full or empty.

BITFIELD	BITS	DESCRIPTION	DECODE
SPR_15_6	15:6		
FullDet	5	Fully_Charged.	Set FullDet = 1 VFSOC>99%; cleared if VFSOC<98.5%. It means ‘setting FullDet bit’ is latched.
SPR_4_2	4:2		
Hib	1	The HCONFIG2 hib Bit is copied to STATUS2 for customer application purposes. Hib indicates whether or not the FG is in hibernate mode.	
SPR_0	0		

TTF_CFG (0xB5)

BITFIELD	BITS	DESCRIPTION
SPR	15:3	
TTF_CFG	2:0	Configures the filtering rate for learning CV halftime for TTF calculation.

CV_MixCap (0xB6)

BITFIELD	BITS	DESCRIPTION
CV_MixCap	15:0	The MixCapacity when CV mode has been observed to begin.

CV_HalfTime (0xB7)

BITFIELD	BITS	DESCRIPTION
CV_Halftime	15:0	CV_HalfTime is the observed half-time from CV_Start until AvgCurrent<CC_Current/2. It is the exponential decay half-life of the current curing CV mode charging.

CGTempCo (0xB8)

BITFIELD	BITS	DESCRIPTION
CGTempCo	15:0	CGTempCo configures the temperature coefficient for metal resistance, if the calculation is enabled. CGTempCo is restored from nCGTempCo OTP if enabled. If metal resistance is enabled, but OTP restore for CGTempCo is not enabled, then CGTempCo gets loaded with a good default value for using copper (0x20C8 for 8%/20degC).

Curve (0xB9)

The CURVE register is used to enable thermistor curvature adjustment. This allows the temperature to be calculated accurately over a wider range than just using TGAIN and TOFF.

BITFIELD	BITS	DESCRIPTION	DECODE
ECURVE	15:8	Ground Resistance Thermistor Compensation. Compensates the thermistor calculation by considering the battery current through the BATT- path and BATT- connector. Normally set to 0 unless the application has high currents or significant GND resistance between chip GND and thermistor GND.	LSB is 0.9765625mΩ, so the range is 0 to 249.0234375mΩ.
TCURVE	7:0	Sets the curvature compensation for thermistor calculations if thermistor curvature compensation is enabled. OTPCFG1.enCRV = 1. When enabled, the temperature translation is modified according to the following equation: (original temp translation equation): TEMPx = (AIN x TGAIN)/0x4000 + TOFF x 2 Combined with new translation work: TEMP = TEMPx + TCURVE x (TEMP-0x1400) x (TEMP-0x1400) /0x40000 x if(Temp<0x1400,-1,1).	

Config2 (0xBB)

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	15:11		
FCThmHot	10	Set to 1 to enable thermistor hot forcedly, regardless of actually sense thermistor temperature.	
ThmHotEn	9	Set to 1 to enable ThmHot function by comparing Voltage/Temp condition with THMHOT (40h). ThmHot function is FG charger input current-limit control.	
ThmHotAlrtEn	8	Set to 1 to enable ThmHotAlrtEn alert. If ThmHotAlrtEn = 0, the alert-on is disabled.	
dSOCen	7	Set to 1 to enable SOC 1% change alert. If dSCOCen = 0, the alert-on is disabled.	
TAlrtEn	6	Set to 1 to enable temperature alert. If TAlrtEn = 0, the alert-on is disabled.	
LdMdl	5	Host sets this bit to 1 in order to initiate firmware to finish processing a newly loaded model. Firmware clears this bit to zero to indicate that model loading is finished.	
OCVQen	4	Set OCVQen=1 to enable automatic empty compensation based on VFOCV information.	
ISysNCurr	3:0	Sets the time constant for the AvgISys register. The default POR value of 0100b gives a time constant of 5.625. The equation setting the period is: AvgISys time constant = 45s x $2^{(ISysNCurr-7)}$.	Sets the time constant for the AvgISys register. The default POR value of 0100b gives a time constant of 5.625. The equation setting the period is: AvgISys time constant = 45s x $2^{(ISysNCurr-7)}$.

RippleCfg (0xBD)

BITFIELD	BITS	DESCRIPTION	DECODE
kDV	15:3	Sets the corresponding amount of capacity to compensate proportional to the ripple. kDV contributes empty compensation as a function of ripple voltage.	The LSB units for kDV are 0.05/256 %/mV.
NR	2:0	Sets the filter magnitude for ripple observation.	Set NR[2:0] for the below filter timing (*i.e., Ripple Time Range*): 0x0 = 1.4s 0x1 = 2.8s 0x2 = 5.6s 0x3 = 11.2s 0x4 = 22.4s 0x5 = 45s 0x6 = 90s 0x7 = 3min

Measurement Registers

Register Details

Temp (0x08)

BITFIELD	BITS	DESCRIPTION	DECODE
TEMP	15:0	This is the most recent trimmed temperature measurement. Temperature is measured every 1.4 seconds.	When using AIN for temperature (Tex = 0), configure TGAIN and TOFF to adjust the AIN measurement to provide units degrees in the high-byte of Temp. When TGAIN and TOFF are configured properly for the selected thermistor, the LSB is 0.0039˚C and the upper byte has units 1°C. Temp is a signed register. To configure the BT07 to receive temperature information from the I^2C, set Tex = 1 and periodically write the Temp register with the appropriate temperature.

Vcell (0x09)

BITFIELD	BITS	DESCRIPTION	DECODE
VCELL	15:0	This is the most recent trimmed cell voltage result. It represents an FIR average of raw results. The VOLT_Raw is sampled every 175.8ms and gain and offset trim are applied to calculate VCELL.	Bits D15 to D0 represent that 15-bit conversion result. VCELL has 78.125µV per LSB.

Current (0x0A)

BITFIELD	BITS	DESCRIPTION
Current	15:0	The IC measures the voltage between the CSP and CSN pins and the result is stored as a two's complement value in the Current register. Voltages outside the minimum and maximum register values are reported as the minimum or maximum value. The register value should be divided by the sense resistance to convert to Amperes. The value of the sense resistor determines the resolution and the full-scale range of the current readings.

AvgCurrent (0x0B)

BITFIELD	BITS	DESCRIPTION	DECODE
AvgCurrent	15:0	This is the 0.7s to 6.4hr (configurable) IIR average of the current. This register represents the upper 16 bits of the 32-bit shift register that filters current. The average should be set equal to Current upon startup.	Units of LSbit are 1.5625µA/Rsns.

AvgTA (0x16)

BITFIELD	BITS	DESCRIPTION	DECODE
AvgTA	15:0	This is the 6min to 12hr (configurable) IIR average of the Temperature.The average is set equal to Temp upon startup.	Units of LSbit are 0.0039˚C. The upper byte has units 1°C.

AvgVCell (0x19)

BITFIELD	BITS	DESCRIPTION	DECODE
AvgVCELL	15:0	This reports the 12s to 24min (configurable) IIR average of VCELL.The average is set equal to VCELL at startup.	AvgVCELL has 78.125uV per LSB

MaxMinTemp (0x1A)

BITFIELD	BITS	DESCRIPTION	DECODE
MaxTemperature	15:8	Records the maximum Temperature.	Units of LSB are 1˚C.
MinTemperature	7:0	Records the minimum Temperature.	Units of LSB are 1˚C.

MaxMinVolt (0x1B)

BITFIELD	BITS	DESCRIPTION	DECODE
MaxVoltage	15:8	Records the VCELL maximum voltage.	Units of LSB are 20mV.
MinVoltage	7:0	Records the VCELL minimum voltage.	Units of LSB are 20mV.

MaxMinCurr (0x1C)

BITFIELD	BITS	DESCRIPTION	DECODE
MaxChargeCurrent	15:8	Records the maximum charge current.	8-bit values with 0.4mA resolution.
MaxDisCurrent	7:0	Records the maximum discharge current.	8-bit values with 0.4mA resolution.

AIN0 (0x27)

BITFIELD	BITS	DESCRIPTION	DECODE
AIN0	15:0	This is the most recent trimmed ratiometric AIN0 measurement, which is generally used for measuring temperature. AIN0 is measured every 1.4 seconds (if Ten=1).	AIN0 is an unsigned register where 0xFFFF indicates 100% ratio between AIN0/THRM. LSb is 2^{-16}

AtTTF (0x33)

BITFIELD	BITS	DESCRIPTION
AtTTF	15:0	

Timer (0x3E)

BITFIELD	BITS	DESCRIPTION
TIMER	15:0	Timer increments once every task period. With default TaskPeriod, timer has units 0.1758 seconds.The timer manages the following tasks: 1) Thermistor measurements occur once every 8 tasks. 2) Debouncing repeats for 8 TIMER ticks. 3) dV is measured based on dTthr TIMER ticks.

ShdnTimer (0x3F)

The SHDNTIMER register sets the timeout period from when a shutdown event is detected until the device disables the LDO and enters low-power mode.

BITFIELD	BITS	DESCRIPTION
SHDN_THR	15:13	Sets the shutdown timeout period from a minimum of 45s to a maximum of 1.6h. The default POR value of 7h gives a shutdown delay of 1.6h. The equation setting the period is: Shutdown Timeout Period = 175.8ms × 2(8+THR)
SHDNCTR	12:0	Shutdown Counter. This register counts the total amount of elapsed time since the shutdown trigger event. This counter value stops and resets to 0 when the shutdown timeout completes. The counter LSb is 1.4s.

QH0 (0x4C)

BITFIELD	BITS	DESCRIPTION
QH0	15:0	Last sampled QH for dQ accumulation.

VRipple (0xBC)

BITFIELD	BITS	DESCRIPTION	DECODE
Vripple	15:0	It is for the voltage compensation on battery capacity report. It is for the internal usage only.	LSB unit = 1.25/16mV.

TimerH (0xBE)

BITFIELD	BITS	DESCRIPTION
TIMERH	15:0	TIMERH is a 16-bit high-word extension to the TIMER register. This extension allows time counting up to 24 years. This register can be enabled in the save and restore registers.

ModelGauge m5 Output Registers

Register Details

RepCap (0x05)

BITFIELD	BITS	DESCRIPTION	DECODE
RepCap	15:0	AvCap is modified to prevent from reporting any sudden changes in capacity when there is a sudden load change. RepCap forecasts the same time-to-empty as AvCap.	0.5mAh per LSB with 10mΩ sense resistor.

RepSOC (0x06)

BITFIELD	BITS	DESCRIPTION	DECODE
RepSOC	15:0	RepSOC is the complete calculation for state-of-charge. This includes all processing, including: ModelGauge mixing, and empty compensation.	16 bit result. The high byte indicates 1% per LSB. The low byte reports fractional percent.

Age (0x07)

BITFIELD	BITS	DESCRIPTION	DECODE
Age	15:0	Age represents the percentage of full capacity relative to the design capacity.	The high byte is 1%/LSB, and the low byte is 1/256 %/LSB. Age is an unsigned int. Equation is FullCap / DesignCap x 100%

QResidual (0x0C)

BITFIELD	BITS	DESCRIPTION	DECODE
Qresidual	15:0	This is the capacity which is not available because of the battery impedance and load current. This value changes when the load current or temperature changes. This is based on a learned parameter.	16-bit value. 0.5mAh per LSB with 10mΩ sense resistor.

MixSOC (0x0D)

BITFIELD	BITS	DESCRIPTION	DECODE
MixSOC	15:0	SOC is the remaining state-of-charge in the battery, including capacity that may be un-available because of the discharge rate.	16 bit result. The high byte indicates 1% per LSB. The low byte reports fractional percent.

AvSOC (0x0E)

BITFIELD	BITS	DESCRIPTION	DECODE
AvSOC	15:0	AvSOC is the available state-of-charge.This includes all processing, including: Model-Gauge mixing, and empty compensation.	16 bit result. The high byte indicates 1% per LSB. The low byte reports fractional percent.

MixCap (0x0F)

BITFIELD	BITS	DESCRIPTION	DECODE
MixCapH	15:0	This is the MS word representing remaining capacity with coulomb-counter + voltage-fuel-gauge mixing. This does not include empty compensation, and includes any capacity which may be unavailable because of the dis-charge rate. Current results are accumulated every 175.8ms.	0.5mAh per LSB with 10mΩ sense resistor.

FullCap (0x10)

BITFIELD	BITS	DESCRIPTION	DECODE
FullCAP	15:0	This register holds the temperature compen-sated full capacity value. This also compen-sates for the temperature dependence of charge termination. The FullCapNom valus is multiplied by a temperature correction factor (FCTC) and the result is stored in this register.	0.5mAh per LSB with 10mΩ sense resistor.

TTE (0x11)

BITFIELD	BITS	DESCRIPTION	DECODE
hr	15:10	Remaining time-to-empty is calculated as (AvCap) / AvgCurrent. When enabled, the AtRate value is substituted for AvgCurrent in this calculation.	LSB unit = 1.6hr
mn	9:4	Remaining time-to-empty is calculated as (AvCap) / AvgCurrent. When enabled, the AtRate value is substituted for AvgCurrent in this calculation.	LSB unit = 1.5mn
sec	3:0	Remaining time-to-empty is calculated as (AvCap) / AvgCurrent. When enabled, the AtRate value is substituted for AvgCurrent in this calculation.	LSB unit = 5.625s

Rslow (0x14)

BITFIELD	BITS	DESCRIPTION	DECODE
RSLOW	15:0	This reports the battery's slow internal resistance.	16 bit value. Units of LSbit are 2-12Ω with 10mΩ sense resistor.

Cycles (0x17)

BITFIELD	BITS	DESCRIPTION	DECODE
Cycles	15:0	Odometer style accumulation of battery cycles.	The LSB indicates 1% of a battery cycle (1% charge + 1% discharge). One cycle (Cycles = 100%) indicates 100% charge and discharge.

AvCap (0x1F)

BITFIELD	BITS	DESCRIPTION	DECODE
AvCap	15:0	This is the remaining capacity with coulomb-counter + voltage-fuel-gauge mixing, after accounting for capacity that is unavailable due to the discharge rate.	16-bit value. 0.5mAh per LSB with 10mΩ sense resistor.

TTF (0x20)

BITFIELD	BITS	DESCRIPTION	DECODE
hr	15:10	Remaining time-to-full as calculated by firmware.	LSB unit = 1.6hr
mn	9:4	Remaining time-to-full as calculated by firmware.	LSB unit = 1.5mn
sec	3:0	Remaining time-to-full as calculated by firmware.	LSB unit = 5.625s

FullCapRep (0x35)

BITFIELD	BITS	DESCRIPTION	DECODE
FullCapRep	15:0	FullCapRep reports the full capacity using the MAX17047 method, where full gets defined as "the RepCap when charge termination occurs". This is different from the new method (see FullCap register) in which FullCap is automatically compensated when the temperature and load condition changes. I.e., if the temperature is reduced, FullCap suddenly reduces (not waiting for any charging or charge termination), while FullCapRep does not update until the next charge termination.	0.5mAh per LSB with 10mΩ sense resistor.

FCTC (0x37)

BITFIELD	BITS	DESCRIPTION	DECODE
FCTC	15:0	This temperature correction factor is used to calculate the FullCap0 as a function of FullCapNom and the present temperature (TA).	Units are $1/2^{21}$C.

dQAcc (0x45)

BITFIELD	BITS	DESCRIPTION	DECODE
dQacc	15:0	For continuous learning and zigzag learning, this is an always increasing number. I.e., as the battery is charged, this register increases. As it is discharged, it also increases.	Units of LSb are 16mAh with 10mΩ sense resistor. Max range is 8X RemCap register.

dPAcc (0x46)

BITFIELD	BITS	DESCRIPTION	DECODE
dPacc	15:0	Similar behavior as dQacc, except this is derived from the VF_SOC.	16 bit value. Units of LSb are 0.015625% (1/64 %).

VFRemCap (0x4A)

BITFIELD	BITS	DESCRIPTION
VFRemCap	15:0	Remaining Capacity according to the voltage fuel-gauge.

MaxError (0xBF)

BITFIELD	BITS	DESCRIPTION	DECODE
MaxError	15:0	At each empty learning event, it is a filter for the new error. It is for internal usage only.	LSB unit = 1/256%.

AtQresidual (0xDC)

BITFIELD	BITS	DESCRIPTION
AtQresidual	15:0	AtQresidual is calculated as normal Qresidual, except using AtRate instead of current.

AtTTE (0xDD)

BITFIELD	BITS	DESCRIPTION	DECODE
AtTTE	15:0	Calculated time-to-empty based on the formula AtTTE = ((AtAvCap,0) / AtRate) >> 5	LSB unit = 5.625s.

AtAvSOC (0xDE)

BITFIELD	BITS	DESCRIPTION
AtAvSOC	15:0	AtAvSOC is calculated as normal AvSOC, except using AtRate instead of current.

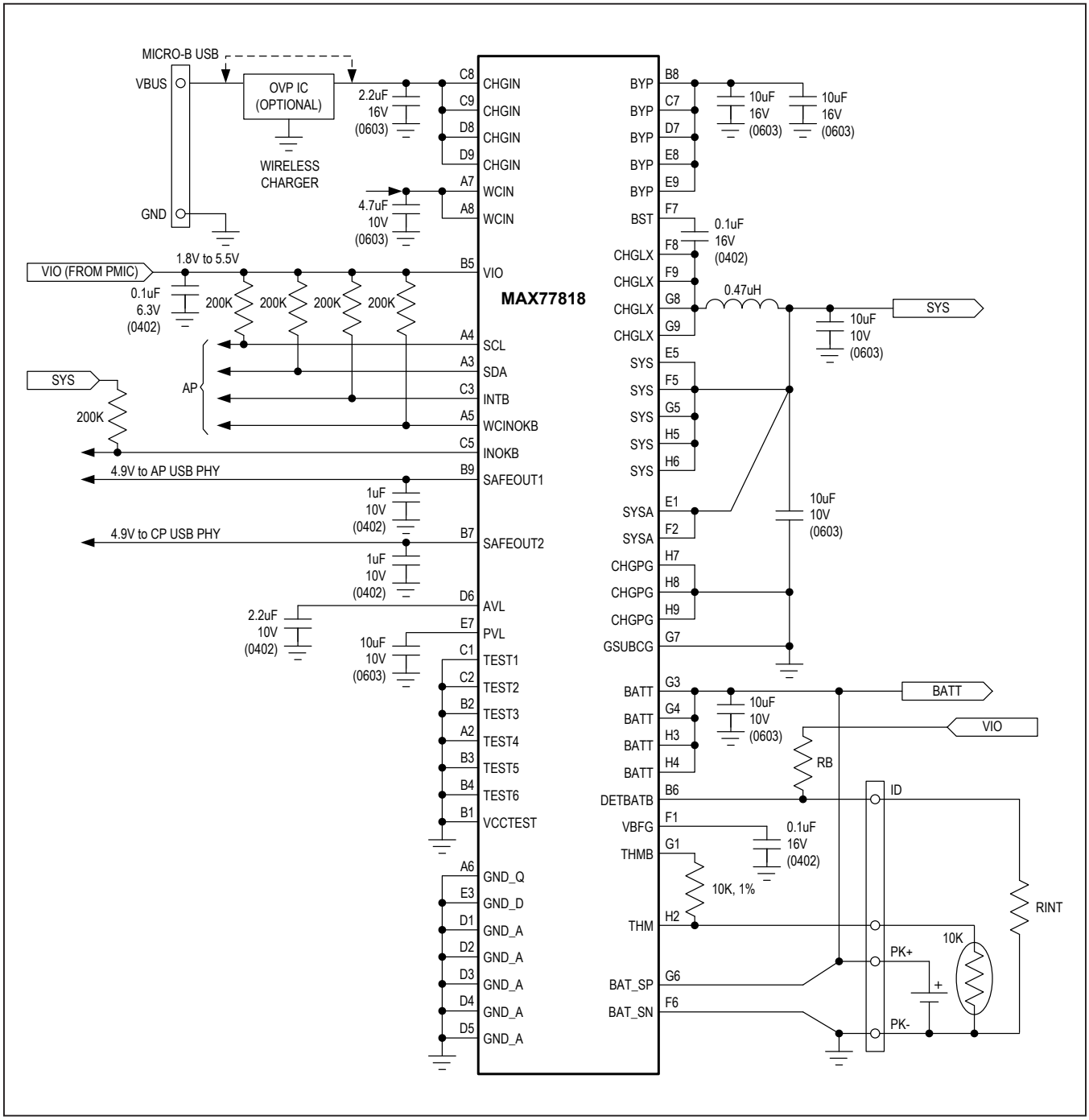
AtAvCap (0xDF)

BITFIELD	BITS	DESCRIPTION
AtAvCap	15:0	AtAvCap is calculated as normal AvCap, except using AtQresidual instead of Qresidual.

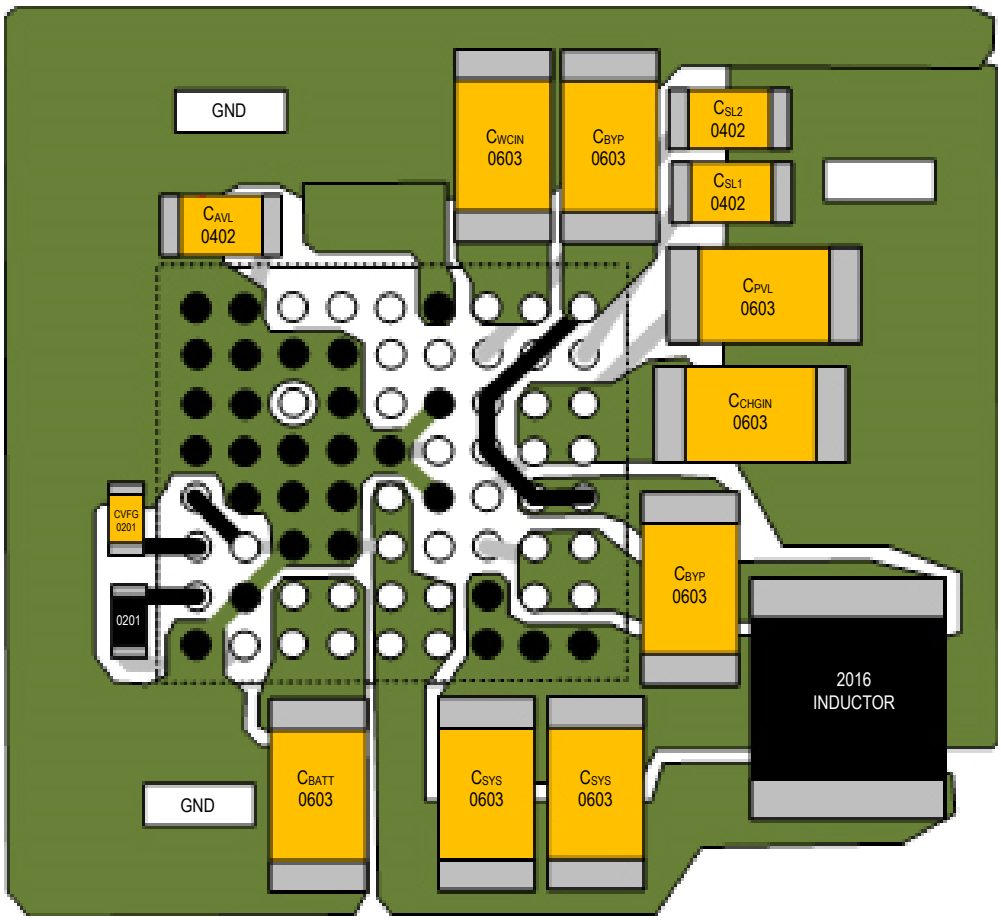
VFOCV (0xFB)

BITFIELD	BITS	DESCRIPTION
VFOCV	15:0	

Typical Application Circuit



PCB Layout Guide



Layout Guidelines

Good PCB layout is essential to minimize ground bounce and EMI and achieve voltage, temperature, and current measurement accuracy. Follow these guidelines:

1) Connect the power ground plane to the analog ground plane with a star connection.
2) Place CHGIN, WCIN, BYP, SYS, and BATT bypass capacitors as close as possible to the IC pins and connect them to the power ground plane on the PCB top layer.
3) Use wide and short traces for high current connections such as CHGIN, WCIN, SYS, and BATT.
4) All bypass capacitors should be placed as close to the chip as possible, connect bypass capacitors to the closest ground plane.
5) BAT_SP and BAT_SN should have direct kelvin sensing connections to the interface of battery.
6) The kelvin traces should not be shared with other circuits and vias on kelvin traces are not recommended.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX77818EWZ+	-40°C to +85°C	72-pin WLP 0.4mm pitch, 3.867mm x 3.608mm (±0.015mm X and Y)

+Denotes lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
72 WLP	W723B3+1	**21-0477**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—
1	10/15	Corrected Figure 5 and minor errors	19, 22, 27, 36
2	2/16	Corrected m5 designation throughout, updated Note 7, *Safeout LDO* section, Figure 2, and Figure 5	1, 16, 21, 23
3	9/17	Corrected errors, added fuel gauge descriptions	1–102
4	3/20	Updated *Typical Operating Circuit*, *Safeout LDOs Electrical Characteristics* table, and Figure 1	1, 18, 19, 28

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