MAX79356

ZENO Flexible Narrowband OFDM Powerline Communication Modem with Integrated Analog Front End

General Description

ZENO™ (MAX79356) is a programmable narrowband orthogonal frequency division multiplexing (OFDM)-based powerline communication (PLC) modem system-on-chip (SoC) device that provides standards compliant high performance and secured powerline communication in a small package. ZENO integrates two pipelined 32-bit RISC (MAXQ®30E) processors to offer high performance and future-proof flexibility. These two 32-bit RISC processors perform dedicated PHY signal processing functions and MAC layer functionality. Maxim provided, certified firmware images allow faster time to market. Factory or in-field firmware update feature allows adoption of changes and updates in PLC communication standards. The integrated high-speed AES-CCM* engine ensures standards compliant data communication security and integrity.

Applications

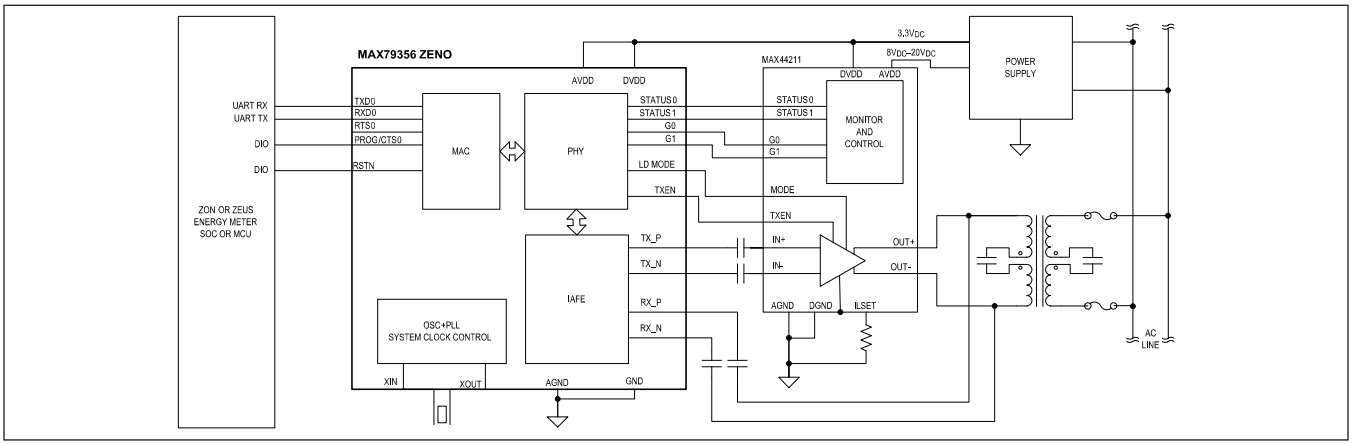
- Smart Grid Communications
- Smart Meters
- Advanced Metering Infrastructure (AMI)
- AMI Concentrators
- Factory and Building Automation
- Electric Vehicle Charging
- Home Energy Monitoring
- Solar and Renewable Energy Management
- Street Lighting Automation and Lighting Control

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Supports All Standards and Frequency Bands to Reduce R&D Investment and Time to Market
  - G3-PLC Certified
  - Compliant with, G3-PLC, IEEE 1901.2, ITU G9903, PRIME
  - Supports Regulated Frequency Bands for Communication: CENELEC, FCC, ARIB
- Accommodates Evolving Standards with Flexible System Architecture That Integrates Dual 32-Bit RISC Processors with 512KB Flash and 288KB RAM for MAC and PHY
  - Universal Firmware Supports Both PAN Coordinator and PAN Device Functionality
  - Programmable Frequency Notching
- Efficient BOM for Building Competitive Modems
  - Supports All G3-PLC Bands with One SKU
  - Integrates MAC, OFDM PHY, and Analog Front End for Simplified Board Design
  - Single 16MHz Crystal Generates All Operating Clocks
  - UART Provides Simple Interface for Host Processor Communications
- Low Power Consumption (typ)
  - 55mW in Listen Mode
  - 70mW in Active Mode
- High-Sensitivity Receiver with Adaptive Gain Control Allows Communication with Low Signal-to-Noise Ratio
- Integrated 128/256-bit AES and AES-CCM* Engine for Encryption/Decryption and Authentication

Typical Operating Circuit



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19-7548; Rev 2; 9/17

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to AGND_0, AGND_1.)

Supplies and Ground Pins

DVDD33_0, DVDD33_1, AVDD33 .....-0.5V to +3.6V

DVDD12, AVDD12.....-0.5V to +1.7V

DGND_0, DGND_1, DGND_2.....-0.2V to +0.2V

Analog Output Pins

DVDD12_REG.....-0.5V to +1.7V

TX_N, TX_P .....-0.5V to V_{AVDD33} + 0.5V

Analog Input Pins

RX_N, RX_P.....-0.5V to V_{AVDD33} + 0.5V

Oscillator Pins

XIN, XOUT.....-0.5V to V_{DVDD33} + 0.5V

Digital Output Pins

TXD0, RTS0, READY, TXEN, LD MODE, G0, G1, MOSI, MOSI, SSEL, SCLK, COLLISION, ACTIVITY.....-0.5V to V_{DVDD33} + 0.5V

Digital Input Pins

RXD0, PROG/CTS0 , ZC1, ZC2, STATUS0, STATUS1, MISO, RSTN.....-0.5V to V_{DVDD33} + 0.5V

Temperature

Operating Junction Temperature (peak, 100ms).....+140°C

Operating Junction Temperature (continuous).....+125°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}).....46°C/W

Junction-to-Case Thermal Resistance (θ_{JC}).....10°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING CONDITIONS						
Digital Supply Voltage	V_{DVDD33_0}, V_{DVDD33_1}	V_{AVDD33} = V_{DVDD33_0} = V_{DVDD33_1} (Note 2)	2.7	3.3	3.6	V
Analog Supply Voltage	V_{AVDD33}	V_{AVDD33} = V_{DVDD33_0} = V_{DVDD33_1} (Note 2)	3.0	3.3	3.6	V
Operating Temperature			-40		+85	°C
INTERNAL LOW DROPOUT (LDO) VOLTAGE REGULATOR						
LDO Output Voltage	V_{DVDD12_REG}	V_{DVDD12_REG} = V_{DVDD12} = V_{AVDD12}, internal LDO enabled (Note 3)	1.18	1.20	1.22	V
SUPPLY MONITORS						
V_{DD33} Fail Warning Voltage (Note 4)	$V_{DD33PFW}$		2.85		3.05	V
V_{DD33} Reset Voltage (Note 4)	$V_{DD33RST}$		2.8		3.0	V
V_{DD12} Fail Warning Voltage (Note 5)	$V_{DD12PFW}$		1.157		1.19	V
V_{DD12} Reset Voltage (Note 5)	$V_{DD12RST}$		1.127		1.16	V

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT/OUTPUT						
Input Low-Level Voltage	V_{IL}		GND		0.29 x V_{DD33}	V
Input High-Level Voltage	V_{IH}		0.7 x V_{DD33}		V_{DD33}	V
Input Voltage Hysteresis	V_{IHYS}			300		mV
Input Leakage Current	I_L	Internal pullup/down resistor disabled	-1		+1	µA
Input Capacitance	C_{IN}			5		pF
Input Pullup Resistance	R_{PU}		50	100	180	kΩ
Input Pulldown Resistance	R_{PD}		50	100	180	kΩ
Output Low-Level Voltage	V_{OL}	Standard drive, I_{OL} = 2mA			0.4	V
		High drive, I_{OL} = 4mA			0.4	V
Output High-Level Voltage	V_{OH}	Standard drive, I_{OH} = 2mA	V_{DD33} - 0.5			V
		High drive, I_{OH} = 4mA	V_{DD33} - 0.5			V
CRYSTAL OSCILLATOR						
Input Capacitance	C_{XIN}			8		pF
Startup Time	T_{SU}			8192		cycles
High-Speed Crystal Frequency (Note 6)	f_{XTAL}			16.0		MHz
POWER CONSUMPTION (Note 7)						
Active Mode Power	P_{ACTIVE}	Combined digital/analog power when transmitting or receiving a packet (CENELEC-A band)		69.7	102.5	mW
Supply Current (DVDD33_0, DVDD33_1)	I_{DVDD33}	Active mode		2.9	4.4	mA
Supply Current (AVDD33)	I_{AVDD33}	Active mode		5.1	7.4	mA
Supply Current (DVDD12) (Note 8)	I_{DVDD12}	Active mode		34.6	45.5	mA
Supply Current (AVDD12)	I_{AVDD12}	Active mode		1.5	2.1	mA
Listening Mode Power	P_{LISTEN}	Combined digital/analog power when listening for SYNC of an RX PACKET (CENELEC-A band)		55.1	80.6	mW

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMITTER							
Full-Scale Voltage, CENELEC-A Band		Frequency = 50kHz TXGAIN = 3		0.9		1.13	V_{PK}
Full-Scale Voltage, FCC Band		Frequency = 150kHz TXGAIN = 3		0.56		0.85	V_{PK}
Common-Mode Voltage					1.2		V
Noise and Spurious Signals, with Respect to Average Tone, CENELEC-A Band		Transmit signal is all 36 tones, TXGAIN = 3, T_A = +25°C	95kHz, bandwidth = 200Hz			-65	dB
			150kHz, bandwidth = 9kHz			-63	
			500kHz, bandwidth = 9kHz			-72.4	
Noise and Spurious Signals, with Respect to Average Tone, ARIB Band		Transmit signal is all 54 tones, TXGAIN = 3, T_A = +25°C	450kHz			-46	dB
			5000kHz			-62	
Noise and Spurious Signals, with Respect to Average Tone, FCC Band		Transmit signal is all 72 tones, TXGAIN = 3, T_A = +25°C	535kHz			-44	dB
			1700kHz			-64	
Load Tolerance 100 x (NoLoadAmp/ WithLoadAmp - 1)		TXGAIN = 3, Z_L = 4kΩ differential, 450kHz				1	%
RECEIVER							
Input Bias Voltage					1.6		V
Common-Mode Rejection		RXGAIN = 24, common-mode input = 1.0V, 450kHz			58		dB
Differential Input Impedance		RXGAIN = 24		57	61		kΩ
		RXGAIN = 23		66	71		
		RXGAIN = 22		54	58		
		RXGAIN = 19		67	71		
		RXGAIN = 18		54	58		
		RXGAIN = 0		54	68		
Equivalent Input Noise, CENELEC-A Band		RXGAIN = 24, V_{IN} = 10mV_{PK}, bandwidth = 35kHz to 91.4kHz			30		μV_{RMS}
Equivalent Input Noise, FCC Band		RXGAIN = 24, V_{IN} = 10mV_{PK}, bandwidth = 152kHz to 490kHz			109		μV_{RMS}

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

Note 2: The AVDD33 DVDD33_0, DVDD33_1 supplies should be connected together at the board level. Appropriate decoupling should be used between the analog AVDD33 supply and the digital DVDD33_0 and DVDD33_1 supplies.

Note 3: The internal LDO voltage regulator should be enabled and the DVDD12_REG supply output should be connected to the AVDD12 and DVDD12 supply inputs at the board level. Appropriate decoupling should be used between the analog AVDD12 supply and the digital DVDD12 supply.

Note 4: V_{DD33} is referencing that AVDD33 DVDD33_0, and DVDD33_1 are connected together at the board level.

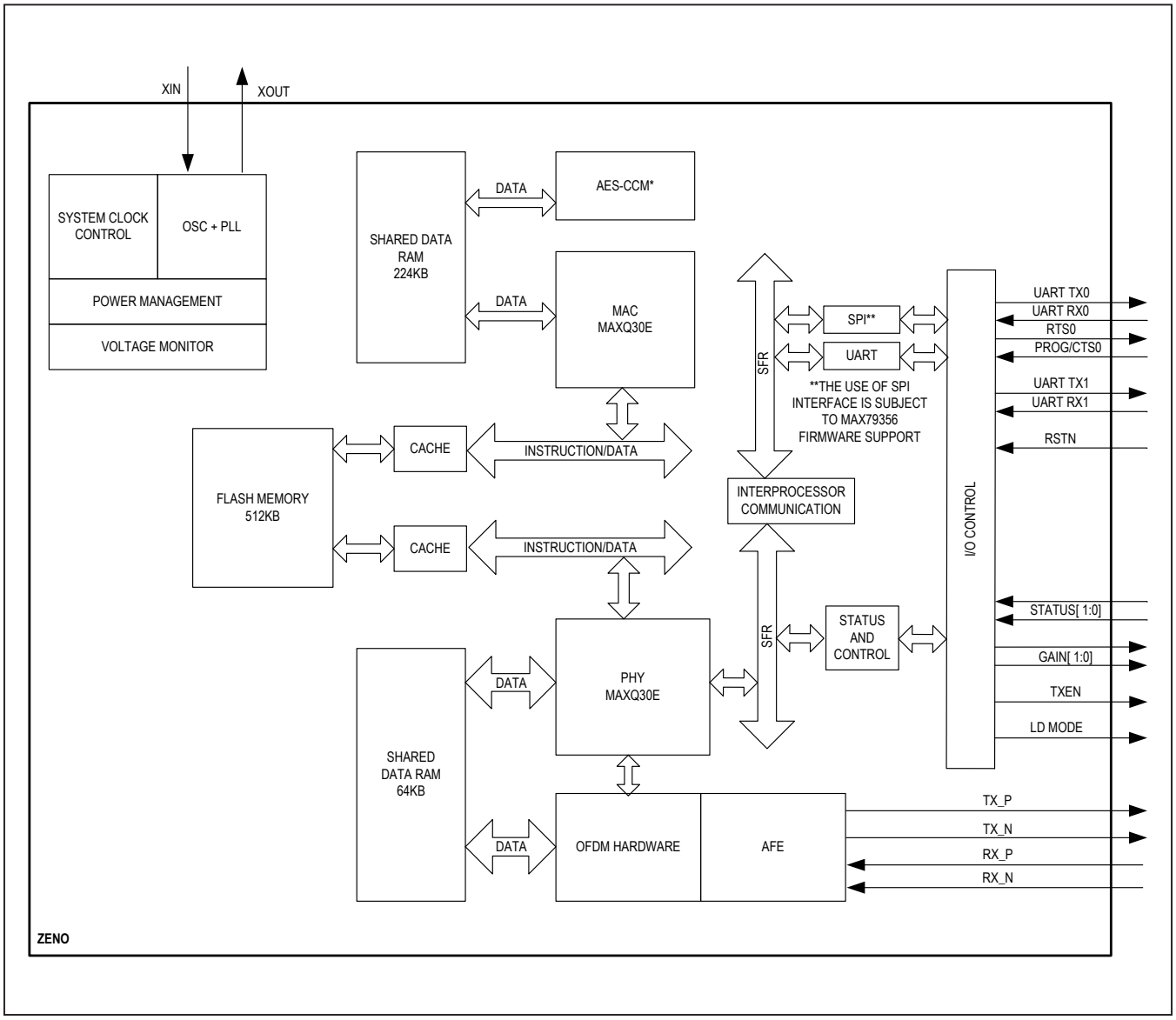
Note 5: V_{DD12} is referencing that DVDD12_REG, DVDD12, and AVDD12 are connected together at the board level.

Note 6: The high-speed crystal should have a calibration tolerance no greater than ±10ppm and a frequency stability better than ±15ppm. The maximum clock frequency deviation must be within ±25ppm.

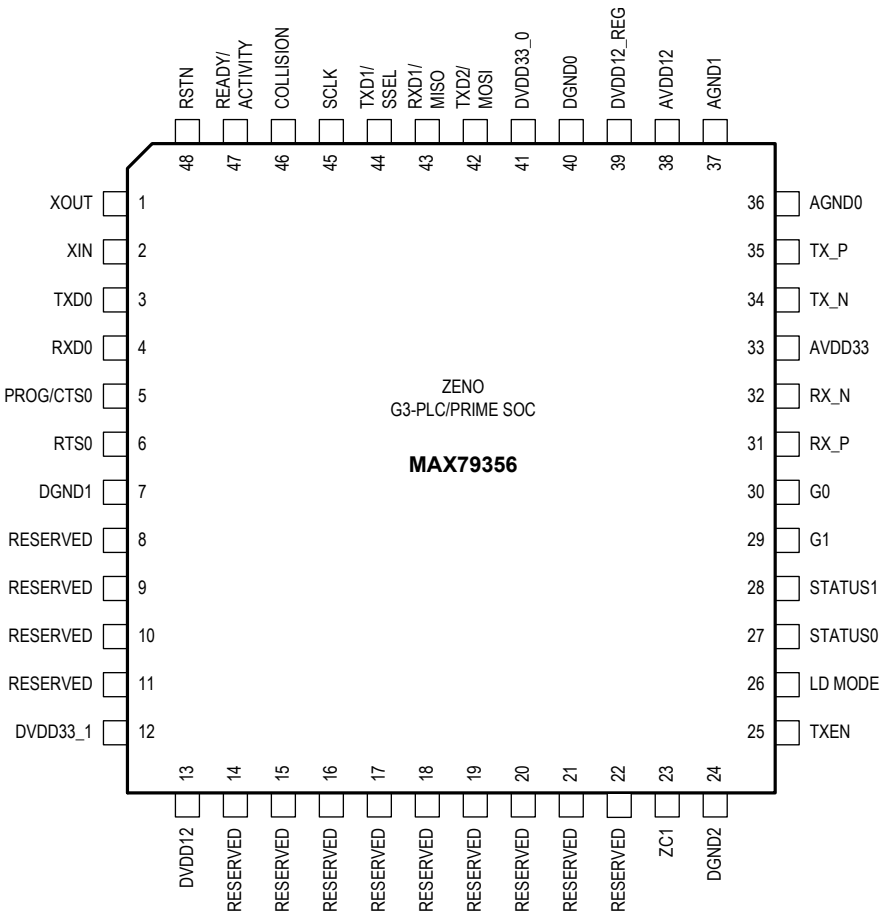
Note 7: All TYP power consumption specifications are based on nominally processed parts running at +25°C and powered with TYP supply voltages.

Note 8: The internal LDO voltage regulator should be enabled and the DVDD12_REG supply output should be connected to the AVDD12 and DVDD12 supply inputs at the board level. Therefore, the current sunk by AVDD12 and DVDD12 is sourced by DVDD12_REG.

Block Diagram



Pin Configuration



Pin Description

PIN	NAME	DESCRIPTION
1	XOUT	Crystal Oscillator Output
2	XIN	Crystal Oscillator Input
3	TXD0	Host Interface (UART0) Transmit Data
4	RXD0	Host Interface (UART0) Receive Data
5	PROG/CTS0	Initiates the UART boot loader if held low when RSTN is pulsed low. Can be used by host to control the flow of data on TXD0. (Subject to FW support.)
6	RTS0	Output. Can be used by modem to control the flow of data from the host. (Subject to FW support.)
7	DGND1	Digital Ground
8	RESERVED	Reserved. Leave unconnected.

Pin Description (continued)

PIN	NAME	DESCRIPTION
9–11, 14–21	RESERVED	Reserved. Connect pins 10, 14, 17, and 19 to 300Ω pulldown resistors to DGND. Connect pins 11, 16, and 18 to 300Ω pullup resistors to DVDD33.
12	DVDD33_1	Digital 3.3V Power Supply. Bypass with a 100nF capacitor as close as possible to the device.
13	DVDD12	Digital 1.2V Power Supply. Connect to DVDD12_REG and bypass with a 100nF capacitor as close as possible to the device.
22	RESERVED	Reserved. Leave unconnected.
23	ZC1	AC Zero-Crossing Detector Input
24	DGND2	Digital Ground
25	TXEN	Line Driver Transmit Enable
26	LD MODE	Active-Low Line Driver Bias Selection
27	STATUS0	Line Driver Status Flag 0
28	STATUS1	Line Driver Status Flag 1
29	G1	Line Driver Gain 1
30	G0	Line Driver Gain 0
31	RX_P	Analog PLC Receive Data. Positive side of differential.
32	RX_N	Analog PLC Receive Data. Negative side of differential.
33	AVDD33	Analog 3.3V Supply. Bypass with a 100nF capacitor as close as possible to the device.
34	TX_N	Analog PLC Transmit Data. Negative side of differential.
35	TX_P	Analog PLC Transmit Data. Positive side of differential.
36	AGND0	Analog GND
37	AGND1	Analog GND
38	AVDD12	Analog 1.2V Power Supply. Connect to DVDD12_REG and bypass with a 100nF capacitor as close as possible to the device.
39	DVDD12_REG	Internal 1.2V LDO Output. Bypass with a 100nF capacitor as close as possible to the device.
40	DGND0	Digital Ground
41	DVDD33_0	Digital 3.3V Power Supply. Bypass with a 100nF capacitor as close as possible to the device.
42	TXD2/MOSI	UART2 TX Output/SPI Mast Output Slave Input
43	RXD1/MISO	UART1 RX Input/SPI Master Input Slave Output
44	TXD1/SSEL	UART1 TX Output/SPI Slave Select. Pull to VDD33 with a 4.7kΩ resistor or leave unconnected.
45	SCLK	SPI Serial Clock
46	COLLISION	Collision. Driven high when a collision is detected on the line.
47	READY/ACTIVITY	Ready/Activity. High level indicates modem is ready to communicate. Driven low when transmit or receive activity is on the line.
48	RSTN	System Reset. Driving RSTN low halts ZENO operation and reinitializes the device. The device restarts when RSTN is returned to a high state.

Detailed Description

Baseband
PHY Overview

ZENO is designed to overcome the challenges associated with the harsh powerline environment for data communications. Some of the challenges are noted below:

- Channel variability with frequency, location, and time
- Narrowband, wideband, and impulse noise and multipath signal propagation commonly present on the power line
- Low and time varying network impedance
- Propagation through transformers that makes the channel subject to severe group delay and attenuation

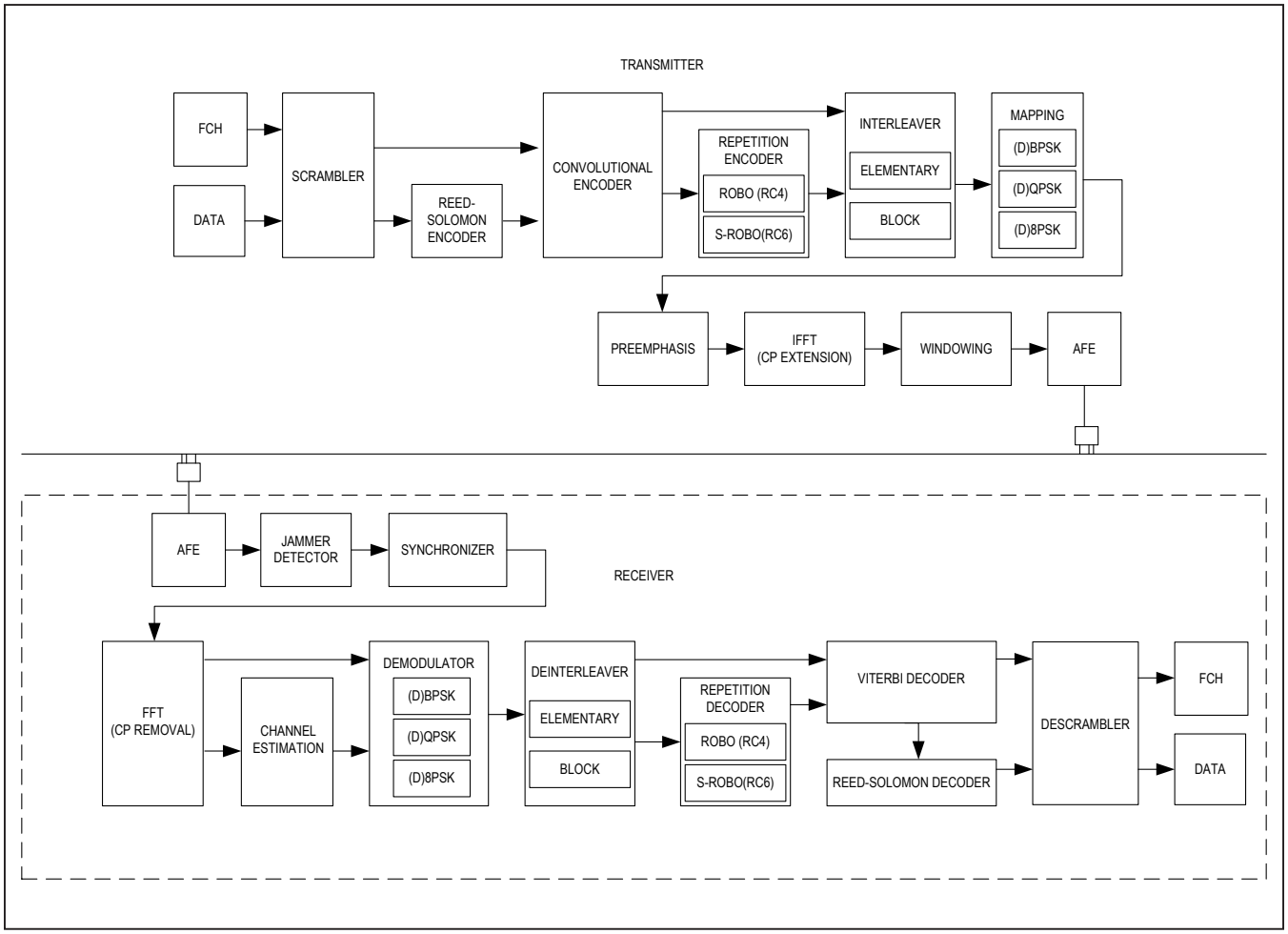


Figure 1. ZENO G3-PLC PHY Block Diagram

ZENO is based on orthogonal frequency division multiplexing (OFDM) to overcome the powerline channel impairment, providing high reliability in data transmission and reception. This method combines spectral efficiency with the flexibility of bandwidth allocation. In combination with error correction coding, ZENO is robust in the presence of frequency selective channels and resilient to jammer signals and impulsive noise.

The OFDM technique places evenly spaced carriers into the available frequency band. ZENO can be configured to operate in a subset of frequencies in the range 10kHz to 490kHz, encompassing CENELEC, FCC, and ARIB frequency bands. The modulation methods supported in differential mode are DBPSK, DQPSK, and D8PSK, and in coherent mode are BPSK, QPSK, and 8PSK. This allows ZENO to trade off channel condition and data rate to achieve the highest efficiency as the channels vary. Additional performance is obtained by adaptive tone mapping, a process by which ZENO automatically detects carriers with poor SNR and redistribute data to carriers with good SNR.

There are several advantages of ZENO OFDM scheme as compared to traditional single carrier FSK or spread-spectrum systems.

ZENO OFDM PHY allows flexible allocation and use of a given channel bandwidth. As an example, the lower and the upper limit of the used frequency band can easily be configured. It is also possible to use any number of sub bands (either contiguous or noncontiguous) for the transmission of a single data stream.

It is considerably more robust against intersymbol interference (ISI) or group delay distortion caused by the transmission channel than narrowband systems. This is mainly due to the fact that the parallel transmission on multiple carriers leads to longer symbol duration. Furthermore, ISI is simply removed by inserting cyclic prefixes between the symbols.

ZENO is robust in presence of narrowband interference because such jammers typically destroy a single carrier only. Through the use of forward error correction (FEC) coding, the erroneous data is detected and corrected using the received coded information.

On the transmitter side of ZENO, data passes through scrambler, FEC encoder (Reed-Solomon encoder, convolutional encoder, and repetition encoder), interleaver, mapping, IFFT with CP extension, windowing, and AFE. On the receiver side of ZENO, digital signal processing blocks accept signals from the AFE, process them, and pass the results to the upper layer. The jammer detector is dedicated to detection and cancellation of narrow band interference. The channel estimator provides critical information such as the link quality and the channel response.

Table 1 shows the frequency bands with which ZENO complies.

Table 1. Supported Frequency Bands

BAND	NUMBER OF CARRIERS	FIRST CARRIER (kHz)	LAST CARRIER (kHz)
CENELEC A	36	35.9375	90.625
CENELEC B	16	98.4375	121.875
FCC	72	154.6875	487.5
ARIB	54	154.6875	403.125

MAC Overview

G3-PLC: MAC/Adaptation Layer

ZENO architecture comprises PHY and MAC/Adaptation layer as shown in Figure 2. Some of the key features of MAC/Adaptation layer are described in the following sections.

Adaptive Tone Mapping (ATM)

To achieve a robust communication, the receiver node automatically detects the subcarriers with low SNR and redistributes the data to other subcarriers with superior channel condition as part of the channel estimation procedure. This information is reported to the remote transmitter using a Tone Map Response packet, which includes the recommended modulation method (ROBO/BPSK/QPSK/8PSK), modulation scheme (coherent/differential), tone map, and frequency selective gain based on latest channel condition to be used when transmitting to the receiver node.

CSMA/CA

Concurrent transmission by multiple nodes can result in frame collisions that distort the signal and cause communication to fail. Carrier-sense multiple access/collision avoidance (CSMA/CA) is a mechanism to reduce the probability of collisions. When using CSMA, as soon as a node is ready to transmit a packet, the device checks the channel for activity. If no other node is transmitting, the node transmits its packet. If another transmitter is detected, the device waits for that transmission to end and then waits for a randomly selected period of time (random back-off time). After this period, the device starts its transmission if no other transmission is detected.

Automatic Repeat Request (ARQ)

To enhance error detection and improve data reliability, ZENO utilizes an automatic repeat request protocol. Since PLC communication is a half-duplex connection, the transmitter waits for an acknowledgment (ACK) of each unicast transmission before it proceeds with the next transmission. If the transmitter does not receive an ACK packet, it resends the packet.

AES-CCM*

To maintain the highest level of security, an on-chip AES-CCM* (an extension of CCM specified in IEEE 802.15.4) coprocessor with AES-128 encryption/decryption is integrated to provide authentication and cyphering/deciphering of the data communication both during the initial association of a node to the network and for all subsequent packet transmissions.

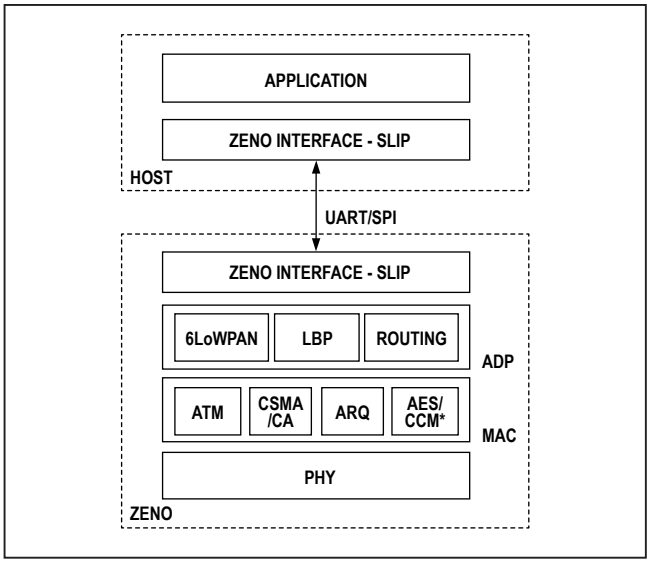


Figure 2 ZENO Architecture.

IPv6 over Low Power PAN (6LoWPAN)

6LoWPAN allows transport of IPv6 packets by providing an IPv6 header compression format for common headers suitable for low power and low-bandwidth networks. This method allows compression of arbitrary prefixes using shared context. Since the IPv6 address can be derived from the short address of a device and PAN Identification, it can omit the IPv6 address in the packet header. Packets up to 1500 bytes are fragmented to fit the maximum packet size allowable by MAC layer. The mesh address header feature enables the implementation of routing algorithm over powerline network and provides a unique routable IPv6 address for each node.

LoWPAN Bootstrap Protocol (LBP)

LBP is used when a new node is trying to join the network. It creates a procedure to send security credentials for identification and authentication of a node followed by secured delivery of a 16-bit short address and group master key (GMK) over an encrypted channel to the node. LBP encapsulates extensible authentication protocol preshared key (EAP-PSK) messages to be exchanged between EAP-PSK server and a node. The preshared key of the node is known to the EAP-PSK server and is used to construct session keys for challenge messages for the node. The short address and GMK are embedded in the protected channel (PCHANNEL) of the second challenge message sent to the node to ensure the confidentiality and integrity of the packet that is forwarded over the network.

LOADng Routing

Lightweight on-demand ad hoc next generation (LOADng) protocol is part of adaptation layer enabling efficient routing of the packets across the powerline network. The automatic route discovery feature can establish an optimized route between two nodes without any further intervention from application layer. If the destination address of a packet is not in the routing table of an originator node (X), it broadcasts a route request (RREQ) packet for that destination (Y) to all its neighbors, which in turn, unicasts (if had a route to destination) or rebroadcasts the RREQ message towards the destination. The route cost (RC) of each route is calculated based on hop by hop forward and reverse link cost using multiple variables such as channel quality and modulation and updated in RREQ packets.

At the destination, the best route is selected by comparing the RC of RREQ packets arrived through different routes. A unicast route REPLY packet is then sent by destination towards the originator and ensures the established route is bidirectional. The blacklisting feature guarantees that links determined to be unidirectional are excluded. A weak link counter in routing messages keeps track of low quality links along the route to be also considered when selecting the best route.

While LOADng delivers a robust and low overhead routing algorithm per G3-PLC and IEEE 1901.2 specifications, the feature can be turned off in ZENO enabling users to experiment their own implementation of routing algorithms in upper layer (e.g., ARIB Route B).

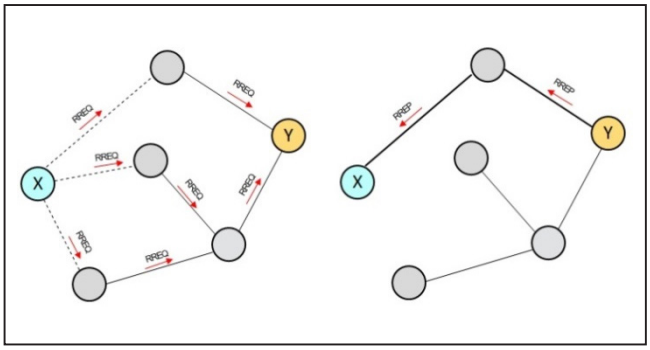


Figure 3. LOADng Route Discovery Process.

Phase Detection Using AC Zero Crossing

In order to identify the phase of each node, ZENO uses a software PLL to lock to the pulses received on the external AC zero-crossing detector input ZC1.

Host Communication

ZENO communicates with the host processor through a serial line interface protocol (SLIP) over the UART0 interface. The ZENO firmware supports operation at either 115,200bps or 230,400bps without flow control. The ZENO G3-PLC Modem Interface Specification describes the host communications protocol.

The host processor can also update the MAC and PHY firmware through UART0 using a memory resident bootstrap loader. The bootstrap loader is started when the PROG input pin is driven low and held low while the reset pin RSTN is pulsed low. To activate the UART bootstrap loader, PROG pin must be held low after RSTN is released until communication with the bootstrap loader is established. A subsequent low pulse on RSTN with PROG driven high disables the bootstrap loader and start normal operation of the ZENO modem.

Hardware

UART

ZENO features two hardware UARTs (UART0, UART1). UART0 is used by the host CPU for data communication, control of the modem, and FW updates. UART1 is used for debugging purposes.

The MAX79356 firmware supports communication at 115,200bps or 230,400bps with no flow control.

Serial Peripheral Interface (SPI)

The use of a SPI interface is subject to MAX79356 firmware support.

ZENO SPI hardware can operate in slave or master modes. This is a common, high-speed, synchronous peripheral interface that shifts a bit stream of variable length and data rate between the microcontroller and other peripheral devices. Programmable clock frequency, character lengths, polarity, and error handling enhance the usefulness of the peripheral. The maximum baud rate of the SPI interface is half the system clock for master mode operation and 1/8th the system clock for slave mode operation.

ZENO Integrated Analog Front End (IAFE)

Capability of IAFE

The IAFE accepts an analog signal from the powerline coupling interface and provides digital samples for demodulation and decoding, and accepts digital samples from the PHY processor and generates an analog signal to excite the line driver. It combines digital and analog circuitry to implement signal conditioning and filtering functions.

The receiver consists of a low-noise automatic-gain control (AGC) amplifier followed by a lowpass filter (LPF), an ADC, and a programmable digital filter engine. An ADC samples the filter output. AGC reduces the receiver channel input-referred noise by providing additional signal gain to the IAFE input. The filter blocks any out-of-band noise, provides antialiasing, and selects a proper IAFE bandwidth. Using the adaptation blocks, AGC scales the received signal to maintain the optimum signal level at the ADC input.

The ADC samples the analog signal and converts it to a digital stream with a maximum 1.2Msps sampling rate. The receiver programmable digital filter engine reduces input noise by limiting input signal spectrum according to supported frequency bands.

The transmitter consists of a programmable digital filter engine, a DAC, an image-reject LPF, and a programmable-gain predriver. The transmitter's programmable digital filter engine reduce out-of-band emissions by limiting the output signal spectrum according to the supported frequency bands. The DAC receives the data stream from the digital PHY and provides a complementary function to the receive channel with a maximum 1.2Msps sampling rate. The DAC converts the 10-bit digital stream to an analog voltage.

The lowpass filter removes spurs and harmonics adjacent to the desired pass band to reduce any out-of-band transmitted frequencies and energy from the DAC output. The lowpass filter ensures that the transmitted signal meets bandwidth requirements specified by the different wideband and narrowband standards.

The predriver controls the output level of the lowpass filter connected to an external line driver, which, in turn, connects to the powerline medium. The output level is adjustable by the predriver gain control.

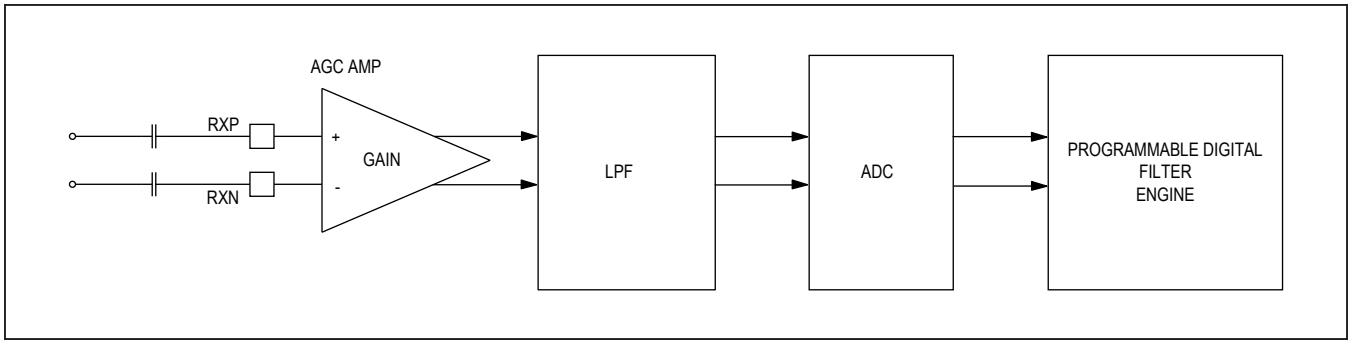


Figure 4. IAFE Receive Path

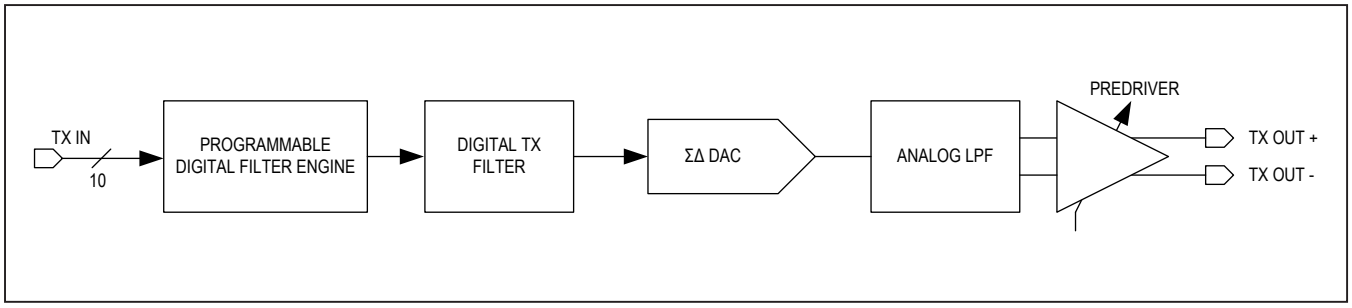


Figure 5. IAFE Transmit Path

Power Management

ZENO's power management feature reduces power consumption by automatically clock gating and providing a means for the firmware to optimize the clock frequency. Clock gating is automatically applied to functional hardware blocks when not in use.

ZENO operates in two power modes: designated active and listening.

Active mode: It is defined as the mode when the ZENO modem is either in active transmit or active receive. In active mode the baseband and the analog front end (AFE) are working at a high level of activity. In active mode all the hardware modules might not be working at the same time, which allows automatic clock gating features to reduce power.

Listening mode: When ZENO is not in active mode, it is in listening mode. Most of the baseband hardware is turned off in this mode. Only the AFE and a small section of the baseband hardware dedicated to packet detection is on at this point. ZENO transitions to active mode when it detects the start of a packet on the line.

Clock Management—PLL and Crystal Oscillator

ZENO provides a built-in crystal oscillator circuit (Figure 6) and an associated PLL. The device can function in multiple clock configurations to support various communication bands and standards. A 16MHz crystal is connected across XOUT and XIN. This crystal and the PLL dividers can synthesize all the system and AFE clock frequencies required for supported standards. The system and AFE clocks can be independently controlled through the PLL dividers.

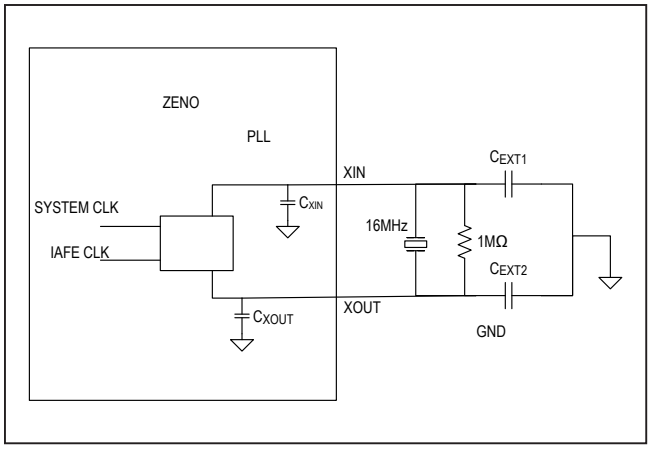


Figure 6. Clock Generation from External Crystal

The values of C_{XIN} and C_{XOUT} depend upon the crystal load capacitance, the XIN/XOUT pins' capacitance, and the parasitic capacitance of the PCB traces connected to XIN and XOUT. The values should be chosen to satisfy the following equation:

$$C_{XTAL} = \left\{\frac{[C_{XIN} + C_{EXT1}] \times [C_{XOUT} + C_{EXT2}]}{[C_{XIN} + C_{EXT1} + C_{XOUT} + C_{EXT2}]}\right\} + C_{PCB}$$

C_{XTAL} is the load capacitance specified for the 16MHz crystal

C_{XIN} and C_{XOUT} are the internal capacitance of the XIN and XOUT pins, respectively

C_{PCB} is the parasitic capacitance of the PCB traces to XIN and XOUT

Assuming $C_{XIN} = C_{XOUT} = C_{INT}$, and $C_{EXT1} = C_{EXT2} = C_{EXT}$, this simplifies to:

$$C_{XTAL} - C_{PCB} = \frac{[C_{INT} + C_{EXT}]^2}{2 \times [C_{INT} + C_{EXT}]}$$

or

$$C_{XTAL} - C_{PCB} = \frac{C_{INT} + C_{EXT}}{2}$$

Solving for C_{EXT}, $C_{EXT} = 2 \times [C_{XTAL} - C_{PCB}] - C_{INT}$

For a crystal with a specified load capacitance of 18pF, using 9pF C_{XIN} and C_{XOUT}, and assuming 3pF for C_{PCB} gives:

$$C_{EXT} = 2 \times [18-3] - 3 = 27pF$$

Table 2. Supported Sampling Rates

STANDARD	SAMPLE RATE (ksps)
CENELEC band	400
FCC band	1200
ARIB band	1200
PRIME CENELEC band	250

System Reset

ZENO can be reset by asserting the RSTN pin low, by the power supply voltage monitor, or by a software command.

External Reset

During normal operation, ZENO can be placed into external reset mode by holding the RSTN pin low for a minimum of eight clock cycles. After the RSTN pin returns high, the MAXQ30E processors exit the reset state within eight clock cycles and begin program execution.

Voltage Monitor Reset

A system reset is generated if any of the supply voltages falls below the power fail reset voltages ($V_{DD12RST}$ $V_{DD33RST}$).

Software Reset

The modem firmware can initiate a reset in response to a command from the host processor.

Table 3. Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
CDVDD33_1	DVDD33_1	GND	Digital 3.3V supply bypass	100	nF
CDVDD33_1	DVDD33_1	GND	Digital 3.3V supply bypass	10	µF
CDVDD33_1	DVDD33_1	GND	Digital 3.3V supply bypass	1	µF
CDVDD12_0	DVDD12_0	GND	Digital 1.2V supply bypass	100	nF
CDVDD12_0	DVDD12_0	GND	Digital 1.2V supply bypass	1	µF
CAVDD33	AVDD33	GND	Analog 3.3V supply bypass	100	nF
CAVDD12	AVDD12	GND	Analog 1.2V supply bypass	100	nF
CAVDD12	AVDD12	GND	Analog 1.2V supply bypass	1	µF
CDVDD12_REG	DVDD12_REG	GND	Internal 1.2V LDO bypass	100	nF
CDVDD33_0	DVDD33_0	GND	Digital 3.3V supply bypass	100	nF
XTAL	XIN	XOUT	Crystal for internal oscillator	16	MHz
CXIN	XIN	GND	Crystal load capacitor	**	pF
CXOUT	XOUT	GND	Crystal load capacitor	**	pF

***The CXIN and CXOUT values depend on the crystal used and the PCB trace capacitance and must be determined at PCB design time.*

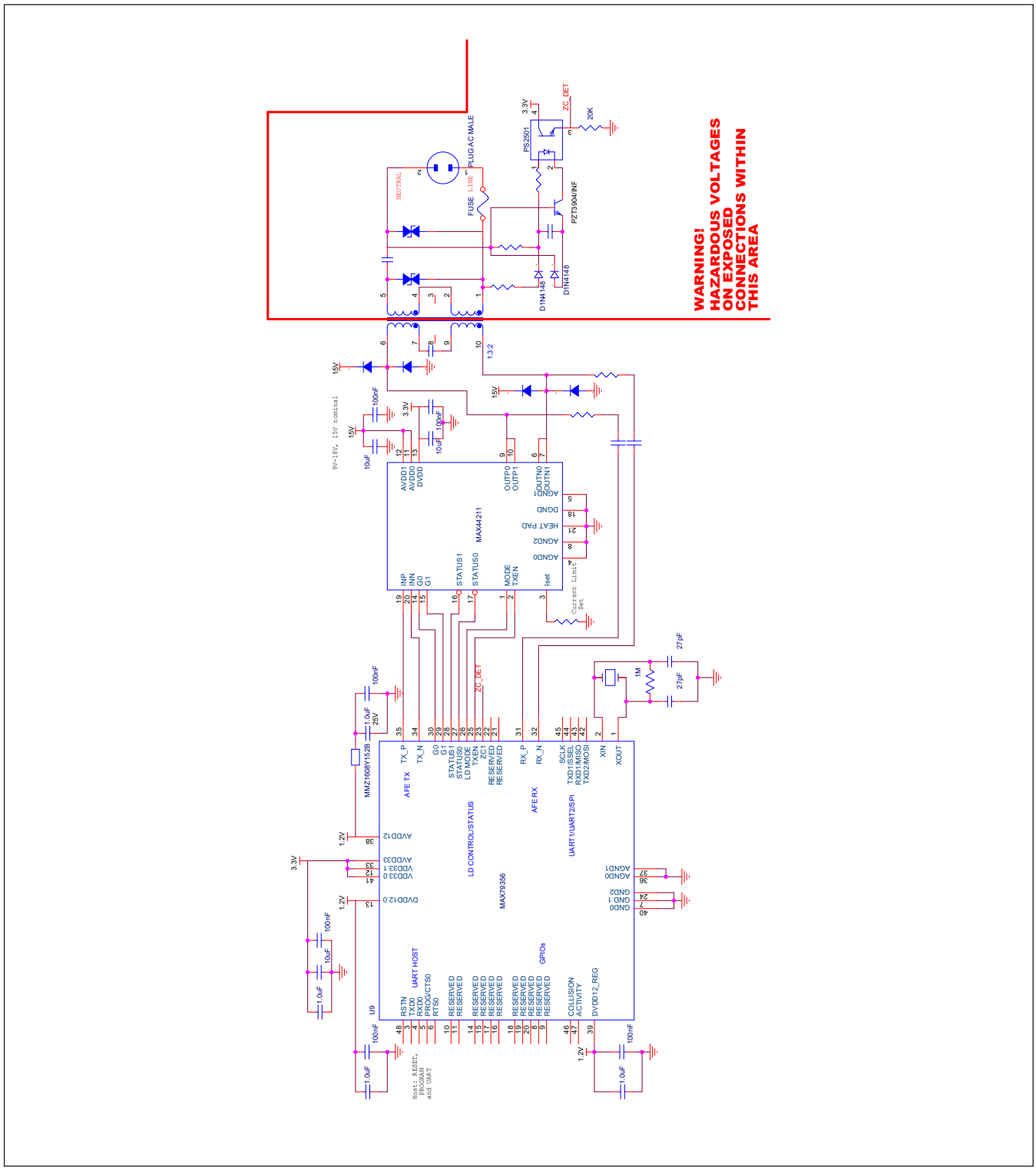


Figure 7. MAX79356 and MAX44211 Typical Configuration

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX79356ECM+	-40°C to +85°C	48 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 LQFP	C48+2	**21-0054**	**90-0093**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	3/16	Updated *Benefits and Features*, *Typical Operating Circuit*, *Electrical Characteristics*, *Block Diagram*, *Pin Configuration*, *Pin Description*, *Automatic Repeat Requestor (ARQ)*, *IPv6 over Low Power PAN (6LoWPAN)*, *Phase Detection Using AC Zero Crossing*, *UART*, *Serial Peripheral Interface (SPI)*, *ZENO Integrated Analog Front End (IAFE)*, Figure 4 caption, Figure 5 caption, *Voltage Monitor Reset*, Table 3, and Figure 7	1, 3, 6–8, 11–13, 15, 16
2	9/17	Updated *Typical Operating Circuit*, *Electrical Characteristics* and *Pin Description* tables, and Figure 7	1, 4, 8, 16

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