19-2586; Rev 2; 2/11

EVALUATION KIT AVAILABLE

Smallest TEC Power Drivers for Optical Modules

General Description

The MAX8520/MAX8521 are designed to drive thermoelectric coolers (TECs) in space-constrained optical modules. Both devices deliver ±1.5A output current and control the TEC current to eliminate harmful current surges. On-chip FETs minimize external components and high switching frequency reduces the size of external components.

The MAX8520/MAX8521 operate from a single supply and bias the TEC between the outputs of two synchronous buck regulators. This operation allows for temperature control without "dead zones" or other nonlinearities at low current. This arrangement ensures that the control system does not hunt when the set-point is very close to the natural operating point, requiring a small amount of heating or cooling. An analog control signal precisely sets the TEC current.

Both devices feature accurate, individually-adjustable heating current limit and cooling current limit along with maximum TEC voltage limit to improve the reliability of optical modules. An analog output signal monitors the TEC current. A unique ripple cancellation scheme helps reduce noise.

The MAX8520 is available in a 5mm x 5mm TQFN package and its switching frequency is adjustable up to 1MHz through an external resistor. The MAX8521 is also available in a 5mm x 5mm TQFN as well as space-saving 3mm x 3mm UCSP™ and 36-bump WLP (3mm x 3mm) packages, with a pin-selectable switching frequency of 500kHz or 1MHz.

Applications

SFF/SFP Modules

Fiber Optic Laser Modules

Fiber Optic Network Equipment

ATE

Biotech Lab Equipment

Pin Configurations appear at end of data sheet

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- **Circuit Footprint 0.31in²**
- **Low Profile Design**
- **On-Chip Power MOSFETs**
- **High-Efficiency Switch-Mode Design**
- **Ripple Cancellation for Low Noise**
- **Direct Current Control Prevents TEC Current Surges**
- **5% Accurate Adjustable Heating/Cooling Current Limits**
- **2% Accurate TEC Voltage Limit**
- **No Dead Zone or Hunting at Low Output Current**
- **ITEC Monitors TEC Current**
- **1% Accurate Voltage Reference**
- **Switching Frequency up to 1MHz**
- **Synchronization (MAX8521)**

Ordering Information

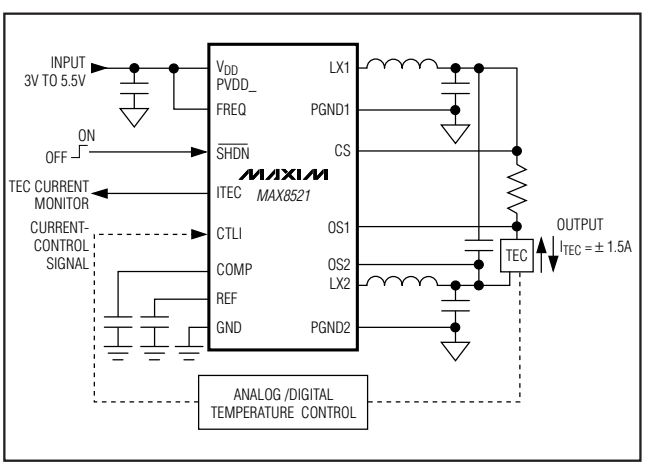
PART	TEMP RANGE	PIN-PACKAGE
MAX8520ETP+	-40°C to +85°C	20 TQFN-EP* 5mm x 5mm
MAX8521EBX	-40°C to +85°C	6 x 6 UCSP 3mm x 3mm
MAX8521ETP+	-40°C to +85°C	20 TQFN-EP* 5mm x 5mm
MAX8521EWX+	-40°C to +85°C	36 WLP** 3mm x 3mm

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

***Four center bumps depopulated.*

Typical Operating Circuit



Smallest TEC Power Drivers for Optical Modules

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
$\overline{SHDN}$, MAXV, MAXIP, MAXIN, CTLI to GND .....-0.3V to +6V
COMP, FREQ, OS1, OS2, CS, REF, ITEC to GND.....-0.3V to (V_{DD} + 0.3V)
PVDD1, PVDD2 to GND .....-0.3V to (V_{DD} + 0.3V)
PVDD1, PVDD2 to V_{DD}.....-0.3V to +0.3V
PGND1, PGND2 to GND .....-0.3V to +0.3V
COMP, REF, ITEC short to GND.....Indefinite
LX Current (Note 1) .....±2.25A LX Current
Continuous Power Dissipation (T_A = +70°C)
6 x 6 UCSP (derate 22mW/°C above +70°C) 1.75W
20-Pin 5mm x 5mm x 0.9mm TQFN (derate 20.8mW/°C above +70°C) (Note 2).....1.67W
36-Bump WLP (derate 22mW/°C above +70°C).....1.75W
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-Free (TQFN, WLP).....+260°C
Containing Lead (UCSP)..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: LX has internal clamp diodes to PGND and PVDD. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.
Note 2: Solders underside metal slug to PCB ground plane.

PACKAGE THERMAL CHARACTERISTICS (Note 3)

20 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....30°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W
6x6 UCSP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....65.5°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....0°C/W
36 WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....38°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....4°C/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{PVDD1} = V_{PVDD2} = $V_{\overline{SHDN}}$ = 5V, 1MHz mode (Note 4). PGND1 = PGND2 = GND, CTLI = MAXV = MAXIP = MAXIN = REF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Range	V_{DD}			3.0		5.5	V
Maximum TEC Current				±1.5			A
Reference Voltage	V_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = 150µA		1.485	1.500	1.515	V
Reference Load Regulation	ΔV_{REF}	V_{DD} = 3V to 5V, I_{REF} = 10µA to 1mA			1.2	5.0	mV
MAXIP/MAXIN Threshold Accuracy		V_{DD} = 5V	$V_{MAXI\_}$ = V_{REF}	140	150	160	mV
			$V_{MAXI\_}$ = V_{REF}/3	40	50	60	
		V_{DD} = 3V	$V_{MAXI\_}$ = V_{REF}	143	150	155	
			$V_{MAXI\_}$ = V_{REF}/3	45	50	55	
nFET On-Resistance	$R_{DS(ON-N)}$	V_{DD} = 5V, I = 0.2A			0.09	0.14	Ω
		V_{DD} = 3V, I = 0.2A			0.11	0.16	
pFET On-Resistance	$R_{DS(ON-P)}$	V_{DD} = 5V, I = 0.2A			0.14	0.23	Ω
		V_{DD} = 3V, I = 0.2A			0.17	0.30	
nFET Leakage	$I_{LEAK(N)}$	V_{LX} = V_{DD} = 5V, T_A = +25°C			0.03	4.00	µA
		V_{LX} = V_{DD} = 5V T_A = +85°C			0.3		
pFET Leakage	$I_{LEAK(P)}$	V_{LX} = 0V, T_A = +25°C			0.03	4.00	µA
		V_{LX} = 0V, T_A = +85°C			0.3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{PVDD1} = V_{PVDD2} = $V_{\overline{SHDN}}$ = 5V, 1MHz mode (Note 4). PGND1 = PGND2 = GND, CTLI = MAXV = MAXIP = MAXIN = REF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
No-Load Supply Current	$I_{DD(NO\ LOAD)}$	V_{COMP} = V_{REF} = 1.500V, V_{DD} = 5V	500kHz mode		11	14	mA
			1MHz mode		16	21	
		V_{COMP} = V_{REF} = 1.500V, V_{DD} = 3.3V	500kHz mode		8	11	
			1MHz mode		11	14	
Shutdown Supply Current	I_{DD-SD}	$\overline{SHDN}$ = GND, V_{DD} = 5V, (Note 5)			2	3	mA
Thermal Shutdown	$T_{SHUTDOWN}$	Hysteresis = 15°C			+165		°C
UVLO Threshold	V_{UVLO}	V_{DD} rising		2.50	2.65	2.80	V
		V_{DD} falling		2.40	2.55	2.70	
Internal Oscillator Switching Frequency	f_{SW-INT}	MAX8521, FREQ = V_{DD}, V_{DD} = 3V to 5V		0.8	1.0	1.2	MHz
		MAX8521, FREQ = GND, V_{DD} = 3V to 5V		0.4	0.5	0.6	
		MAX8520, R_{EXT} = 60kΩ, V_{DD} = 5V		0.8	1.0	1.2	
		MAX8520, R_{EXT} = 60kΩ, V_{DD} = 3V		0.76	0.93	1.10	
		MAX8520, R_{EXT} = 150kΩ, V_{DD} = 5V		0.4	0.5	0.6	
		MAX8520, R_{EXT} = 150kΩ, V_{DD} = 3V		0.36	0.46	0.56	
External Sync Frequency Range		25% < duty cycle < 75% (MAX8521 only)		0.7		1.2	MHz
LX_ Duty Cycle		(Note 6)		0		100	%
OS1, OS2, CS Input Current	I_{OS1}, I_{OS2}, I_{CS}	0V or V_{DD}		-100		+100	µA
$\overline{SHDN}$, FREQ Input Current	$I_{\overline{SHDN}}$, I_{FREQ}	0V or V_{DD}, FREQ applicable for the MAX8521 only		-5		+5	µA
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IL}	V_{DD} = 3V to 5.5V, FREQ applicable for the MAX8521 only				V_{DD} x 0.25	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IH}	V_{DD} = 3V to 5.5V, FREQ applicable for the MAX8521 only		V_{DD} x 0.75			V
MAXV Threshold Accuracy		V_{MAXV} = V_{REF} x 0.67, V_{OS1} to V_{OS2} = ±4V, V_{DD} = 5V		-2		+2	%
		V_{MAXV} = V_{REF} x 0.33, V_{OS1} to V_{OS2} = ±2V, V_{DD} = 3V		-3		+3	%
MAXV, MAXI_ Input Bias Current	$I_{MAXV-BIAS}$, I_{MAXI_-BIAS}	V_{MAXV} = $V_{MAXI\_}$ = 0.1V or 1.5V		-0.1		+0.1	µA
CTLI Gain	A_{CTLI}	V_{CTLI} = 0.5V to 2.5V (Note 7)		9.5	10.0	10.5	V/V
CTLI Input Resistance	R_{CTLI}	1MΩ terminated at REF		0.5	1.0	2.0	MΩ
Error-Amp Transconductance	g_m			50	100	160	µS
V_{ITEC} Accuracy		V_{OS1} to V_{CS} = ±100mV V_{OS1} = V_{DD}/2		-10		+10	%

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ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{PVDD1} = V_{PVDD2} = $V_{\overline{SHDN}}$ = 5V, 1MHz mode (Note 4). PGND1 = PGND2 = GND, CTLI = MAXV = MAXIP = MAXIN = REF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Input Supply Range	V_{DD}			3.0	5.5	V
Maximum TEC Current				±1.5		A
Reference Voltage	V_{REF}	V_{DD} = 3V to 5.5V, I_{REF} = 150µA		1.480	1.515	V
Reference Load Regulation	ΔV_{REF}	V_{DD} = 3V to 5V, I_{REF} = 10µA to 1mA			5	mV
MAXIP/MAXIN Threshold Accuracy		V_{DD} = 5V	$V_{MAXI\_}$ = V_{REF}	140	160	mV
			$V_{MAXI\_}$ = V_{REF}/3	40	60	
		V_{DD} = 3V	$V_{MAXI\_}$ = V_{REF}	143	155	
			$V_{MAXI\_}$ = V_{REF}/3	45	55	
nFET On-Resistance	$R_{DS(ON-N)}$	V_{DD} = 5V, I = 0.2A			0.14	Ω
		V_{DD} = 3V, I = 0.2A			0.16	
pFET On-Resistance	$R_{DS(ON-P)}$	V_{DD} = 5V, I = 0.2A			0.23	Ω
		V_{DD} = 3V, I = 0.2A			0.30	
No Load Supply Current	$I_{DD(NO\ LOAD)}$	V_{COMP} = V_{REF} = 1.500V, V_{DD} = 5V	500kHz mode		14	mA
			1MHz mode		21	
		V_{COMP} = V_{REF} = 1.500V, V_{DD} = 3.3V	500kHz mode		11	
			1MHz mode		14	
Shutdown Supply Current	I_{DD-SD}	$\overline{SHDN}$ = GND, V_{DD} = 5V (Note 5)			3	mA
UVLO Threshold	V_{UVLO}	V_{DD} Rising		2.50	2.80	V
		V_{DD} Falling		2.40	2.70	
Internal Oscillator Switching Frequency	f_{SW-INT}	MAX8521, FREQ = V_{DD}, V_{DD} = 3V to 5V		0.8	1.2	MHz
		MAX8521, FREQ = GND, V_{DD} = 3V to 5V		0.4	0.6	
		MAX8520, R_{EXT} = 60kΩ, V_{DD} = 5V		0.8	1.2	
		MAX8520, R_{EXT} = 60kΩ, V_{DD} = 3V		0.76	1.10	
		MAX8520, R_{EXT} = 150kΩ, V_{DD} = 5V		0.4	0.6	
		MAX8520, R_{EXT} = 150kΩ, V_{DD} = 3V		0.36	0.56	
External Sync Frequency Range		25% < duty cycle < 75% (MAX8521 only)		0.7	1.2	MHz
LX_ Duty Cycle		Note 6		0	100	%
OS1, OS2, CS Input Current	I_{OS1}, I_{OS2}, I_{CS}	0V or V_{DD}		-100	+100	µA
$\overline{SHDN}$, FREQ Input Current	$I_{\overline{SHDN}}$, I_{FREQ}	0V or V_{DD}, FREQ applicable for the MAX8521 only		-5	+5	µA
$\overline{SHDN}$, FREQ Input Low Voltage	V_{IL}	V_{DD} = 3V to 5.5V, FREQ applicable for the MAX8521 only			V_{DD} x 0.25	V
$\overline{SHDN}$, FREQ Input High Voltage	V_{IH}	V_{DD} = 3V to 5.5V, FREQ applicable for the MAX8521 only		V_{DD} x 0.75		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{PVDD1} = V_{PVDD2} = $V_{\overline{SHDN}}$ = 5V, 1MHz mode (Note 4). PGND1 = PGND2 = GND, CTLI = MAXV = MAXIP = MAXIN = REF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
MAXV Threshold Accuracy		V_{MAXV} = V_{REF} x 0.67, V_{OS1} to V_{OS2} = ±4V, V_{DD} = 5V	-2	+2	%
		V_{MAXV} = V_{REF} x 0.33, V_{OS1} to V_{OS2} = ±2V, V_{DD} = 3V	-3	+3	%
MAXV, MAXI_ Input Bias Current	$I_{MAXV-BIAS}$, I_{MAXI_-BIAS}	V_{MAXV} = $V_{MAXI\_}$ = 0.1V or 1.5V	-0.1	+0.1	µA
CTLI Gain	A_{CTLI}	V_{CTLI} = 0.5V to 2.5V (Note 7)	9.5	10.5	V/V
CTLI Input Resistance	R_{CTLI}	1MΩ terminated at REF	0.5	2.0	MΩ
Error-Amp Transconductance	g_m		50	160	µS
V_{ITEC} Accuracy		V_{OS1} to V_{CS} = ±100mV V_{OS1} = V_{DD}/2	-10	+10	%

Note 4: Enter 1MHz mode by connecting a 60kΩ resistor from FREQ to ground for the MAX8520, and connecting FREQ to V_{DD} for the MAX8521.

Note 5: Includes power FET leakage.

Note 6: Duty-cycle specification is guaranteed by design and not production tested.

Note 7: CTLI Gain is defined as:

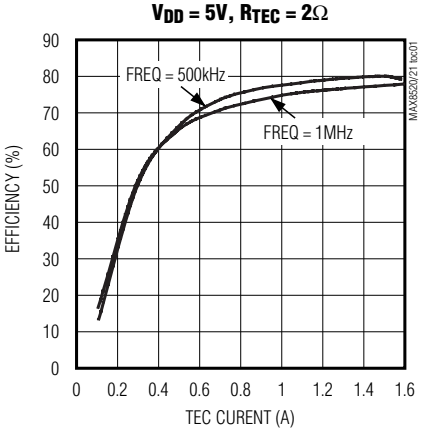
$$A_{CTLI} = \frac{\Delta V_{CTLI}}{\Delta(V_{OS1} - V_{CS})}$$

Note 8: Specifications to -40°C are guaranteed by design and not production tested.

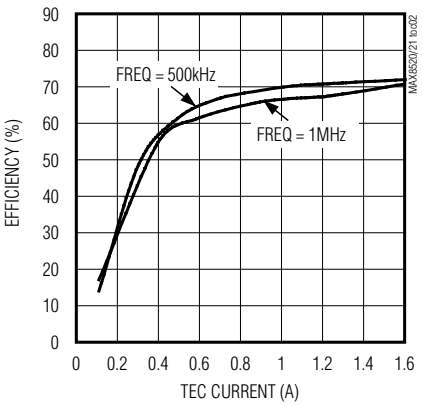
Typical Operating Characteristics

(V_{DD} = 5V, circuit of Figure 1, T_A = +25°C unless otherwise noted.)

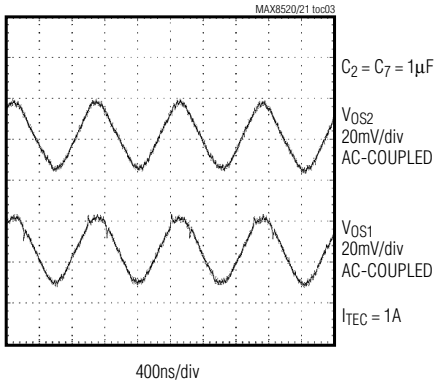
EFFICIENCY vs. TEC CURRENT
V_{DD} = 5V, R_{TEC} = 2Ω



EFFICIENCY vs. TEC CURRENT
V_{DD} = 3.3V, R_{TEC} = 1.3Ω



COMMON-MODE OUTPUT VOLTAGE RIPPLE

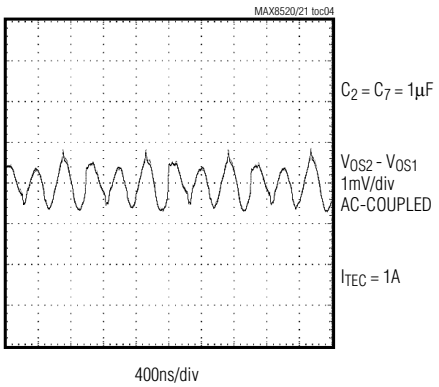


Smallest TEC Power Drivers for Optical Modules

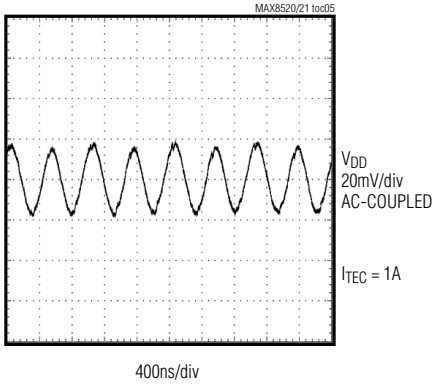
Typical Operating Characteristics (continued)

(V_{DD} = 5V, circuit of Figure 1, T_A = +25°C unless otherwise noted.)

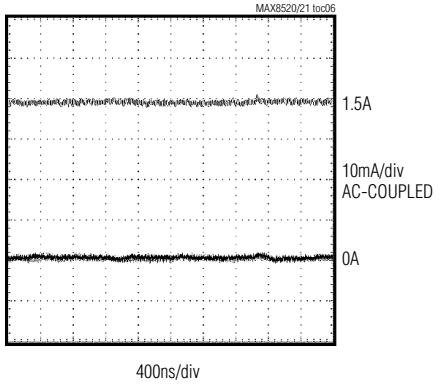
DIFFERENTIAL OUTPUT VOLTAGE RIPPLE



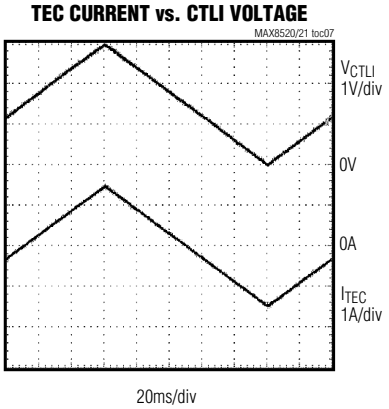
V_{DD} RIPPLE



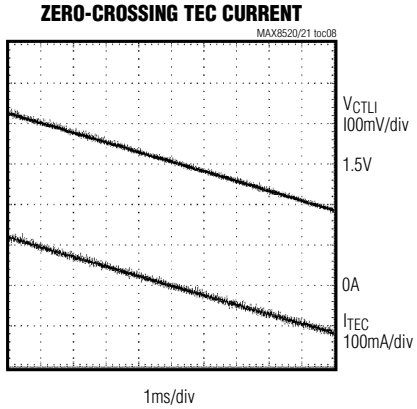
TEC CURRENT RIPPLE



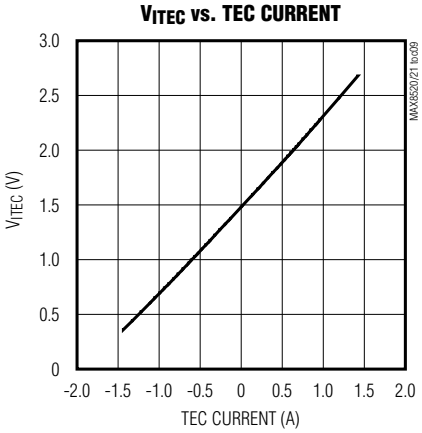
TEC CURRENT vs. CTLI VOLTAGE



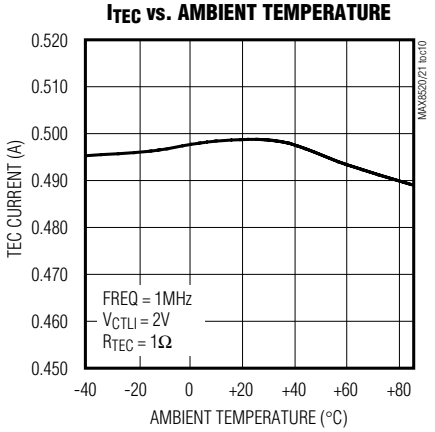
ZERO-CROSSING TEC CURRENT



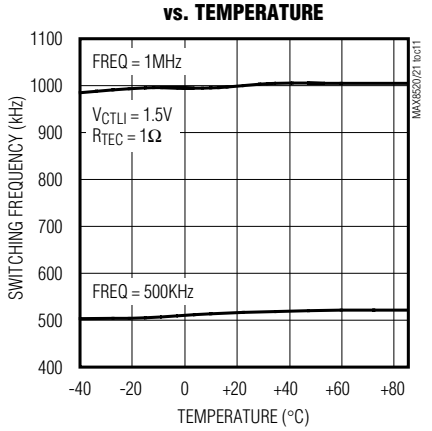
V_{ITEC} vs. TEC CURRENT



I_{TEC} vs. AMBIENT TEMPERATURE



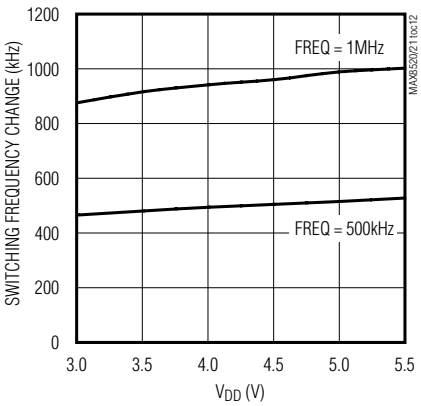
SWITCHING FREQUENCY vs. TEMPERATURE



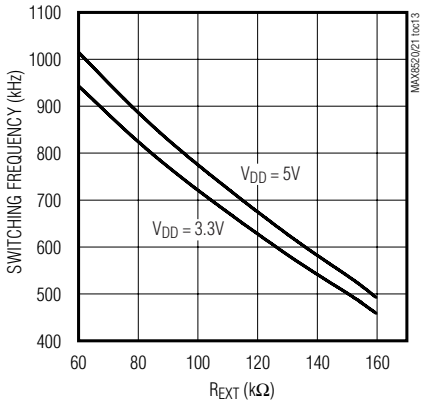
Typical Operating Characteristics (continued)

(V_{DD} = 5V, circuit of Figure 1, T_A = +25°C unless otherwise noted.)

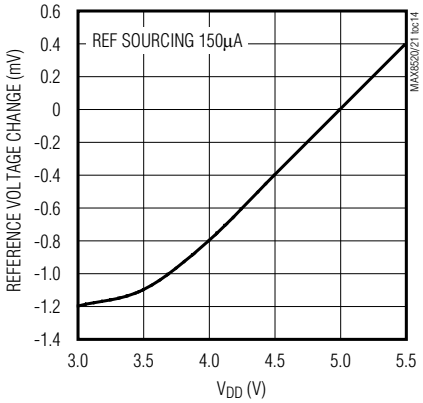
SWITCHING FREQUENCY CHANGE vs. V_{DD}



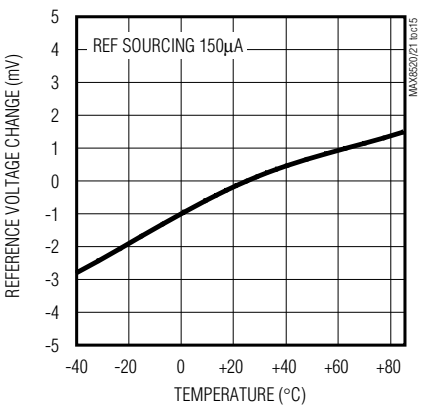
SWITCHING FREQUENCY vs. R_{EXT}



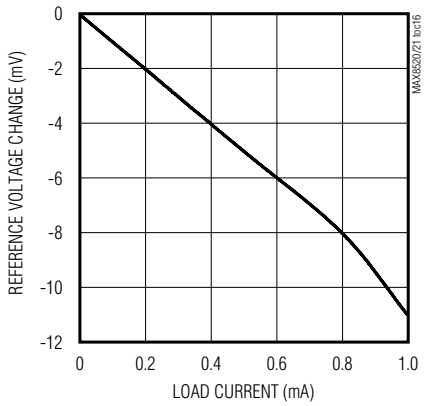
REFERENCE VOLTAGE CHANGE vs. V_{DD}



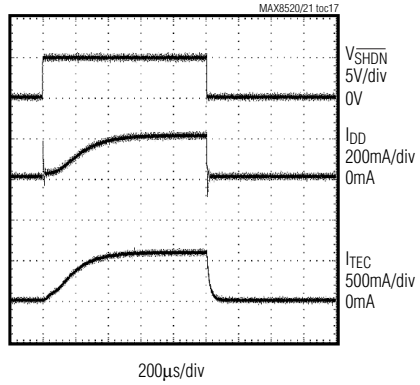
REFERENCE VOLTAGE CHANGE vs. TEMPERATURE



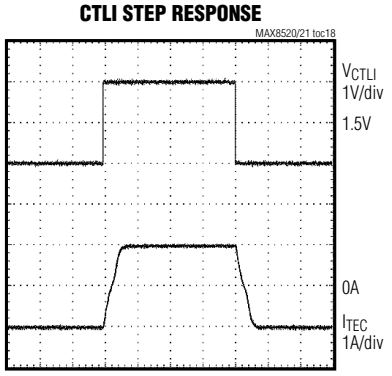
REFERENCE VOLTAGE CHANGE vs. LOAD CURRENT



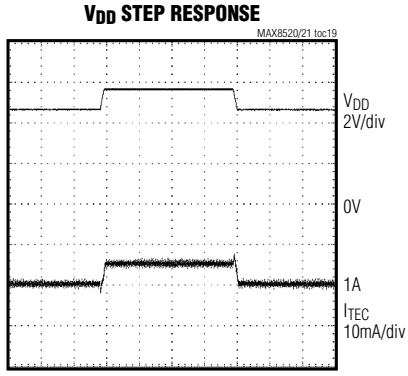
STARTUP AND SHUTDOWN WAVEFORMS



CTLI STEP RESPONSE



V_{DD} STEP RESPONSE

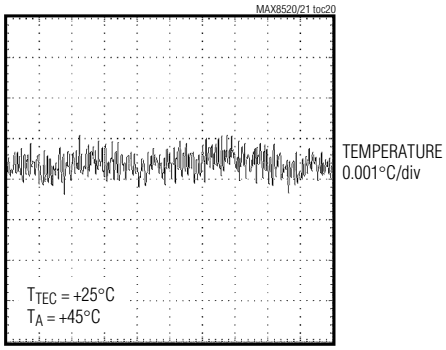


Smallest TEC Power Drivers for Optical Modules

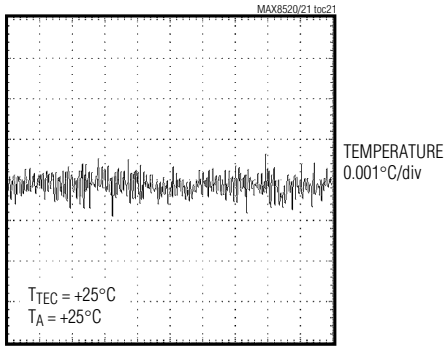
Typical Operating Characteristics (continued)

(V_{DD} = 5V, circuit of Figure 1, T_A = +25°C unless otherwise noted.)

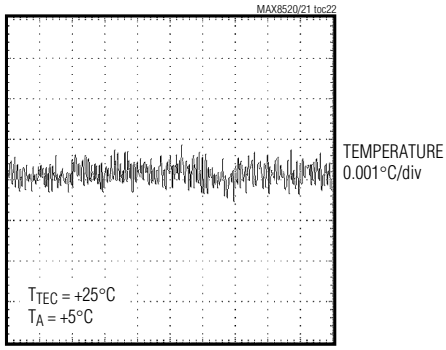
THERMAL STABILITY, COOLING MODE



THERMAL STABILITY, ROOM TEMPERATURE



THERMAL STABILITY, HEATING MODE



Pin Description

PIN		NAME	FUNCTION
TQFN	UCSP/WLP		
1	E1, E2	LX1	Inductor Connection. LX1 is high-impedance in shutdown.
2	D1, D2, D3	PGND1	Power Ground 1. Internal synchronous-rectifier ground connection. Connect all PGND pins together at power ground plane.
3	C1	$\overline{SHDN}$	Shutdown Control Input. Pull $\overline{SHDN}$ low to turn off PWM control and ITEC output.
4	C2	COMP	Current-Control Loop Compensation. See the *Compensation Capacitor* section.
5	B1	ITEC	TEC Current-Monitor Output. The ITEC output voltage is a function of the voltage across the TEC current-sense resistor. $V_{ITEC} = V_{REF} + 8 (V_{OS} - V_{CS})$. Keep capacitance on ITEC < 150pF.
6	A1	MAXIN	Maximum Negative TEC Current. Connect MAXIN to REF to set default negative current limit to - 150mV/R_{SENSE}. To lower this current limit, connect MAXIN to a resistor-divider network from REF to GND. The current limit will then be equal to -(V_{MAXIN}/V_{REF}) x (150mV/R_{SENSE}).
7	A2	MAXIP	Maximum Positive TEC Current. Connect MAXIP to REF to set default positive current limit to 150mV/R_{SENSE}. To lower this current limit, connect MAXIP to a resistor-divider network from REF to GND. The current limit will then be equal to (V_{MAXIP}/V_{REF}) x (150mV/R_{SENSE}).
8	A3	MAXV	Maximum Bipolar TEC Voltage. Connect MAXV to REF to set default maximum TEC voltage to V_{DD}. To lower this limit, connect MAXV to a resistor-divider network from REF to GND. The maximum TEC voltage is equal to 4 x V_{MAXV} or V_{DD}, whichever is lower.
9	A4	REF	1.50V Reference Output. Bypass REF to GND with a 0.1µF ceramic capacitor.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	UCSP/WLP		
10	A5	CTLI	TEC Current-Control Input. Sets TEC current. Center point is 1.50V (no TEC current). The current is given by: $I_{TEC} = (V_{OS1} - V_{CS}) / R_{SENSE} = (V_{CTLI} - 1.50) / (10 \times R_{SENSE})$. When $(V_{CTLI} - V_{REF}) > 0V$ then $V_{OS2} > V_{OS1} > V_{CS}$.
11	A6	GND	Analog Ground. Star connect to PGND at underside exposed pad for TQFN package.
12	B6	V_{DD}	Analog Supply Voltage Input. Bypass V_{DD} to GND with a 1µF ceramic capacitor.
13	C5	FREQ	For MAX8520: Analog FREQ Set Pin (see the *Switching Frequency* section).
			For MAX8521: Digital FREQ Selection Pin. Connect to V_{DD} for 1MHz operation, connect to GND for 500kHz operation. The PWM oscillator can synchronize to FREQ by switching at FREQ between 700kHz and 1.2MHz.
14	D6, D5, D4	PGND2	Power Ground 2. Internal synchronous rectifier ground connection. Connect all PGND pins together at the power ground plane.
15	E5, E6	LX2	Inductor Connection. LX2 is high-impedance in shutdown.
16	F5, F6	PVDD2	Power Input 2. Connect all PVDD inputs together at the V_{DD} power plane.
17	F4	CS	Current-Sense Input. The current through the TEC is monitored between CS and OS1. The maximum TEC current is given by $150mV/R_{SENSE}$ and is bipolar.
18	C6	OS2	Output Sense 2. OS2 senses one side of the differential TEC voltage. OS2 is a sense point, not a power output. OS2 discharges to ground in shutdown.
19	F3	OS1	Output Sense 1. OS1 senses one side of the differential TEC voltage. OS1 is a sense point, not a power output. OS1 discharges to ground in shutdown.
20	F1, F2	PVDD1	Power Input 1. Connect all PVDD inputs together at the V_{DD} power plane.
	B2, B5, C3, C4	GND2	Ground. Additional ground pads aid in heat dissipation. Short to either GND or PGND plane.
	B3, B4 E3, E4	N.C.	No Connect. Connect N.C. pads to GND2 to aid in heat dissipation.
—	—	EP	Exposed Paddle (TQFN Only). Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Smallest TEC Power Drivers for Optical Modules

Detailed Description

The MAX8520/MAX8521 TEC drivers consist of two switching buck regulators that operate together to directly control the TEC current. This configuration creates a differential voltage across the TEC, allowing bi-directional TEC current for controlled cooling and heating. Controlled cooling and heating allow accurate TEC temperature control to within 0.01°C. The voltage at CTLI directly sets the TEC current. An external thermal-control loop is typically used to drive CTLI. Figures 1 and 2 show examples of the thermal-control-loop circuit.

Ripple Cancellation

Switching regulators like those used in the MAX8520/MAX8521 inherently create ripple voltage on the output. The dual regulators in the MAX8520/MAX8521 switch in-phase and provide complementary in-phase duty cycles so ripple waveforms at the TEC are greatly reduced. This feature suppresses ripple currents and electrical noise at the TEC to prevent interference with the laser diode.

Switching Frequency

For the MAX8521, FREQ sets the switching frequency of the internal oscillator. With FREQ = GND, the oscillator frequency is set to 500kHz. The oscillator frequency is 1MHz when FREQ = V_{DD}.

For the MAX8520, connect a resistor (R_{EXT} in Figure 2) from FREQ to GND. Choose R_{EXT} = 60kΩ for 1MHz operation, and R_{EXT} = 150kΩ for 500KHz operation. For any intermediary frequency between 500kHz and 1MHz, use the following equation to find the value of R_{EXT} value needed for V_{DD} = 5V:

$$R_{EXT} = 90 \times \left(\frac{1}{fs} - \frac{1}{3} \right)$$

where R_{EXT} is the resistance given in kΩ, and fs is the desired frequency given in MHz. Note that for V_{DD} < 5V, the frequency is reduced slightly, to the extent of about 7% when V_{DD} reaches 3V. This should be taken into consideration when selecting the value for R_{EXT} at known supply voltage.

Voltage and Current-Limit Setting

Both the MAX8520 and MAX8521 provide control of the maximum differential TEC voltage. Applying a voltage to MAXV limits the maximum voltage across the TEC. The voltage at MAXIP and MAXIN sets the maximum positive and negative current through the TEC. These current limits can be independently controlled.

Table 1. TEC Connection for Figure 1

TEC Connection	Thermistor
Heating Mode	PTC
Cooling Mode	NTC

Table 2. TEC Connection for Figure 2

TEC Connection	Thermistor
Heating Mode	NTC
Cooling Mode	PTC

Current Monitor Output

ITEC provides a voltage output proportional to the TEC current (I_{TEC}). See the *Functional Diagram* for more detail:

$$V_{ITEC} = 1.5V + (8 \times (VOS1 - VCS))$$

Reference Output

The MAX8520/MAX8521 include an on-chip voltage reference. The 1.50V reference is accurate to 1% over temperature. Bypass REF with 0.1µF to GND. REF can be used to bias an external thermistor for temperature sensing as shown in Figures 1 and 2.

Thermal and Fault-Current Protection

The MAX8520/MAX8521 provide fault-current protection in either FETs by turning off both high-side and low-side FETs when the peak current exceeds 3A in either FETs. In addition, thermal-overload protection limits the total power dissipation in the chip. When the device's die junction temperature exceeds +165°C, an on-chip thermal sensor shuts down the device. The thermal sensor turns the device on again after the junction temperature cools down by +15°C.

Design Procedures

Duty-Cycle Range Selection

By design, the MAX8520/MAX8521 are capable of operating from 0% to 100% duty cycle, allowing both LX outputs to enter dropout. However, as the LX pulse width narrows, accurate duty-cycle control becomes difficult. This can result in a low-frequency noise appearing at the TEC output (typically in the 20kHz to 50kHz range). While this noise is typically filtered out by the low thermal-loop bandwidth, for best result, operate the PWM with a pulse width greater than 200ns. For 500kHz application, the recommended duty-cycle range is from 10% to 90%. For 1MHz application, it is from 20% to 80%.

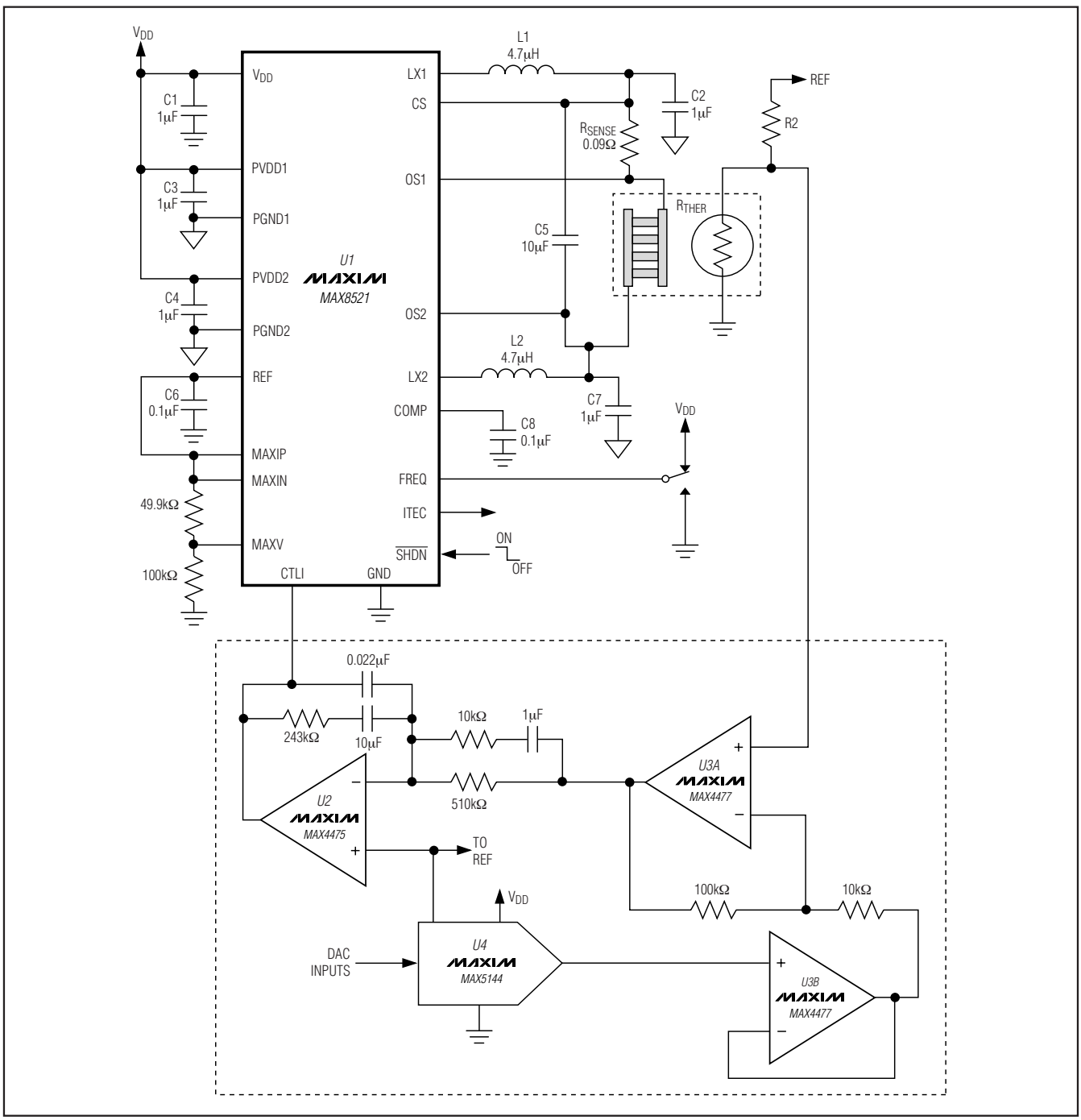


Figure 1. MAX8521 Typical Application Circuit

Smallest TEC Power Drivers for Optical Modules

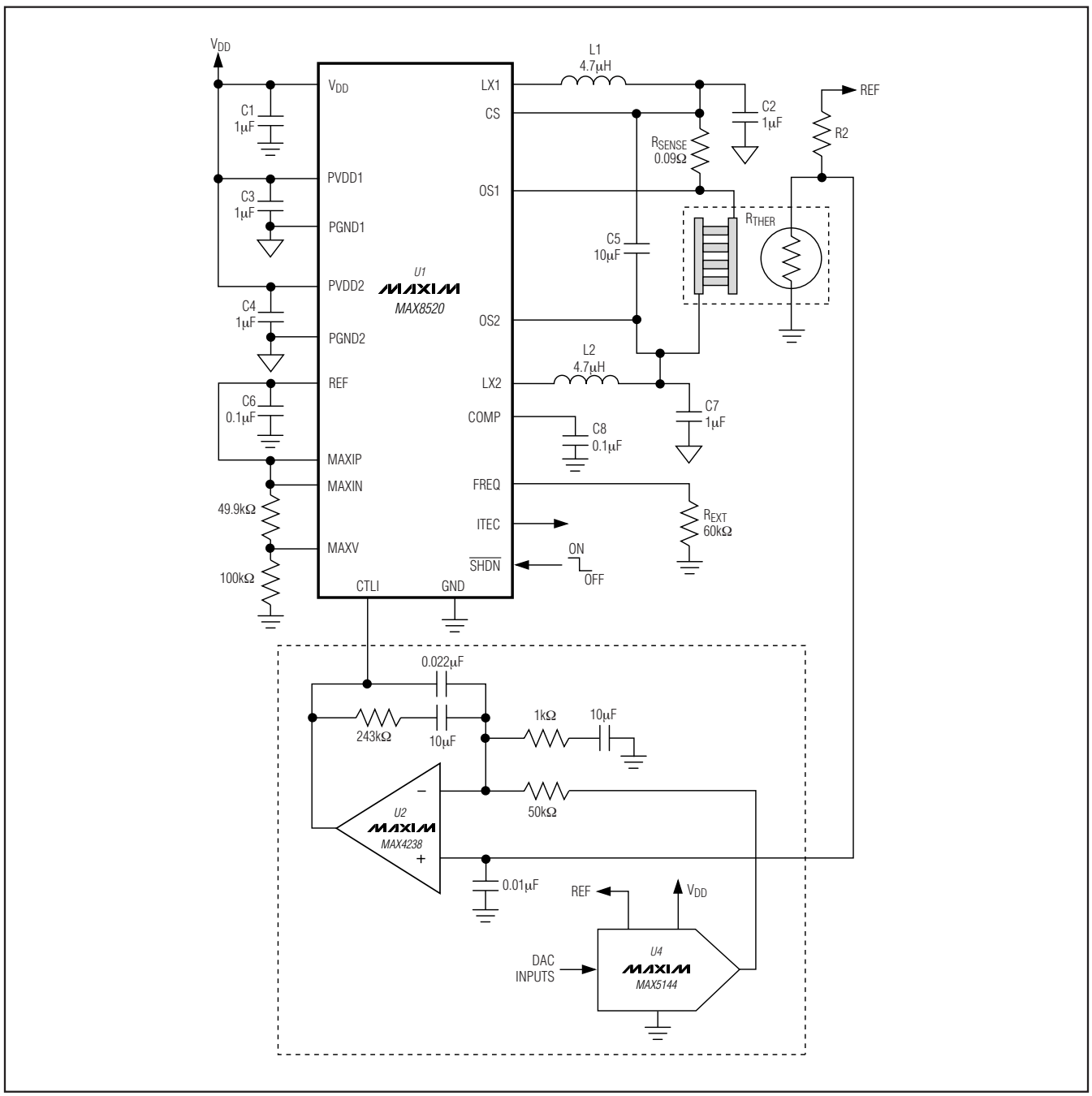


Figure 2. Typical Application Circuit for the MAX8520 with Reduced Op-Amp Count Configuration

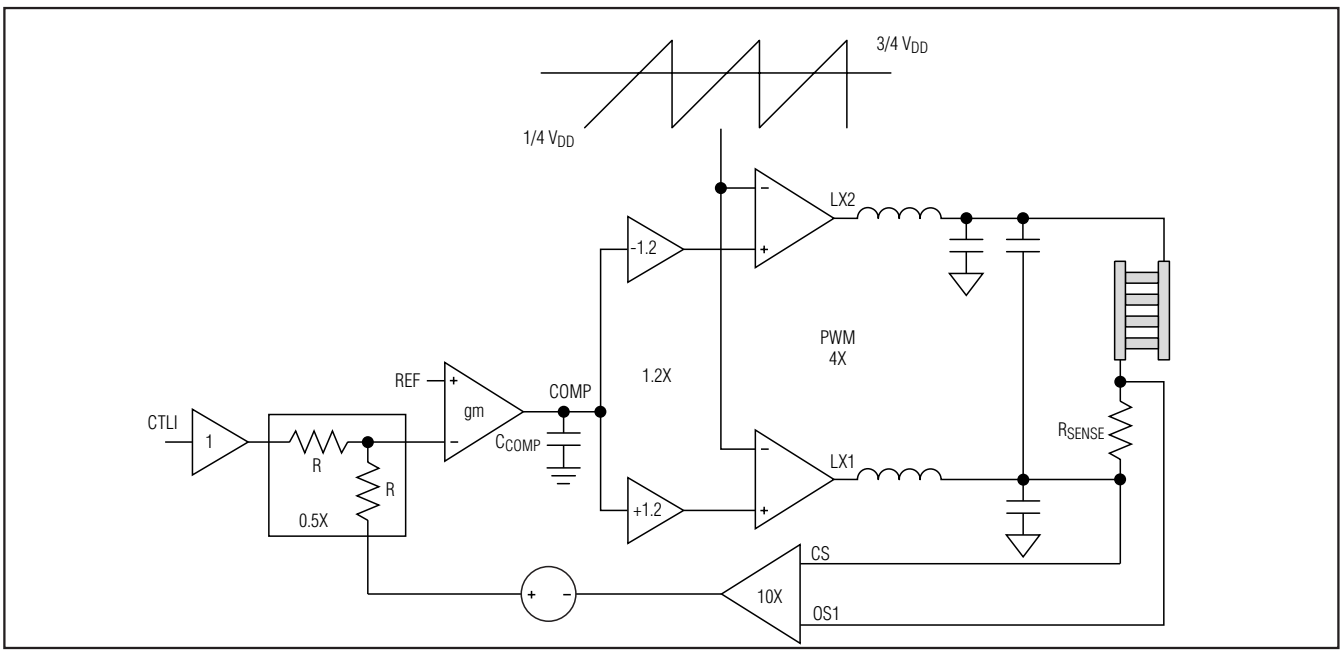


Figure 3. Functional Diagram of the Current-Control Loop

Inductor Selection

The MAX8520/MAX8521 dual buck converters operate in-phase and in complementary mode to drive the TEC differentially in a current-mode control scheme. At zero TEC current, the differential voltage is zero, hence the outputs with respect to GND are equal to half of V_{DD}. As the TEC current demand increases, one output will go up and the other will go down from the initial point of $0.5V_{DD}$ by an amount equal to $0.5 \times V_{TEC}$ ($V_{TEC} = I_{TEC} \times R_{TEC}$). Therefore, the operating duty cycle of each buck converter depends on the operating I_{TEC} and R_{TEC}. Since inductor current calculation for heating and cooling are identical, but reverse in polarity, the calculation only needs to be carried out for either one.

For a given inductor, and input voltage, the maximum inductor ripple current happens when the duty cycle is at 50%. Therefore, the inductor should be calculated at 50% duty cycle to find the maximum ripple current. The maximum desired ripple current of a typical standard buck converter is in the range of 20% to 40% of the maximum load. The higher the value of the inductor, the lower the ripple current. However, the size will be physically larger. For the TEC driver the thermal loop is inherently slow, so the inductor can be larger for lower ripple current for better noise and EMI performance. Picking an inductor to yield ripple current of 10% to 20% of the maximum TEC current is a good starting point.

Calculate the inductor value as follows:

$$L = \frac{(0.25 \times V_{DD})}{LIR \times I_{TEC(MAX)} \times fs}$$

where LIR is the selected inductor ripple-current ratio, $I_{TEC(MAX)}$ is the maximum TEC current, and fs is the switching frequency

As an example, for V_{DD} = 3.3V, LIR = 12%, and fs = 1MHz, L = 4.58µH

Even though each inductor ripple current is at its maximum at 50% duty cycle (zero TEC current), the ripple cancels differentially because each is equal and in-phase.

Output Filter Capacitor Selection

Common-Mode Filter Capacitors

The common-mode filter capacitors (C2 and C7 of Figure 1) are used as filter capacitors to ground for each output. The output ripple voltage depends on the capacitance, the ESR of these capacitors, and the inductor ripple current. Ceramic capacitors are recommended for their low ESR and impedance at high frequency.

Smallest TEC Power Drivers for Optical Modules

The output common-mode ripple voltage can be calculated as follows:

$$V_{RIPPLEpk\text{-}pk} = LIR \times I_{TEC(MAX)} (ESR + 1/8 \times C \times fs)$$

A 1µF ceramic capacitor with ESR of 10 mΩ with LIR = 12% and $I_{TEC(MAX)}$ = 1.5A will result in $V_{RIPPLE(P\text{-}P)}$ of 24.3mV. For size-constraint application, the capacitor can be made smaller at the expense of higher ripple voltage. However, the capacitance must be high enough so that the LC resonant frequency is less than 1/5 the switching frequency:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

where f is the resonant frequency of the output filter.

Differential Mode Filter Capacitor

The differential-mode filter capacitor (C5 in Figure 1) is used to bypass differential ripple current through the TEC as the result of unequal duty cycle of each output. This happens when the TEC current is not at zero. As TEC current increases from zero, both outputs move away from the 50% duty-cycle point complementarily. The common-mode ripple decreases, but the differential ripple does not cancel perfectly, and there will be a resulting differential ripple. The maximum value happens when one output is at 75% duty cycle and the other is at 25% duty cycle. At this operating point, the differential ripple is equal to 1/2 of the maximum common-mode ripple. The TEC ripple current determines the TEC performance, because the maximum temperature differential that can be created between the terminals of the TEC depends on the ratio of ripple current and DC current. The lower the ripple current, the closer to the ideal maximum. The differential-mode capacitor provides a low-impedance path for the ripple current to flow, so that the TEC ripple current is greatly reduced. The TEC ripple current then can be calculated as follows:

$$I_{TEC(RIPPLE)} = (0.5 \times LIR \times I_{TEC(MAX)}) \times (Z_{C5})/(R_{TEC} + R_{SENSE} + Z_{C5})$$

where Z_{C5} is the impedance of C5 at twice the switching frequency, R_{TEC} is the TEC equivalent resistance, and R_{SENSE} is the current-sense resistor.

Decoupling Capacitor Selection

Decouple each power supply input (V_{DD}, PVDD1, PVDD2) with a 1µF ceramic capacitor close to the supply pins. In applications with long distances between the source supply and the MAX8520/MAX8521, additional bypassing may be needed to stabilize the input supply. In such cases, a low-ESR electrolytic or ceramic capacitor of 100µF or more at V_{DD} is sufficient.

Compensation Capacitor

A compensation capacitor is needed to ensure current-control-loop stability (see Figure 3). Select the capacitor so that the unity-gain bandwidth of the current-control loop is less than or equal to 10% the resonant frequency of the output filter:

$$C_{COMP} \geq \left(\frac{g_m}{f_{BW}}\right) \times \left(\frac{24 \times R_{SENSE}}{2\pi(R_{SENSE} \times R_{TEC})}\right)$$

where:

f_{BW} = Unity-gain bandwidth frequency, less than or equal to 10% the output filter resonant frequency

g_m = Loop transconductance, typically 100µA/V

C_{COMP} = Value of the compensation capacitor

R_{TEC} = TEC series resistance, use the minimum resistance value

R_{SENSE} = Sense resistor

Setting Voltage and Current Limits

Certain TEC parameters must be considered to guarantee a robust design. These include maximum positive current, maximum negative current, and the maximum voltage allowed across the TEC. These limits should be used to set the MAXIP, MAXIN, and MAXV voltages.

Setting Max Positive and Negative TEC Current

MAXIP and MAXIN set the maximum positive and negative TEC currents, respectively. The default current limit is ±150mV/R_{SENSE} when MAXIP and MAXIN are connected to REF. To set maximum limits other than the defaults, connect a resistor-divider from REF to GND to set $V_{MAXI\_}$. Use resistors in the 10kΩ to 100kΩ range. $V_{MAXI\_}$ is related to ITEC by the following equations:

$$V_{MAXIP} = 10(I_{TECP(MAX)} \times R_{SENSE})$$

$$V_{MAXIN} = 10(I_{TECN(MAX)} \times R_{SENSE})$$

where $I_{TECP(MAX)}$ is the maximum positive TEC current and $I_{TECN(MAX)}$ is the negative maximum TEC current. Positive TEC current occurs when CS is less than OS1:

$$I_{TEC} \times R_{SENSE} = OS1 - CS$$

when I_{TEC} > 0A.

$$I_{TEC} \times R_{SENSE} = CS - OS1$$

when I_{TEC} < 0A.

Take care not to exceed the positive or negative current limit on the TEC. Refer to the manufacturer's data sheet for these limits.

Setting Max TEC Voltage

Apply a voltage to the MAXV pin to control the maximum differential TEC voltage. V_{MAXV} can vary from 0V to V_{REF}. The voltage across the TEC is four times V_{MAXV} and can be positive or negative:

$|V_{OS1} - V_{OS2}| = 4 \times V_{MAXV}$ or V_{DD}, whichever is lower

Set V_{MAXV} with a resistor-divider between REF and GND using resistors from 10kΩ to 100kΩ. V_{MAXV} can vary from 0V to V_{REF}.

Control Inputs/Outputs

Output Current Control

The voltage at CTLI directly sets the TEC current. CTLI is typically driven from the output of a temperature control loop. The transfer function relating current through the TEC (I_{TEC}) and V_{CTLI} is given by:

$$I_{TEC} = (V_{CTLI} - V_{REF})/(10 \times R_{SENSE})$$

where V_{REF} is 1.50V and:

$$ITEC = (V_{OS1} - V_{CS})/R_{SENSE}$$

CTLI is centered around REF (1.50V). I_{TEC} is zero when CTLI = 1.50V. When $V_{CTLI} > 1.50V$ the current flow is from OS2 to OS1. The voltages on the pins relate as follows:

$$V_{OS2} > V_{OS1} > V_{CS}$$

The opposite applies when $V_{CTLI} < 1.50V$ current flows from OS1 to OS2:

$$V_{OS2} < V_{OS1} < V_{CS}$$

Shutdown Control

The MAX8520/MAX8521 can be placed in a power-saving shutdown mode by driving $\overline{SHDN}$ low. When the MAX8520/MAX8521 are shut down, the TEC is off (OS1 and OS2 decay to GND) and supply current is reduced to 2mA (typ).

ITEC Output

ITEC is a status output that provides a voltage proportional to the actual TEC current. $V_{ITEC} = V_{REF}$ when TEC current is zero. The transfer function for the ITEC output is:

$$V_{ITEC} = 1.50V + 8 \times (V_{OS1} - V_{CS})$$

Use ITEC to monitor the cooling or heating current through the TEC. For stability keep the load capacitance on ITEC to less than 150pF.

Applications Information

The MAX8520/MAX8521 typically drive a thermo-electric cooler inside a thermal-control loop. TEC drive polarity and power are regulated based on temperature information read from a thermistor or other temperature-measuring device to maintain a stable control temperature. Temperature stability of +0.01°C can be achieved with carefully selected external components.

There are numerous ways to implement the thermal loop. Figures 1 and 2 show designs that employ precision op amps, along with a DAC or potentiometer to set the control temperature. The loop can also be implemented digitally, using a precision A/D to read the thermistor or other temperature sensor, a microcontroller to implement the control algorithm, and a DAC (or filtered-PWM signal) to send the appropriate signal to the MAX8520/MAX8521 CTLI input. Regardless of the form taken by the thermal-control circuitry, all designs are similar in that they read temperature, compare it to a set-point signal, and then send an error-correcting signal to the MAX8520/MAX8521 that moves the temperature in the appropriate direction.

PCB Layout and Routing

High switching frequencies and large peak currents make PCB layout a very important part of design. Good design minimizes excessive EMI and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow these guidelines for good PCB layout:

1) Place decoupling capacitors as close to the IC pins as possible.

2) Keep a separate power ground plane, which is connected to PGND1 and PGND2. PVDD1, PVDD2, PGND1 and PGND2 are noisy points. Connect decoupling capacitors from PVDD_ to PGND_ as direct as possible. Output capacitors C2, C7 returns are connected to PGND plane.

3) Connect a decoupling capacitor from V_{DD} to GND. Connect GND to a signal ground plane (separate from the power ground plane above). Other V_{DD} decoupling capacitors (such as the input capacitor) need to be connected to the PGND plane.

4) Connect GND and PGND_ pins together at a single point, as close as possible to the chip.

5) Keep the power loop, which consists of input capacitors, output inductors and capacitors, as compact and small as possible.

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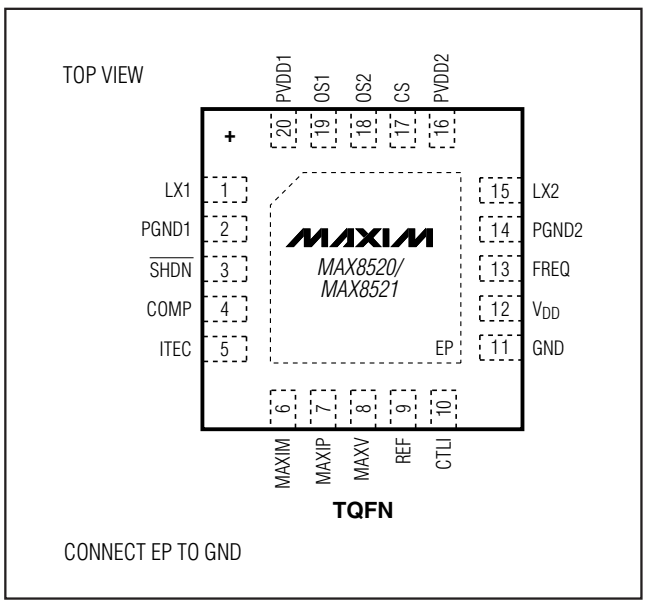
6) To ensure high DC-loop gain and minimum loop error, keep the board layout adjacent to the negative input pin of the integrator (U2 in Figure1) clean and free of moisture. Any contamination or leakage current into this node can act to lower the DC gain of the integrator which can degrade the accuracy of the thermal loop. If space is available, it can also be helpful to surround the negative input node of the integrator with a grounded guard ring.

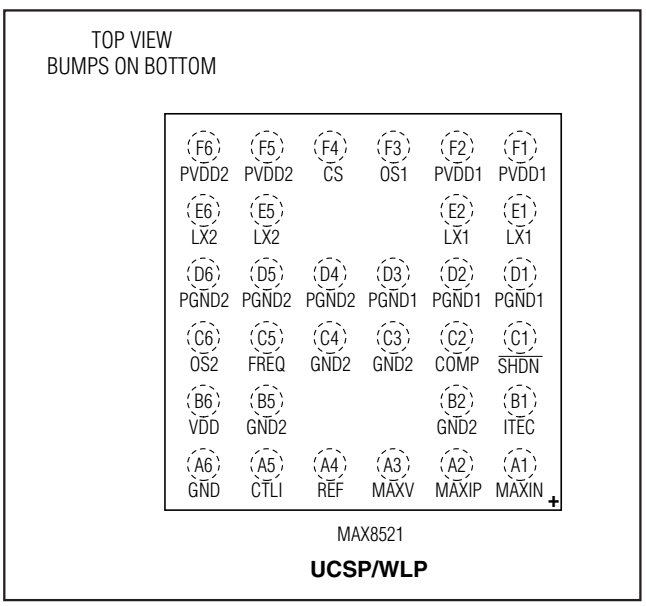
Refer to the MAX8520/MAX8521 evaluation kit for a PCB layout example.

Chip Information

PROCESS: BiCMOS

Pin Configurations



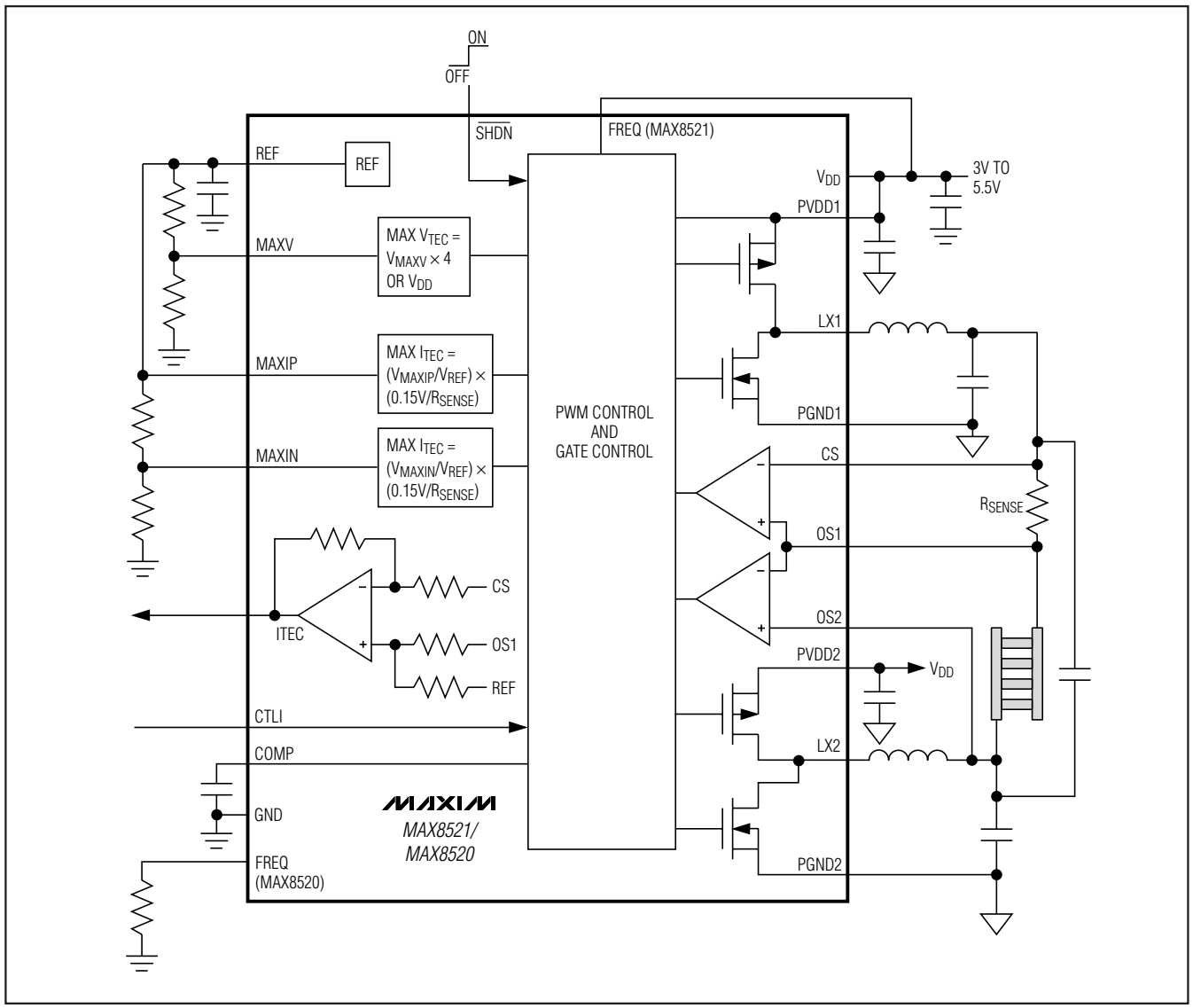


Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2055+4	**21-0140**	**90-0009**
6 x 6 UCSP	B36-2	**21-0082**	Refer to **Application Note 1891**
36 WLP	W363A3+2	**21-0024**	Refer to **Application Note 1891**

Functional Diagram



Smallest TEC Power Drivers for Optical Modules

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/02	Initial release	—
1	12/08	Added WLP package to *Ordering Information*, updated *Electrical Characteristics*, *Absolute Maximum Ratings*, *Pin Description*, and *Package Information*.	1–5, 8, 9, 15–18
2	2/11	Update *Absolute Maximum Ratings*, add WLP to *Pin Description*, update style	1–5, 8, 9, 11, 14–18

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