19-3141; Rev 1; 6/05

EVALUATION KIT AVAILABLE

MAXIM

Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

General Description

The MAX8537/MAX8539 controllers provide a complete power-management solution for both double-data-rate (DDR) and combiner supplies. The MAX8537 and MAX8539 are configured for out-of-phase and in-phase DDR power-supply operations, respectively, and generate three outputs: the main memory voltage (V_{DDQ}), the tracking sinking/sourcing termination voltage (V_{TT}), and the termination reference voltage (V_{TTR}). The MAX8538 is configured as a dual out-of-phase controller for point-of-load supplies. Each buck controller can source or sink up to 25A of current, while the termination reference can supply up to 15mA output.

The MAX8537/MAX8538/MAX8539 use constant-frequency voltage-mode architecture with operating frequencies of 200kHz to 1.4MHz. An internal high-bandwidth (25MHz) operational amplifier is used as an error amplifier to regulate the output voltage. This allows fast transient response, reducing the number of output capacitors. An all-N-FET design optimizes efficiency and cost. The MAX8537/MAX8538/MAX8539 have a 1% accurate reference. The second synchronous buck controller in the MAX8537/MAX8539 and the VTTR amplifier generate 1/2 V_{DDQ} voltage for V_{TT} and V_{TTR}, and track the V_{DDQ} within ±1%.

This family of controllers uses a high-side current-sense architecture for current limiting. ILIM pins allow the setting of an adjustable, lossless current limit for different combinations of load current and R_{DSON}. Alternately, more accurate overcurrent limit is achieved by using a sense resistor in series with the high-side FET. Overvoltage protection is achieved by latching off the high-side MOSFET and latching on the low-side MOSFET when the output voltage exceeds 17% of its set output. Independent enable, power-good, and soft-start features enhance flexibility.

Applications

DDR Memory Power Supplies
Notebooks and Desknotes
Servers and Storage Systems
Broadband Routers
XDSL Modems and Routers
Power DSP Core Supplies
Power Combiner in Advanced VGA Cards
Networking Systems
RAMBUS Memory Power Supplies

Features

- **MAX8537/MAX8539: Complete DDR Supplies**
- **MAX8538: Dual Nontracking Controller**
- **Out-of-Phase (MAX8537/MAX8538) or In-Phase (MAX8539) Operation**
- **4.5V to 23V Wide Input Range (Operate Down to 1.8V Input with External 5V Supply)**
- **Tracking Supply Maintains V_{TT} = V_{TTR} = 1/2 V_{DDQ}**
- **Adjustable Output from 0.8V to 3.6V with 1% Accuracy**
- **VTTR Reference Sources and Sinks Up to 15mA**
- **200kHz to 1.4MHz Adjustable Switching Frequency**
- **All-Ceramic Design Achievable**
- **>90% Efficiency**
- **Independent POK_ and EN_**
- **Adjustable Soft-Start and Soft-Stop for Each Output**
- **Lossless Adjustable-Hiccup Current Limit**
- **Output Overvoltage Protection**
- **28-Pin QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OPERATION
MAX8537EEI	-40°C to +85°C	28 QSOP	Out-of-phase tracking
MAX8537EEI+	-40°C to +85°C	28 QSOP	Out-of-phase tracking
MAX8538EEI	-40°C to +85°C	28 QSOP	Out-of-phase nontracking
MAX8538EEI+	-40°C to +85°C	28 QSOP	Out-of-phase nontracking
MAX8539EEI	-40°C to +85°C	28 QSOP	In-phase tracking
MAX8539EEI+	-40°C to +85°C	28 QSOP	In-phase tracking

+Denotes lead-free package.

Pin Configurations appear at end of data sheet.

Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +25V
AVL, VL to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
FB_, EN_, POK_ to GND .....-0.3V to +6V
REFIN, VTTR, FREQ, SS_, COMP_ to GND ....-0.3V to (AVL + 0.3V)
BST_, ILIM_ to GND .....-0.3V to +30V
DH1 to LX1 .....-0.3V to (BST1 + 0.3V)
DH2 to LX2 .....-0.3V to (BST2 + 0.3V)
LX_ to BST_ .....-6V to +0.3V
LX_ to GND .....-2V to +25V
DL_ to PGND .....-0.3V to (VL + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C).....860mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 12V, EN_ = VL, BST_ = 6V, LX_ = 1V, VL load = 0mA, C_{VL} = 10µF (ceramic), REFIN = 1.25V, PGND = AGND = FB_ = ILIM_ = 0V, C_{SS} = 10nF, C_{VTTR} = 1µF, R_{FREQ} = 20kΩ, DH_ = open, DL_ = open, POK_ = open, circuit of Figure 1, **T_A = 0°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
V+ Operating Range	VL regulator drops out below 5.5V (Note 1)	4.5		23.0	V
V+/VL Operating Range	VL is externally generated (Note 1)	4.5		5.5	V
V+ Operating Supply Current	IL(VL) = 0, FB_ forced 50mV above threshold		3.5	7	mA
V+ Standby Supply Current	IL(VL) = 0, BST_ = VL, EN = LX_ = FB_ = 0V		350	700	µA
VL REGULATOR					
Output Voltage	5.5V < V+ < 23V, 1mA < I_{LOAD} < 70mA	4.75	5	5.25	V
VL Undervoltage-Lockout Trip Level	Rising edge, hysteresis = 550mV (typ) (trip level is typically 85% of VL)	4.18	4.3	4.42	V
Output Current	This is for gate current of DL_ /DH_ drivers, C(VL) = 1µF/10mA ceramic capacitor			70	mA
Thermal Shutdown	Rising temperature, typical hysteresis = 10°C		+160		°C
CURRENT-LIMIT THRESHOLD (all current limits are tested at V+ = VL = 4.5V and 5.5V)					
ILIM Sink Current	ILIM_ = LX - 200mV, 1.8V < LX < 23V, BST = LX +5V	180	200	220	µA
SOFT-START					
Soft-Start Source Current	SS_ = 100mV	-7	-5	-3	µA
Soft-Start Sink Current	SS_ = 0.8 or REFIN	3	5	7	µA
Soft-Start Full-Scale Voltage			0.8 or REFIN		V
FREQUENCY					
Low End of Range	R_{FREQ} = 100kΩ, V+ = VL = 5V	160	200	240	kHz
Intermediate Range	R_{FREQ} = 20kΩ, V+ = VL = 5V	800	1000	1200	kHz
High End of Range	R_{FREQ} = 14.3kΩ, V+ = VL = 5V	1120	1400	1680	kHz
Maximum Duty Cycle	R_{FREQ} = 100kΩ	95			%
	R_{FREQ} = 20kΩ	80			
	R_{FREQ} = 14.3kΩ	72			

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 12V, EN_ = VL, BST_ = 6V, LX_ = 1V, VL load = 0mA, C_{VL} = 10µF (ceramic), REFIN = 1.25V, PGND = AGND = FB_ = ILIM_ = 0V, C_{SS} = 10nF, C_{VTTR} = 1µF, R_{FREQ} = 20kΩ, DH_ = open, DL_ = open, POK_ = open, circuit of Figure 1, **T_A = 0°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Duty Cycle	R_{FREQ} = 100kΩ		2.4	4	%
	R_{FREQ} = 20kΩ		12	18	
	R_{FREQ} = 14.3kΩ		16	25	
DH_ Minimum Off-Time			140	200	ns
DH_ Minimum On-Time			120		ns
ERROR AMPLIFIER					
FB_ Input Bias Current	$V_{FB\_}$ = 0.8V			250	nA
FB1 Input-Voltage Set Point	Over line and load	0.792	0.800	0.808	V
FB2 Input-Voltage Set Point	MAX8538	0.792	0.800	0.808	V
	MAX8537/MAX8539, REFIN = 0.9V	0.894	0.900	0.906	
Op-Amp Open-Loop Voltage Gain	COMP_ = 1.3V to 2.3V	72	>80		dB
Op-Amp Gain Bandwidth			25		MHz
Op-Amp Output-Voltage Slew Rate			15		V/µs
DRIVERS					
Break-Before-Make Time			30		ns
DH1, DH2 On-Resistance in Low State			0.9	2.5	Ω
DH1, DH2 On-Resistance in High State			1.3	2.5	Ω
DL1, DL2 On-Resistance in Low State			0.7	1.5	Ω
DL1, DL2 On-Resistance in High State			1.6	2.8	Ω
LOGIC INPUTS (EN_)					
Input Low Level	4.5V < VL < 5.5V			0.8	V
Input High Level	4.5V < VL < 5.5V	2.4			V
Input Bias Current	0V to 5.5V	-1	+0.1	+1	µA
VTTR					
VTTR Output Voltage Range	Source or sink 15mA	0.5		2.5	V
VTTR Output Accuracy	-15mA ≤ I_{VTTR} ≤ +15mA, REFIN = 0.9V or 1.25V	-1.0	REFIN	+1.0	%
REFIN					
REFIN Input Bias Current	REFIN = 0.9V or 1.25V	-250		+250	nA

Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 12V, EN_ = VL, BST_ = 6V, LX_ = 1V, VL load = 0mA, C_{VL} = 10µF (ceramic), REFIN = 1.25V, PGND = AGND = FB_ = ILIM_ = 0V, C_{SS} = 10nF, C_{VTTR} = 1µF, R_{FREQ} = 20kΩ, DH_ = open, DL_ = open, POK_ = open, circuit of Figure 1, **T_A = 0°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFIN Input Voltage Range		0.5		2.5	V
REFIN Undervoltage-Lockout Trip Level	Rising and falling edge, hysteresis = 15mV	0.4	0.45	0.5	V
OUTPUT-VOLTAGE FAULT COMPARATORS					
Upper FB2 Fault Threshold	Rising voltage, hysteresis = 15mV	115	117	120	% of REFIN
Lower FB2 Fault Threshold	Falling voltage, hysteresis = 15mV	68	70	72	% of REFIN
Upper FB1 Fault Threshold	Rising voltage, hysteresis = 15mV	115	117	120	% of 0.8V
Lower FB1 Fault Threshold	Falling voltage, hysteresis = 15mV	68	70	72	% of 0.8V
POWER-OK OUTPUT (POK_)					
POK_ Delay			64		Clock cycles
Upper FB2 POK_ Threshold	Rising voltage, hysteresis = 20mV	110	112	114	% of REFIN
Lower FB2 POK_ Threshold	Falling voltage, hysteresis = 20mV	86	88	90	% of REFIN
Upper FB1 POK_ Threshold	Rising voltage, hysteresis = 20mV	110	112	114	% of 0.8V
Lower FB1 POK_ Threshold	Falling voltage, hysteresis = 20mV	86	88	90	% of 0.8V
POK_ Output Low Level	I_{SINK} = 2mA			0.4	V
POK_ Output High Leakage	POK_ = 5.5V			1	µA

ELECTRICAL CHARACTERISTICS (Note 2)

(V+ = 12V, EN_ = VL, BST_ = 6V, LX_ = 1V, VL load = 0mA, C_{VL} = 10µF (ceramic), REFIN = 1.25V, PGND = AGND = FB_ = ILIM_ = 0V, C_{SS} = 10nF, C_{VTTR} = 1µF, R_{FREQ} = 20kΩ, DH_ = open, DL_ = open, POK_ = open, circuit of Figure 1, **T_A = -40°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Operating Range	VL regulator drops out below 5.5V (Note 1)	4.75		23.00	V
FB_ Input-Voltage Set Point	Over line and load	0.788	0.800	0.812	V
FB2 Input-Voltage Set Point	MAX8537/MAX8539, REFIN = 0.9V	0.891	0.900	0.909	V
VTTR Output Accuracy	-15mA < I_{VTTR} ≤ +15mA, REFIN = 0.9V or 1.25V	-1	REFIN	+1	%

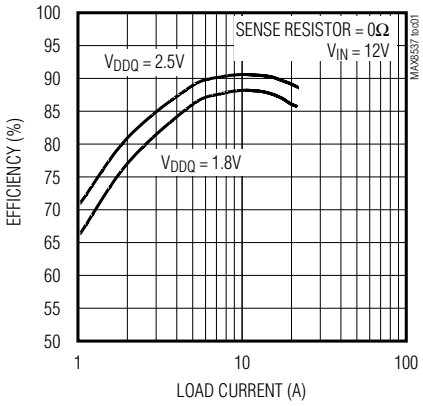
Note 1: Operating supply range is guaranteed by the VL line-regulation test. User must short V+ to VL if a fixed 5V supply is used (i.e., if V+ is less than 5.5V).

Note 2: Specifications to -40°C are guaranteed by design, not production tested.

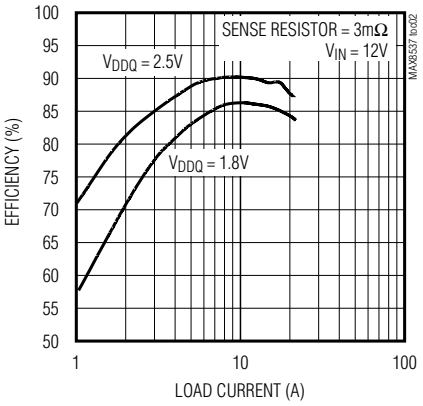
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, 400kHz switching frequency, V_{IN} = 12V, unless otherwise noted.)

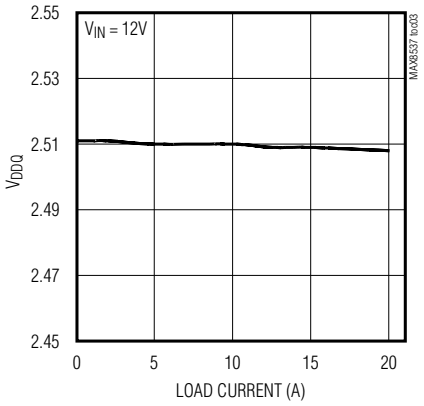
V_{DDQ} EFFICIENCY vs. LOAD CURRENT



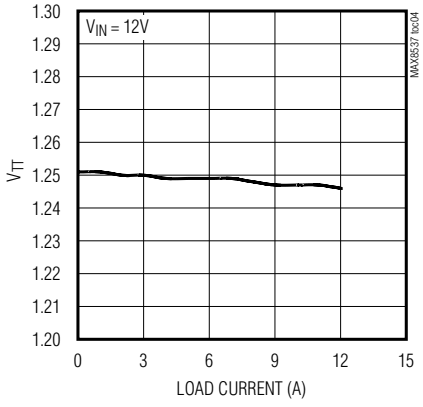
V_{DDQ} EFFICIENCY vs. LOAD CURRENT



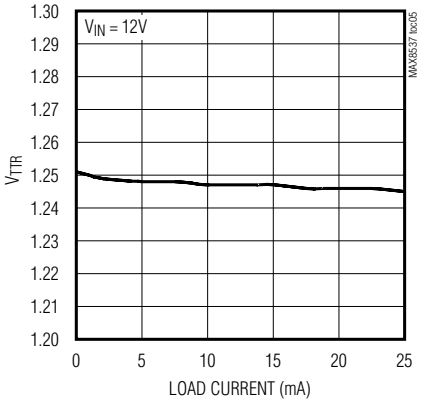
V_{DDQ} vs. LOAD CURRENT



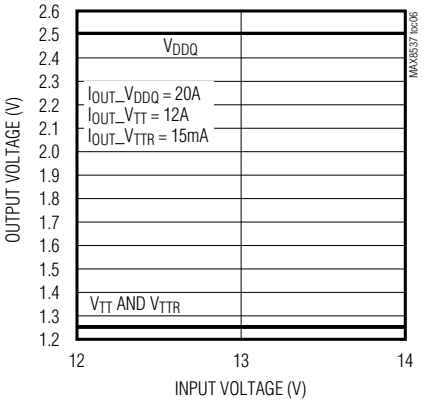
V_{TT} vs. LOAD CURRENT



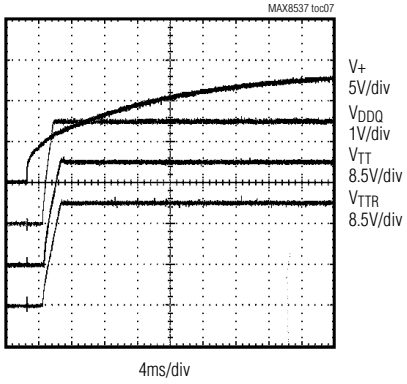
V_{TTR} vs. LOAD CURRENT



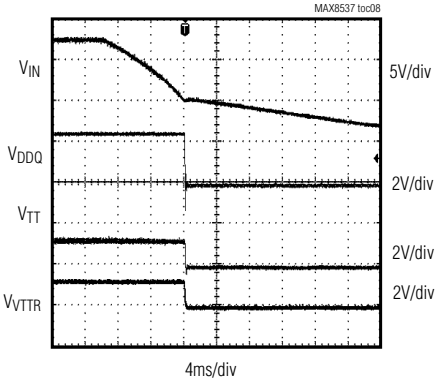
OUTPUT VOLTAGE vs. INPUT VOLTAGE



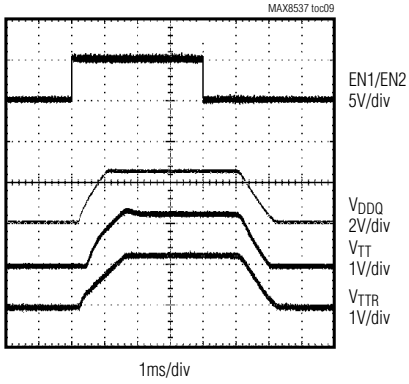
POWER-UP



POWER-DOWN



STARTUP AND SHUTDOWN

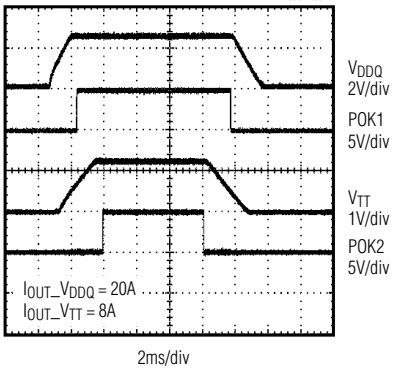


Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

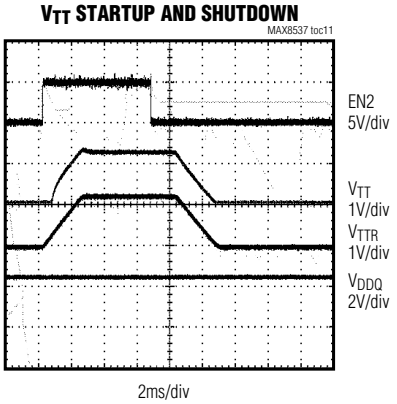
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, 400kHz switching frequency, V_{IN} = 12V, unless otherwise noted.)

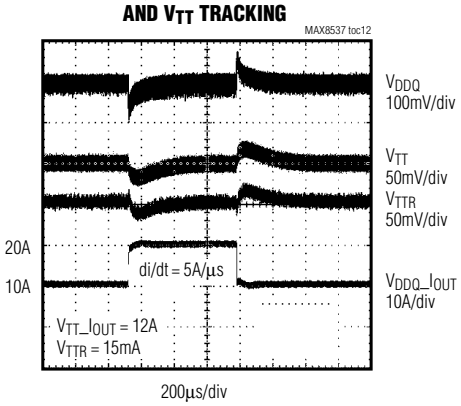
POWER-OK



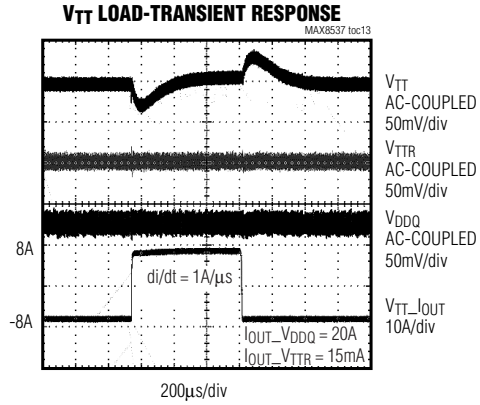
V_{TT} STARTUP AND SHUTDOWN



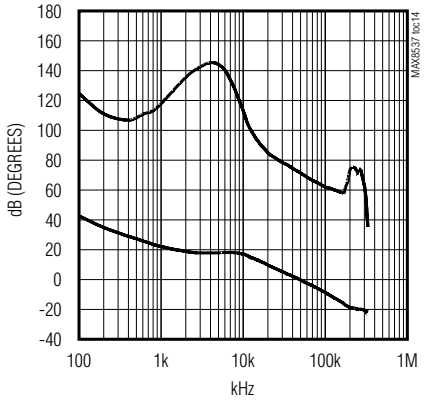
V_{DDQ} LOAD TRANSIENT AND V_{TT} TRACKING



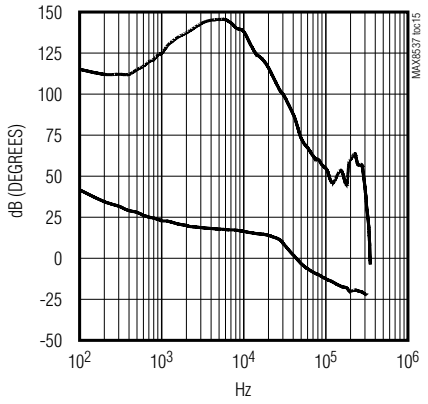
V_{TT} LOAD-TRANSIENT RESPONSE



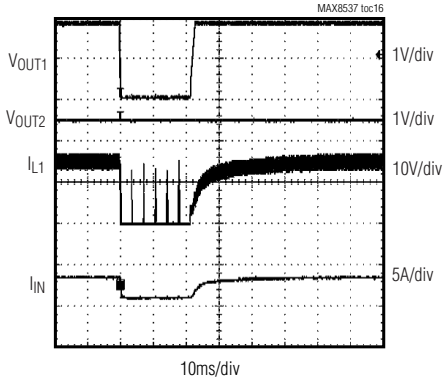
V_{DDQ} = 2.5V AT 20A BODE PLOT, V_{IN} = 12V



V_{TT} = 1.25V AT 12A BODE PLOT, V_{IN} = 12V



SHORT CIRCUIT AND RECOVERY



Pin Description

PIN	NAME (MAX8537/ MAX8539)	NAME (MAX8538)	FUNCTION
1	BST2	BST2	Bootstrap Input to Power Internal High-Side Driver for Step-Down 2. Connect to an external capacitor and diode according to Figure 1.
2	DH2	DH2	High-Side Gate-Driver Output for Step-Down 2. Swings from LX2 to BST2.
3	LX2	LX2	External Inductor Input for Step-Down 2. Connect to the switched side of the inductor. LX2 serves as the lower supply-voltage rail for the DH2 high-side gate driver and the current-limit circuitry.
4	ILIM2	ILIM2	Output Current-Limit Setting for Step-Down 2. Connect a resistor from ILIM2 to the drain of the step-down 2 high-side MOSFET, or to the junction of the source of the high-side MOSFET and the current-sense resistor to set the current-limit threshold. See the *Current-Limit Setting* section.
5	POK1	POK1	Open-Drain Output. High impedance when step-down 1 is within 12% of its regulation voltage. POK1 is pulled low in shutdown.
6	DL2	DL2	Low-Side Gate-Driver Output for Step-Down 2. Swings from PGND to VL.
7	POK2	POK2	Open-Drain Output. High impedance when step-down 2 is within 12% of its regulation voltage. POK2 is pulled low in shutdown or if REFIN is undervoltage.
8	EN2	EN2	Enable Input for Step-Down 2 (also for VTTR for the MAX8537 and MAX8539)
9	EN1	EN1	Enable Input for Step-Down 1
10	FREQ	FREQ	Frequency Adjust. Connect a resistor from this pin to ground to set the frequency. The range of the FREQ resistor is 163kΩ, 20kΩ, and 100kΩ (corresponding to 1.4MHz, 1.0MHz, and 200kHz).
11	COMP2	COMP2	Compensation Pin for Step-Down 2. Connect to compensation networks.
12	FB2	FB2	Feedback Input for Step-Down 2 with V_{REFIN} as the Threshold. User must have impedance <40kΩ.
13	SS2	SS2	Soft-Start for Step-Down 2. Connect a capacitor to GND to set the soft-start time.
14	REFIN	—	Reference Input for V_{TT} and V_{TTR}. Connect it to a resistor-divider from V_{DDQ}. REFIN common-mode voltage range is 0.5V to 2.5V. Current through the divider-resistors must be ≥100µA.
	—	N.C.	For the MAX8538, connect pin 14 to GND.
15	GND	GND	Analog Ground for Internal Circuitry
16	SS1	SS1	Soft-Start for Step-Down 1. Connect a capacitor to GND to set the soft-start time.
17	FB1	FB1	Feedback Input for Step-Down 1 with 0.8V Threshold. User must have impedance <40kΩ.
18	COMP1	COMP1	Compensation Pin for Step-Down 1. Connect to compensation networks.
19	VTTR	—	VTTR Output Capable of Sourcing and Sinking Up to 15mA. Always bypass with a 1µF ceramic capacitor (or larger) to GND.
	—	GND	Analog Ground for Internal Circuitry
20	AVL	AVL	Analog VL Input Pin. Connect to VL through a 4.7Ω resistor. Bypass with a 0.1µF (or larger) ceramic capacitor to GND.
21	V+	V+	Input Supply Voltage

Pin Description (continued)

PIN	NAME (MAX8537/ MAX8539)	NAME (MAX8538)	FUNCTION
22	VL	VL	Internal 5V Linear Regulator to Power the IC. VL is always on. Bypass with a ceramic capacitor with 1µF/10mA of load current. The internal VL regulator can be disabled by connecting VL and V+ to an externally generated 5V. VL output current can be boosted with an external PNP transistor.
23	DL1	DL1	Low-Side Gate-Driver Output for Step-Down 1. Swings from PGND to VL.
24	PGND	PGND	Power Ground for Gate-Driver Circuits
25	ILIM1	ILIM1	Output Current-Limit Setting for Step-Down 1. Connect a resistor from ILIM1 to the drain of the step-down 1 high-side MOSFET, or to the junction of the source of the high-side MOSFET and the current-sense resistor to set the current-limit threshold. See the *Current-Limit Setting* section.
26	LX1	LX1	External Inductor Input for Step-Down 1. Connect to the switched side of the inductor. LX1 serves as the lower supply-voltage rail for the DH1 high-side gate driver and current-limit circuitry.
27	DH1	DH1	High-Side Gate-Driver Step-Down 1. Swings from LX1 to BST1.
28	BST1	BST1	Bootstrap Input to Power Internal High-Side Driver for Step-Down 1. Connect to an external capacitor and diode according to Figure 1.

Detailed Description

The MAX8537/MAX8539 controllers provide a complete power-management solution for both DDR and combiner supplies. The MAX8537 and MAX8539 are configured for out-of-phase and in-phase DDR power-supply operations, respectively. In addition to the dual-synchronous buck controllers, they also contain an additional amplifier to generate a total of three outputs: the main memory voltage (V_{DDQ}), the tracking sinking/sourcing termination voltage (V_{TT}), and the termination reference voltage (V_{TTR}). The MAX8538 is configured as a dual out-of-phase controller for point-of-load supplies. Each buck controller can source or sink up to 25A of current, while the termination reference can supply up to 15mA output.

The MAX8537/MAX8539 have a 1% accurate reference. The first buck controller generates V_{DDQ} using external resistor-dividers. The second synchronous buck controller and the amplifier generate 1/2 V_{DDQ} voltage for V_{TT} and V_{TTR}. The V_{TT} and V_{TTR} voltages are maintained within 1% of 1/2 V_{DDQ}.

The MAX8537/MAX8538/MAX8539 use a constant-frequency voltage-mode architecture with operating frequencies of 200kHz to 1.4MHz to allow flexible design. An internal high-bandwidth (25MHz) operational amplifier is used as an error amplifier to regulate the output voltage. This allows fast transient response, reducing the number of output capacitors. Synchronous rectification ensures high efficiency and balanced current sourcing and sinking capability for V_{TT}. An all-N-FET design optimizes efficiency and cost. The two converters can be operated in-phase or out-of-phase to minimize capacitance and optimize performance for all V_{IN}/V_{OUT} combinations.

Both channels have independent enable and power-good functions. They also have high-side current-sense architectures. ILIM pins allow the setting of an adjustable, lossless current limit for different combinations of load current and $R_{DS(ON)}$. Additionally, accurate overcurrent protection is achieved by using a sensing resistor in series with the high-side FET. The positive current-limit threshold is programmable through an external resistor. Overvoltage protection is achieved by latching off the high-side MOSFET and latching on the low-side MOSFET when the output voltage exceeds 17% of its set output.

DC-DC Controller

The MAX8537/MAX8538/MAX8539 step-down DC-DC converters use a PWM voltage-mode control scheme. An internal high-bandwidth (25MHz) operational amplifier is used as an error amplifier to regulate the output voltage. The output voltage is sensed and compared with an internal 0.8V reference or REFIN to generate an error signal. The error signal is then compared with a fixed-frequency ramp by a PWM comparator to give the appropriate duty cycle to maintain output voltage regulation. At the rising edge of the internal clock, and with DL (the low-side MOSFET gate drive) at 0V, the high-side MOSFET turns on. When the ramp voltage reaches the error-amplifier output voltage, the high-side MOSFET latches off until the next clock pulse. During the high-side MOSFET on-time, current flows from the input, through the inductor, and to the output capacitor and load. At the moment the high-side MOSFET turns off, the energy stored in the inductor during the on-time is released to support the load as the inductor current ramps down by commutation through the low-side MOSFET body diode. After a fixed delay, the low-side MOSFET turns on to shunt the current from its body diode for lower voltage drop and increased efficiency. The low-side MOSFET turns off at the rising edge of the next clock pulse, and when its gate voltage discharges to zero, the high-side MOSFET turns on and another cycle starts.

The controllers sense peak inductor current and provide hiccup-mode overload and short-circuit protection (see the *Current Limit* section).

The MAX8537/MAX8538/MAX8539 operate in forced-PWM mode where the inductor current is always continuous, so even under light load the controller maintains a constant switching frequency to minimize noise and possible interference with system circuitry.

Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces the conduction loss in the rectifier by replacing the normal Schottky catch diode with a low-resistance MOSFET switch. The MAX8537/MAX8538/MAX8539 controllers also use the synchronous rectifier to ensure proper startup of the boost gate-drive circuit.

High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit (Figure 1). The capacitor between BST and LX is alternately charged from the VL supply and placed in parallel to the high-side MOSFET's gate-source terminals.

On startup, the synchronous rectifier (low-side MOSFET) forces LX to ground and charges the boost capacitor to VL. On the second half-cycle, the switch-mode power supply turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary gate-to-source voltage to turn on the high-side switch, an action that boosts the 5V gate-drive signal above the input voltage.

Internal 5V Linear Regulator

All MAX8537/MAX8538/MAX8539 functions are powered from the on-chip low-dropout 5V regulator with the input connected to V+. Bypass the regulator's output (VL) with a 1µF/10mA or greater ceramic capacitor. The V+ to VL dropout voltage is typically 500mV, so when V+ is less than 5.5V, VL is typically (V+ - 500mV).

The internal linear regulator can source up to 70mA to supply the IC, power the low-side gate drivers, and charge the external boost capacitors. The current required to drive the external MOSFETs is calculated as the total gate charge of the MOSFETs at 5V multiplied by the switching frequency. At higher frequency, the MOSFET drive current may exceed the capability of the internal linear regulator. The output current at VL can be supplemented with an external PNP transistor as shown in Figures 4 and 5, which also moves most of the power dissipation off the IC. The external PNP can increase the output current at VL to over 200mA. The dropout voltage increases to 1V (typ).

Undervoltage Lockout (UVLO)

If VL drops below 3.75V, the MAX8537/MAX8538/MAX8539 assume that the supply voltage is too low to make valid decisions, so UVLO circuitry inhibits switching and forces POK and DH low and DL high. After VL rises above 4.3V, the controller powers up the outputs (see the *Startup* section).

Startup

Externally, the MAX8537/MAX8538/MAX8539 start switching when VL rises above the 4.3V UVLO threshold. However, the controller does not start unless all four of the following conditions are met: 1) EN_ is high, 2) VL > 4.3V, 3) the internal reference exceeds 80% of its nominal value (V_{REF} > 0.64V), and 4) the thermal limit is not exceeded. Once the MAX8537/MAX8538/MAX8539 assert the internal enable signal, the controller starts switching and enables soft-start.

Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

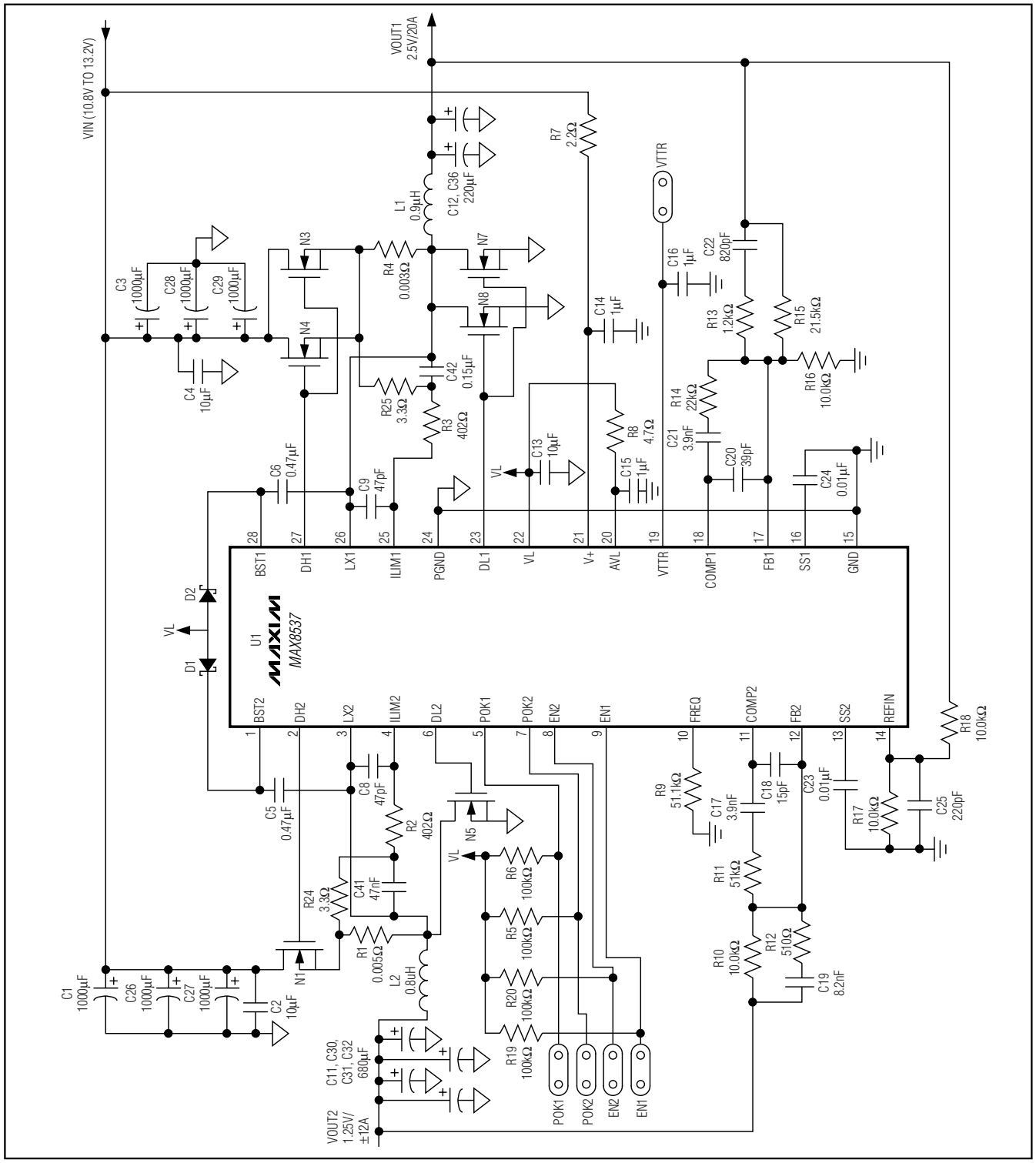


Figure 1. Typical Application Circuit: MAX8537 DDR Memory Application (400kHz Switching)

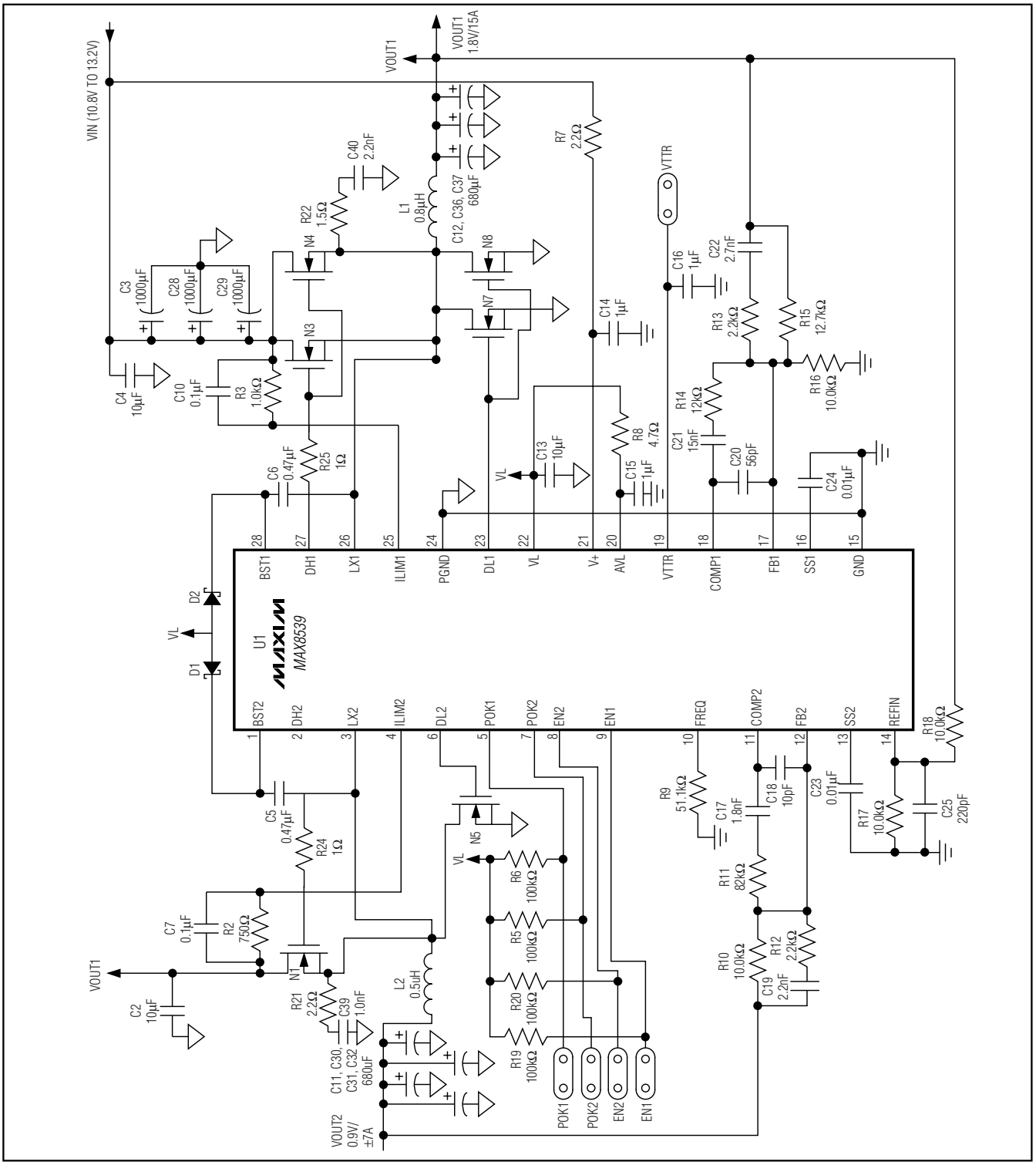


Figure 2. MAX8539 DDR Memory Application (400kHz Switching)

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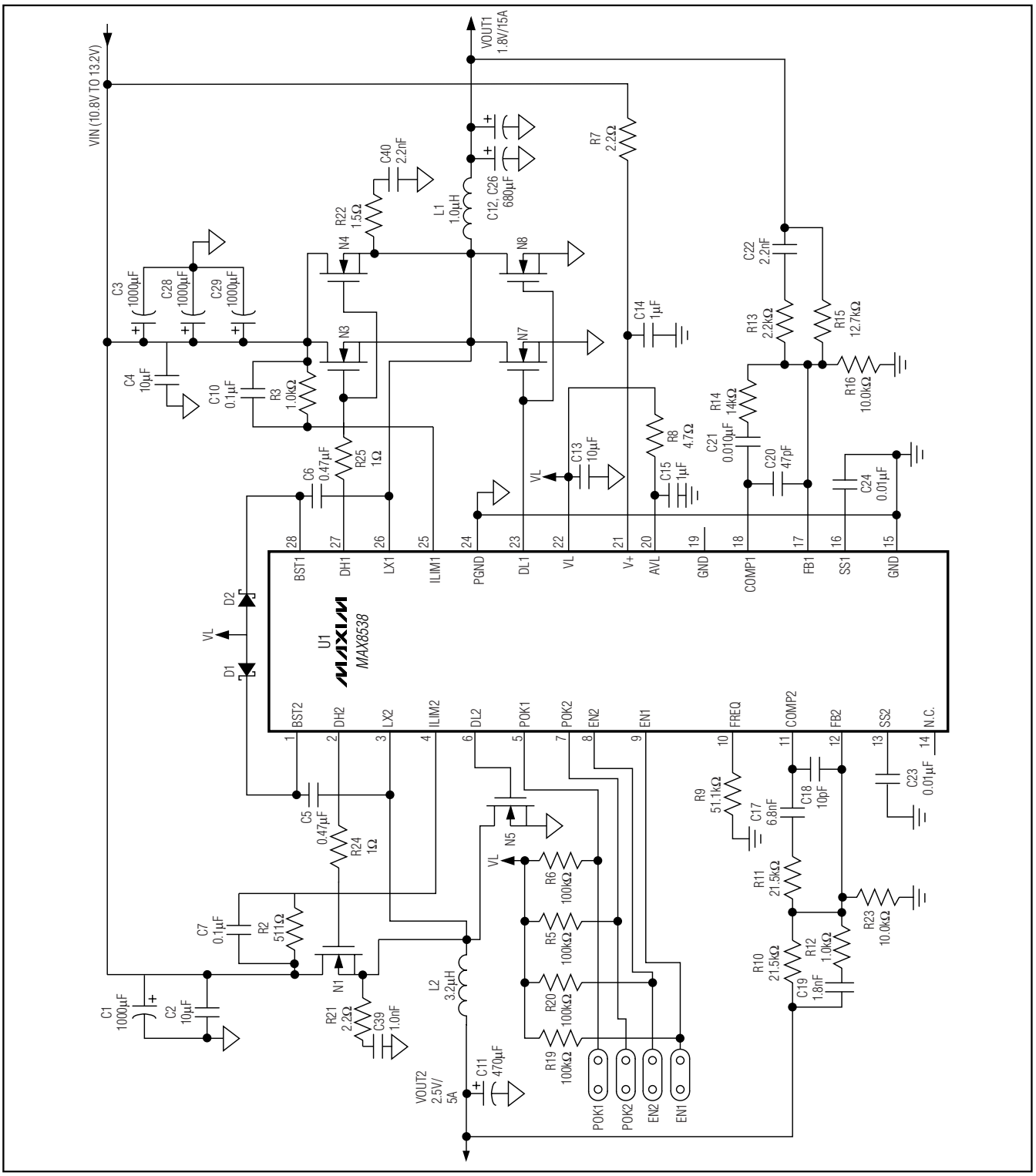

Figure 3. MAX8538 PowerPC™ Application (400kHz Switching)

PowerPC is a trademark of Motorola, Inc.

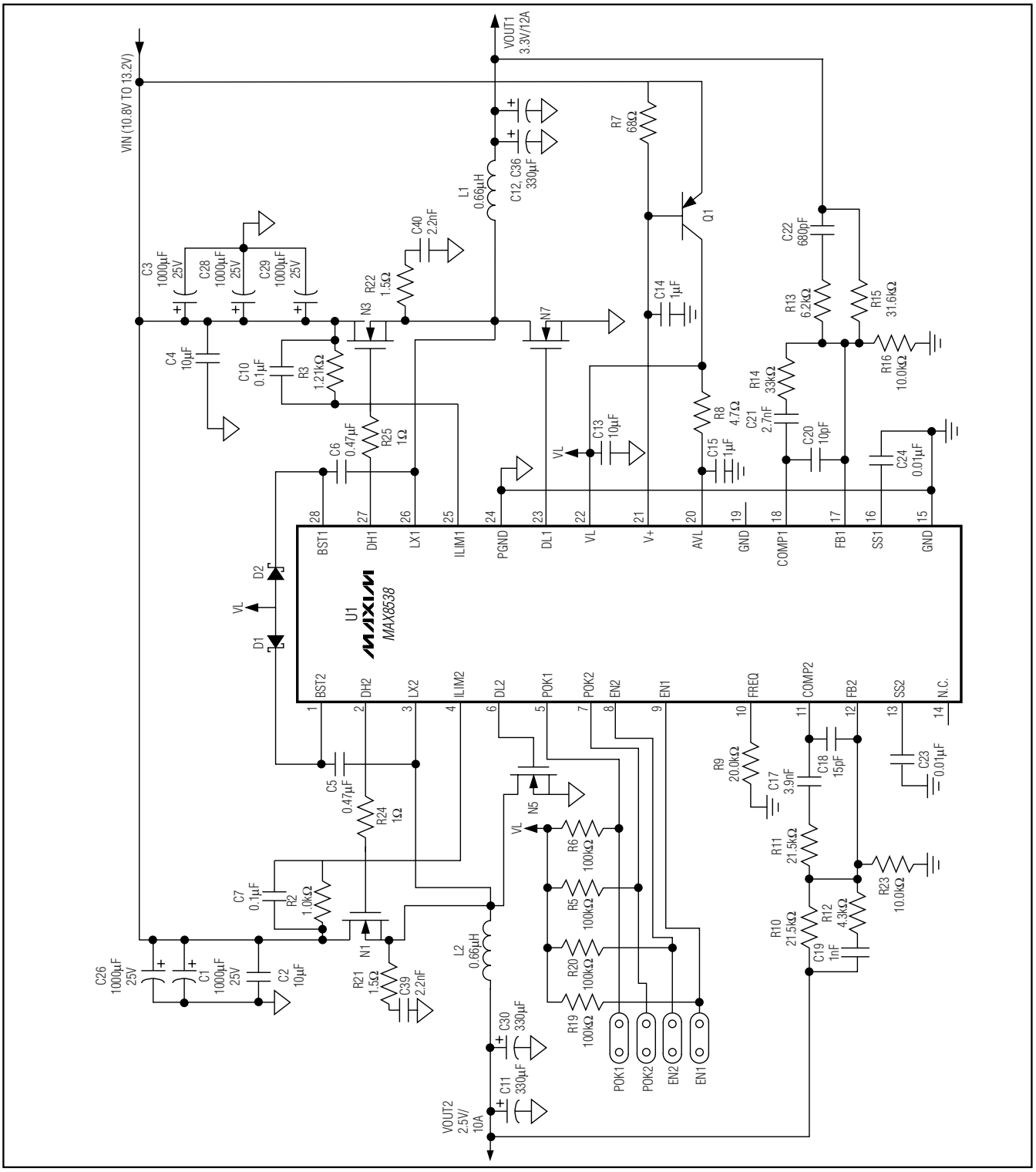

Figure 4. MAX8538 Dual-Output Application (1MHz Switching)

Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

Power-Good Signal (POK_)

The power-good signal (POK_) is an open-drain output. The MOSFET turns on and POK_ is held low until FB_ is ±12% from its nominal threshold (0.8V for FB1 and V_{REFIN} for FB2). Then there is a 64 clock-cycle delay before POK_ goes high impedance. For 400kHz switching frequency, this delay is 160µs. To obtain a logic voltage output, connect a pullup resistor from POK_ to VL. A 100kΩ resistor works well for most applications. If unused, leave POK_ grounded or unconnected.

Enable (EN_), Soft-Start, and Soft-Stop

Outputs of the MAX8537/MAX8538/MAX8539 can be turned on with logic high and off with logic low independently at EN1 and EN2. EN1 controls step-down 1, and EN2 controls step-down 2 and VTTR (MAX8537/MAX8539 only).

On the rising edge of EN_, the controller enters soft-start. Soft-start gradually ramps up the reference voltage seen by the error amplifier to control the output's rate of rise and reduce the input surge current during startup. The soft-start period is determined by a 5µA pullup current, the external soft-start capacitor connected from SS_ to ground, and the reference voltage (0.8V for FB1 and V_{REFIN} for FB2, on the MAX8537/MAX8539; 0.8V for FB2 on the MAX8538). The output reaches regulation when soft-start is completed. On the falling edge of EN_, the controller enters soft-stop, which reverses the soft-start ramp. However, there is a delay due to 1V overcharge on the soft-start capacitor. The delay time can be calculated as $t_{DELAY} = C_{SS} \times 1V / 5\mu A$. At the end of soft-stop, DH is low and DL is high.

Current Limit

The MAX8537/MAX8538/MAX8539 DC-DC step-down controllers sense the peak inductor current either through the on-resistance of the high-side MOSFET for lossless sensing, or with a series resistor for more accurate sensing. In either case, when peak voltage across the sensing circuit (which occurs at the peak of the inductor current) exceeds the current-limit threshold set by the ILIM pin, the controller turns off the high-side MOSFET and turns on the low-side MOSFET. The MAX8537/MAX8538/MAX8539 current-limit threshold can be set by an external resistor that works in conjunction with an internal 200µA current sink. See the *Design Procedure* section for how to set the ILIM with an external resistor.

As the output load current increases above the threshold required to trip the peak current limit, the output voltage sags because the truncated duty cycle is insufficient to support the load current. When FB_ is 30% below its nominal threshold, output undervoltage protection is triggered and the controller enters hiccup mode to limit the power dissipation in a fault condition. See the *Output Undervoltage Protection (UVP)* section for a description of hiccup operation.

Output Undervoltage Protection (UVP)

Output UVP begins when the controller is at its current limit, FB_ is 30% below its nominal threshold, and soft-start is complete. This condition causes the controller to drive DH and DL low, and to discharge the soft-start capacitor with a 5µA pulldown current until V_{SS} reaches 50mV. Then the controller begins switching and enables soft-start. If the overload condition still exists when soft-start is complete, UVP triggers again. The result is hiccup mode, where the controller attempts to restart periodically as long as the overload condition exists. In hiccup mode, the soft-start capacitor voltage ramps from the nominal FB_ threshold + 12% down to 50mV.

For the MAX8537/MAX8539, the tracking step-down must also have $V_{REFIN} > 0.45V$ to trigger UVP. Then the soft-start capacitor voltage ramps from V_{REFIN} + 12% down to 50mV. Additionally, in the MAX8537/MAX8539 if output 1 is shorted, output 2 latches off. Recycle the input power or enable to restart output 2.

Output Overvoltage Protection (OVP)

The output voltages are continuously monitored for overvoltage. If the output voltage is more than 17% above the reference of the error amplifier, OVP is triggered after a 10µs delay and the controller turns off. The DL low-side gate driver is latched high until EN_ is toggled or V+ power is cycled below 3.75V. This action turns on the synchronous-rectifier MOSFET with 100% duty cycle and, in turn, rapidly discharges the output filter capacitor and forces the output to ground.

Note that DL latching high causes the output voltage to go slightly negative due to energy stored in the output LC at the instant OVP activates. If the load cannot tolerate being forced to a negative voltage, it can be desirable to place a power Schottky diode across the output to act as a reverse-polarity clamp.

For step-down 2 of the MAX8537/MAX8539, the OVP threshold is 560mV for $V_{REFIN} \le 0.45V$, and the OVP threshold is V_{REFIN} + 17% for $V_{REFIN} > 0.45V$.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8537/MAX8538/MAX8539. When the junction temperature exceeds $T_J = +160°C$, a thermal sensor shuts down the device, forcing DH and DL low and allowing the IC to cool. The thermal sensor turns the part on again after the junction temperature cools

by 10°C, resulting in a pulsed output during continuous thermal-overload conditions.

During a thermal event, the switching converters are turned off, POK1 and POK2 are pulled low, and the soft-starts are reset.

Design Procedure

Output Voltage Setting

The output voltage can be set by a resistive divider network. Select R2, the resistor from FB to GND, between 5kΩ and 15kΩ. Then calculate R1 by:

$$R1 = R2 \times [(V_{OUT} / 0.8) - 1]$$

Inductor Selection

There are several parameters that must be examined when determining which inductor to use: input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor current ripple to DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple. A good compromise between size and efficiency is a 30% LIR. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_S \times I_{LOAD(MAX)} \times LIR}$$

where f_S is the switching frequency. Choose a standard value close to the calculated value. The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. Find a low-loss inductor with the lowest possible DC resistance that fits the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well up to 300kHz. The chosen inductor's saturation current rating must exceed the peak inductor current determined as:

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = \frac{\sqrt{[I_{OUT1}2 \times V_{OUT1} \times (V_{IN} - V_{OUT1})] + [I_{OUT2}2 \times V_{OUT2} \times (V_{IN} - V_{OUT2})]}}{V_{IN}}$$

Combinations of large electrolytic and small ceramic capacitors in parallel are recommended. Almost all of the RMS current is supplied from the large electrolytic capacitor, while the smaller ceramic capacitor supplies the fast rise and fall switching edges. Choose the electrolytic capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements, which affect the overall stability, output ripple voltage, and transient response.

The output ripple has three components: variations in the charge stored in the output capacitor, voltage drop across the capacitor's ESR, and voltage drop across the capacitor's ESL, caused by the current into and out of the capacitor. The following equations estimate the worst-case ripple:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

$$V_{RIPPLE(ESR)} = I_{P-P}\ ESR$$

$$V_{RIPPLE(C)} = I_{P-P} / (8 \times C_{OUT} \times f_{SW})$$

$$V_{RIPPLE(ESL)} = V_{IN} \times ESL / (L + ESL)$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_{SW}\ L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current (see the *Inductor Selection* section). Higher output current requires paralleling multiple capacitors to meet the output ripple voltage.

The MAX8537/MAX8538/MAX8539s' response to a load transient depends on the selected output capacitor. After a load transient, the output instantly changes by (ESR x ΔI_{LOAD}) + (ESL x dI/dt). Before the controller can respond, the output deviates further depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. With higher bandwidth, the response time is faster, pre-

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venting the output capacitor voltage from further deviation from its regulating value.

Do not exceed the capacitor's voltage or ripple current ratings.

MOSFET Selection

The MAX8537/MAX8538/MAX8539 controllers drive two external, logic-level, N-channel MOSFETs as the circuit-switch elements. The key selection parameters are:

1) On-resistance ($R_{DS(ON)}$): the lower, the better.
2) Maximum drain-to-source voltage (V_{DSS}): should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
3) Gate charges (Q_g, Q_{gd}, Q_{gs}): the lower, the better.

Choose MOSFETs with $R_{DS(ON)}$ rated at V_{GS} = 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET that has conduction loss equal to the switching loss at the nominal input voltage and maximum output current. For the low-side MOSFET, make sure it does not spuriously turn on due to dV/dt caused by the high-side MOSFET turning on, as this results in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{gd}/Q_{gs} ratio have higher immunity to dV/dt.

For proper thermal-management design, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for low-side MOSFET, worst case is at $V_{IN(MAX)}$; for high-side MOSFET, it could be either at $V_{IN(MIN)}$ or $V_{IN(MAX)}$). High-side and low-side MOSFETs have different loss components due to the circuit operation. The low-side MOSFET, operates as a zero-voltage switch; therefore, the major losses are the channel conduction loss (P_{LSCC}) and the body-diode conduction loss (P_{LSDC}):

$$P_{LSCC} = [1 - (V_{OUT} / V_{IN})] \times (I_{LOAD})^2 \times R_{DS,ON}$$

Use $R_{DS,ON}$ at $T_{J(MAX)}$:

$$P_{LSDC} = 2 \times I_{LOAD} \times V_F \times t_{dt} \times f_S$$

where V_F is the body-diode forward voltage drop, t_{dt} is the dead-time between the high-side MOSFET and the low-side MOSFET switching transitions, and f_S is the switching frequency.

The high-side MOSFET operates as a duty-cycle control switch and has the following major losses: the channel conduction loss (P_{HSCC}), the V I overlapping switching loss (P_{HSSW}), and the drive loss (P_{HSDR}). The high-side MOSFET does not have body-diode conduction loss because the diode never conducts current.

$$P_{HSCC} = (V_{OUT} / V_{IN}) \times I^2_{LOAD} \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{HSSW} = V_{IN} \times I_{LOAD} \times f_S \times [(Q_{gs} + Q_{gd}) / I_{GATE}]$$

where I_{GATE} is the average DH-high driver output-current capability determined by:

$$I_{GATE(ON)} = 2.5 / (R_{DH} + R_{GATE})$$

where R_{DH} is the high-side MOSFET driver's average on-resistance (1.1Ω typ) and R_{GATE} is the internal gate resistance of the MOSFET (~2Ω):

$$P_{HSDR} = Q_{gs} \times V_{GS} \times f_S \times R_{GATE} / (R_{GATE} + R_{DH})$$

where V_{GS} ~ VL = 5V.

In addition to the losses above, approximately 20% more for additional losses due to MOSFET output capacitances and low-side MOSFET body-diode reverse-recovery charge dissipated in the high-side MOSFET that exists, but is not well defined in the MOSFET data sheet. Refer to the MOSFET data sheet for thermal-resistance specification to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above-calculated power dissipation.

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors in series with DH and DL to slow down the switching transitions. However, adding series resistors increases the power dissipation of the MOSFETs, so be sure this does not overheat the MOSFETs.

The minimum load current must exceed the high-side MOSFET's maximum leakage current over temperature if fault conditions are expected.

Current-Limit Setting

The MAX8537/MAX8538/MAX8539 controllers sense the peak inductor current to provide constant current and hiccup current limit. The peak current-limit threshold is set by an external resistor together with the internal current sink of 200µA. The voltage drop across the resistor $R_{ILIM\_}$ with 200µA current through it sets the maximum peak inductor current that can flow through the high-side MOSFET or the optional current-sense resistor by the equations below:

$$I_{PEAK(MAX)} = 200\mu A \times R_{ILIM\_} / R_{DSON(HSFET)}$$

or

$$I_{PEAK(MAX)} = 200\mu A \times R_{ILIM\_} / R_{SENSE}$$

$R_{ILIM\_}$ should be less than 1.5kΩ for optimum current-limit accuracy. The actual corresponding maximum load current is lower than the $I_{PEAK(MAX)}$ above by half

of the inductor ripple current (see the *Inductor Selection* section). If $R_{DS(ON)}$ of the high-side MOSFET is used for current sensing, make sure to use the maximum $R_{DS(ON)}$ at the highest operating junction temperature to avoid fault tripping of the current limit at elevated temperature. Consideration should also be given to the tolerance of the 200µA current sink.

When $R_{DS(ON)}$ of the high-side MOSFET is used for current sensing, ringing on the LX voltage waveform can interfere with the current limit. Below is the procedure for selecting the value of the series RC snubber circuit:

1) Connect a scope probe to measure V_{LX} to GND, and observe the ringing frequency, f_R.
2) Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half.

   The circuit parasitic capacitance (C_{PAR}) at LX is then equal to 1/3rd the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R_{SNUB}) is equal to $2\pi \times f_R \times L_{PAR}$. Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion.

The capacitor (C_{SNUB}) should be at least 2 to 4 times the value of the C_{PAR} in order to be effective. The power loss of the snubber circuit is dissipated in the resistor (P_{RSNUB}) and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_{SW}$$

where V_{IN} is the input voltage and f_{SW} is the switching frequency. Choose an R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Additionally, there is parasitic inductance of the current-sensing element, whether the high-side MOSFET $R_{DS(ON)}$ (L_{SENSE_FET}) or the actual current-sense resistor R_{SENSE} (L_{RSENSE}) are used, which is in series with the output filter inductor. This parasitic inductance, together with the output inductor, form an inductive divider and cause error in the current-sensing voltage. To compensate for this error, a series RC circuit can be added in parallel with the sensing element (see Figure 1). The RC time constant should equal L_{RSENSE} / R_{SENSE}, or L_{SENSE_FET} / $R_{DS(ON)}$. First, set the value of R equal to or less than $R_{ILIM\_}$ / 100. Then, the value of C can be calculated as:

$$C = L_{RSENSE} / (R_{SENSE} \times R) \text{ or}$$
$$C = L_{SENSE\_FET} / (R_{DS(ON)} \times R)$$

Any PC board trace inductance in series with the sensing element and output inductor should be added to the specified FET or resistor inductance per the respective manufacturer's data sheet. For the case of the MOSFET, it is the inductance from the drain to the source lead.

An additional switching noise filter may be needed at ILIM_ by connecting a capacitor in parallel with $R_{ILIM\_}$ (in the case of $R_{DS(ON)}$ sensing) or from ILIM_ to LX (in the case of resistor sensing). For the case of $R_{DS(ON)}$ sensing, the value of the capacitor should be:

$$C > 50 / (3.1412 \times f_S \times R_{ILIM\_})$$

For the case of resistor sensing:

$$C < 25 \times 10^{-9} / R_{ILIM\_}$$

Soft-Start Capacitor Setting

The two step-down converters have independent, adjustable soft-start. External capacitors from SS1/SS2 to ground are charged by an internal 5µA current source to the corresponding feedback threshold. Therefore, the soft-start time can be calculated as:

$$T_{SS} = C_{SS} \times V_{FB} / 5\mu A$$

For example, 0.01µF from SS1 to ground corresponds to approximately a 1.6ms soft-start period for step-down 1.

Compensation Design

The MAX8537/MAX8538/MAX8539 use a voltage-mode control scheme that regulates the output voltage by comparing the error-amplifier output (COMP) with a fixed internal ramp to produce the required duty cycle. The error amplifier is an operational amplifier with 25MHz bandwidth to provide fast response. The output lowpass LC filter creates a double pole at the resonant frequency that introduces a gain drop of 40dB per decade and a phase shift of 180 degrees per decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system.

The basic regulator loop can be thought of as consisting of a power modulator and an error amplifier. The power modulator has DC gain set by V_{IN} / V_{RAMP}, with a double pole, f_{P_LC}, and a single zero, f_{Z_ESR}, set by the output inductor (L), the output capacitor (C_O), and its equivalent series resistance (R_{ESR}). Below are the equations that define the power modulator:

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$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}, \text{ where } V_{RAMP} = 1V \text{ (typ)}$$

$$f_{P\_LC} = \frac{1}{2\pi \ L \ C_O}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

When the output capacitor is composed of paralleling n number of the same capacitors, then:

$$C_O = n \times C_{EACH}$$

and

$$R_{ESR} = \frac{R_{ESR\_EACH}}{n}$$

Thus, the resulting f_{Z_ESR} is the same as that of a single capacitor.

The total closed-loop gain must be equal to unity at the crossover frequency, where the crossover frequency is less than or equal to 1/5th the switching frequency (f_S):

$$f_C \le f_S / 5$$

So the loop-gain equation at the crossover frequency is:

$$G_{EA(FC)} \times G_{MOD(FC)} = 1$$

where $G_{EA(FC)}$ is the error-amplifier gain at f_C, and $G_{MOD(FC)}$ is the power-modulator gain at f_C.

The loop compensation is affected by the choice of output filter capacitor due to the position of its ESR-zero frequency with respect to the desired closed-loop crossover frequency. Ceramic capacitors are used for higher switching frequencies (above 750kHz) and have low capacitance and low ESR; therefore, the ESR-zero frequency is higher than the closed-loop crossover frequency. Electrolytic capacitors (e.g., tantalum, solid polymer, and OS-CON) are needed for lower switching frequencies and have high capacitance and higher ESR; therefore, the ESR-zero frequency is lower than the closed-loop crossover frequency. Thus, the compensation design procedures are separated into two cases:

Case 1: Crossover frequency is less than the output-capacitor ESR-zero ($f_C < f_{Z\_ESR}$).

The modulator gain at f_C is:

$$G_{MOD(FC)} = G_{MOD(DC)} \times (f_{P\_LC} / f_C)^2$$

Since the crossover frequency is lower than the output capacitor ESR-zero frequency and higher than the LC double-pole frequency, the error-amplifier gain must have a +1 slope at f_C so that, together with the -2 slope of the LC double pole, the loop crosses over at the desired -1 slope.

The error amplifier has a dominant pole at a very low frequency (~0Hz), and two additional zeros and two additional poles as indicated by the equations below and illustrated in Figure 6:

$$f_{Z1\_EA} = 1 / (2\pi \times R4 \times C2)$$

$$f_{Z2\_EA} = 1 / (2\pi \times (R1 + R3) \times C1)$$

$$f_{P2\_EA} = 1 / (2\pi \times R3 \times C1)$$

$$f_{P3\_EA} = 1 / (2\pi \times R4 \times (C2 \times C3 / (C2 + C3)))$$

Note that f_{Z2_EA} and f_{P2_EA} are chosen to have the converter closed-loop crossover frequency, f_C, occur when the error-amplifier gain has +1 slope, between f_{Z2_EA} and f_{P2_EA}. The error-amplifier gain at f_C must meet the requirement below:

$$G_{EA(FC)} = 1 / G_{MOD(FC)}$$

The gain of the error amplifier between f_{Z1_EA} and f_{Z2_EA} is:

$$G_{EA}(f_{Z1\_EA} - f_{Z2\_EA}) = G_{EA(FC)} \times f_{Z2\_EA} / f_C = f_{Z2\_EA} / (f_C \times G_{MOD(FC)})$$

This gain is set by the ratio of R4/R1, where R1 is calculated in the *Output Voltage Setting* section. Thus:

$$R4 = R1 \times f_{Z2\_EA} / (f_C \times G_{MOD(FC)})$$

where $f_{Z2\_EA} = f_{P\_LC}$.

Due to the underdamped (Q > 1) nature of the output LC double pole, the first error-amplifier zero frequency must be set less than the LC double-pole frequency in order to provide adequate phase boost. Set the error-amplifier first zero, f_{Z1_EA}, at 1/4th the LC double-pole frequency. Hence:

$$C2 = 2 / (\pi \times R4 \times f_{P\_LC})$$

Set the error amplifier f_{P2_EA} at f_{Z_ESR} and f_{P3_EA} equal to half the switching frequency. The error-amplifier gain between f_{P2_EA} and f_{P3_EA} is set by the ratio of $R4/R_I$ and is equal to:

$$G_{EA}(f_{Z1\_EA} - f_{Z2\_EA}) \times (f_{Z\_ESR} / f_{P\_LC})$$

where $R_I = R1 \times R3 / (R1 + R3)$. Then:

$$R_I = R4 \times f_{P\_LC} / (G_{EA}(f_{Z1\_EA} - f_{Z2\_EA}) \times f_{Z\_ESR}) = R4 \times f_C \times G_{MOD(FC)} / f_{Z\_ESR}$$

The value of R3 can then be calculated as:

$$R3 = R1 \times R_I / (R1 - R_I)$$

Now we can calculate the value of C1 as:

$$C1 = 1 / (2\pi \times R3 \times f_{Z\_ESR})$$

and C3 as:

$$C3 = C2 / ((2\pi \times C2 \times R4 \times f_{P3\_EA}) - 1)$$

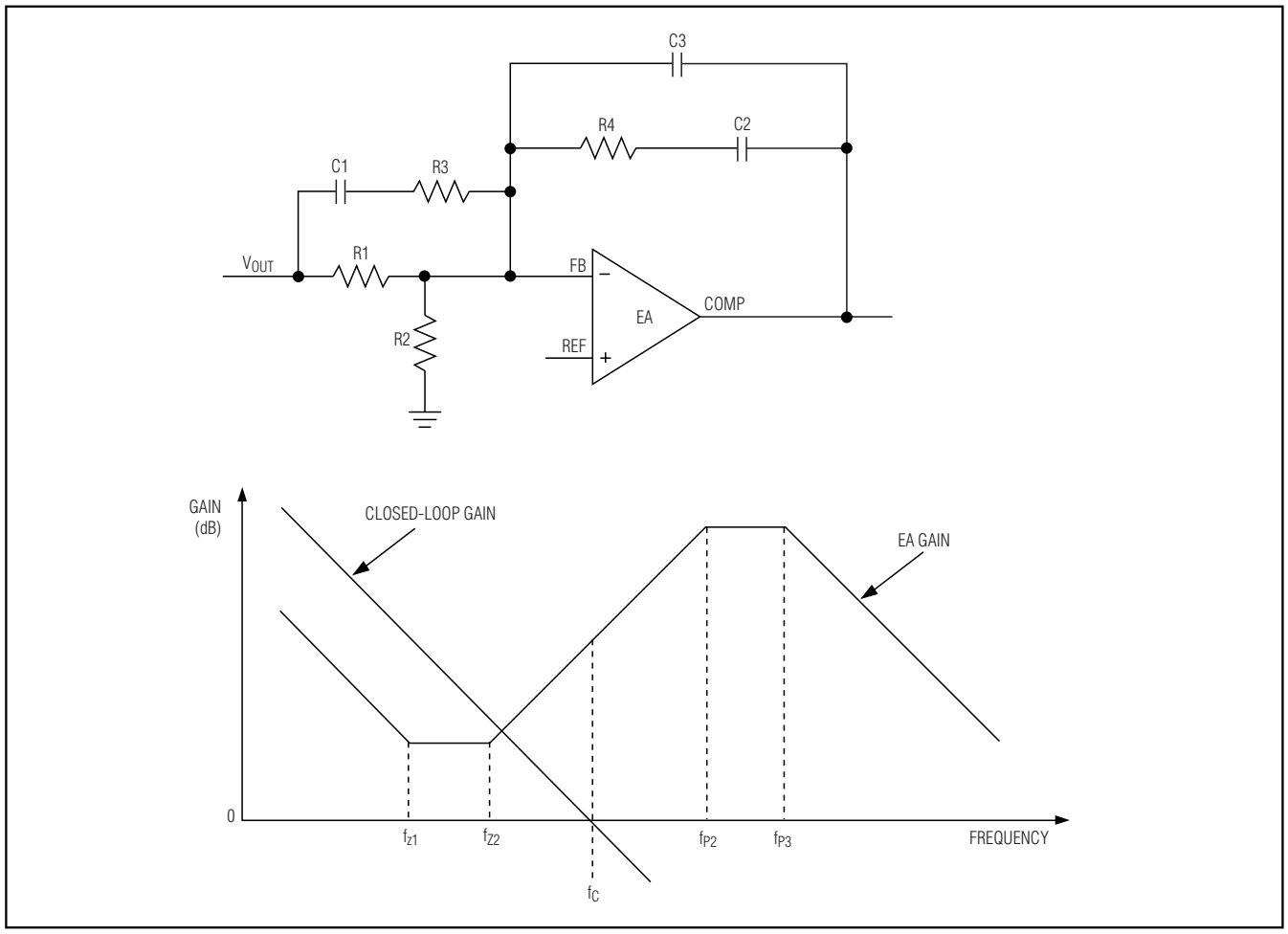

Figure 6. Error-Amplifier Compensation Circuit; Closed-Loop and Error-Amplifier Gain Plot for Case 1

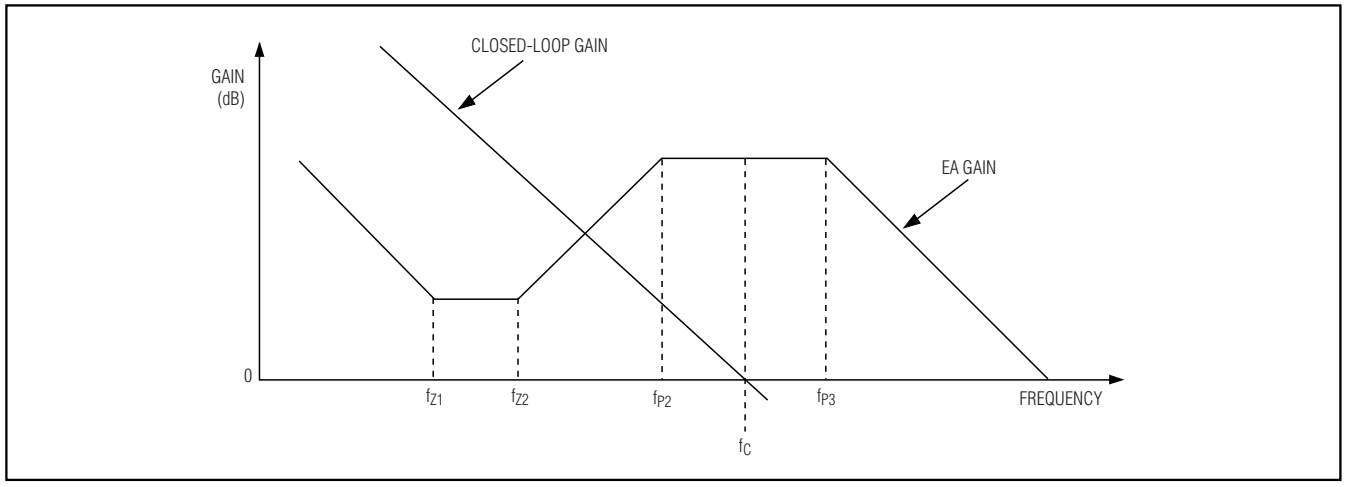

Figure 7. Closed-Loop and Error-Amplifier Gain Plot for Case 2

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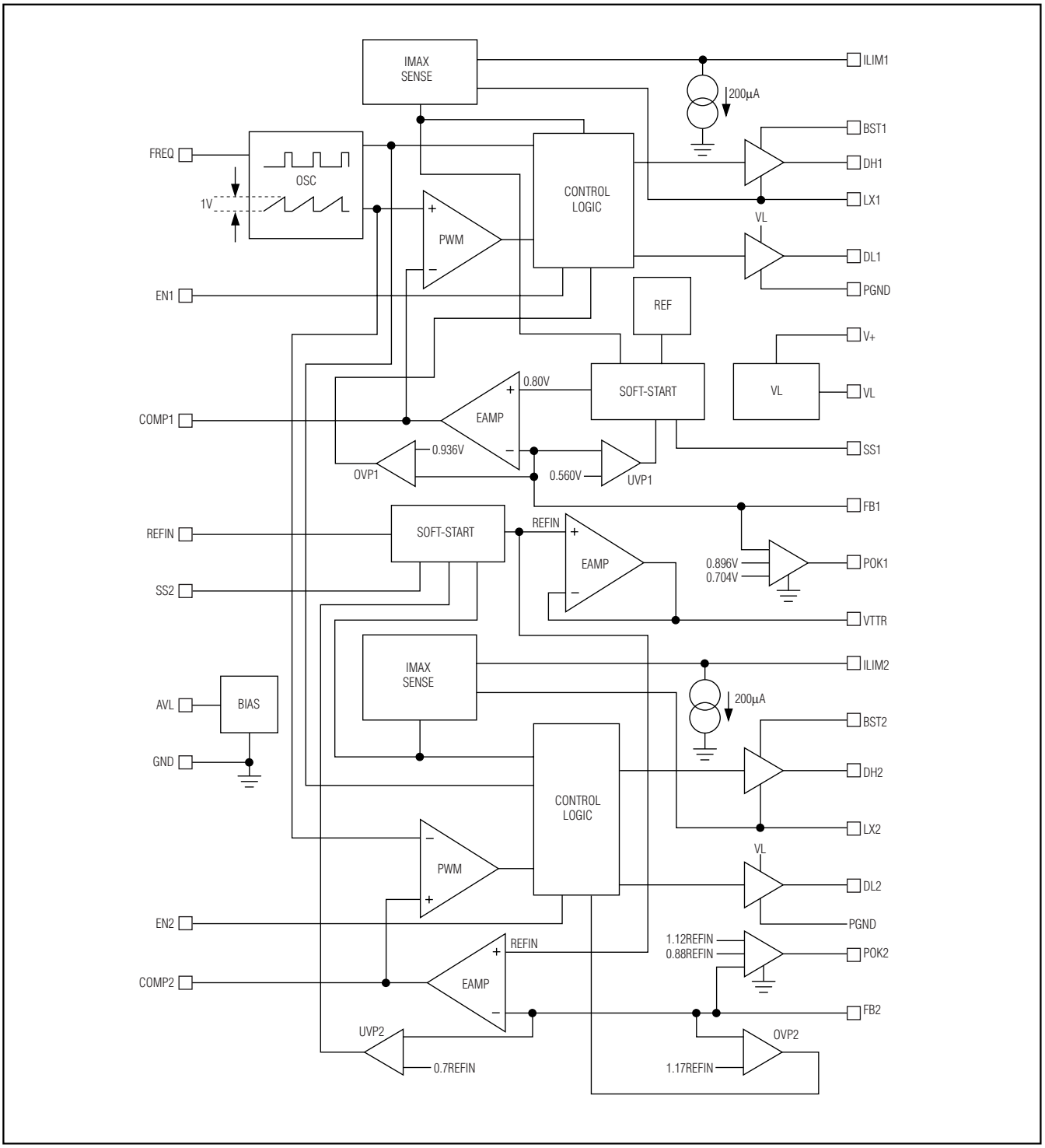
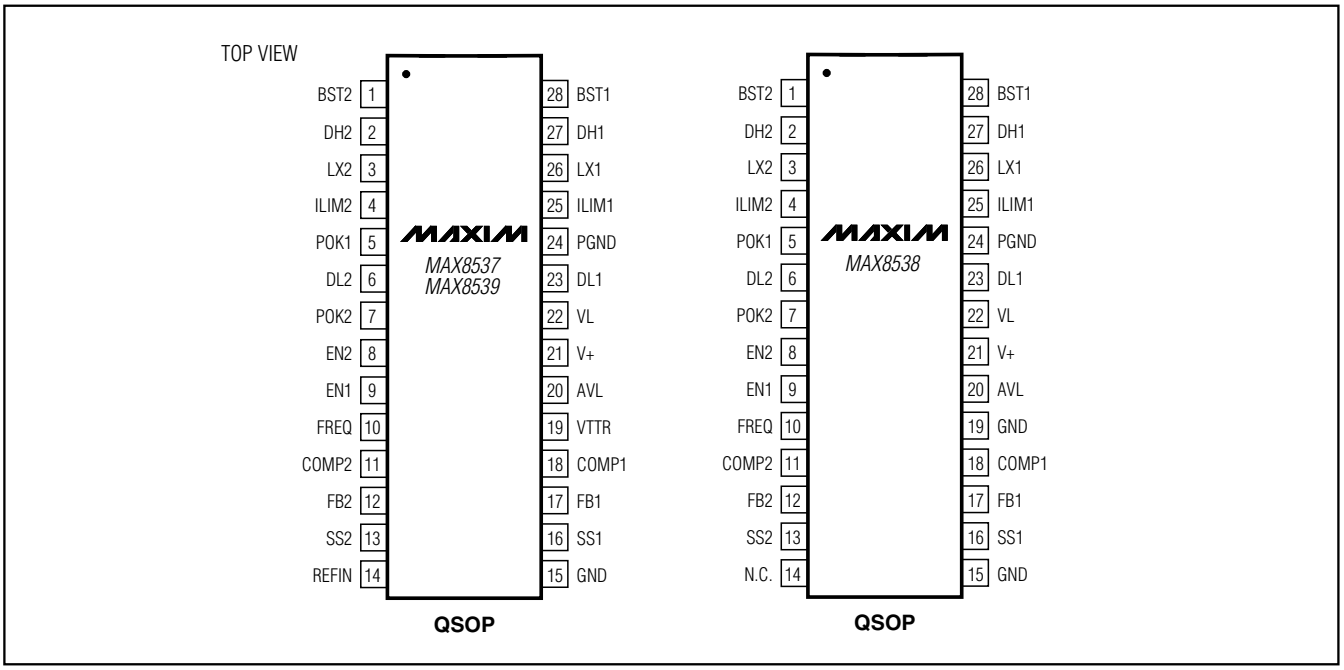
MAX8537/MAX8539 Functional Diagram



Pin Configurations



Case 2: Crossover frequency is greater than the output-capacitor ESR zero ($f_C > f_{Z\_ESR}$).

The modulator gain at f_C is:

$$G_{MOD(FC)} = G_{MOD(DC)} \times (f_{P\_LC})^2 / (f_{Z\_ESR} \times f_C)$$

Since the output-capacitor ESR-zero frequency is higher than the LC double-pole frequency but lower than the closed-loop crossover frequency, where the modulator already has -1 slope, the error-amplifier gain must have zero slope at f_C so the loop crosses over at the desired -1 slope.

The error-amplifier circuit configuration is the same as case 1 above; however, the closed-loop crossover frequency is now between f_{P2} and f_{P3} as illustrated in Figure 7.

The equations that define the error amplifier's zeros (f_{Z1_EA}, f_{Z2_EA}) and poles (f_{P2_EA}, f_{P3_EA}) are the same as case 1; however, f_{P2_EA} is now lower than the closed-loop crossover frequency. Therefore, the error-amplifier gain between f_{Z1_EA} and f_{Z2_EA} is now calculated as:

$$G_{EA}(f_{Z1\_EA} - f_{Z2\_EA}) = G_{EA(FC)} \times f_{Z2\_EA} / f_{P2\_EA} = f_{Z2\_EA} / (f_{P2\_EA} \times G_{MOD(FC)})$$

This gain is set by the ratio of R4/R1, where R1 is calculated in the *Output Voltage Setting* section. Thus:

$$R4 = R1 \times f_{Z2\_EA} / (f_{P2\_EA} \times G_{MOD(FC)})$$

where $f_{Z2\_EA} = f_{P\_LC}$ and $f_{P2\_EA} = f_{Z\_ESR}$.

Similar to case 1, C2 can be calculated as:

$$C2 = 2 / (\pi \times R4 \times f_{P\_LC})$$

Set the error-amplifier third pole, f_{P3_EA}, at half the switching frequency, and let $R_I = (R1 \times R3) / (R1 + R3)$. The gain of the error amplifier between f_{P2_EA} and f_{P3_EA} is set by the ratio of $R4/R_I$ and is equal to $G_{EA(FC)} = 1 / G_{MOD(FC)}$. Then:

$$R_I = R4 \times G_{MOD(FC)}$$

Similar to case 1, R3, C1, and C3 can be calculated as:

$$R3 = R1 \times Ri / (R1 - R_I)$$

$$C1 = 1 / (2\pi \times R3 \times f_{Z\_ESR})$$

$$C3 = C2 / ((2\pi \times C2 \times R4 \times f_{P3\_EA}) - 1)$$

Applications Information

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching-power stage requires particular attention. Follow these guidelines for good PC board layout:

1) Place the decoupling capacitors as close to the IC pins as possible.

2) Keep separate the power ground plane (connected to the sources of the low-side MOSFETs, pin 24, input capacitor ground, output capacitor ground, and VL decoupling capacitor ground) and the signal ground plane (connected to GND pin and the rest of the circuit ground returns). Place the input decoupling ceramic capacitor as directly and close to the high-side MOSFET drain and the low-side MOSFET source as possible. Place the RC snubber circuit as close to the low-side MOSFET as possible.
3) Keep the high-current paths as short as possible.
4) Connect the drains of the MOSFETs to a large land area to help cool the devices and further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).
7) Refer to the evaluation kit for a sample board layout.

Chip Information

TRANSISTOR COUNT: 5504

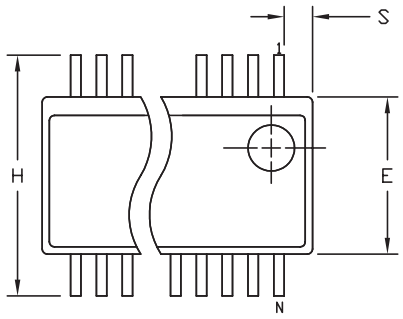
PROCESS: BiCMOS

Dual-Synchronous Buck Controllers for Point-of-Load, Tracking, and DDR Memory Power Supplies

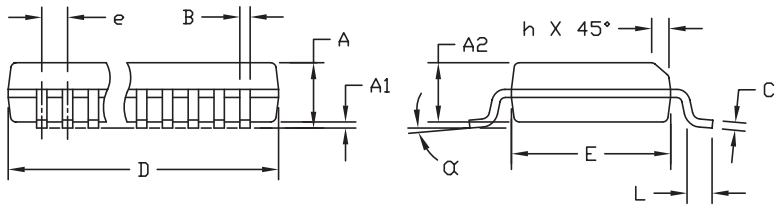
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV. E | 1/1

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